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Quadrature Phase-Domain ADPLL with Integrated On-line Amplitude Locked Loop Calibration for 5G Multi-band Applications

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QUADRATURE PHASE-DOMAIN ADPLL WITH INTEGRATED ON-LINE AMPLITUDE LOCKED LOOP CALIBRATION FOR 5G MULTI-BAND APPLICATIONS

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requirements for the degree of
Doctor of Philosophy

by

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I HEREBY RECOMMEND THAT THE DISSERTATION PREPARED UNDER MY SUPERVISION BY Xiaomeng Zhang ENTITLED Quadrature Phase-Domain ADPLL with Integrated On-line Amplitude Locked Loop Calibration for 5G Multi-band Applications BE ACCEPTED IN PARTIAL FULFILLMENT OF THE REQUIREMENTS FOR THE DEGREE OF Doctor of Philosophy.

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Abstract

Zhang, Xiaomeng. Ph.D., Department of Electrical Engineering, Wright State University, 2022. Quadrature Phase-Domain ADPLL with Integrated On-line Amplitude Locked Loop Calibration for 5G Multi-band Applications.

5th generation wireless systems (5G) have expanded frequency band coverage with the low-band 5G and mid-band 5G frequencies spanning 600 MHz to 4 GHz spectrum. This dissertation focuses on a microelectronic implementation of CMOS 65 nm design of an All-Digital Phase Lock Loop (ADPLL), which is a critical component for advanced 5G wireless transceivers. The ADPLL is designed to operate in the frequency bands of 600MHz-930MHz, 2.4GHz-2.8GHz and 3.4GHz-4.2GHz. Unique ADPLL sub-components include: 1) Digital Phase Frequency Detector, 2) Digital Loop Filter, 3) Channel Bank Select Circuit, and 4) Digital Control Oscillator. Integrated with the ADPLL is a 90-degree active RC-CR phase shifter with on-line amplitude locked loop (ALL) calibration to facilitate enhanced image rejection while mitigating the effects of fabrication process variations and component mismatch. A unique high-sensitivity high-speed dynamic voltage comparator is included as a key component of the active phase shifter/ALL calibration subsystem. 65nm CMOS technology circuit designs are included for the ADPLL and active phase shifter with simulation performance assessments. Phase noise results for 1 MHz offset with carrier frequencies of 600MHz, 2.4GHz, and 3.8GHz are -130, -122, and -116 dBc/Hz, respectively. Monte Carlo simulations to account for process variations/component mismatch show that the active phase shifter with ALL calibration maintains accurate quadrature phase outputs when

operating within the frequency bands 600MHz-930MHz, 2.4GHz-2.8GHz and 3.4GHz-4.2GHz.

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I. Introduction

1.1 Background

5G is short for “5th generation”, and in telecommunication, it is the next generation wireless network technology of existing 4th Generation Long-Term Evolution (4G LTE) network [1]. 5G network is expected to provide faster speed, lower latency, and connect more devices compared to current 4G network. Such benefit enables new methods that people live and work [2]. For example, with new 5G technology, the autonomous vehicles can communicate with each other on the road to improve safety and performance. Moreover, the concept of future “Smart City” can be a reality only with the help of 5G technology. Taking the advantages of ultra-low latency and wide bandwidth, almost everything in the city is connected and operated coordinately to reduce the energy consumption and resources efficiency [3] [4] [5].

The 5G spectrum are sliced into multiple bands, and each band provides unique features to deliver the overall best performance of 5G network. The operating spectrum of 5G is not uniform across countries, in this case, the transceiver system is very important. As shown in Fig 1.1.1, the standard transceiver system consists of receiving path and transmitting path. The Radio Frequency (RF) signal is down converted into either Intermediate Frequency (IF) signal or baseband signal by a mixer in receiving path. Similarly, the IF or baseband signal is up converted into RF signal through the mixer in transmitting path. The relationship between RF, IF and Local Oscillator (LO) is expressed in (1-1-1):

$$\omega_{RF} = \omega_{IF} + \omega_{LO} \quad (1\text{-}1\text{-}1)$$

To keep the same Analog to Digital Converter (ADC), Digital to Analog Converter (DAC) and Digital Signal Processor (DSP) in one device, an adjustable and wideband frequency synthesizer is the key.

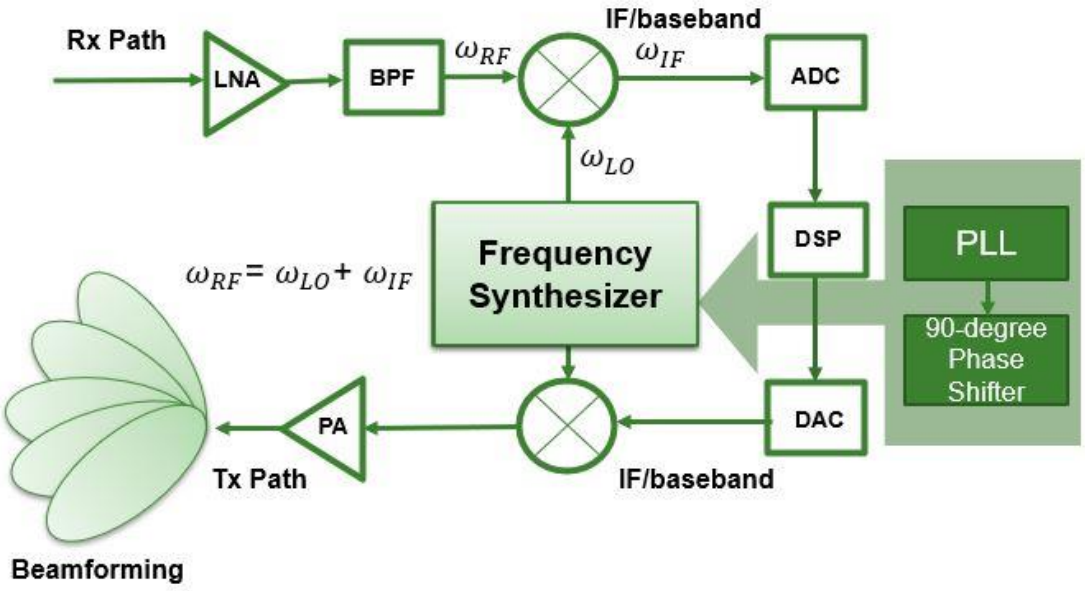


Fig 1.1.1 Standard transceiver system

This dissertation is focusing on frequency synthesizer design to support different regulations among countries within one device. Usually, it consists of a phase locked loop and a 90-degree phase shifter. The phase locked loop generates accurate frequency signals, and the 90-degree phase shifter provides precise quadrature phases and constant gain. In 5G transceiver system, the 90-degree phase shifter can be used for beamforming and image rejection purpose. A quadrature phase-domain ADPLL with integrated on-line amplitude locked loop calibration system is proposed in this dissertation to meet the 5G multi-band standard.

1.2 5G Spectrum

1.2.1 5G 3-Band Spectrum Architecture

With the consideration of both signal coverage area and performance, most 5G regulations are using 3 bands to support the network. The 5G network is establish under the topology of "Cells", which describes the service area of each base station. As shown in Fig 1.2.1, the largest cell provides the stable connection in wide area, and low band is used for this cell. It can be used in big factories or warehouses to control the machines and robots to realize automation; Mid band is used for middle size cell such as office buildings or schools, which deliver high quality signal within a smaller zone. The ultra-small cell with high band is designed to allow large number of connection and achieve the highest speed in a compact environment like stadium or shopping mall.

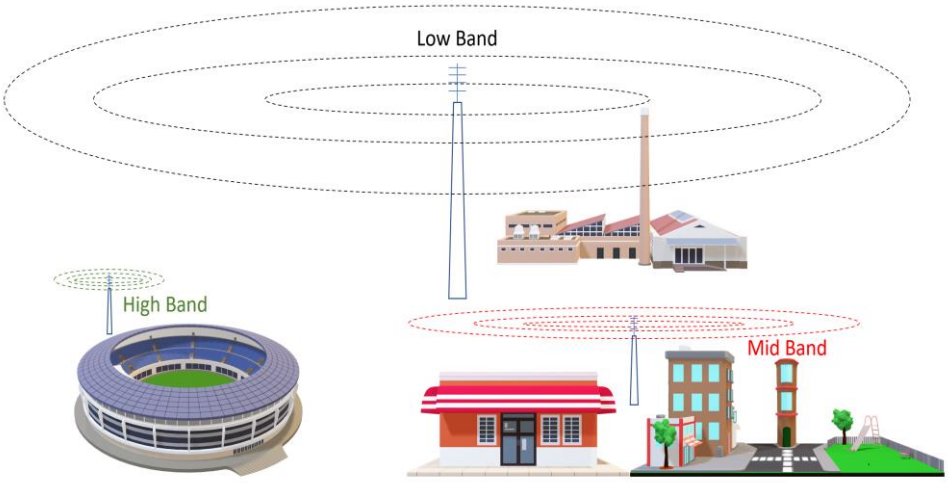


Fig 1.2.1 "Cell" concept of 5G network.

The low band usually is operating below 2 GHz. The advantage of this band is good transmission distance that covers hundreds of square miles service area. Another benefit of this band is the penetration capability of low frequency radio wave, which

provides the connection inside of the building or even basement [6]. Even though this band 5G service offers the slowest peak speed, the data rate is still much faster than current 4G LTE common speed.

The mid band spectrum takes 2 to 6 GHz frequency band to enable larger bandwidth than the low band. Such frequency range is currently used by 2G, 3G, and 4G services, which will be re-used by 5G in the future. The mid band is expected to serve the most of user as it carries plenty of data with descent covered area (several-mile radiuses coverage). The peak speed of this band is 600 – 700 Mbps in US currently and can go up to 2 Gbps in China, Korean, and other countries. Many carriers and chip makers recognize this band as the optimal point in terms of cost, coverage, quality, and latency [7].

The high band of 5G system uses millimeter Wave (mmWave) signal as the carrier to transfer data. The spectrum of this band is above 24 GHz that can easily provide very large channel bandwidth to achieve high-speed data transmission. Even though the signal at this frequency band suffers a huge path loss referring to (1-2-1), where d is the path distance, f is signal frequency and c is speed of light, the incredible data rate still enables the future of many applications in industry and daily life.

$$P_{Path\ Loss} = (\frac{4\pi * d * f}{c})^2 \quad (1\text{-}2\text{-}1)$$

1.2.2 5G Spectrum Allocations

As describe in the section 1.2.1, most of the 5G spectrum are sliced into multiple bands to work jointly. Each band provides unique features to provide the overall

performance of 5G system.

Just like previous generations of communication bands, the operating spectrum is not uniform across countries. In the following content of this section, the 5G spectrum of several countries is listed in the tables below. Some bands have already been auctioned or licensed, and others are in the auction process or under serious consideration.

Table 1.2.1 US 5G spectrum [8]

Band	Frequency (GHz)
Low-Band	0.6 (Upcoming)
	0.8 (Upcoming)
	0.9 (Upcoming)
Mid-Band	2.5 (Upcoming)
	3.5 (Upcoming)
	3.7 – 4.2 (Upcoming)
High-Band	24
	28
	37
	39
	47

Table 1.2.2 China 5G spectrum [9]

Band	Frequency (GHz)
Low-Band	0.7
Mid-Band	2.515 – 2.675
	3.4 – 3.5
	3.5 – 3.6
	4.8 – 4.9

High-Band	24.75 – 27.5 (Upcoming)
	37 – 40 (Upcoming)
	3 – 42.5 (Upcoming)

Table 1.2.3 France 5G spectrum

Band	Frequency (GHz)
Mid-Band	3.4 – 3.8
High-Band	3.2 – 27.5 (Upcoming)

Table 1.2.4 United Kingdom 5G spectrum

Band	Frequency (GHz)
Mid-Band	3.4 – 3.6
	3.6 – 3.8 (Upcoming)
High-Band	3.2 – 27.5 (Upcoming)

Table 1.2.5 Japan 5G spectrum

Band	Frequency (GHz)
Mid-Band	3.6 – 3.7
	3.7 – 3.8
	3.8 – 3.9
	3.9 – 4
	4 – 4.1
	4.5 – 4.6
High-Band	27 – 27.4
	27.4 – 27.8
	27.8 – 28.2
	28.3 – 29.1 (Upcoming)

Table 1.2.6 South Korea 5G spectrum

Band	Frequency (GHz)
Mid-Band	3.42 – 3.5
	3.5 – 3.6
	3.6 – 3.7
	4.5 – 4.6
High-Band	26.5 – 27.3
	27.3 – 28.1
	28.1 – 28.9

1.3 Beamforming and Image Rejection in 5G System

To deliver the best performance of 5G network, many technologies are used in both analog and digital domain. On carrier side, two main techniques help improve the signal quality and they are beamforming and image rejection. Both techniques require multi-phase feature of carrier generator.

1.3.1 Beamforming

Beamforming is widely used in RF phase array design to narrow the transmission beam in certain angle. Every antenna in the array is connected with a phase shifter which can steer the phase of feeding signal. As shown in Fig 1.3.1, the signal emitting from each antenna is constructed to a new beam pattern based on the phase difference between transmitters. Using such technique in 5G system, multiple users can connect to base-station simultaneously with better quality of communication.

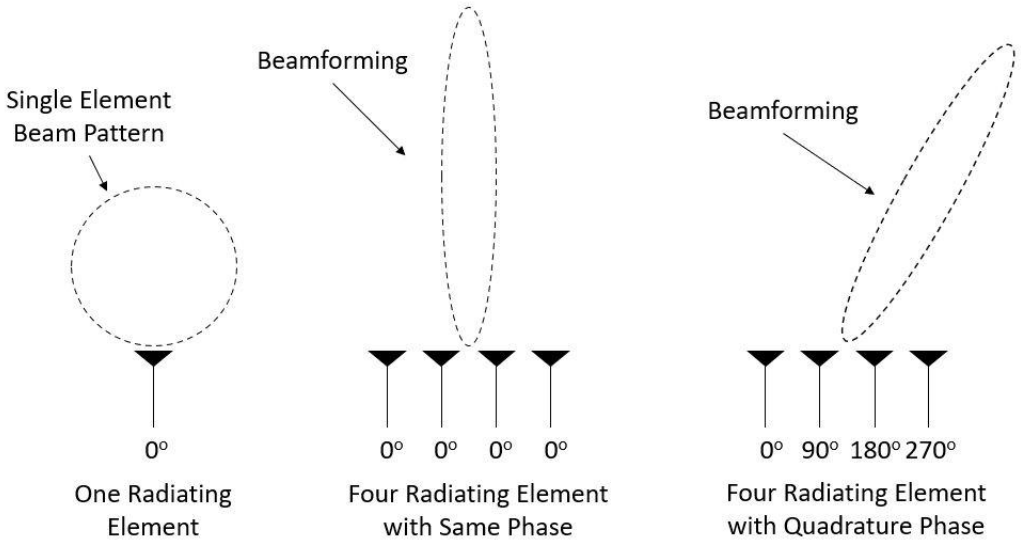


Fig 1.3.1 Analog beamforming

1.3.2 Image Rejection

For RF transceiver design, Low-IF baseband architecture has the advantages of high integration, less passive components and low flicker noise properties compared with high-IF Heterodyne and Zero-IF receivers [10] [11] [12]. In a low-IF receiver, the desired radio frequency signal is down-converted to intermediate frequency by a mixer. There is an RF image signal (offset from the desired RF signal) that is down converted to the same IF frequency as the desired RF signal causing interference noise in the IF bandwidth. The noise cannot be filtered out at the IF section and it degrades the wanted signal quality. To reject the image signal with front-end design and reduce the high-level interference effect, the Hartley system is widely studied based on phase cancellation methodology [12]. The key circuit element in Hartley system is the 90-degree phase shifter after local oscillator as shown in Fig 1.3.2. The desired signal is preserved, and image signal is suppressed if the phase shifter generates a precise quadrature phase and matched gain across the entire operating bands. However, the

power of the image signal with respect to the desired tone becomes worse with the imbalance of gain and phase of I/Q (in phase and quadrature) signals, resulting in degradation of the Signal to Noise Ratio (SNR) in the receiver system. There is approximately a 40dB loss in SNR for 1-4 degree phase mismatch or 0.2-0.6dB gain imbalance [13] [14]. Therefore, the frequency synthesizer in 5G system should be featured with quadrature phase and high accuracy phase shifting over wide frequency range to cover as many spectrum bands as possible.

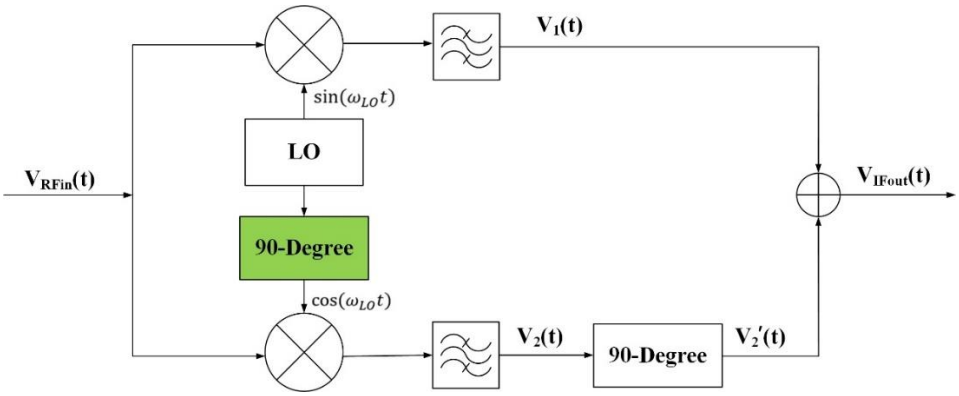


Fig 1.3.2 Hartley architecture

1.4 Frequency Synthesizer

In RF transceiver system, frequency synthesizer is a key component to dominant system noise performance. It should generate precise signals with high spectral purity. The signal generator block not only oscillate at carrier frequency with channel spacing resolution but also translate into baseband clock frequency for DSP. Phase Noise (PN) is a particularly important property for frequency synthesizer. Excessive phase noise can create channel-to-channel interference, and the higher PN will increase the noise floor and degrades SNR so that the ADC performance is limited [15]. Besides, high resolution of channel spacing is also demanded in wireless communication because of the high customer density in limited bandwidth. Thirdly, a wide bandwidth or multiple

bands are desired in portable wireless devices to meet the Federal Communication Commission (FCC) arrangement for different applications. Meanwhile, the response/locking time is another important property, which represents the efficiency of the frequency synthesizer, and a fast speed is needed in transceiver system. In other words, the design of frequency synthesizer for portable wireless devices becomes challenging because of the tradeoffs of phase noise, frequency resolution, response time, bandwidth, circuit size and power consumption.

The frequency synthesizer can be divided into three categories: Direct Analog Synthesizer (DAS), Direct Digital Synthesizer (DDS) and indirect or Phase Locked Loop (PLL). Usually, there are three kinds of PLLs, which are All Analog PLL (AAPLL), All Digital PLL (ADPLL) and hybrid PLL (combination of both analog and digital circuit). The definition of each category is discussed as followed.

1.4.1 Direct Analog Synthesizer

Direct analog synthesizer is a way to use mixing, frequency multiplication and abundant of filters to generate the desired frequency from one stable signal source with good phase noise performance [16]. However, it is not widely used in frequency synthesizer design due to the poor phase noise performance.

1.4.2 Direct Digital Synthesizer

Direct digital synthesizer is using digital control words to control system generating desired frequency from reference digitally. Basically, a DDS is formed by phase accumulator, phase to amplitude converter, DAC and Low Pass Filter (LPF). As shown in Fig 1.4.1, the phase accumulator is controlled by the Frequency Control Word (FCW), and it is sampled by reference clock to construct the time-sampled phase. A

Programmable Read Only Memory (PROM) is the next stage of the synthesizer, where stores the phase information of the sinewave, and the memory is regarded as the lookup table to generate the desired phase based on the phase accumulator outputs. The digitized output from the memory is processed by a DAC followed by an LPF to realize the analog output signal [16] [17].

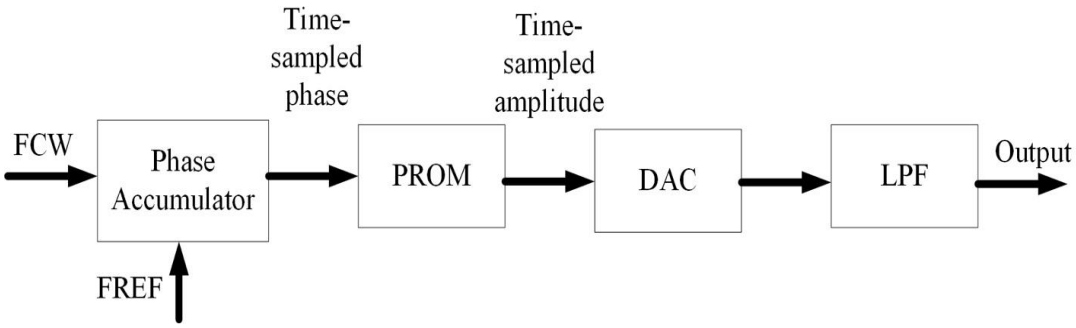


Fig 1.4.1 General architecture of DDS

1.4.3 Phase Locked Loop

A phase locked loop generates stable high frequencies from fixed low frequency reference, and it is widely used in data recovery, coherent demodulation, bit synchronization, etc. [18] [19]. As described in Fig. 1.4.2, it consists of a Voltage Control Oscillator (VCO), divider, Phase Frequency Detector (PFD), Charge Pump (CP) and Loop Filter (LF). There are three operating states for a PLL, and they are frequency free running, comparing and locking. Initially, the oscillator is oscillating at its natural frequency. Then, the loop is closed, and the feedback frequency is comparing and adjusting to make it equal to reference frequency. The phase error will be eliminated at the matched point. It can be implemented in either an analog intensive or digitally intensive. The PLLs can also be categorized in fractional-N or integer-N operations based on its frequency resolution.

Among these different kinds of frequency synthesizers, PLL is mostly used in wireless transceivers than the first and second types. The DDS sometimes can be used as the reference to replace crystal oscillator reference, but the penalty is the complexity of the circuit implementation. The PLL architecture is employed for the multi-band 5G frequency synthesizer, and a detailed architecture of phase locked loop will be introduced in this chapter.

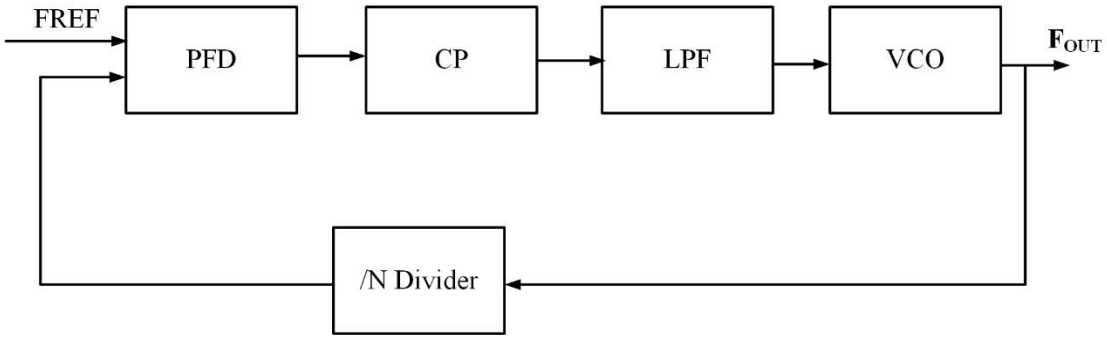


Fig 1.4.2 Architecture of phase locked loop

1.5 90-Degree Phase Shifter

For 5G wireless communication, beam forming technique is widely used to transmit and process more useful information, which requires quadrature phases of the carrier signal. Ring oscillator has the advantage of generating multiple phases [20], but the poor phase noise performance is the limitation for 5G applications. LC tank oscillator is a good candidate to generate signals for 5G standard with low phase noise [21], however, only a pair of differential outputs is generated by the LC tank. Therefore, a phase shifter block is needed after the LO circuit to generate the quadrature phase as described in Fig 1.3.2.

There are many approaches to phase shifter designs for transceiver sub-systems; e.g. Gilbert mixer in the quadrature signal generator and image rejection for the dual band low IF application [12], phase selector circuit for a phased array beamforming

system application [22] [23], and differential scheme in the VCO/phase locked loop application [24]. The passive RC-CR phase shifter is a good candidate for narrowband I/Q generator since it achieves the 90-degree phase difference outputs at all frequencies [25] and the gain of the I and Q are matched at the pole frequency ($f_P = 1/2\pi RC$). Acceptable IMMRs are achieved for narrow bands near the pole frequency, but output gain matching degrades at frequencies away from the pole frequency, so additional techniques are needed for wideband applications. A polyphase filter can be employed to increase the accuracy of the passive RC-CR phase shifter over a wide bandwidth; however, multiple stages increase the design complexity [12] [26]. Other designs using capacitor bank achieves good Image Rejection Ratio (IMRR) compensation with the penalty of increasing layout size [27]. A hardware calibration system coupled with an active RC-CR phase shifter is proposed in this paper to generate quadrature output after the phase lock loop. The objective is the reduction of image interference with high quality IMRR resulting in enhanced quality of the desired signal while maintaining low circuit complexity. Pole frequencies are adjusted and monitored by a feedback loop, and precise phase and gain are realized within a wide frequency band in this proposed architecture.

1.6 Motivation

With the advantages of the faster speed, higher volume of customers, and wider bandwidth, the 5G network has a promising prospect of Internet-of-Things (IoTs). This new generation of communication also enables the full potential of smart city, telehealth, and autonomous driving.

However, the spectrum allocations currently are varied in different countries. To satisfy the protocols and regulations with one single electric device, a CMOS wideband

or multi-band phase locked loop is preferred. Meanwhile, the phase shifter circuit is a key component in 5G beamforming and image rejection techniques. An integrated wideband and high accuracy 90-degree phase shifter is also desired.

The top-level block diagram of proposed circuit is shown in Fig 1.6.1. In order to meet the frequency synthesizer requirement for 5G network, a multiple band highly programmable and fine resolution all digital PLL is implemented in this dissertation. Meanwhile, a multiband (600MHz-930MHz, 2.4GHz-2.8GHz and 3.4GHz-4.2GHz) active 90-degree RC-CR phase shifter is also designed after the PLL stage, followed with integrated on-line amplitude locked loop calibration system to provide constant output gain for transceiver system.

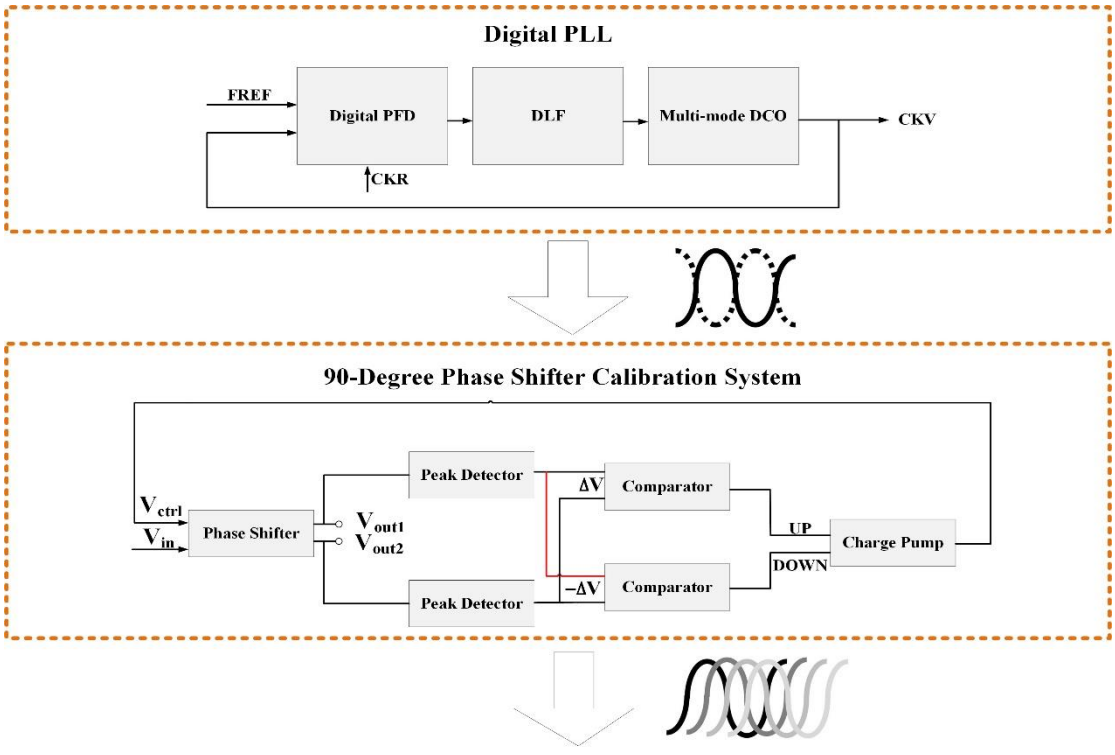


Fig 1.6.1 Top-level block diagram of proposed multi-band quadrature phase-domain DPLL with ALL calibration system

1.7 Objective

- Design a wideband 90-degree phase shifter which can be used after the LC tank oscillator to generate quadrature phase for 5G beamforming and image rejection purpose.
- Design a hardware integrated on-line amplitude locked loop calibration system for active RC-CR phase shifter to reduce the image interference with high quality IMRR resulting in enhanced quality of desired signal while maintaining low circuit complexity.
- Design a digital phase locked loop that can operate with multiple bandwidths for 5G standard.
- Design and simulate the digital PLL with active RC-CR phase shifter circuit in 65nm technology.

II. 90-Degree Active RC-CR Phase Shifter

(The discussion in the following chapter is substantially drawn from [28], where we first reported the development and evaluation of this technique.)

2.1 Introduction

For the purpose of beamforming and image rejection in 5G communication network, quadrature phase is needed at the frequency synthesizer output over multiple frequency bands (600MHz-930MHz, 2.4GHz-2.9GHz and 3.4GHz-4.2GHz). In transceiver system, the desired signal is preserved, and image signal is suppressed if the phase shifter generates a precise quadrature phase and matched gain across the entire operating bands. However, the power of the image signal with respect to the desired tone becomes worse with the imbalance of gain and phase of I/Q (in phase and quadrature) signals, resulting in degradation of the SNR in the receiver system. There is approximately a 40dB loss in SNR for 1-4 degree phase mismatch or 0.2-0.6dB gain imbalance [29] [30].

The passive RC-CR phase shifter generates the required two quadrature outputs with an accurate 90-degree phase shift over the required bandwidth but lack the required accuracy in amplitude matching. In this chapter, a wide band active 90-degree RC-CR phase shifter is proposed to improve the IMRR performance.

2.2 Conventional RC-CR Phase Shifter

As shown in Fig 2.2.1, a conventional RC-CR phase shifter consists of two identical capacitors and resistors, which forms a pair of parallel high-pass and low-pass filters with the same pole frequency. The outputs (V_{out1} and V_{out2}) and their equivalent

phases are expressed in (2-2-1) to (2-2-3). According to these equations, the phase differences between I and Q paths are equal to 90 degree and are independent of frequencies.

$$V_{out1} = \frac{j\omega RC}{1+j\omega RC} \cdot V_{in} \Rightarrow \angle V_{out1} = \frac{\pi}{2} - \tan^{-1}(\omega RC) \quad (2\text{-}2\text{-}1)$$

$$V_{out2} = \frac{1}{1+j\omega RC} \cdot V_{in} \Rightarrow \angle V_{out2} = -\tan^{-1}(\omega RC) \quad (2\text{-}2\text{-}2)$$

$$\angle V_{out} = \angle V_{out1} - \angle V_{out2} = \frac{\pi}{2} \quad (2\text{-}2\text{-}3)$$

However, the amplitudes of V_{out1} and V_{out2} are equal only at the pole frequency in (2-2-4) as shown in Fig 2.2.2. In this case, the wideband performance of conventional RC-CR phase shifter is limited by the passive resistors and capacitors.

$$f_P = \frac{1}{2\pi R_1 C_1} = \frac{1}{2\pi R_2 C_2} \quad (2\text{-}2\text{-}4)$$

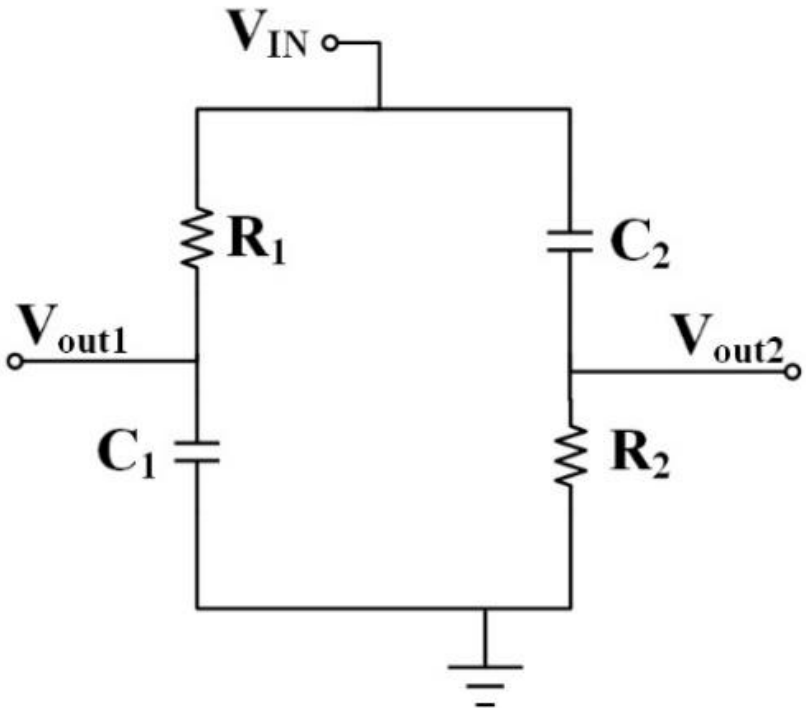


Fig 2.2.1 Conventional 90-degree RC-CR phase shifter

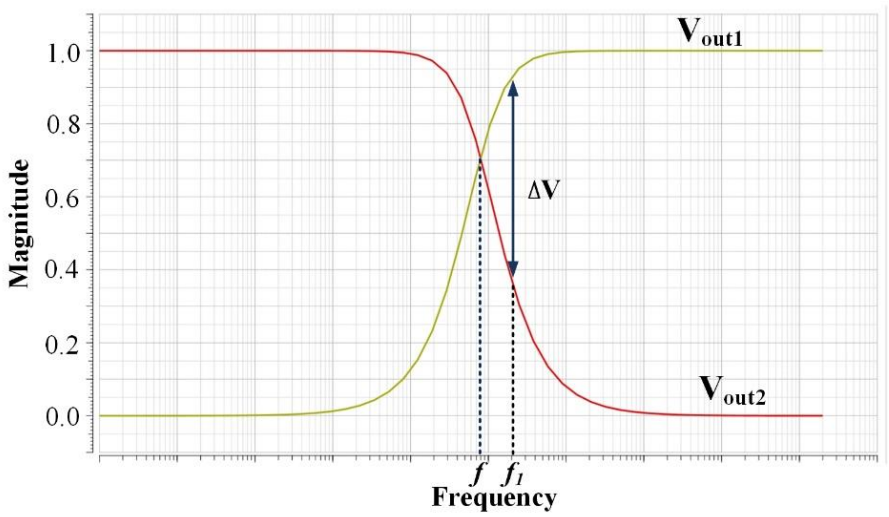


Fig 2.2.2 Frequency response of conventional RC-CR phase shifter

2.3 Active RC-CR Phase Shifter

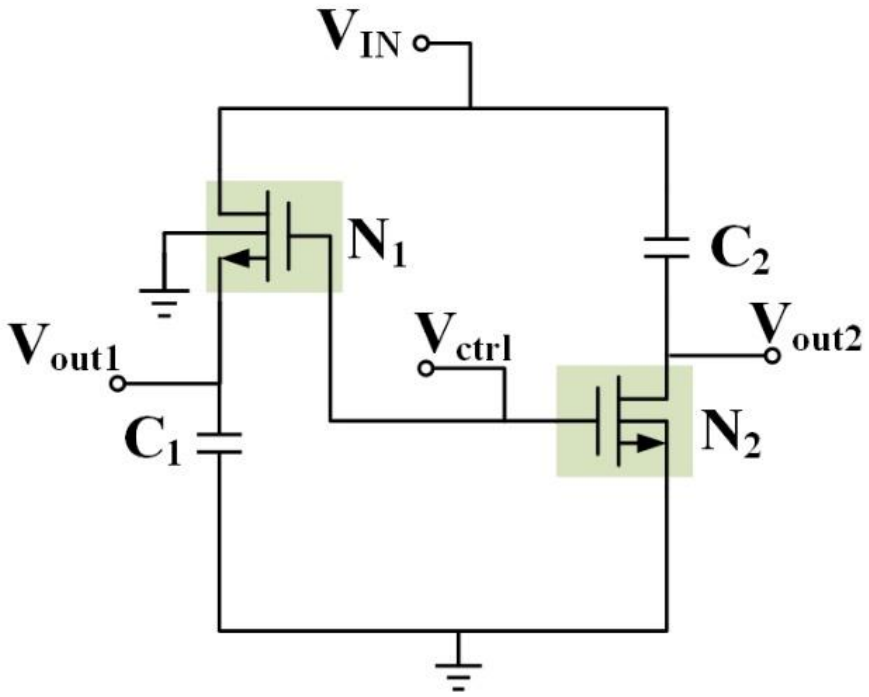


Fig 2.3.1 Active RC-CR phase shifter

As explained in Fig 2.2.2, gain mismatch (ΔV) happens when input frequency varies from the pole frequency, and the gain error increases with deviation of the

operating frequency from the pole frequency. As a result, the image rejection performance is not guaranteed within the required input bandwidth.

An active RC-CR 90-degree phase shifter is proposed in this section (Fig 2.3.1), where the passive resistors are replaced by active resistors with controllable gate voltage (V_{ctrl}). The output amplitudes are forced to be equal, then $R_1C_1 = R_2C_2 = 1/(2\pi f_P)$, and the 90-degree phase differential is obtained with equality of the RC products.

A second issue is post fabrication process variation which varies the components parameter from the designed value. Such variation on R1, C1, R2, and C2 potentially results in both gain and phase error on phase shifter outputs at any input frequency.

Thus, to design a wideband 90° phase shifter with constant gain, the pole frequency of the two paths should be aligned as the input frequency varies over the required bandwidth and considering process variation effects on the resistor/capacitor pairs. The proposed active RC-CR 90-degree phase shifter in Fig 2.3.1 is used to keep the magnitudes of Vout1 and Vout2 equal over the bandwidth and considering post fabrication circuit value variation due to process variation. The capacitors C1 and C2 are designed with a fixed value. Since C1 and C2 are designed with symmetry and are close together on the chip layout, the difference of their value for given fabrication run is very small [31] [32]. The proposed design facilitates adjusting the resistor values equally to obtain equal output amplitudes under the assumption that with careful design layout procedures the magnitudes of the C1 and C2 remain essentially equal.

When a CMOS transistor is in triode mode, the drain to source current I_D is estimated by (2-3-1):

$$I_D = \beta(V_{GS} - V_T)V_{DS} \quad (2\text{-}3\text{-}1)$$

Where β=k(W/L) and k is the process gain factor. W and L describe the width and length of a transistor and V_T is the threshold voltage. Note that the gate-to-source voltage V_{GS} must be greater than V_T to allow I_D flowing through transistor and to operate in liner region; also, the drain-to-source voltage V_{DS} needs to be smaller than (V_{GS}-V_T).

Thus, the equivalent resistance R_{ON} is expressed in (2-3-2).

$$R_{ON} = \frac{V_{DS}}{I_D} = \frac{1}{\beta(V_{GS}-V_T)} \quad (2\text{-}3\text{-}2)$$

So R_1 and R_2 are expressed as (2-3-3) and (2-3-4):

$$R_1 = \frac{1}{\beta(V_G-V_{out1}-V_T)} \quad (2\text{-}3\text{-}3)$$

$$R_2 = \frac{1}{\beta(V_G-V_T)} \quad (2\text{-}3\text{-}4)$$

In the proposed design, an input frequency range of 600MHz to 3.8GHz is needed to meet 5G network requirement. A set of 130fF capacitor is used for the lower frequency band (600MHz to 930MHz) and two 40fF capacitors are used for higher frequency band (2.4GHz to 4.2GHz). With the input frequency varying from 600MHz to 3.8GHz, the gate voltage of N_1 and N_2 can be adjusted over a certain range to vary the active resistance. Note that V_{in} is a sine wave with a relatively small magnitude (about 0.1V) and no offset (mean value=0V). V_{out1} and V_{out2} are sine wave with almost equal small magnitudes, zero mean, and almost 90-degree phase difference. The drain of N_1 is connected to the input sine wave and the source is the output sine wave with 45-degree relative to input, and the source is grounded. The mean value of the drains and sources are zero for both transistors. With the gate of both N_1 and N_2 converging

to a constant DC value, both N_1 and N_2 assume a resistance value associated with the zero mean of their source and drain. In this case, the wide band active RC-CR phase shifter is realized by adjusting the gate voltage of N_1 and N_2 based on R_{ON} being inversely proportional to V_{GS}.

2.4 Circuit Implementation and Simulation

An active RC-CR 90-degree phase shifter circuit is implemented in Cadence 65nm process as explained in Fig 2.4.1. Without modifying the gate voltage V_{ctrl}, V_{out1} and V_{out2} are 90-degree phase difference but with different gain as shown in Fig 2.4.2 (a). By adjusting V_{ctrl}, the pole frequency is moved to the input case, and the 90-degree phase with identical amplitude for V_{out1} and V_{out2} is achieved. For the input frequency range from 600MHa to 3.8GHz, three different cases (930MHz for 600MHz to 930MHz band, 2.4GHz for 2.4GHz to 2.9GHz band and 3.8GHz for 3.4GHz to 4.2GHz band) are listed in Fig 2.4.2 (b) to (d) for simplicity.

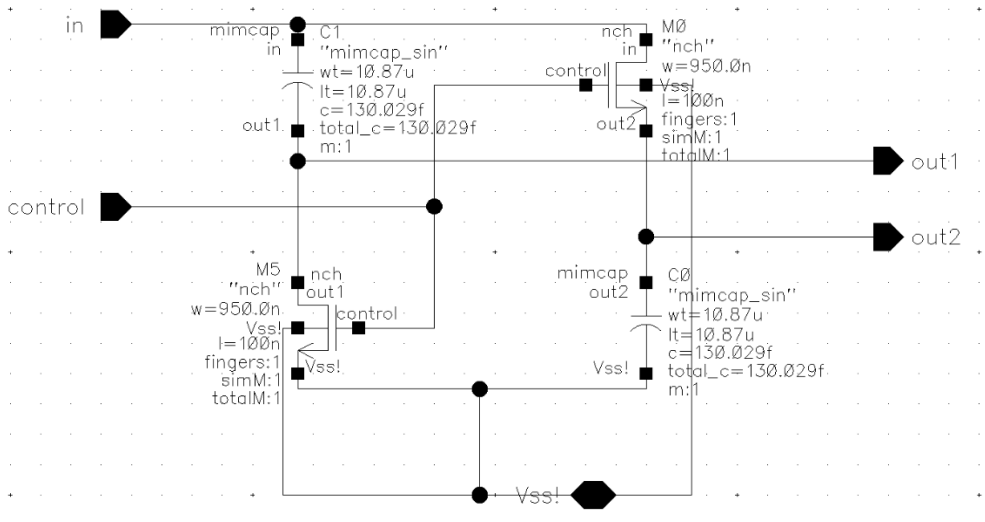
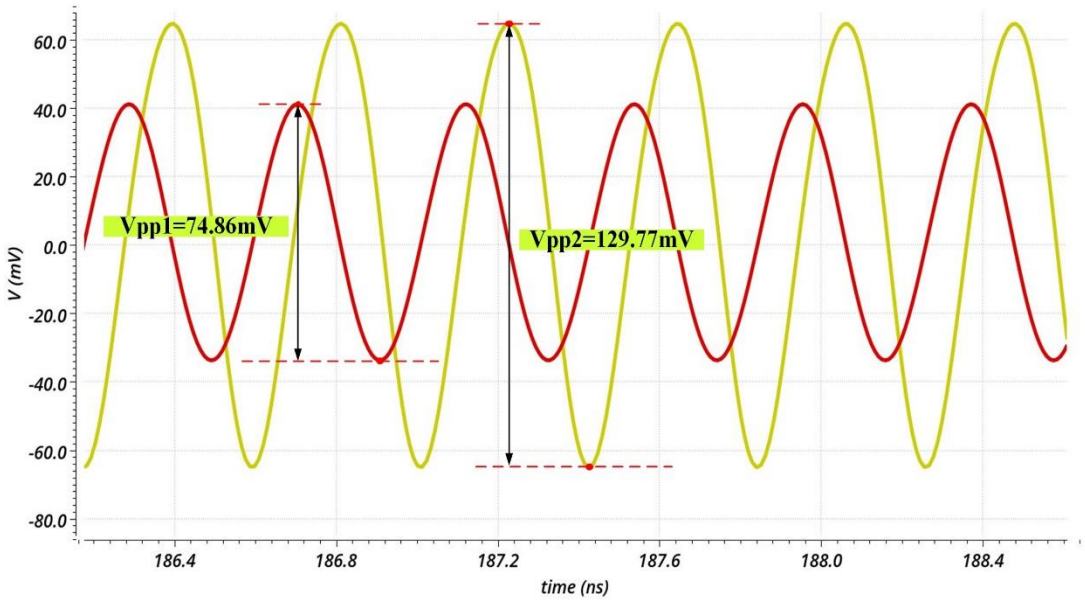
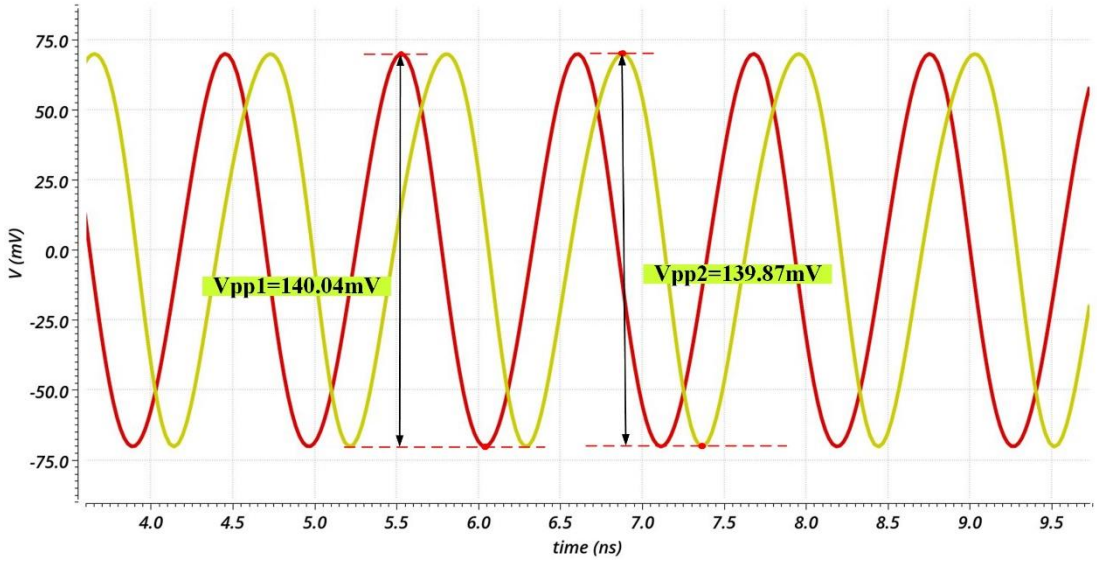


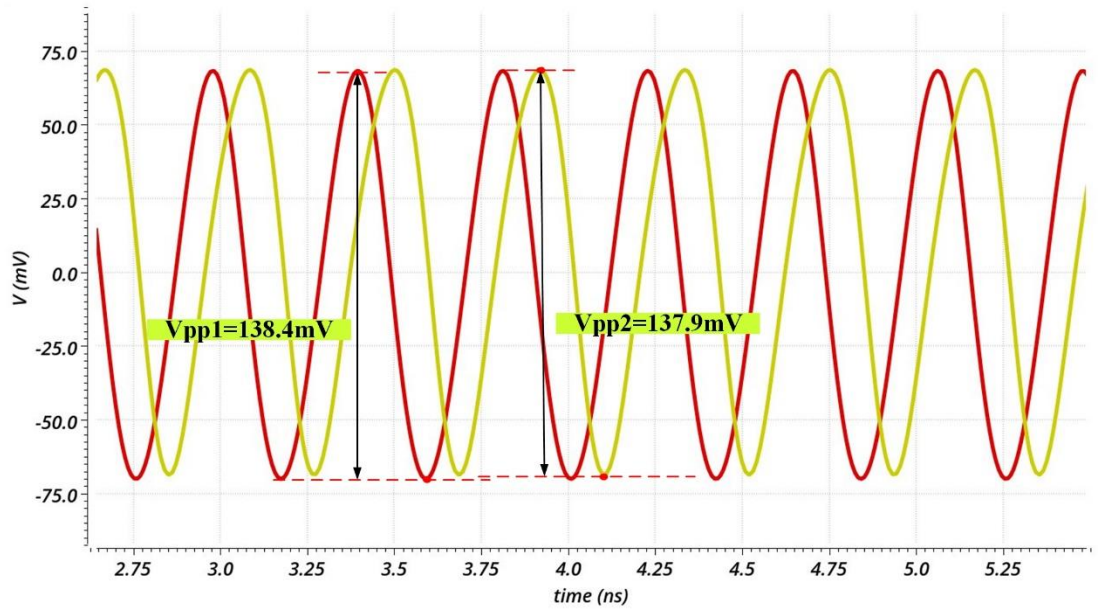
Fig 2.4.1 Schematic circuit of active RC-CR phase shifter


Vpp1=74.86mV
Vpp2=129.77mV
V (mV)
time (ns)

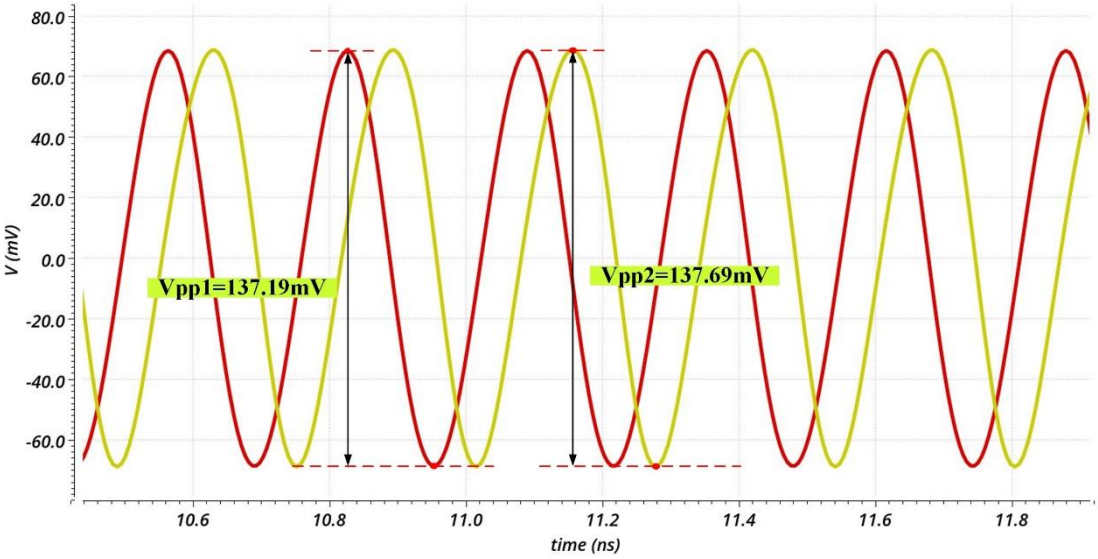
(a)


Vpp1=140.04mV
Vpp2=139.87mV
V (mV)
time (ns)

(b)



(c)



(d)

Fig 2.4.2 Simulation plots (a) Free run outputs with 3.8GHz input frequency (b) Adjusted output signals at 930MHz input frequency (c) Adjusted output signals at 2.4GHz input frequency (d) Adjusted output signals at 3.8GHz

2.5 Conclusion

The active RC-CR 90-degree phase shifter is implemented by replacing the passive resistors with NMOS transistors. By adjusting the gate voltage of the transistors, the

pole frequency of the low/high pass filters can be varied with input frequency, and the wide band property for the phase shifter is realized. However, it is very complicate to change gate voltages with the variation of input frequencies manually. Besides, the accuracy of the phase shifter cannot be guaranteed with considering process variation effect when a look up table is used. In other words, an integrated and automatic calibration system is necessary for the active RC-CR circuit. The transistor gate voltages can be used in calibration system to vary the pole frequency as the input frequency changes and compensate for the gain mismatch error between two paths.

A top-level block diagram of the proposed in the loop real time calibration system is shown in Fig 2.5.1. Two peak detectors are connected to each output of active phase shifter to convert the AC amplitude into a unique DC voltage. Then, these two DC signals are fed into two parallel and identical comparators to cross check the two output amplitudes. When two DC inputs are very close (within the comparator resolution), the two comparator outputs are the same (‘00’ or ‘11’); When the difference between the two DC values is greater than the resolution, the comparator outputs have opposite results (‘01’ or ‘10’). Hence, the comparison results control the output of the next stage charge pump. If comparator outputs are ‘01’ or ‘10’, then charge pump modifies the gate voltage of the phase shifter (V_{ctrl}) up or down to vary the active resistance and adjust the pole frequency to match the input frequency for gain error compensation. If the two comparators output ‘00’ or ‘11’, the charge pump keeps V_{ctrl} constant to preserve equal gain in the I and Q paths.

According to the analysis in this chapter, the amplitude of V_{out1} and V_{out2} is function of frequency, resistance, and capacitance. Therefore, by changing the value of

resistance in each path, the amplitude mismatch due to frequency variation can be significantly reduced if capacitance in the path is fixed. A more detailed analysis of the comparator circuit of the calibration system is introduced in Chapter 2, and the proposed RC-CR phase shifter ALL calibration system is explained in Chapter 3.

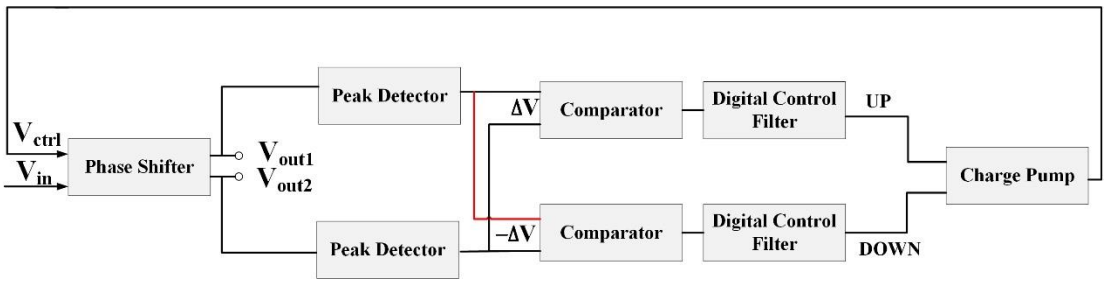


Fig 2.5.1 Block diagram of RC-CR phase shifter ALL calibration system

III.Dynamic Voltage Comparator

(The discussion in the following chapter is substantially drawn from [33], where we first reported the development and evaluation of this technique.)

3.1 Introduction

Comparators are widely used in CMOS designs such as flash and Successive-Approximation Register (SAR) Analog-to-Digital Converters (ADCs) [34], memory sense amplifiers [35], peak detectors of calibration systems [36], etc. It senses the voltage difference between two inputs and converts the analog signals into digital outputs. The response time, power consumption, sensitivity, input referred offset, and kickback noise are key elements for a comparator design, which decide the speed, power, signal to noise ratio and bit error rate of the system.

As discussed in previous chapter, to maintain the phase shifter generating constant gain quadrature outputs a voltage comparator stage is used after the peak detector to convert the voltage signal into a digital sign for charge pump adjusting feedback gate voltage V_{ctrl}. The resolution of the comparator directly decides the variation of the quadrature outputs V_{out1} and V_{out2}. Thereby, the IMRR performance is depending on the sensitivity of the voltage comparator block.

This chapter presents a high-sensitivity high-speed dynamic voltage comparator, which is a key component for low power CMOS mixed signal application. The proposed dynamic comparator employs ten transistors with only one cross-coupled latch to reduce the circuit complexity. The parallel clocked input switches reduce parasitic resistance in the latch ground path that results in a significant decrease in latch delay time. In addition, a symmetric, three stacked transistor, single stage architecture

reduces the process variation effects, increases input resolution, and provides more head room for low power-supply applications.

3.2 Comparator Architecture

3.2.1 Static Comparator

A conventional static comparator is shown in Fig 3.2.1 referred from [37], which is an opamp-type comparator. It consists of a pair of differential inputs V_{in} and V_{ip}, a current source and a pair of current load transistors M_3 and M_4. Clock signal is not applied in this circuit, so the system compares the inputs constantly. However, this circuit consumes large static power because of the constant source current.

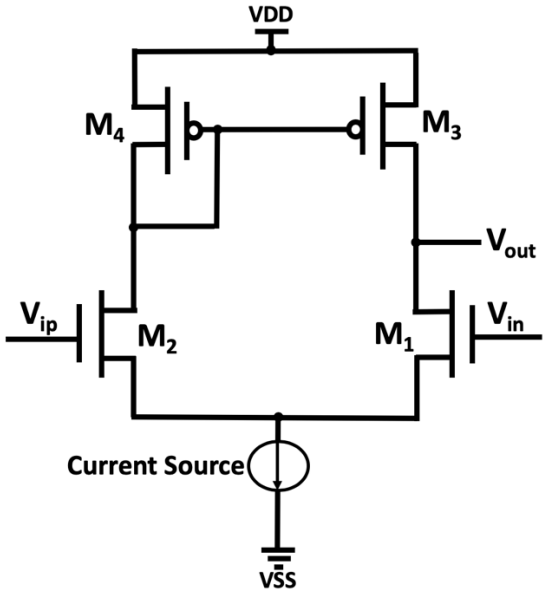


Fig 3.2.1 Conventional static comparator

A static latched comparator is expressed in Fig 3.2.2 referred from [37], which add a latch stage after the conventional static comparator. The operation of this comparator is as follows. When circuit is in reset mode, latch transistor $M_{7,8}$ is on with latch signal low, and the differential outputs V_{op} and V_{on} are pulled down to ground. While latch signal goes high, the comparator is in comparison mode, so $M_{7,8}$ turns off. M_5 and M_6

starts to charge the outputs V_{op} and V_{on} associated with first stage current mirror transistor $M_{3,4}$ and V_{ip} and V_{in}. Once one output V_{on}/V_{op} is charging to M_{10}/M_9 threshold voltage V_{tn}, the other node will go down to ground and keep the other one charging to V_{DD}. The latch block in this comparator provides more gains in regeneration process, however, the static power in this circuit is not attractive in comparator designs.

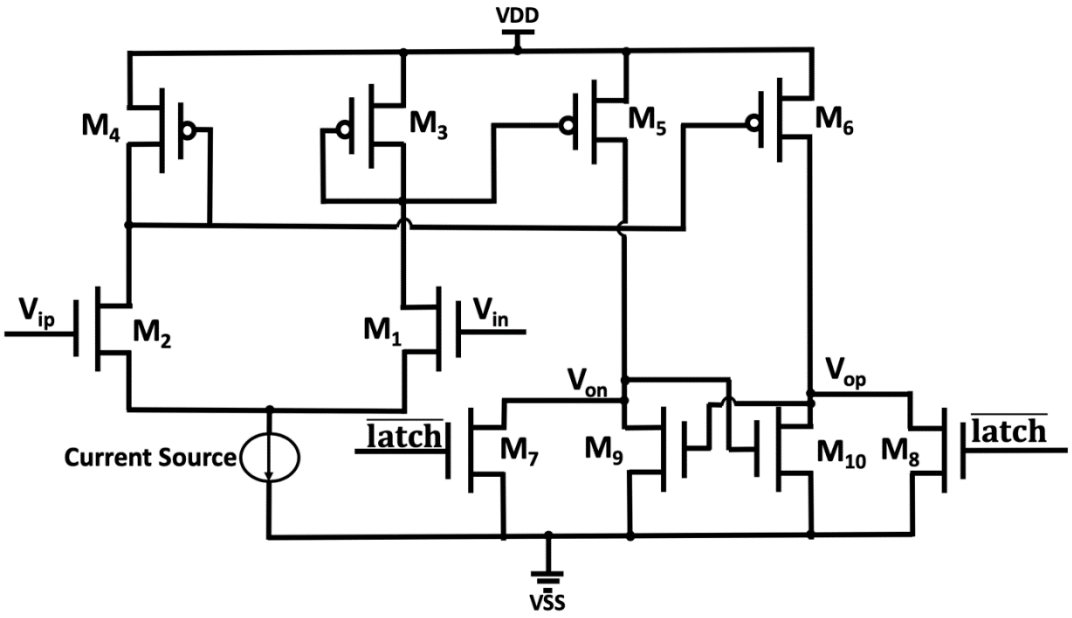


Fig 3.2.2 Static latched comparator

3.2.2 Dynamic Comparator

Dynamic comparators have the advantage of low static power consumption compared with static architectures. The conventional dynamic comparator architecture analyzed in [38] was first published by Kobayashi in [39] and continues to be a widely used structure for comparator/sense amplifier circuits in low power microelectronic applications. The high-speed rail-to-rail swing is obtained by the positive feedback of the cross-coupled latch circuit, which reduces the response time, boosts the operating frequency, and decreases the static power in evaluation mode.

There have been many alternative proposals for dynamic comparator structures

targeted for low power, high frequency, nano-scale microelectronic applications. The double-tail structure in Fig 3.2.3 provides more head room for low power-supply design due to less stacked transistors [40] [41], and an input amplifying stage is added to decrease the latch delay time for the latched dynamic comparator. Nonetheless, it suffers the trade-offs of extra delay elements and circuit complexity, which reduces the speed and sensitivity of the comparator compared with single stage dynamic comparator.

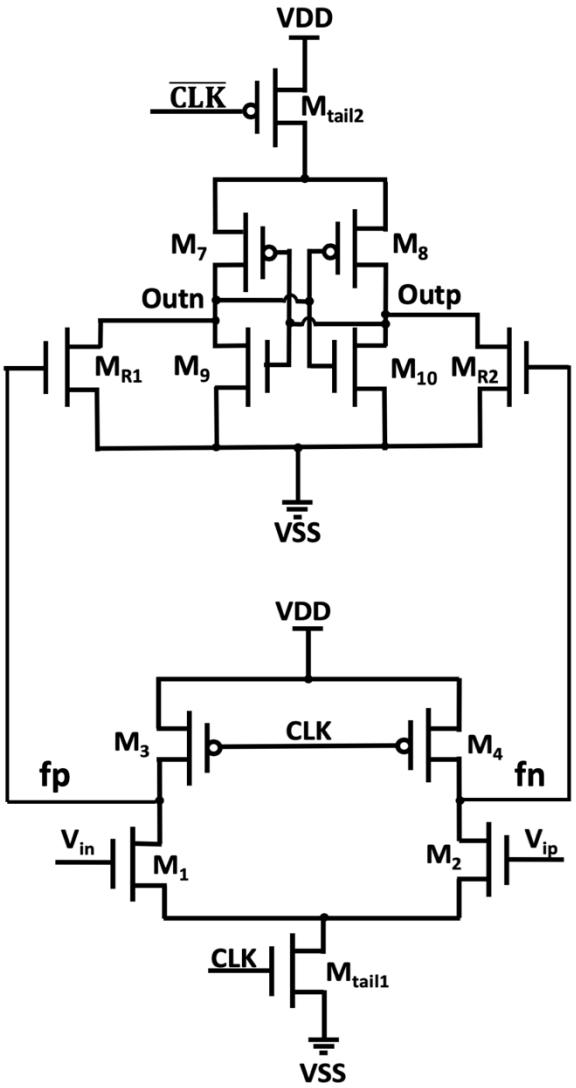


Fig 3.2.3 Conventional double-tail dynamic comparator

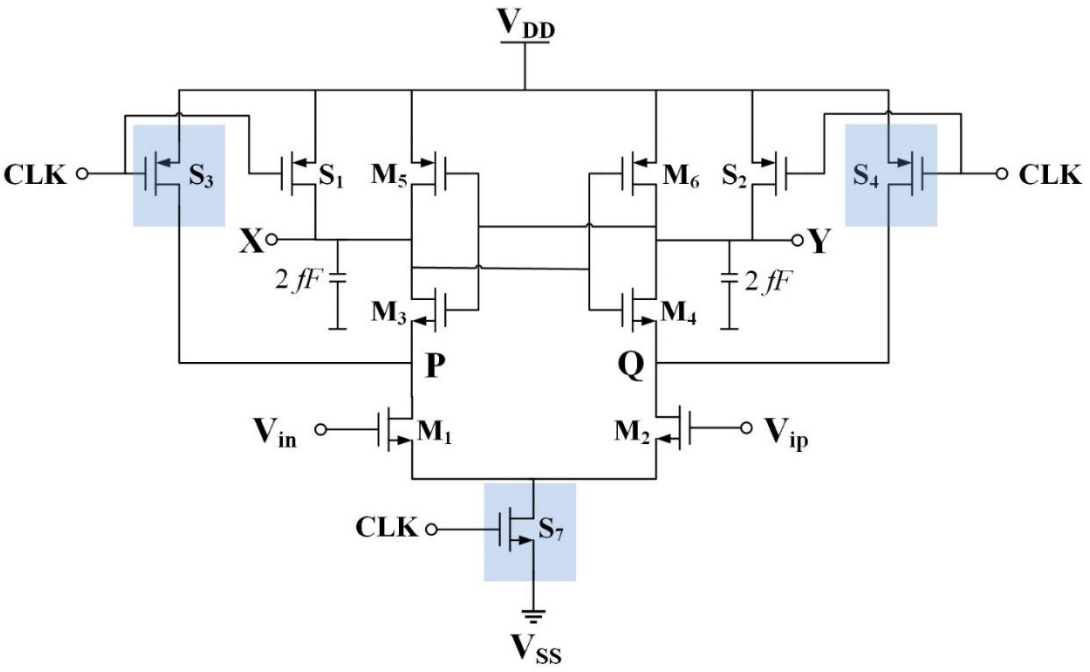


Fig 3.3.1 Conventional single-stage dynamic comparator

3.3 Conventional Single-Stage Dynamic Comparator

A conventional dynamic comparator produces rail-to-rail outputs in response to the differential inputs V_{in} and V_{ip}, while consuming no static power [38]. As shown in Fig 3.3.1, the basic components are a differential pair (M_1, M_2), four precharge switches (S_1-S_4), a tail switch S_7, and two cross coupled pairs (M_3-M_4 and M_5-M_6) to form a back-to-back latch.

The operation is as follows. The output nodes X, Y and nodes P, Q are charged to V_{DD} during the precharge phase (CLK is low). The shared source of M_1 and M_2 is charged to $V_{cm} - V_{tn}$. V_{in} and V_{ip} have the values of V_{cm} and $V_{cm} + \Delta V_{in,p}$ or vice versa. After charging of capacitors, the only current flow is leakage since the tail switch is off.

When CLK is high the circuit is in evaluation mode, which can be divided into three phases. In phase 1, evaluation begins with the tail transistor S_7 switching on as an

active resistor (R_{ON_S7}) in triode mode, and it takes the sources of M_1 and M_2 to a voltage of $2I_{cm1,2}R_{ON\_S7}$, where $R_{ON\_S7} = 1/g_{ON\_S7}$ and g_{ON_S7} represents the conductance of S_7. The switch action of S_7 activates the differential pair M_1 and M_2, which initially operate in the saturation mode with transconductance $g_{m1,2}$ in (3-3-1):

$$g_{m1,2} = \beta_{M1,2}(V_{cm} - V_{tn}) \quad (3\text{-}3\text{-}1)$$

Where $\beta_{M1,2} = K_{M1,2} \cdot (\frac{W}{L})$ and $K_{M1,2}$ is the process gain factor of $M_{1,2}$. The P and Q node capacitors at the sources of M_3 and M_4 are discharged through M_1 and M_2 at slightly unequal rates due to the $\Delta V_{in,p}$ at the inputs.

Note that the values of g_{m1} and g_{m2} are degraded by negative feedback resistance R_{ON_S7} in the source to ground path; the effective values of g_{m1} and g_{m2} are estimated as (3-3-2):

$$g_{m1,2eff} = \frac{g_{m1,2} \cdot g_{ON\_S7}}{g_{m1,2} + g_{ON\_S7}} \quad (3\text{-}3\text{-}2)$$

The differential voltage $\Delta V_{P,Q}$ at time t_1 can be estimated by (3-3-3):

$$\Delta V_{P,Q}(t_1) = |V_P - V_Q| = \frac{g_{m1,2eff} \cdot \Delta V_{in,p}}{C_{P,Q}} t_1 \quad (3\text{-}3\text{-}3)$$

M_3 and M_4 starts to turn on when P and Q reach $V_{DD} - V_{tn}$, so time t_1 ends when this occurs and is estimated by the time to discharge $C_{P,Q}$ by V_{tn} volts, which is expressed as (3-3-4):

$$t_1 = C_{P,Q} \cdot V_{tn}/I_{cm1,2} \quad (3\text{-}3\text{-}4)$$

t_2 is the time for M_3 and M_4 to discharge X and Y from V_{DD} to V_{DD}-$|V_{tp}|$ to activate the back-to-back latch formed by $M_{3,4}$ and $M_{5,6}$, and this time is recorded as phase 2. The estimated value of t_2 is calculated by (3-3-5):

$$t_2 = \frac{C_{X,Y} \cdot |V_{tp}|}{I_{m3,4}} \quad (3\text{-}3\text{-}5)$$

The differential voltage at P and Q at time t_1 results in a small difference in discharge rate of X and Y node capacitance $C_{X,Y}$. So a differential voltage $\Delta V_{X,Y}$ is developed and estimated by (3-3-6).

$$\Delta V_{X,Y}(t_2) = |V_X - V_Y| = \frac{g_{m3,4eff} \cdot \Delta V_{P,Q}(t_1)}{C_{X,Y}} t_2 \quad (3\text{-}3\text{-}6)$$

M_1 and M_2 go into triode when $V_{P,Q} = V_{cm} - V_{tn}$ and at this time the sources of M_3 and M_4 are connected to ground through active resistor $R_{ON\_M1,2}$ in series with active resistor R_{ON_S7}. With both S_7 and $M_{1,2}$ in triode, $g_{\mathrm{ON\_M1,2eff}}$ is calculated as (3-3-7):

$$g_{\mathrm{ON\_M1,2eff}} = \frac{g_{\mathrm{ON\_M1,2}} \cdot g_{ON_{S7}}}{g_{\mathrm{ON\_M1,2}} + g_{ON_{S7}}} \quad (3\text{-}3\text{-}7)$$

The effective value of $g_{m3,4eff}$ is reduced by the series active resistors in the source to ground path based on $g_{m3,4eff} = (g_{m3,4} \cdot g_{ON_{M1,2eff}})/(g_{m3,4} + g_{ON\_M1,2eff})$, and $g_{m3,4eff}$ is reduced compared to $g_{m3,4}$. The comparator is in phase 3 with $M_{5,6}$ transistor on, and the back to back latch takes the outputs to the rails with time t_3 as expressed in (3-3-8) [42]:

$$t_3 = \frac{C_{X,Y}}{g_{m,latcheff}} \ln \frac{V_{DD}/2}{\Delta V_{X,Y}(t_2)} \quad (3\text{-}3\text{-}8)$$

Where $g_{m,latcheff}$ is the effective transconductance of the latch, and it is proportional to the sum of $g_{m,latcheff}$ and $g_{m5,6eff}$. The smaller value of $g_{m3,4eff}$ due to the ground path resistance results in a smaller value of $g_{m,latcheff}$ and longer t_3. The total delay t_{total} for evaluation phase is $(t_1 + t_2 + t_3)$. Based on previous discussion, our proposed comparator will focus on reducing the parasitic resistance in the ground path for latch phase resulting in a significant reduction in the delay time. Also, if the

input voltage difference can be sensed and translated to an output voltage difference $\Delta V_{X,Y}$ during precharge phase, then the first phase t_1 for conventional comparator can be eliminated with the additional benefit of increased sensitivity.

3.4 Proposed Dynamic Comparator with Clocked Parallel Switches

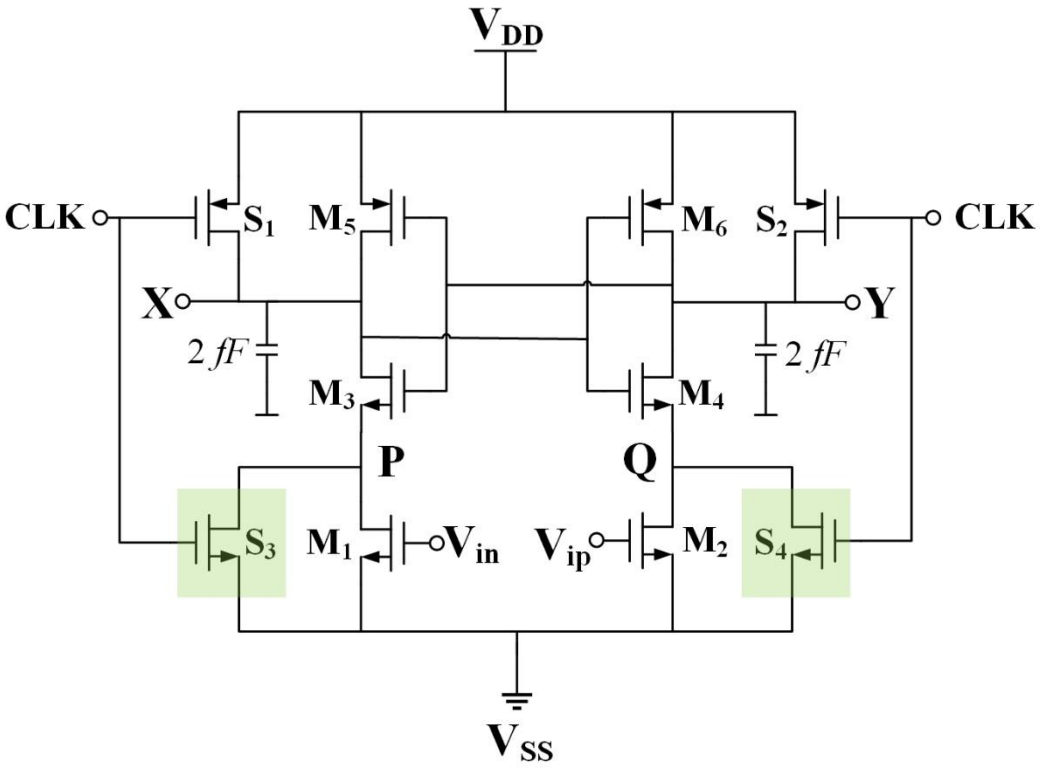


Fig 3.4.1 Proposed dynamic comparator with parallel clocked input switches

The proposed dynamic comparator is shown in Fig 3.4.1. As seen the structure has similarities to the conventional comparator but with addition of two clocked parallel n-channel switches S_3 and S_4 and the deletion of the tail switch S_7 and two clocked p-channel precharge switches S_3 and S_4. The basic motivation is to reduce the parasitic active resistance in the ground path during evaluation phase resulting in significant decrease in delay time. Additionally, a differential voltage proportional to the input difference $\Delta V_{in,p}$ is produced at the output nodes during precharge mode to eliminate

the requirement for differential sensing during evaluation phase and also presenting the opportunity for increased sensitivity.

The basic operation is as follows. When CLK is low, the comparator is in precharge mode. S_3 and S_4 switch off, while S_1 and S_2 are switched on to precharge $V_{X,Y}$ to near V_{DD} causing $M_{5,6}$ to be off. M_1 and M_2 are on with input difference $\Delta V_{in,p}$, which creates a current difference $\Delta I_{in,p}$ at nodes X and Y. Since the precharge phase is relatively long, the capacitors $C_{P,Q}$ and $C_{X,Y}$ reach a steady state value drawing no current. Then drain currents and current differences of $M_{1,2}$, $M_{3,4}$ and $S_{1,2}$ must be the same at the end of the precharge phase. Note that the node voltage $V_{P,Q}$ are near a value of $V_{DD} - V_{cm}$ (depending on the ratios of $\beta m_{1,2}$ to $\beta m_{3,4}$) to force $I_{cm1,2} = I_{cm3,4}$. The equality of drain currents requires the following ratio to hold in (3-4-1) to (3-4-2):

$$\frac{\Delta V_{P,Q}(t_0)}{\Delta V_{in,p}(t_0)} = \frac{\beta_{m1,2}(V_{cm}-V_{tn1,2})}{\beta_{m3,4}(V_{DD}-V_{P,Q}-V_{tnm3,4})} \tag{3-4-1}$$

$$\frac{\Delta V_{X,Y}(t_0)}{\Delta V_{in,p}(t_0)} = \frac{\beta_{m1,2}(V_{cm}-V_{tn1,2})}{\beta_{S1,2}(V_{DD}-|V_{tpS1,2}|)} \tag{3-4-2}$$

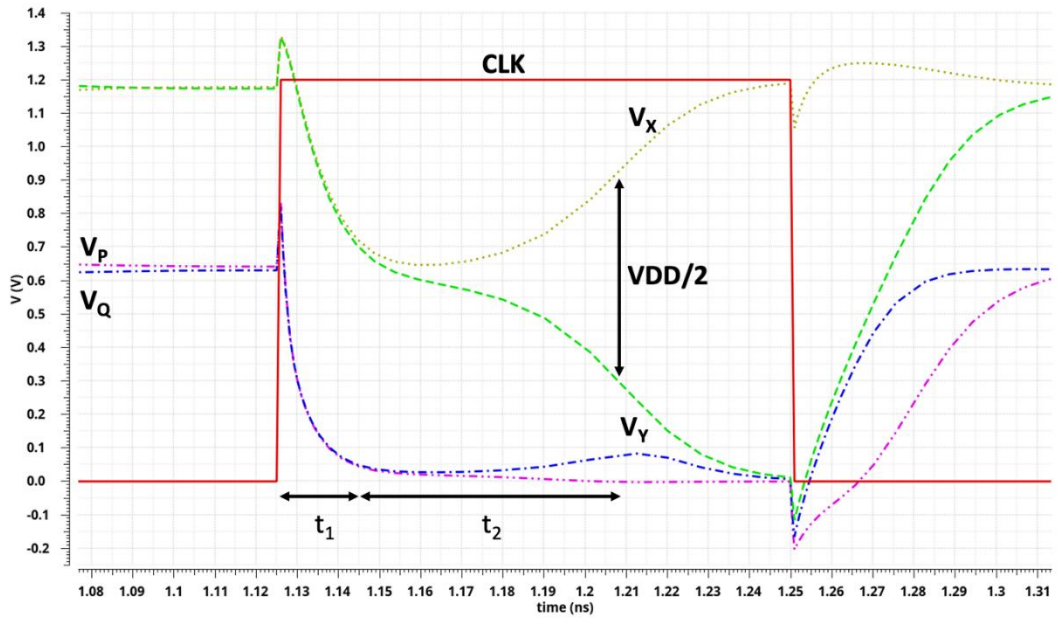


Fig 3.4.2 Evaluation mode of proposed dynamic comparator

In this case, at the end of precharge phase, the differential voltages have been

established at $\Delta V_{P,Q}$ and $\Delta V_{X,Y}$ proportional to $\Delta V_{in,p}$. Note that the $\Delta V_{X,Y}/\Delta V_{in,p}$ and $\Delta V_{P,Q}/\Delta V_{in,p}$ are independent of the node capacitances $C_{P,Q}$ and $C_{X,Y}$. When clock is high, the comparator is in evaluation mode, and it can be divided into two phases as shown in Fig 3.4.2. Phase 1 is the latch activation mode, switches S_3 and S_4 are clocked on (in triode mode) with relatively large conductance $g_{ON\_S3,4}$. M_1 and M_2 are initially in the saturation state with drain voltage of about $V_{DD} - V_{cm}$, but quickly enter triode mode due to fast pull-down action of $S_{3,4}$ in parallel with $M_{1,2}$. Then the effective transconductance in $M_{3,4}$ ground path is $g_{ON\_S3,4} + g_{ON\_M1,2}$ so the effective transconductance $M_{3,4}$ ($g_{m3,4}$) is derived in (3-4-3).

$$g_{m3,4eff} = \frac{g_{m3,4}(g_{ON\_S3,4}+g_{ON\_M1,2})}{g_{m3,4}+g_{ON\_S3,4}+g_{ON\_M1,2}} \approx g_{m3,4} \quad (3\text{-}4\text{-}3)$$

Unlike the conventional dynamic comparator, the transconductance $g_{m3,4}$ has very little reduction due to the ground path resistance. So the effective action of $M_{1,2}$ and $S_{3,4}$ quickly discharge $C_{P,Q}$, which increases the drain currents $I_{m3,4}$ to discharge node voltage of $V_{X,Y}$ from near V_{DD} to $V_{DD} - |V_{tp}|$ turning on $M_{5,6}$ and activating the back to back latch. The latch activation time t_1 is calculated as $t_1 = C_{X,Y} \cdot |V_{tp}|/I_{m3,4}$, and voltage difference for output nodes at t_1 are expressed in (3-4-4):

$$\Delta V_{X,Y}(t_1) = \frac{g_{m3,4eff} \cdot \Delta V_{P,Q}(t_0)}{C_{X,Y}} t_1 + \Delta V_{X,Y}(t_0) \quad (3\text{-}4\text{-}4)$$

The second phase in evaluation mode is the latch delay t_2. With $M_{5,6}$ on, the back-to-back latch takes the outputs to the rails with time t_2 [42] in (3-4-5):

$$t_2 = \frac{C_{X,Y}}{g_{m,latcheff}} \ln \frac{V_{DD}/2}{\Delta V_{X,Y}(t_1)} \quad (3\text{-}4\text{-}5)$$

Where $g_{m,latcheff}$ is the effective transconductance of the latch, and is proportional to the sum of $g_{m5,6eff}$ and $g_{m3,4eff}$. For this proposed dynamic

comparator, $g_{m3,4eff}$ has not been reduced by ground path resistance so the total delay of evaluation phase $t_{total} = t_1 + t_2$ is much smaller than the latch delay in conventional comparator.

3.5 Simulation Results

The proposed dynamic comparator is implemented in Cadence Virtuoso software (shown in Fig 3.5.1) with transistor size shown in Table 3.5.1. A conventional latched comparator in [38] is also implemented under the same process for comparison with the sizes in Table 3.5.1. A comparison of the response time (evaluation delay time) between conventional and proposed dynamic comparator is given in Fig 3.5.2 under 30μV $\Delta V_{in,p}$, 0.6V V_{cm}, 500MHz clock frequency and 2fF load capacitance. The response delay of conventional latch is 452ps compared to 175ps for the proposed comparator, demonstrating that the maximum operating frequency is limited by the large parasitic resistance in ground path and longer latch delay in a conventional design.

Table 3.5.1 Transistor Sizes

Conventional Dynamic Comparator		Proposed Dynamic Comparator	
Transistor Name	Aspect ratio (W/L in μm)	Transistor Name	Aspect ratio (W/L in μm)
S_1/S_2	1/0.1	S_1/S_2	1.8/0.1
S_3/S_4	1/0.1	S_3/S_4	1.2/0.1
S_7	3/0.1	-	-
M_1/M_2	1.5/0.1	M_1/M_2	0.88/0.1
M_3/M_4	1.25/0.1	M_3/M_4	1.25/0.1
M_5/M_6	2.5/0.1	M_5/M_6	2.5/0.1

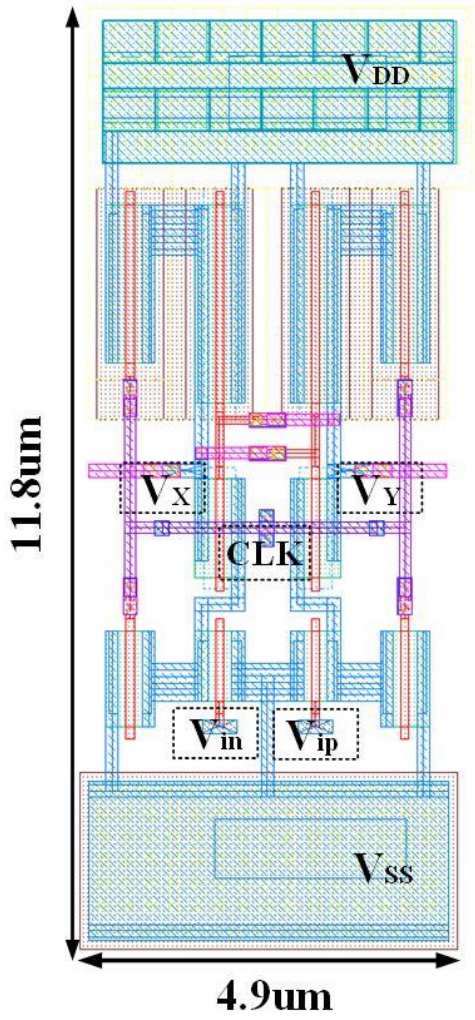


Fig 3.5.1 CMOS implementation of proposed dynamic voltage comparator

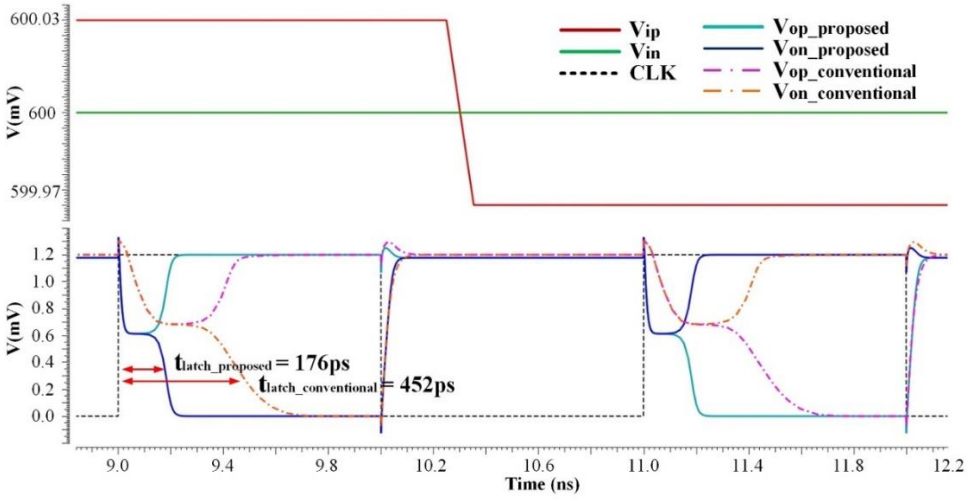
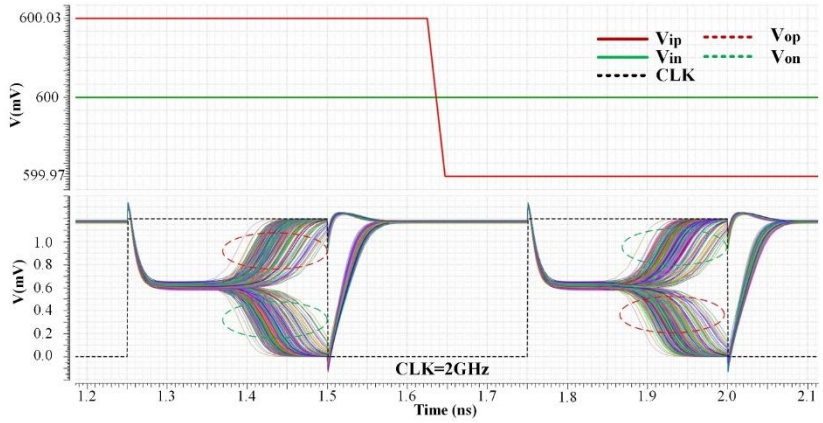
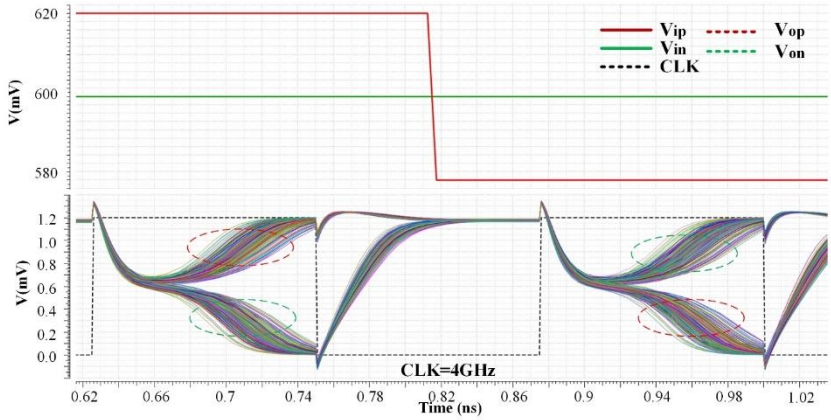


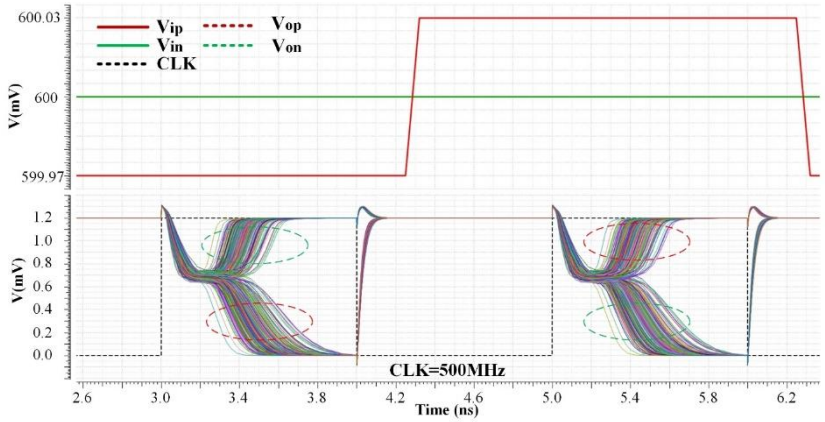
Fig 3.5.2 Transient simulation of proposed comparator versus conventional comparator



(a)



(b)



(c)

Fig 3.5.3 Transient simulation results with considering process variations: (a) Proposed design for CLK=2GHz (b) Proposed design for CLK=4GHz (c) Conventional design for CLK=500MHz

Monte Carlo Analysis is applied to assess process variation effects with 200 runs. The test configuration is 0.6V V_{cm} with 2fF output load capacitance. A transient

simulation plot of the proposed design under process variations is shown in Fig 3.5.3. The average power consumption of the proposed comparator over the 200 Monte Carlo runs is 100.8μW with 30μV $\Delta V_{in,p}$ and 2GHz CLK, and 131.4μW with 20mV $\Delta V_{in,p}$ and 4GHz CLK . The response delay is averaged at 189.4ps and 77.8ps with 30μV and 20mV input resolution, respectively. The 1-sigma value of delay and power are calculated as 19.64ps and 6.89μW at 30μV $\Delta V_{in,p}$ and 7.17ps and 5.89μW at 20mV $\Delta V_{in,p}$ compared with 68.66ps and 0.59μW for 500MHz clock for the conventional dynamic comparator in Fig 3.5.4. The proposed comparator retains full functionality for all of the 200 runs of the Monte Carlo analysis.

Performance comparisons of this work with conventional dynamic comparator and other alternatives are summarized in Table 3.5.2. The structures in [34], [43], [40], [37] and [44] all incorporate an input amplifying/latch stage to generate a differential input voltage to the output latch resulting in increased complexity and delay compared to the proposed design. The data under [38] is based on our implementation of conventional latch in same process.

Table 3.5.2 Performance comparison of dynamic voltage comparators

Parameters	[34]	[43]	[40]	[37]	[44]	[38]	This work		
Technology	65nm 1.2V	180nm 1.8V	180nm 1.2V	40nm 1.1V	180nm 1.8V	90nm 1.2V	90nm 1.2V		
Design Type	Layout	Layout	Layout	Fabrication	Layout	Schematic	Layout		
Power (μW)	376	420	1400	346	347	22	106	77	131
Frequency (GHz)	0.02	0.5	2.4	6	0.5	0.5	2	2	4
Sensitivity (mV)	0.036	1	7.8	20	2.19	0.03	0.03	20	20
Delay Time (ns)	13	0.3	0.3	0.06	0.35	0.45	0.19	0.08	0.08
Area (μm^2)	-	486	392	64.5	361	-	57.8		

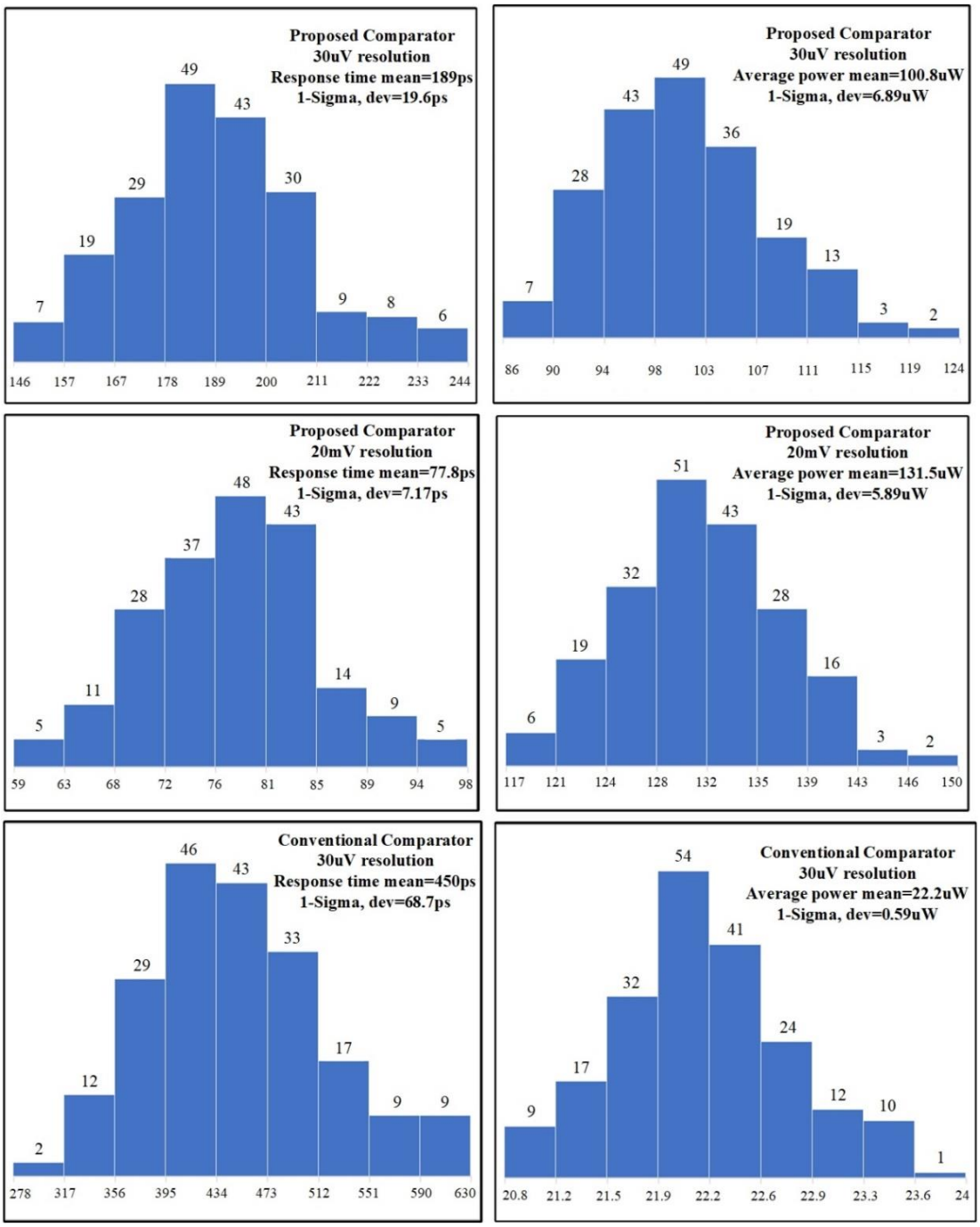


Fig 3.5.4 Monte-Carlo simulation results for proposed and conventional dynamic comparator

3.6 Conclusion

This dissertation presents a 10-transistor dynamic comparator with parallel clocked input switches that decreases the response time in evaluation mode along with

improved sensitivity. The proposed circuit performs input differential sensing simultaneously with pre-charge and the magnitude of the differential output voltage is independent of the magnitude of the output node capacitance. This eliminates the need for generating differential output voltages during evaluation phase resulting in the back-to-back latch activation at earlier time. The parallel clocked input switches with relatively high conductance result in low parasitic resistance in ground path of latch circuit significantly reducing latch delay. The proposed circuit draws static power in precharge phase, but the current is limited by the drain current of input transistors. Also, only two nodes are precharged to V_{DD}, so the average power consumption compares favorably to existing implementations. Meanwhile, it maintains 100% functionality under simulated process variations due to the symmetric and low-complexity architecture. Compared with conventional single stage and double-tail dynamic comparators, the proposed design has balanced properties of sensitivity, speed and power consumption, which is used in the integrated on-line amplitude locked loop calibration system.

IV. Integrated On-line Amplitude Locked Loop Calibration System

(The discussion in the following chapter is substantially drawn from [28], where we first reported the development and evaluation of this technique.)

4.1 Introduction

As mentioned in previous chapters, a calibration system is needed to vary the control voltage of active RC-CR phase shifter for variable input frequency and compensate process variation. A top-level block diagram of the proposed calibration system is explained in Chapter 2. A detailed analysis of sub-circuits in integrated on-line amplitude locked loop calibration system is added in this chapter.

4.2 Sub-circuits in Calibration System

4.2.1 Peak Detector

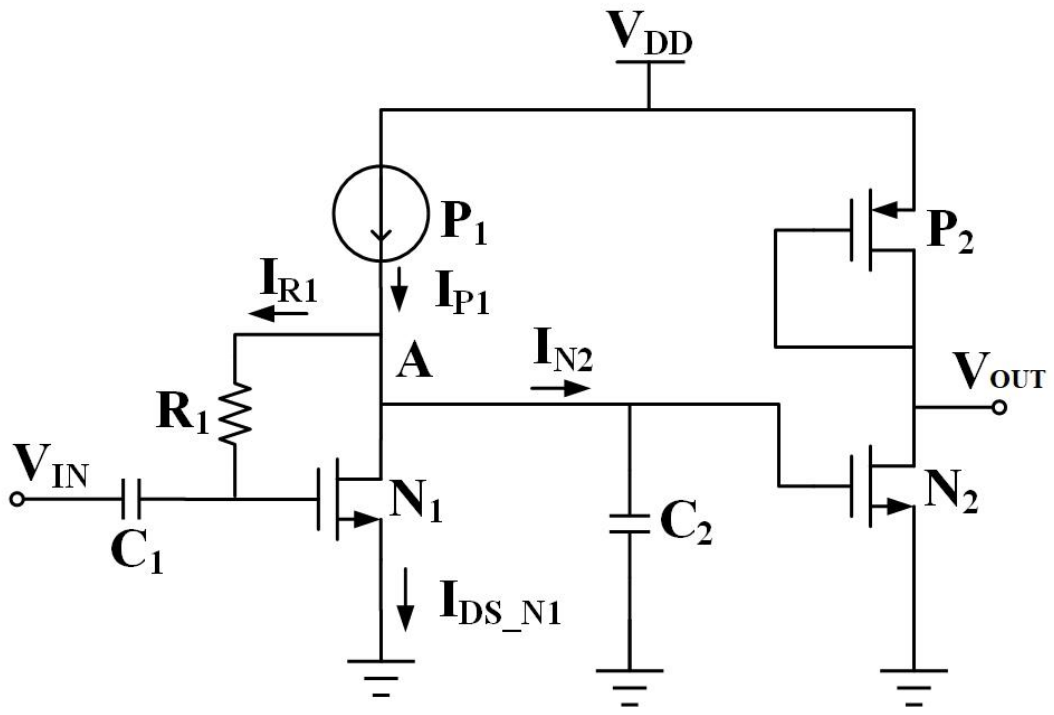


Fig 4.2.1 Schematic diagram of peak detector

A low power CMOS peak detector is used in this proposed architecture as the second stage to convert the amplitude of $V_{out1,2}$ into corresponding DC voltage [45]. It consists of two stages. The first stage detects the amplitudes and converts them into DC results, and the second stage is an active load amplifier to enhance the detection sensitivity and flip the inverted results of stage-one.

As seen in Fig 4.2.1, C_1 is a DC blocking capacitor, and R_1 is a voltage feedback resistor between the drain of N_1 and the AC input voltage (gate voltage). In the first stage, the current of current source P_1, feedback current through R_1, and drain to source current of N_1 are balanced at node A. Since current across R_1 is also the gate leakage current of N_1 which is very small, I_{DS} of N_1 is approximately equal to I_{P1}. To maintain the equality, if the amplitude of V_{in} increases, the drain voltage of N_1 (also the voltage of node A) must be reduced to keep the same current as I_{P1}. Thus, the DC voltage at node A is inversely proportional to input amplitude, and this DC result is held by C_2. To improve the detection sensitivity and reduce following circuits design complexity, an active load inverter amplifier/buffer is used as an output stage to drive the follow-on comparators which is consisted of P_2 and N_2 transistors

4.2.2 Comparator

A high-speed high-sensitivity dynamic latched comparator is placed at the third stage to convert the voltage signal from peak detector to digital signal. As mentioned in Chapter 3, the proposed dynamic voltage comparator is used in the calibration system. The high sensitivity of the latched comparator significantly improves the comparison resolution of peak detector outputs.

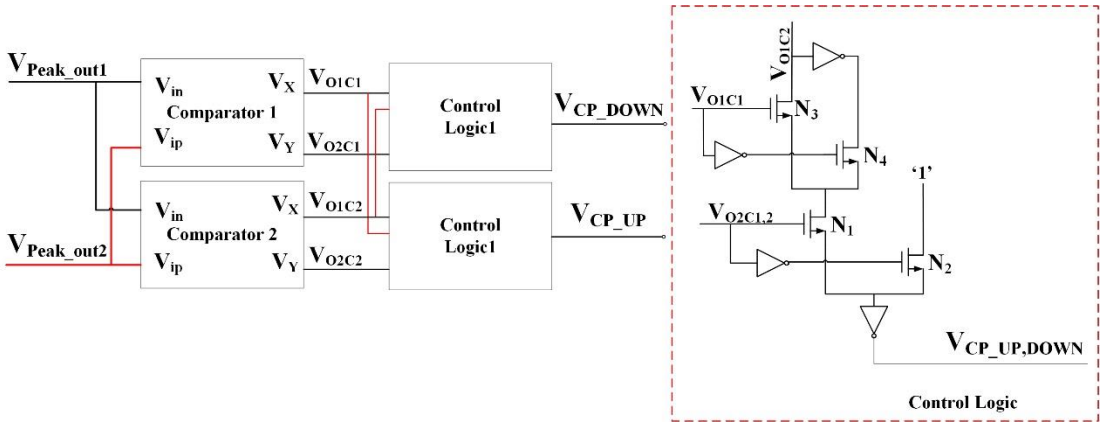
However, a small variation of amplitude difference between V_{out1} and V_{out2}

caused by the input AC signal coupling onto V_{ctrl} exists in the active 90-degree phase shifter. It triggers the high sensitivity comparators to keep output opposite results and oscillates the charge pump to generate up or down signals. To eliminate the high frequency oscillations, a digital filter logic block is added after the parallel comparators.

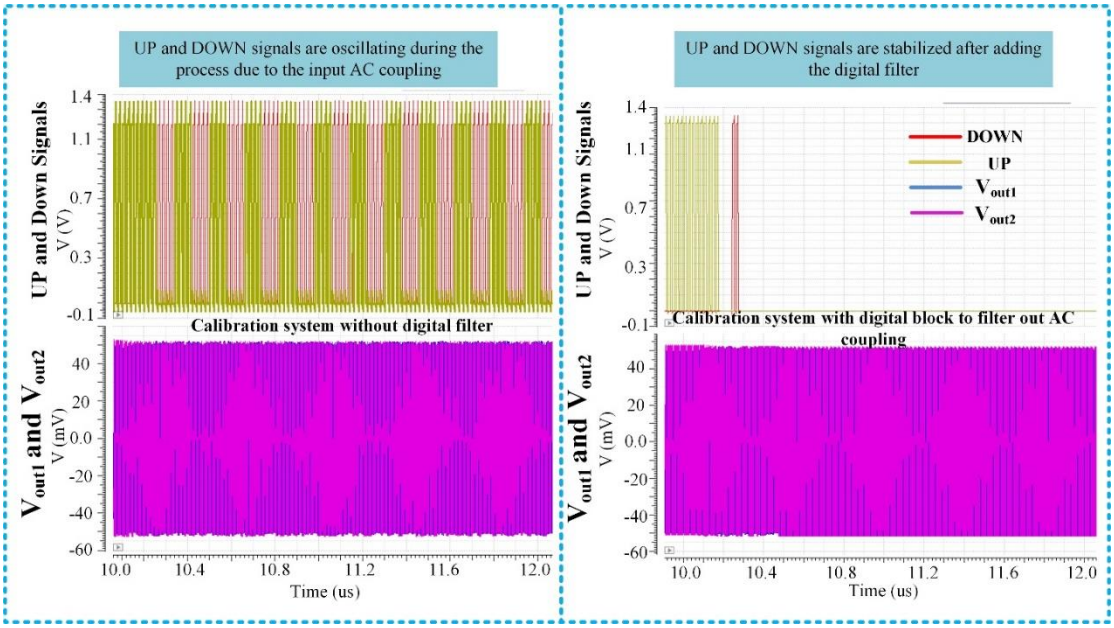
4.2.3 Proposed Digital Control Logic

The basic operation of the digital logic block is as follows. The outputs of comparators V_{O1C1} and V_{O1C2} are inputs to the control block in digital logic system as demonstrated in Fig 4.2.2 (a), which works as a switch to select either V_{O2C1} or V_{O2C2} passing through next stage charge pump. The truth table of the operation is shown in Table 4.2.1. Charge pump only regulates the system when two comparators have reverse results, which only occurs during the calibration process. Then the logic block stops passing adjusting commands to charge pump when two outputs from comparators are very close and have the same digital results ('00' or '11'). It limits the jitters on V_{ctrl} so that V_{out1} and V_{out2} are specified in constant amplitudes.

Transient simulation plots of the comparison between with and without digital control logic in this system is shown in Fig 4.2.2 (b), which is simulated in Cadence 90nm technology with 1.2V V_{DD}. The calibration system is much more stable after adding this digital control logic. Note that, two identical inverters are placed after comparator outputs V_X and V_Y to keep same output load, and the connections between comparator outputs and charge pumps are reversed (V_{O2C1} to 'DOWN', and V_{O2C2} to 'UP').



(a)



(b)

Fig 4.2.2 Proposed digital control logic system: (a) System architecture (b) Comparison of transient simulation waveform

Table 4.2.1 Truth table of digital control logic

V_{O1C1}	V_{O1C2}	$V_{O2C1,2}$	$V_{CP\_UP,DOWN}$
0	0	DN	0
1	1	DN	0
0	1	0	0
1	0	0	0
0	1	1	1
1	0	1	1

4.2.4 Charge Pump

A standard charge pump shown in Fig 4.2.3 is used in this system followed by a loop filter [46]. When the amplitude of V_{out1} is greater than V_{out2}, a positive ΔV is generated from two peak detectors (Fig 2.5.1), which propagates a 'DOWN' signal from the logic block to control the pull up network of charge pump. The top current source is activated to charge capacitor C_P and increases the V_{ctrl} through the Analog Buffer (AB). If V_{out1} has a smaller amplitude, then a negative ΔV will activate the 'UP' signal through comparators and logic gate, and V_{ctrl} is reduced by the bottom current source discharging C_P. The loop filter formed by R, C_P, and C results in a stable feedback voltage (V_{ctrl}) with the required damping and no oscillation.

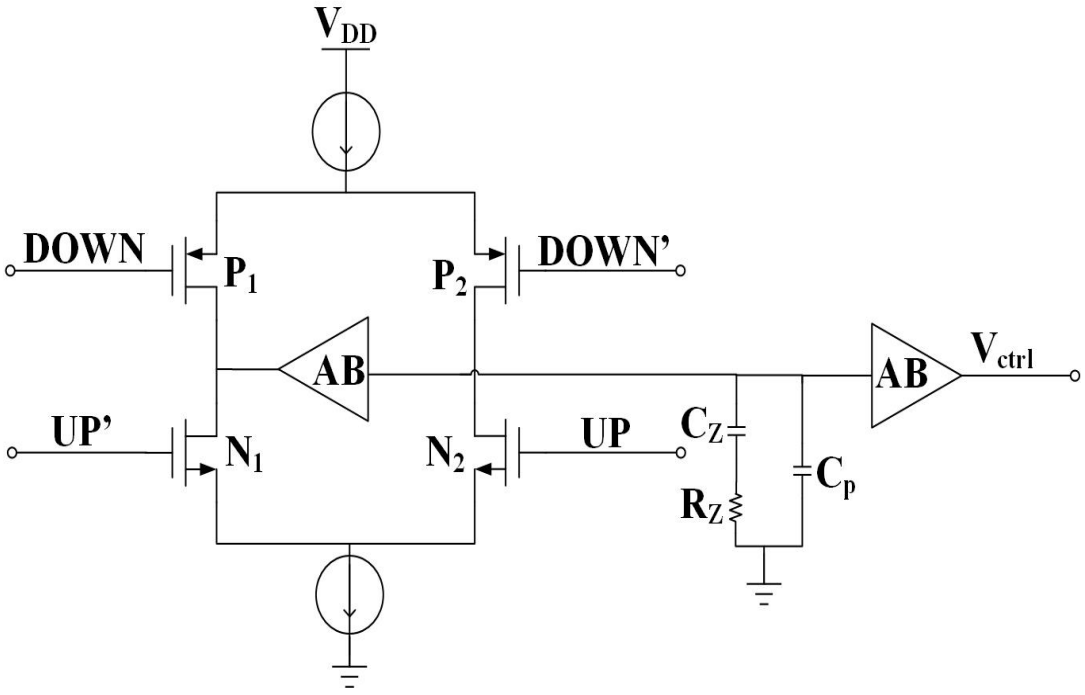


Fig 4.2.3 Schematic diagram of charge pump circuit

4.3 Simulation Results

The proposed 90-degree phase shifter calibration system is designed and simulated

in 65nm technology with Cadence Virtuoso software shown in Fig 4.3.1. The schematic implementation of each sub-circuits is also explained in Fig 4.3.2 (a)-(d) for peak detector, comparator, control logic and charge pump separately.

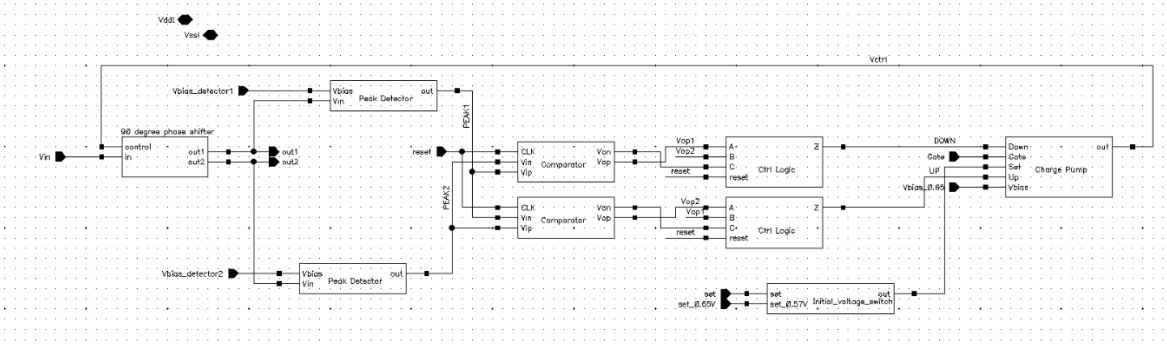
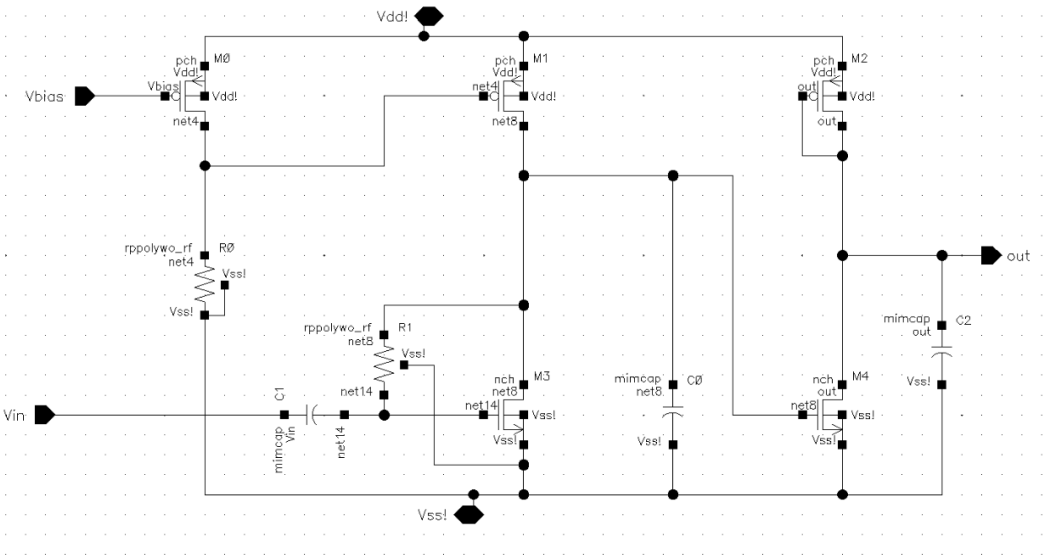
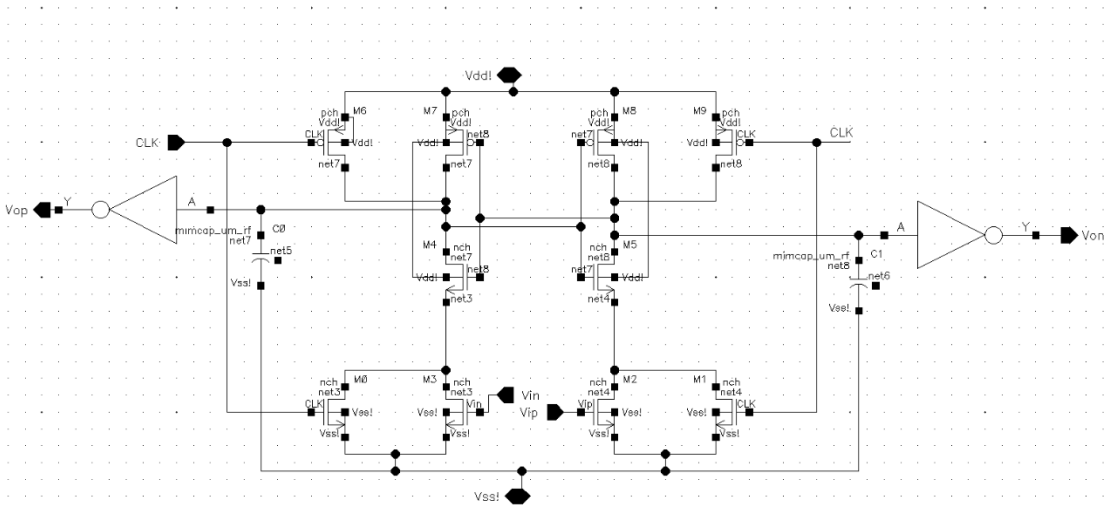


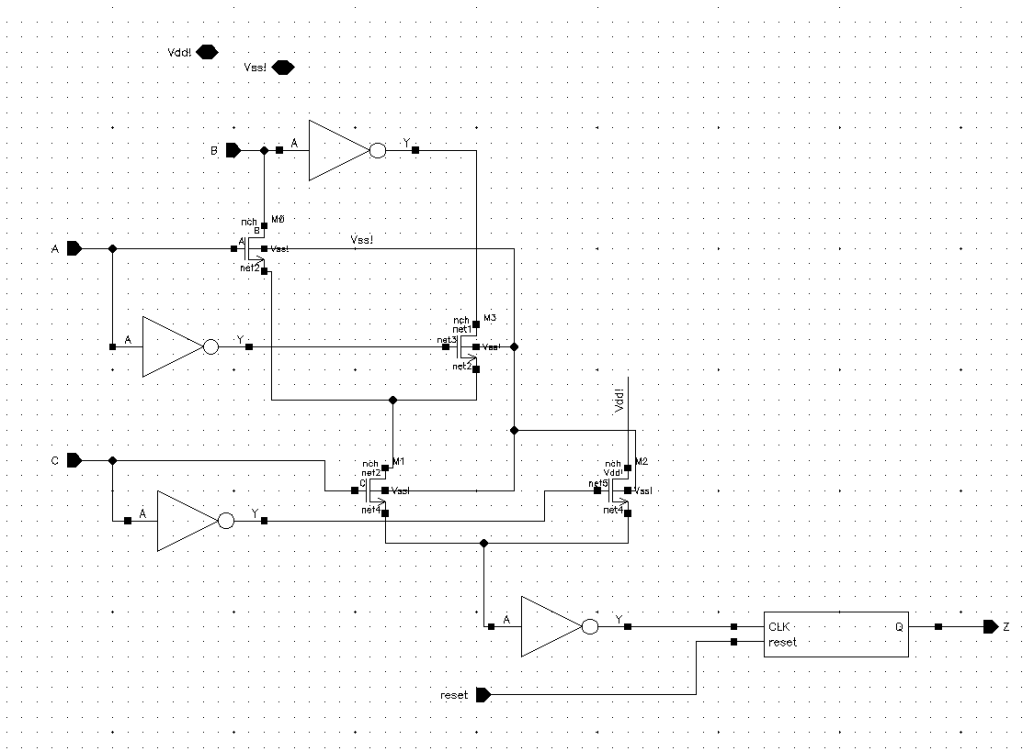
Fig 4.3.1 Block diagram of proposed 90-degree active phase shifter with integrated on-line amplitude locked loop calibration



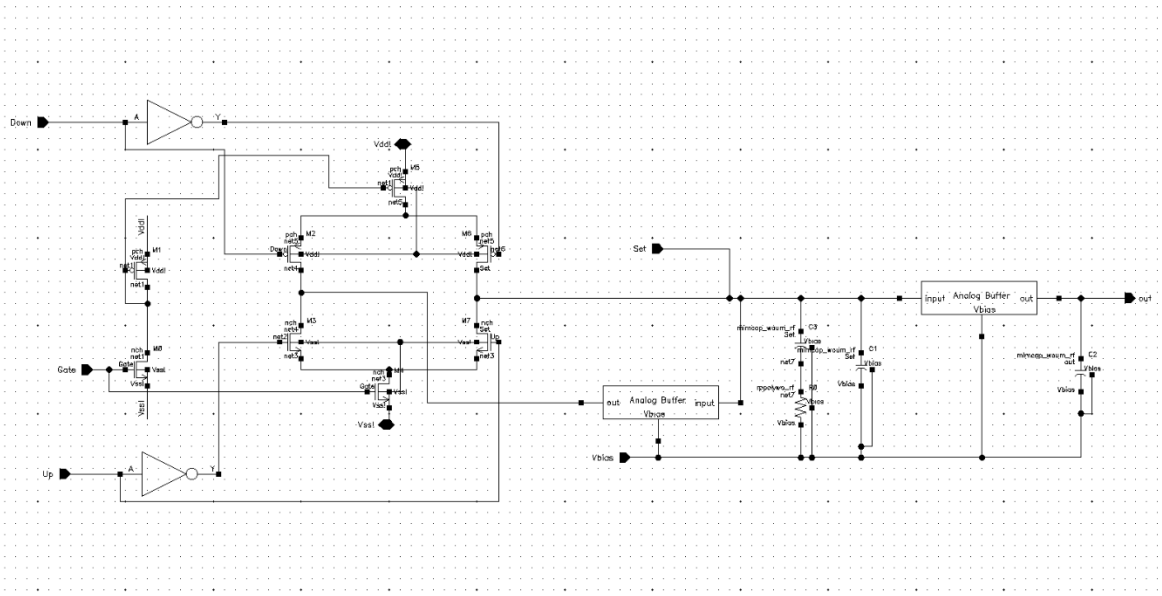
(a)


Vdd!
CLK
Vop
Y
A
mimcap_um_rf
C0
net5
Vss!
M6
M7
M8
M9
M4
M5
M0
M3
M2
M1
Vin
Vip
net3
net4
net6
C1
Von

(b)


Vdd!
Vss!
B
A
Y
C
M0
M1
M2
M3
CLK
reset
Q
Z

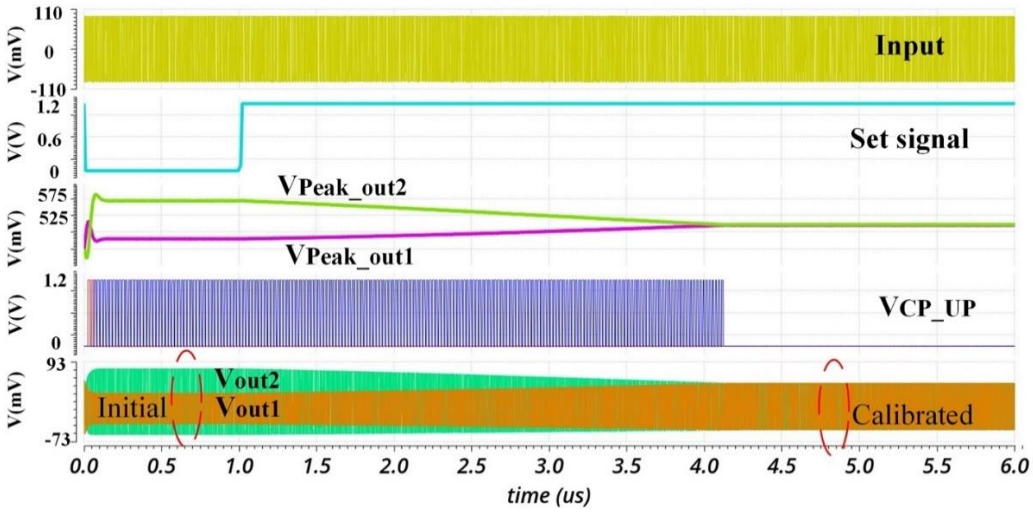
(c)



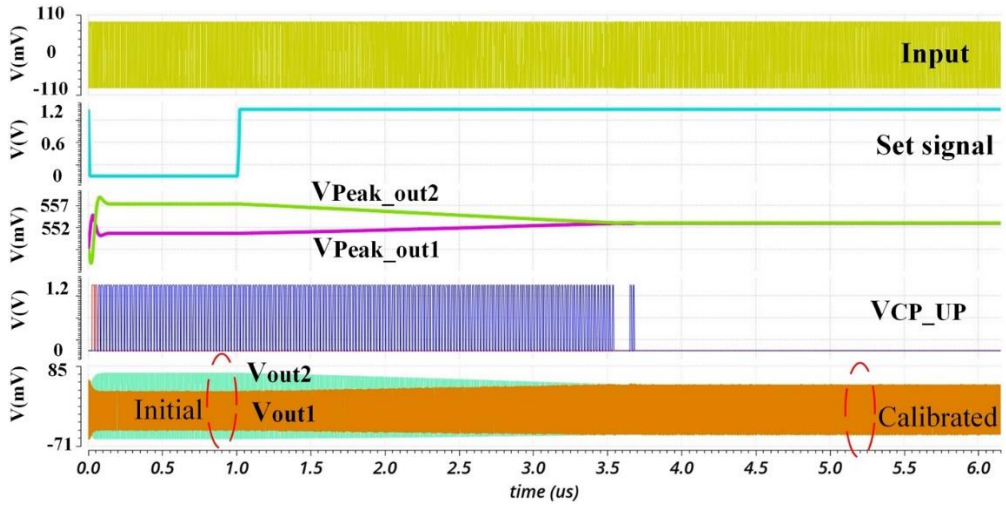
(d)

Fig 4.3.2 Schematic diagram of (a) Peak detector (b) Dynamic comparator (c) Digital logic filter (d) Charge pump

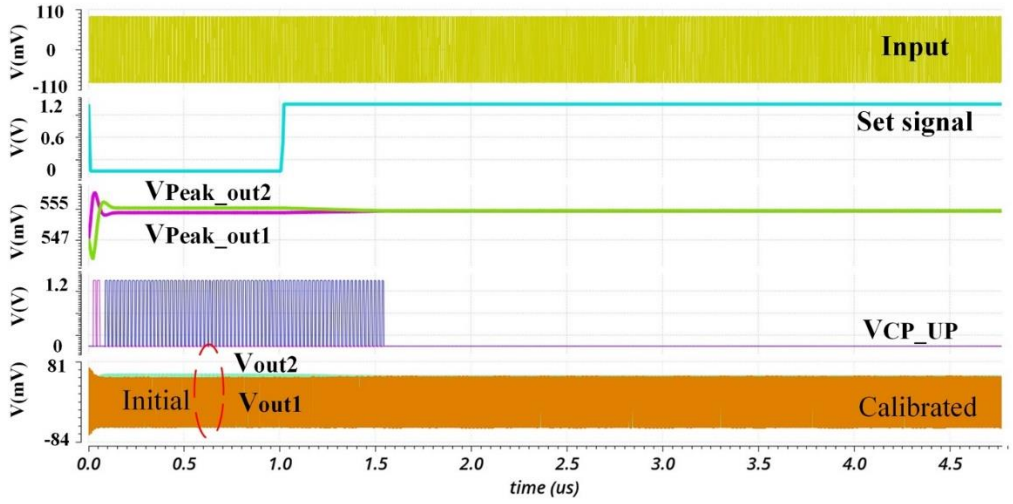
The transient simulation plots of the proposed calibration system working at 600MHz, 2.4GHz and 3.8GHz are shown in Fig 4.3.3 (a)-(c) respectively, and a zoom in version of the circuit outputs before and after calibration at 3.8GHz input frequency is presented in Fig 4.3.4 (a) and (b) for simplicity.



(a)

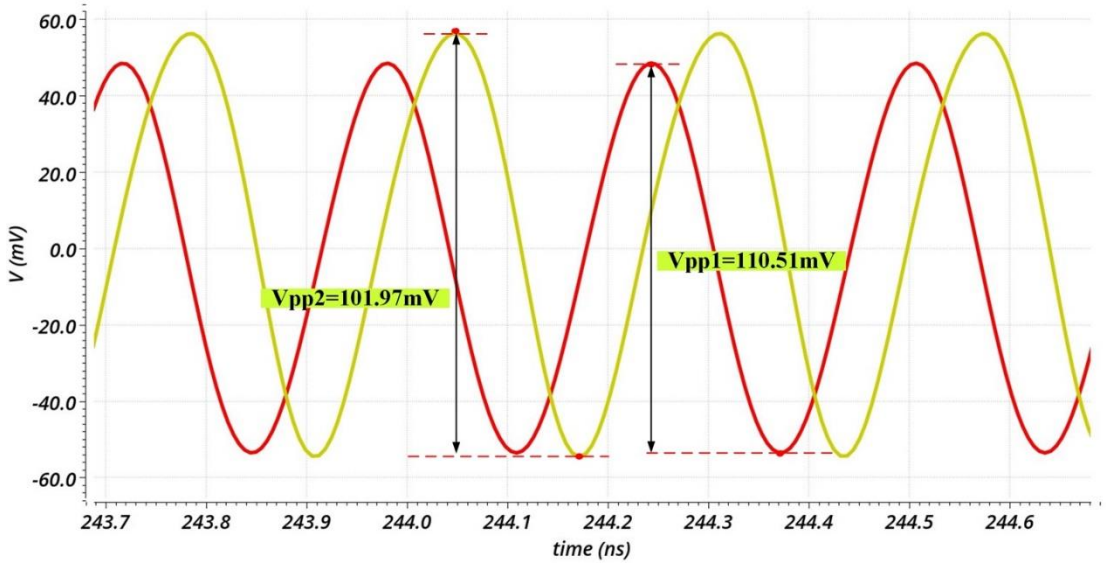


(b)

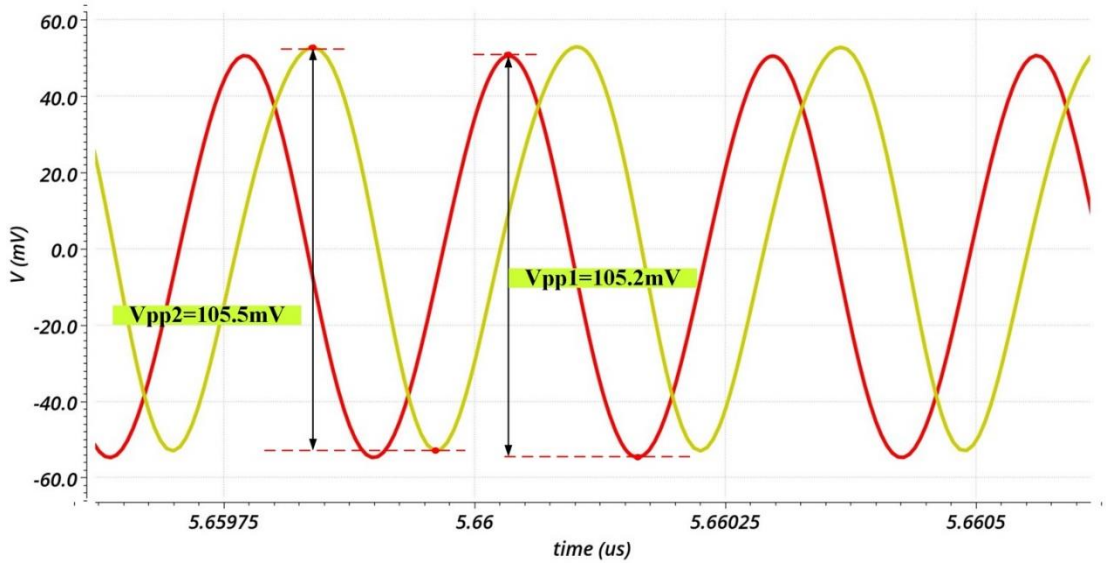


(c)

Fig 4.3.3 Transient simulation waveform of proposed 90-degree phase shifter with on-line ALL calibration system at (a) 600MHz (b) 2.4GHz (c) 3.8GHz



(a)



(b)

Fig 4.3.4 Transient simulation results of output waveforms (a) Before calibration (b) After calibration

The circuit starts to adjust output $V_{out1,2}$ after the set signal going to high, and decisions are made by comparing peak detector output $V_{Peak\_out1,2}$. For the case $V_{Peak\_out1} < V_{Peak\_out2}$, comparator logic blocks generate a UP signal for charge pump to increase theV_{ctrl} in order to reduce R_{ON}, and the pole frequency in this case is adjusted to input frequency. The phase shifter system is then locked at the desired

frequency and pauses calibration process.

4.4 Conclusion

The integrated on-line amplitude locked loop calibration system introduced in this chapter can be used for active RC-CR 90-degree phase shifter. The proposed system successfully converts the output amplitudes information into voltage, and compares the voltage error between two outputs, then, uses the digital signal from comparators to control the feedback signal, and realizes the calibration loop. The input frequency range is 600MHz to 930MHz for lower band phase shifter, and 2.4GHz to 3.8GHz for higher band phase shifter. The power consumption of the proposed calibration system is 1.64mW at 600MHz, 1.66mW at 2.4GHz and 1.77mW at 3.8GHz. The response time of the calibration system is 3.21us for 600MHz, 2.74us for 2.4GHz and 624.74ns for 3.8GHz.

V. Phase-Domain Digital Phase Locked Loop

5.1 Introduction

Phase locked loop is a negative feedback system to maintain the oscillator generating constant phase and frequency outputs related with the low frequency reference signal [47]. A conventional PLL is shown in Fig 5.1.1 with Laplace Transform theory, where the basic components are phase frequency detector, charge pump, voltage control oscillator and feedback frequency divider. Phase detector detects the phase difference between the divided VCO output frequency and crystal reference frequency. Charge pump converts the phase error information e(s) of PD to voltage information after loop filter to control VCO output frequency

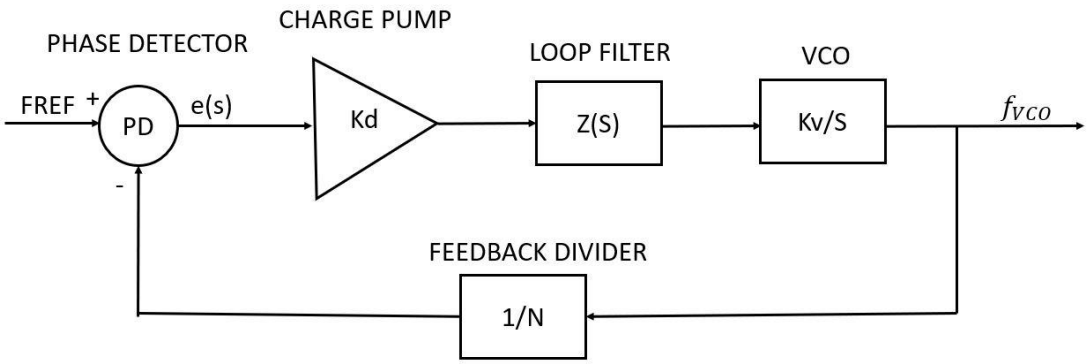


Fig 5.1.1 Basic model of PLL

There are three types of PLLs, analog PLL, all digital PLL and mixed analog and digital PLL. Compared to analog PLL, Digital PLL (DPLL) has the advantages of small area, high performance, highly programmable, low cost, and immunity of noise. With CMOS process feature size shrinks and power voltage goes down, and digital PLL's flexibility of redesigning and low phase noise nature [48] [49] [50] [51] [52], this

research focuses on ADPLL design.

In digital PLLs, the subcircuits are implemented digitally. The phase frequency detector is replaced by Digital Phase Frequency Detector (DPFD) with Time to Digital Converter (TDC) to encode the phase error information between DCO output and reference signal; A Digital Loop Filter (DLF) is used to replace the passive loop filter and convert the DPFD outputs into DCO varactor bank control codes; Digital control oscillator is employed instead of VCO to generate constant outputs; Dual-modulus pre-scaler or delta-sigma modulator is also implemented digitally to realize dividing function.

There are two categories of digital PLLs: integer DPLL and fractional DPLL. For the integer DPLL, the output frequency is an integer number times the reference frequency. However, the Phase Noise (PN) of the system is dramatically increased for a higher order of integer-N divider when finer resolution is required. In wireless communication, PN is particularly produced by a frequency synthesizer, which plays an important role in Signal-to-Noise Ratio (SNR) for a receiver system and affects the Effective Number of Bits (ENB) for ADC. The fractional DPLLs are proposed to realize the fractional dividing function without increasing the order of N-dividers. The pre-scalers and dual modulus pre-scalers techniques are proposed to replace the conventional N-dividers and realize fractional-N dividing function [53] [54] [55], but periodical signal introduced by the pre-scaler module appears as sidebands around the operating frequencies. The Delta-Sigma Modulator (DSM) is widely used in fractional-N PLLs [56], but the VCO output is not a constant signal of exact relationship with the FREF. The output signal is shifting between higher and lower based on the division

patten. In this situation, a fractional spur occurs at a fraction of the comparison frequency. The higher order DSMs spread the noise to reduce the quantization noise in signal band and make the system much more stable [57] [58], but the implementation of higher order design increases the circuit complexity and power consumption.

In divider-less PLL, the TDC is directly driven by DCO outputs, so the reference signal and oscillator output are in a linear form, and the difference produced by phase frequency detector is also linear with no spurs and the loop filter would not be needed. Therefore, the fractional spurs generated by fractional-N divider architecture can be significantly reduced. Besides the strong loop filter that degrades the transients time is also simplified [51].

Phase-Domain PLL (PDPLL) is a divider-less PLL architecture, and it is a fully digital control architecture, which avoids any analog tuning controls for fine voltage, and it is more advantageous over conventional analog based PLLs due to its capability of signal process. [59]. Only basic digital blocks such as accumulators, D-flipflops, subtractors, etc. are used in this design, so it is much easier to implement compared to architectures with fractional dividers [60] [61] [62].

The top-level block diagram of a conventional PDDPLL is shown in Fig. 5.1.2, where FCW stands for frequency control word, FREF is the reference signal and CKV is the variable clock generated by DCO. In conventional PDDPLL, a reference phase estimator is used to estimate the accumulated results of FCW by reference cycles $R_R[k]$; a variable phase estimator is employed to estimate the accumulated results of number of DCO cycles $R_V[i]$; a TDC error detection and calculation block estimates the

fractional result of time interval between FREF and CKV; a comparator is placed after the accumulators to compare the integer and fractional results and generate phase error signal to control the varactor bank of DCO through DLF.

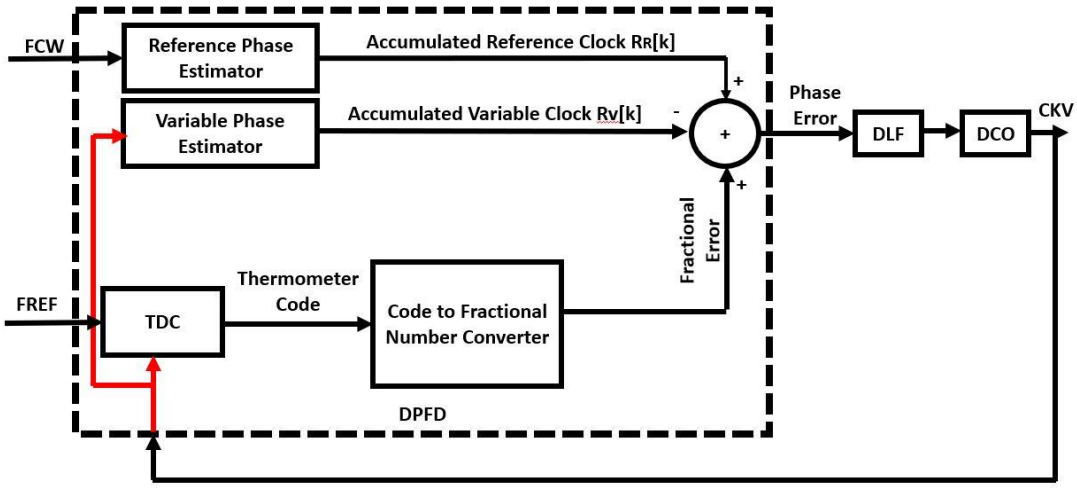


Fig 5.1.2 Top level diagram of conventional PD DPLL

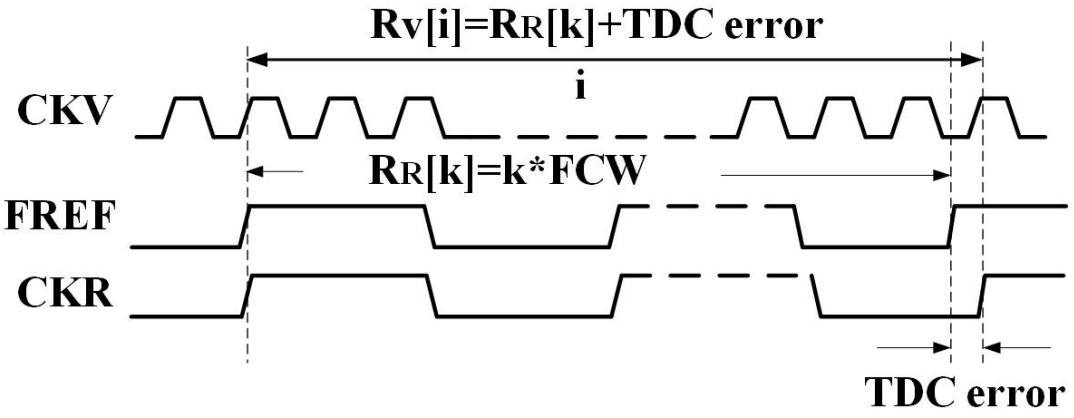


Fig 5.1.3 Waveform of conventional PDDPLL

A time domain waveform of conventional PDDPLL is explained in Fig 5.1.3, the edges of variable clock signal from DCO (CKV) and reference signal (FREF) are not aligned when FCW is a fractional value (Assume $FCW = N_{cycle} + Frac$). A retimed signal CKR is generated by sampling FREF with CKV to synchronous the CKV and CKR, and the ratio between CKR and CKV is an integer number ($N_{cycle} + 1$). In this

case, phase estimators and TDC circuit are used to compare accumulated results of CKV ($R_V[i]$) and FREF ($R_R[k]$). However, an extra system clock is needed to capture the accumulated result $R_V[i]$ and $R_R[k]$ to do the comparison. Besides, the comparison time is also decided by ($k \cdot T_R$) (T_R is the period of FREF), which significantly increase the processing time of the PDPLL.

In this dissertation, a simplified phase-domain divider-less PLL is proposed without accumulating FCW and no extra system clock to capture $R_V[i]$ and $R_R[k]$ to decrease the comparison time and simplify the circuit complexity, and it realizes the multi-band fractional-N function with good PN performance to meet 5G network standard.

5.2 Proposed Simplified Phase-Domain PLL

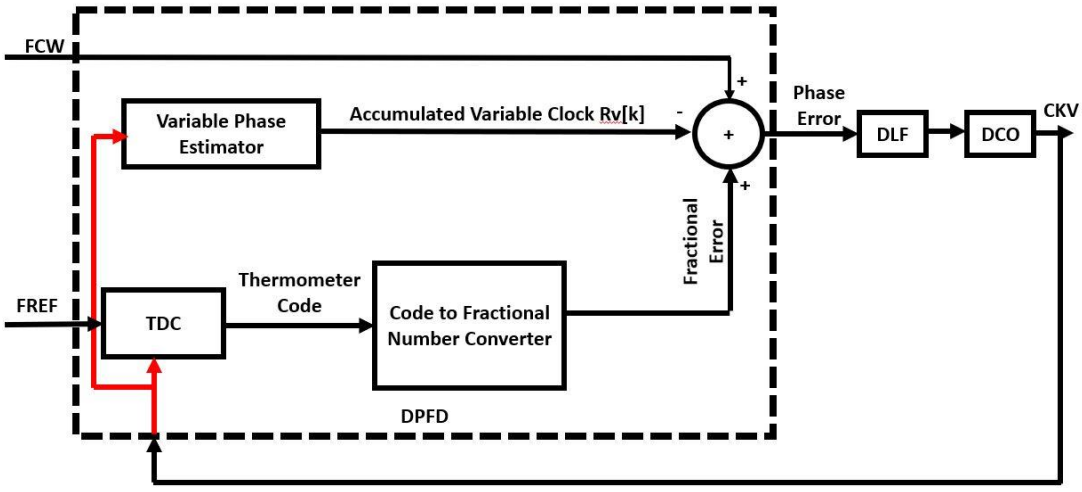


Fig 5.2.1 Top level diagram of proposed simplified phase-domain DPLL

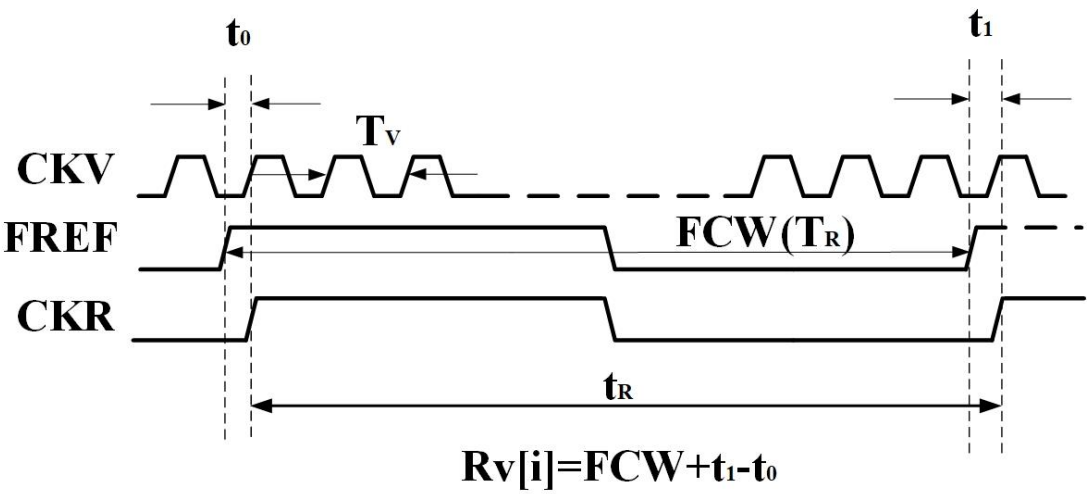


Fig 5.2.2 Time domain waveform of proposed simplified phase-domain PFD

The top-level diagram of proposed simplified phase domain DPLL is shown in Fig 5.2.1, which also consists of a DPFD, a DLF and a DCO. However, the DPFD architecture is simplified compared with the conventional PDDPLL, where the reference phase estimator is eliminated, and the FCW is directly used to check the locking status at the comparison stage without extra system clock signal. The design theory is as followed:

As described in Fig 5.2.2, FREF and CKV are asynchronous at the initial point with a phase error t_0, and the phase error is detected and saved by a TDC block. A reference retimed signal CKR is created by capturing FREF with CKV, so CKV and CKR are synchronized. In one CKR period (t_R), the number of cycles counted by variable phase estimator is i:

$$t_R = iT_v \tag{5-2-1}$$

Where T_V is the period of CKV. After one reference cycle T_R, the new phase error between CKV and FREF becomes t_1, so FREF and CKR can be synchronized with the relationship:

$$t_R = T_R + t_1 - t_0 \quad (5\text{-}2\text{-}2)$$

In other words, CKV and FREF are normalized by introducing retimed CKR signal. When the system is locked, the ratio between FREF and CKV is decided by FCW (Assume $FCW = N_{cycle} + Frac$). In the proposed simplified PDDPLL, the locking condition of PDDPLL can be verified within one reference cycle by comparing the accumulated result of variable phase estimator $R_V[i]$ and TDC error to FCW.

In this proposed design, the reference phase estimator is eliminated. Besides, extra signal generator that capture the TDC and accumulator outputs at a different frequency is not needed. The response time is shorter with $1/k$ by using single FREF to check the locking condition, and the longest response time is the multiplication of FREF and 2^m (m is the number-of-bit of DCO capacitor bank input). The detailed analysis and implementation for the sub-circuits of the proposed simplified PDDPLL are discussed in Section 5.3 to Section 5.7.

5.3 Time to Digital Converter

TDC is used to measure the time interval between two events and quantize it in digital codes [63] [64] [65], which has many applications like the laser ranging, phase meters, space science instruments, lifetime measurements of atomic, physical measurement instruments [66] [67] [68] [69] [70]. It is very popular in digital PLLs to measure the time difference between FREF and feedback signal from DCO.

Using digital method to convert signal into digital type is more stable compared to analog method, it has better performance in immune external disturbances such as process, voltage, and temperature variations. Besides, digital circuit has shorter

transition time and easy to implement. It also has the benefits of large dynamic range and low dead-zone.

5.3.1 Conventional Flash TDC

As shown in Fig 5.3.1(a), a Conventional Flash TDC (CFTDC) is implemented with a series of DFFs and delay elements. The feedback signal of divider output is delayed by inverters and captured at each FREF rising edge, so the feedback signal is converted into thermometer code with one delay element resolution (τ). The time interval T_{in} can be calculated as (5-3-1):

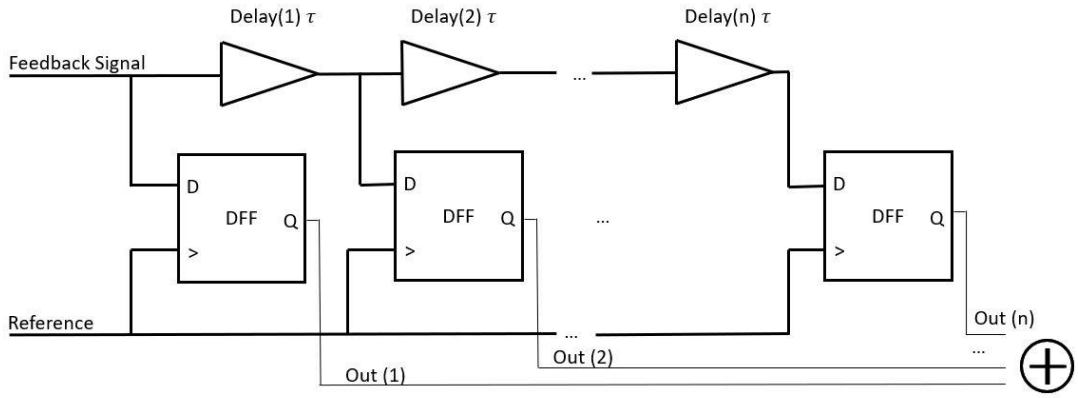
$$T_{in} = k \cdot res + \varepsilon \quad (5\text{-}3\text{-}1)$$

Where k is the number of stages which delayed signal greater than reference signal, and ε is the error within the resolution.

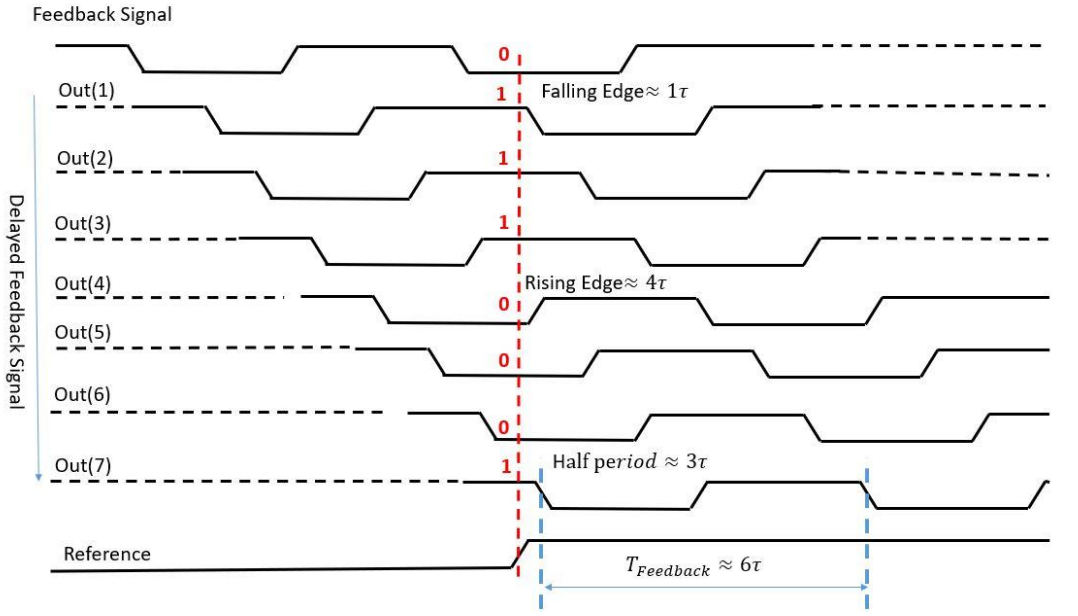
As the example in Fig 5.3.1(b), the feedback signal is digitized into thermometer code "01110001" through the TDC circuit, where the "01" and "10" transitions are the falling edge and rising edge of the feedback signal detected by reference signal. Based on the transition points of the thermometer code, the period of the feedback can be estimated as 6τ in this example. Furthermore, the time interval of the rising edges between the reference and feedback signal can also be estimated, which is 2τ in this example (calculated by $6\tau\ period = 4\tau\ rising - to - rising\ delay$).

The conventional TDC is easy to implement and low power consumption [71] [72]. In this dissertation, a conventional 128-bit /15ps delay element TDC is used to calculate the time interval between reference signal and feedback signal from DCO, followed

with a thermometer code digitizer block to convert the thermometer code into digital number for further processing.



(a)



(b)

Fig 5.3.1 (a) Conventional flash TDC architecture (b) Thermometer outputs of conventional flash TDC

5.3.2 Conventional Flash TDC Design of Proposed ADPLL

Based on the frequency band specifications of proposed ADPLL (600MHz to 930MHz, 2.4GHz to 2.8GHz and 3.4GHz to 4.2GHz), the period range for each frequency band can be calculated as below:

For the oscillating frequency at 600MHz, the period of the output signal is:

$$T_{600M} = \frac{1}{600MHz} = 1.667ns \quad (5\text{-}3\text{-}6)$$

For the oscillating frequency at 930MHz, the period of the output signal is:

$$T_{930M} = \frac{1}{930MHz} = 1.075ns \quad (5\text{-}3\text{-}7)$$

For the oscillating frequency at 2.4GHz, the period of the output signal is:

$$T_{2.4G} = \frac{1}{2.4GHz} = 417ns \quad (5\text{-}3\text{-}8)$$

For the oscillating frequency at 2.8GHz, the period of the output signal is:

$$T_{2.8G} = \frac{1}{2.8GHz} = 357ps \quad (5\text{-}3\text{-}9)$$

For the oscillating frequency at 3.4GHz, the period of the output signal is:

$$T_{2.8G} = \frac{1}{3.4GHz} = 294ps \quad (5\text{-}3\text{-}10)$$

For the oscillating frequency at 4.2GHz, the period of the output signal is:

$$T_{4.2G} = \frac{1}{4.2GHz} = 238ps \quad (5\text{-}3\text{-}11)$$

For the case of resonating frequency at 4.2GHz, the period of the signal is:

$$T_{4.2G} = \frac{1}{4.2GHz} = 240ps \quad (5\text{-}3\text{-}12)$$

In this case, the detection range of the TDC circuit should be greater than 1.67ns for worst case delay with a maximum step size of 240ps. The 15ps delay element is chosen in the conventional TDC design because of the trade-off between the resolution

and number of stages, so the minimum number of required delay stages ($Number_\tau$) is:

$$Number_\tau = \frac{1.667ns}{15ps} = 112 \quad (5\text{-}3\text{-}13)$$

A 128-stage conventional flash TDC is implemented in this dissertation to meet the 240ps to 1.667ns detection requirement. The channel numbers for each operating band can be calculated as below:

For 600MHz to 930MHz, the channel number (N_{Band1}) is:

$$N_{Band1} = \frac{1.667ns - 1.075ns}{15ps} = 40 \quad (5\text{-}3\text{-}14)$$

For 2.4GHz to 2.8GHz, the channel number (N_{Band2}) is:

$$N_{Band2} = \frac{417ps - 357ps}{15ps} = 4 \quad (5\text{-}3\text{-}15)$$

For 3.4GHz to 4.2GHz, the channel number (N_{Band3}) is:

$$N_{Band3} = \frac{294ps - 238ps}{15ps} = 4 \quad (5\text{-}3\text{-}16)$$

The frequency resolution of each frequency band for proposed ADPLL are listed in Table 5.3.1

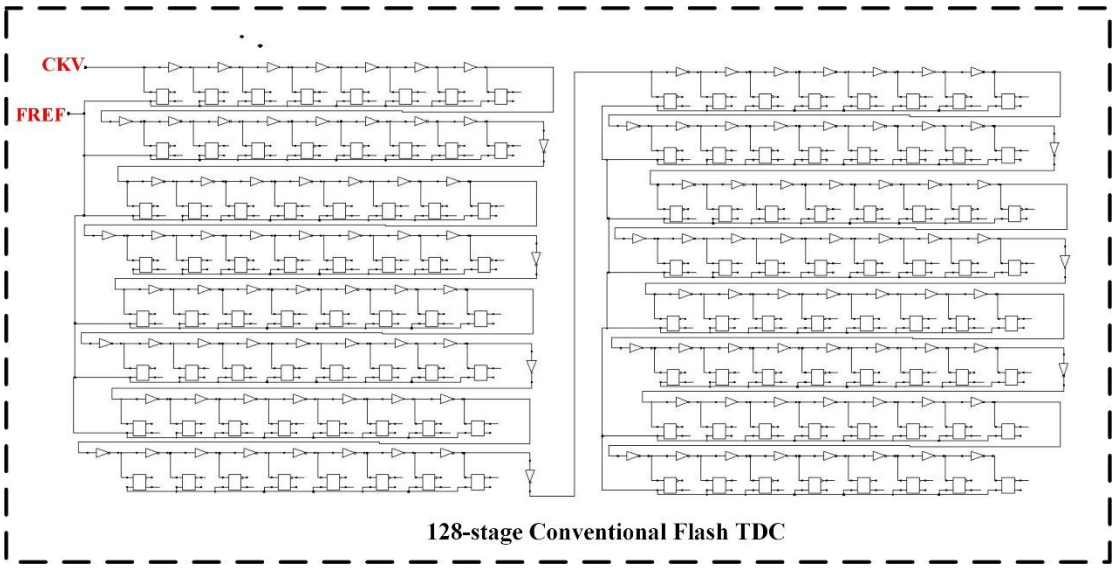
Table 5.3.1 Design specifications of frequency resolution for proposed ADPLL

Band	Step Size (MHz)
600MHz-930MHz	8.25MHz
2.4GHz – 2.8GHz	100MHz
3.4GHz – 4.2GHz	200MHz

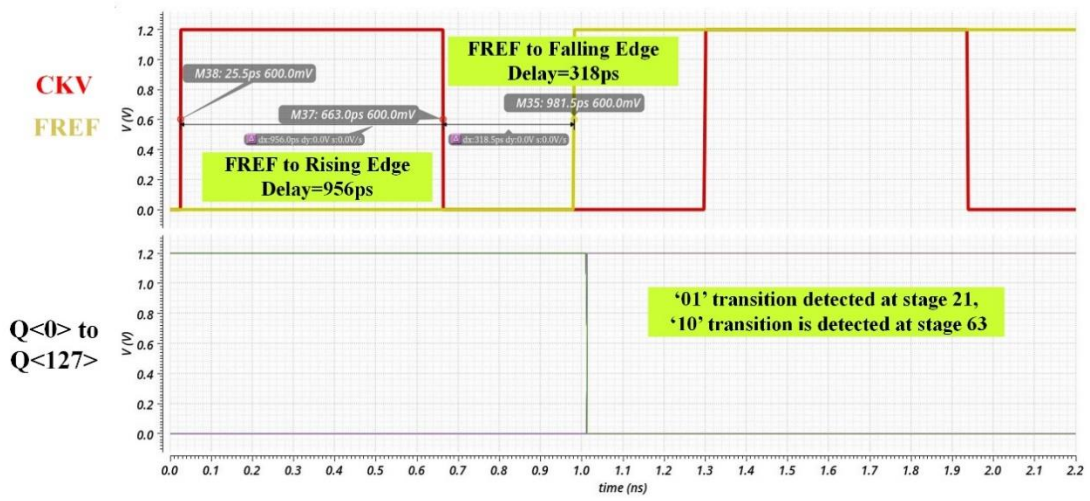
5.3.3 Flash TDC Implementation

A 128-stage, 15ps-delay-stage conventional flash TDC is used to calculate the time interval between reference signal and feedback signal in the proposed simplified PDDPLL, and the circuit implemented in CMOS 65nm technology with Cadence Virtuoso Tool is shown in Fig 5.3.2(a). The simulation result of an example where the

period of FREF is 1.275ns and a 319ps rising edge time interval between FREF and CKV is expressed in Fig 5.3.2(b), and the thermometer code generated by the 128-stage TDC is ’000…0111…10…0’, where the first ’01’ transition is detected at stage 21, and the first ‘10’ transition is detected at stage 63. The half period of the CKV signal can be calculated as 42 stage delay, so the period of the CKV signal is estimated as 84 stages delay by employing a multiplier, and the time interval is calculated as 21 stages (84-63=21 stage) based on the rising/falling transition information. To realize the function, the thermometer code to fractional digital converter is designed and introduced in Section 5.3.4.



(a)



(b)

Fig 5.3.2 (a) Circuit implementation of Flash TDC (b) Simulation plots of Flash TDC

5.3.4 Thermometer Code to Fractional Digital Number Converter

To convert the thermometer code into fractional result and compare it with frequency control word, a Thermometer Code to Fractional Digital number Converter (TCFDC) is designed in this section.

The top-level block diagram of the TCFDC is shown in Fig 5.3.3, which includes an edge detector; a first rising/falling transition stage calculator (FRFTSC); an absolute subtractor; a rising edge time interval calculator; a fractional code generator. Based on the thermometer code from TDC, the edge detector detects all the '01' /'10' transitions, and the first rising/falling transition stage number is extracted by the FRFTSC. An absolute subtractor is used to compare the absolute value between the first rising/falling transition stage and calculate the half period of CKV. Then, the time interval information is generated based on the period information and first '10' transition stage. A fractional code generator is the last stage of TCFDC to convert the information of

time interval and CKV period into a TDC error digital code.

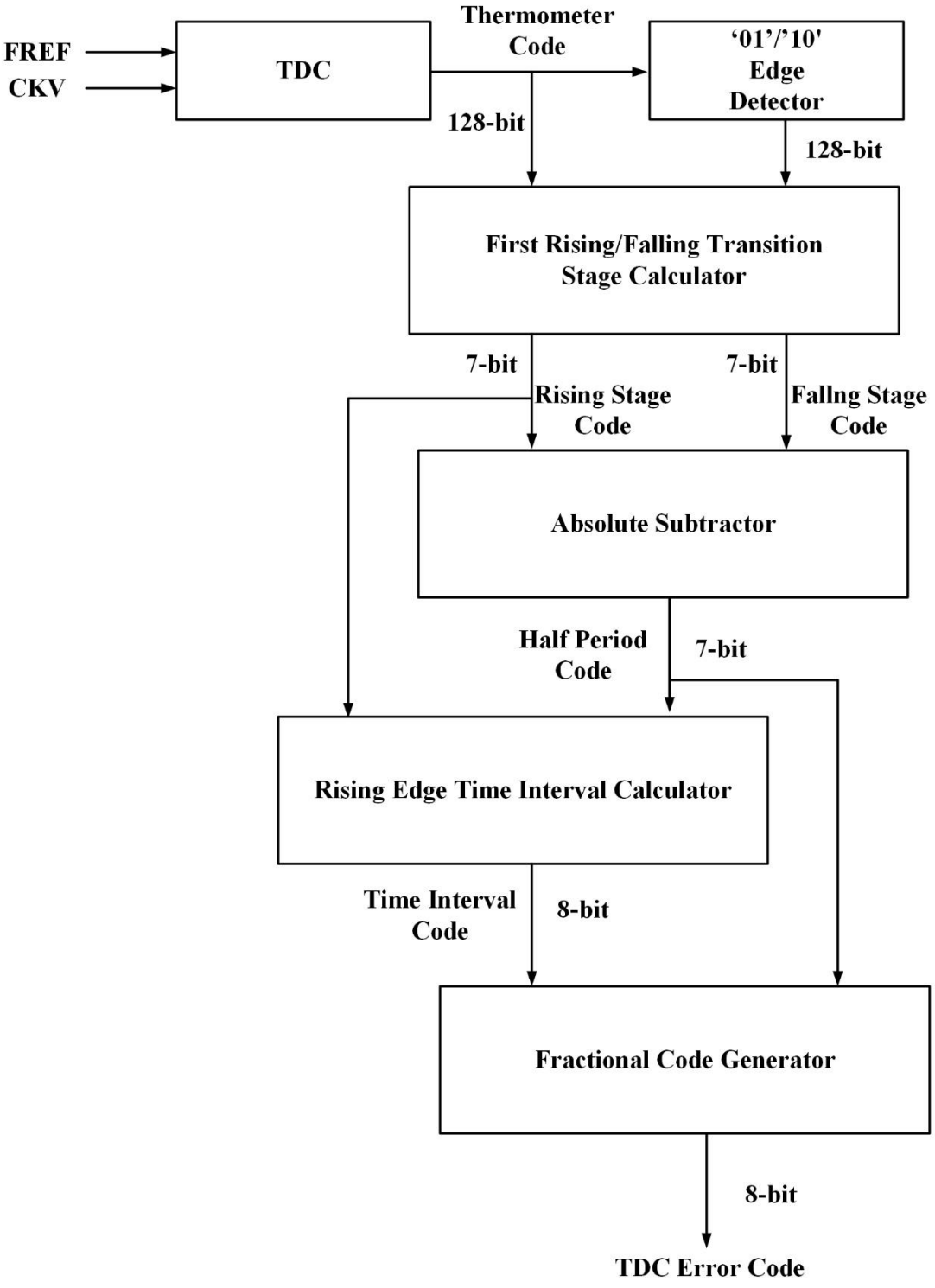


Fig 5.3.3 Design theory of TCFDC

The first stage of TCFDC is edge detector circuit as shown in Fig 5.3.4, which consists of 128 XOR gates to test the relationship between the adjacent bits. The look-up table of the edge detector circuit is listed in Table 5.3.2, where T_x is the stage for '01' transition, T_y is the '10' transition stage and n is the bit number. By using the XOR bank, all the '01' and '10' transitions within the TDC detection range are detected.

However, the cycle number of CKV signal is varied with operating frequency. In this case, the FRFTSC is designed with an AND gate bank (shown in Fig 5.3.5) to eliminate either all rising cases or falling cases, and a $(\bar{A} \cdot B)$ gate bank to capture the first transition stage.

As explained in Table 5.3.2, the rising transition is extracted from the edge detector based on equation (5-3-17). Similarly, the falling edge transition is also extracted from the edge detector according to (5-3-18):

$$Rising\ Stage = TC_n \cdot XOR_n \tag{5-3-17}$$

$$Falling\ Stage = TC_{n+1} \cdot XOR_n \tag{5-3-18}$$

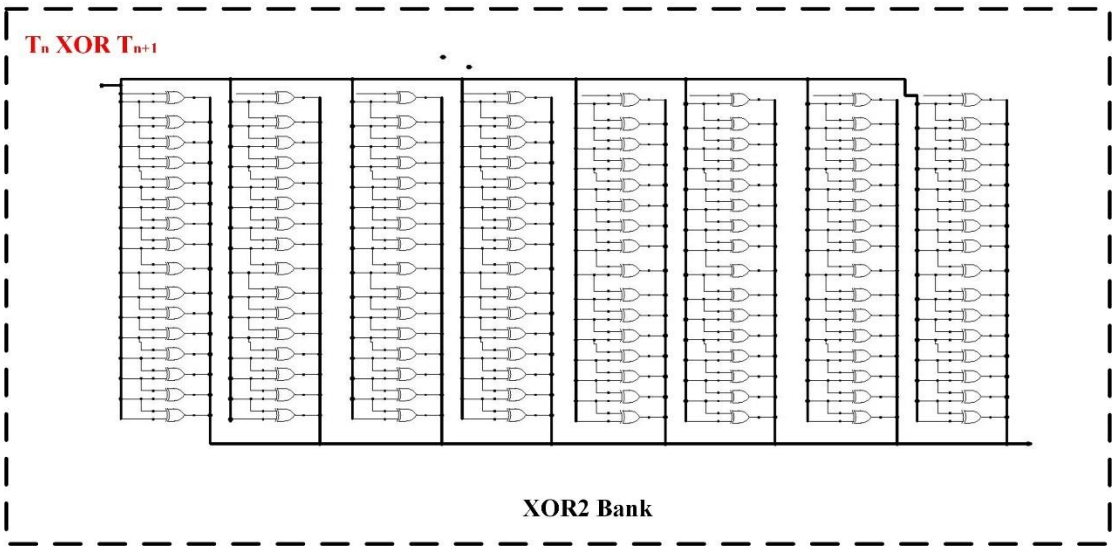


Fig 5.3.4 Circuit implementation of '01'/'10' edge detector

Table 5.3.2 TCFDC Look-up Table

	T_0	T_1	…	T_{x-1}	T_x	…	T_{y-1}	y	…	n
Thermometer Code (TC)	0	0	…	0	1	…	1	0	…	0
$T_n\ XOR\ T_{n+1}$	0	0	…	1	0	…	1	0	…	0
$TC_n\ AND\ XOR_n$	0	0	…	0	0	…	1	0	…	0
$TC_{n+1}\ AND\ XOR_n$	0	0	…	1	0	…	0	0	…	0

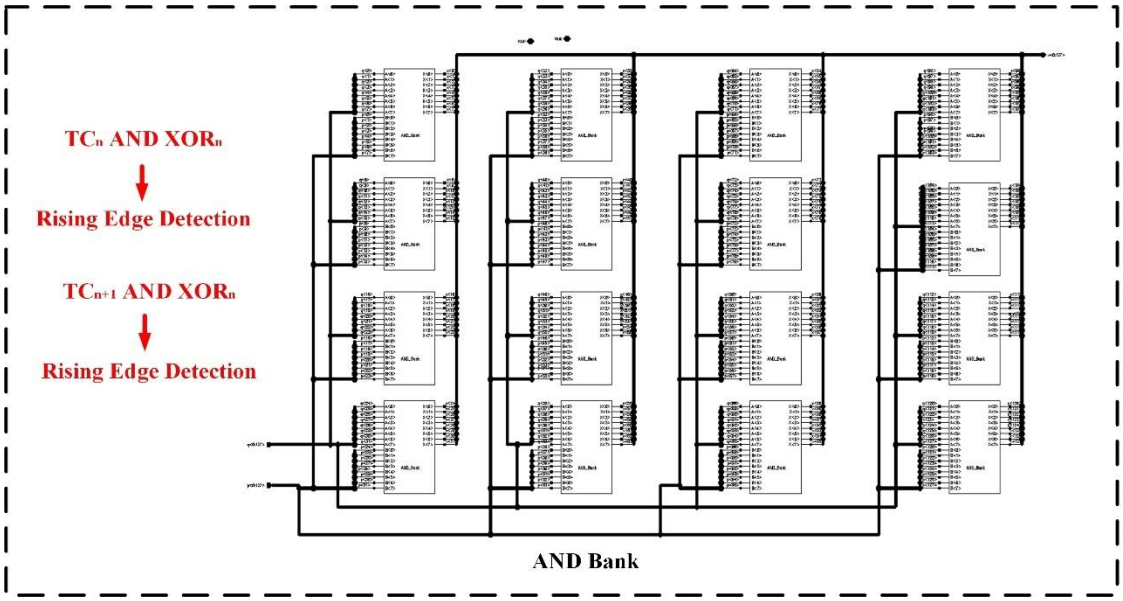


Fig 5.3.5 Circuit implementation of AND bank

An $(\bar{A} \cdot B)$ gate bank is used to capture the first '01'/'10' transition stage among all rising/falling states (as shown in Fig 5.3.6), and the design methodology is expressed in (5-3-19):

$$First\ transistion\ stage = \overline{A_0 + A_1 + \cdots + A_{k-1}} \cdot A_k \quad (5\text{-}3\text{-}19)$$

Where A is the digital code from AND gate bank and k is the first transition edge. A NOR gate generates a logic high only when no transitions are detected before the first rising/falling state. The first transition stage is triggered whenever the first transition

edge is detected.

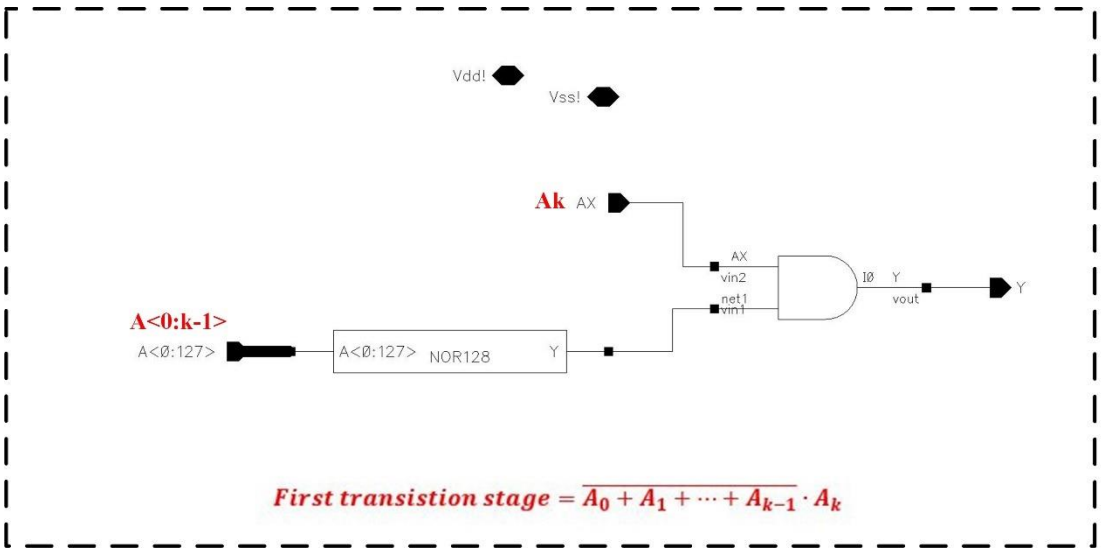


Fig 5.3.6 Circuit implementation of first transition edge detector

The signal from first transition edge detector is still a thermometer code, so a 128-to-7 encoder is placed as the last stage of FRFTSC to convert it into a 7-bit number. 65-bit OR gate is used to realize the function based on (5-3-19) to (5-3-25):

$$A_0 = Y_1 + Y_3 + Y_5 + Y_7 + \cdots + Y_{127} \quad (5\text{-}3\text{-}19)$$

$$A_1 = Y_2 + Y_3 + Y_6 + Y_7 + \cdots + Y_{126} + Y_{127} \quad (5\text{-}3\text{-}20)$$

$$A_2 = Y_4 + Y_5 + Y_6 + Y_7 + \cdots + Y_{124} + \cdots + Y_{127} \quad (5\text{-}3\text{-}21)$$

$$A_3 = Y_8 + Y_9 + \cdots + Y_{14} + Y_{15} + \cdots + Y_{120} + \cdots + Y_{127} \quad (5\text{-}3\text{-}22)$$

$$A_4 = Y_{16} + Y_{17} + \cdots + Y_{30} + Y_{31} + \cdots + Y_{112} + \cdots + Y_{127} \quad (5\text{-}3\text{-}23)$$

$$A_5 = Y_{32} + Y_{33} + \cdots + Y_{62} + Y_{63} + \cdots + Y_{96} + \cdots + Y_{127} \quad (5\text{-}3\text{-}24)$$

$$A_6 = Y_{64} + Y_{65} + \cdots + Y_{127} \quad (5\text{-}3\text{-}25)$$

Where Y is the input signal, and A is the encoder output. The circuit implementation of the 128-to-7 encoder is illustrated in Fig 5.3.7. The encoded 7-bit first rising/falling edge information is generated and used to calculate the period and

time interval of the CKV and FREF signals.

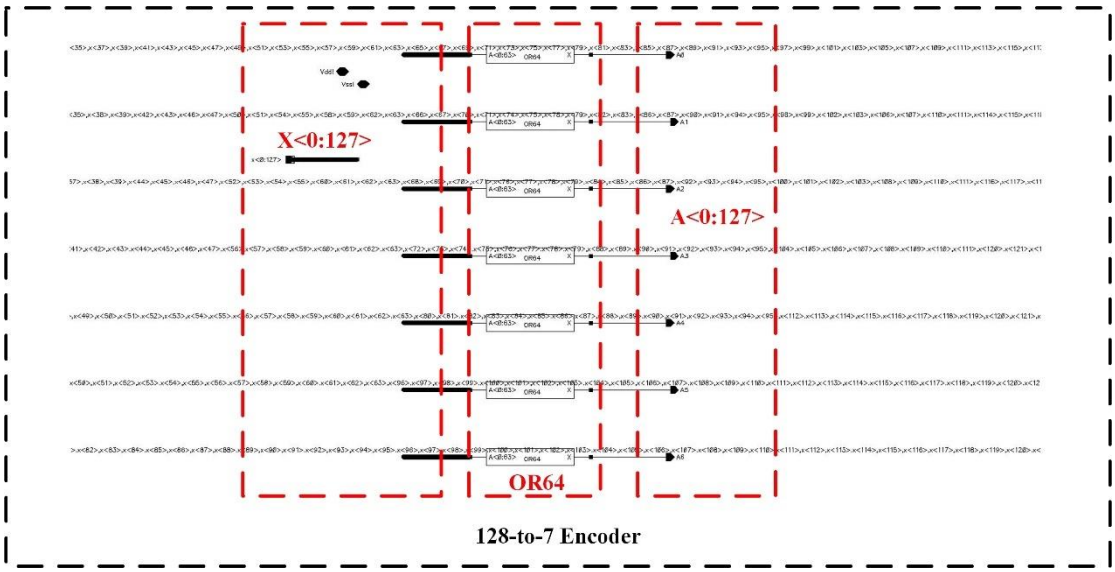


Fig 5.3.7 Circuit implementation of 128 to 7 encoder

A 7-bit absolute subtractor is connected after the FRFTSC block to calculate the absolute value between the first rising and falling results. The circuit is expressed in Fig 5.3.8, which consists of two subtractor (one is for A-B, and another one is for B-A), and a 2-to-1 MUX selected by the carryout signal from (A-B) subtractor. The outputs of the 2-to-1 MUX is the half period of CKV.

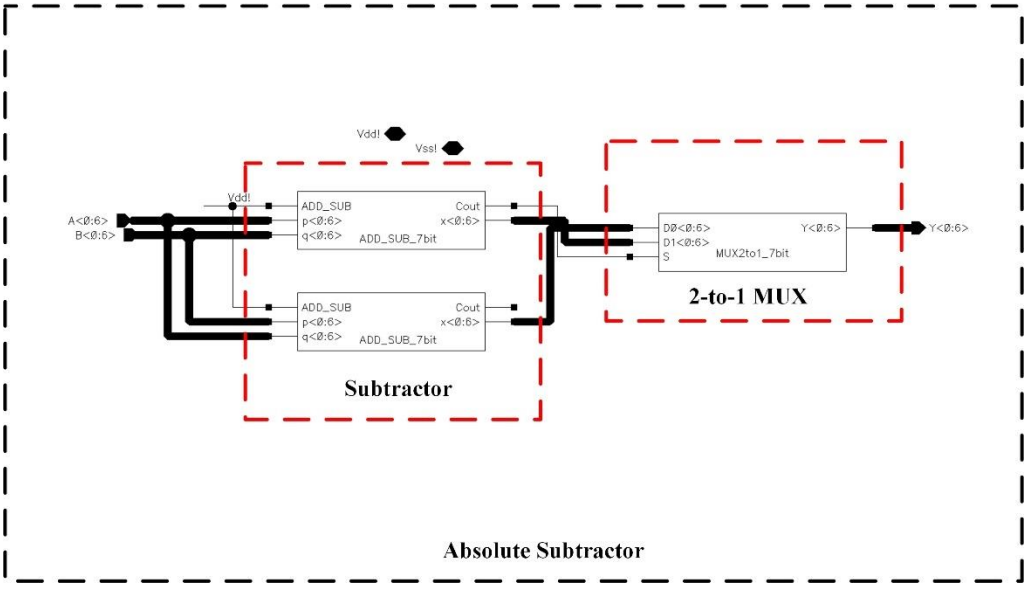


Fig 5.3.8 Delay Calculator

The time interval between FREF and CKV is calculated by the difference of CKV period and first rising stage delay. An 8-bit subtractor is employed since the full period of CKV signal is calculated by doubling the half period result.

The last block of the TCFDC is a fractional code generator, which consists of a division code look-up table block and a multiplier. As explained in Fig 5.3.9, the $1/T_{CKV}$ fractional code is created based on detected full period of CKV. For example, the fractional code is '01000000' when 4-delay-stage is the result of the full period. For the 8-bit TDC error digital result, the $1/T_{CKV}$ fractional code is created based on (5-3-26):

$$\frac{1}{T_{CKV}}\text{fractional code} = \frac{2^8}{\#delay\ stages\ of\ \ full\ CKV\ period} \quad (5\text{-}3\text{-}26)$$

Then, an 8×8 multiplier is used to create the final TDC error digital code, but only 8-bit outputs are required in this design since the division value is always greater than the multiplier value.

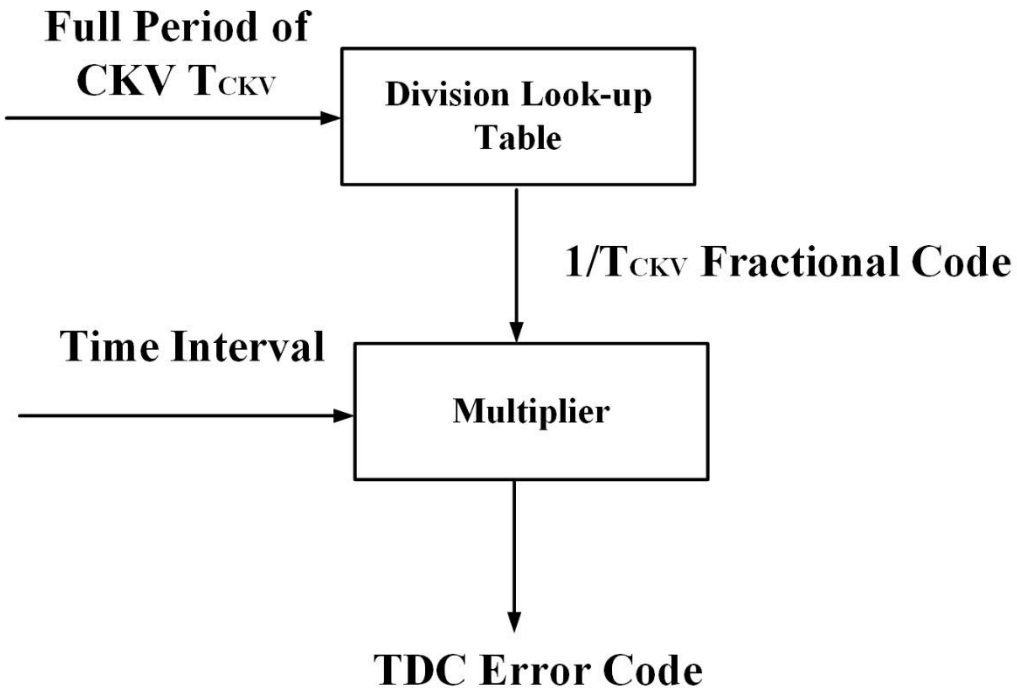
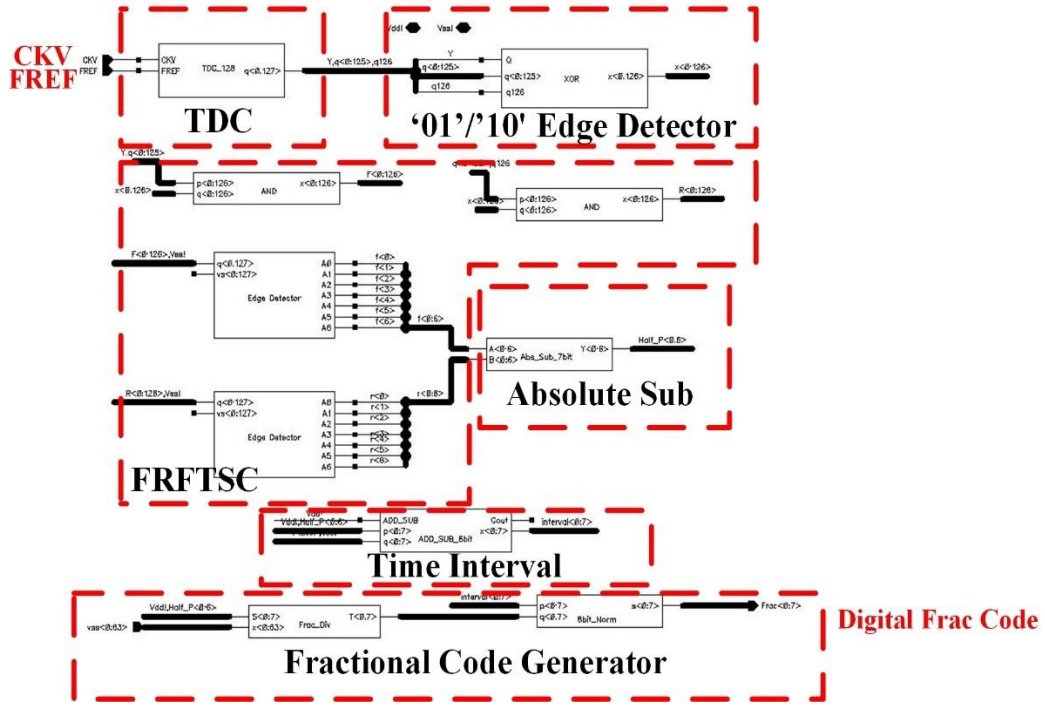
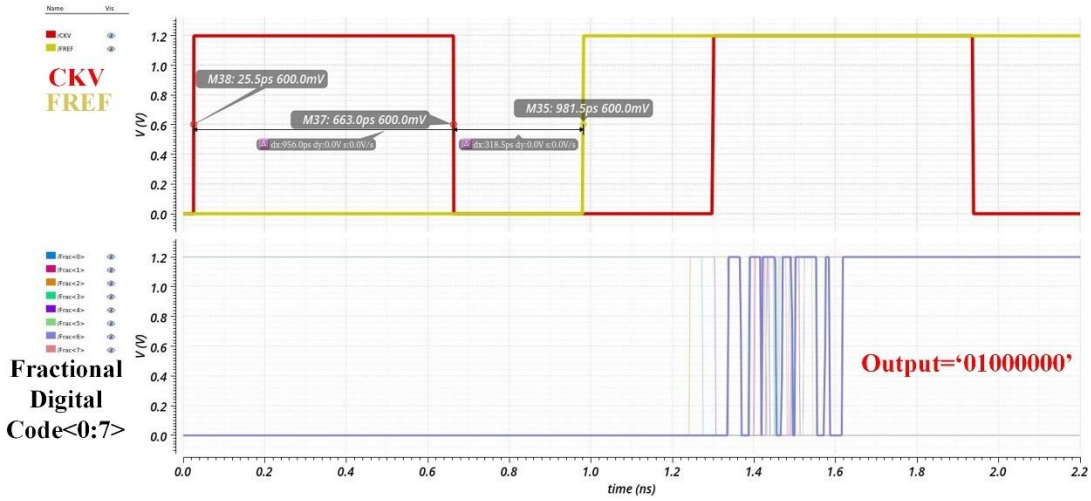


Fig 5.3.9 Fractional code generator



(a)



(b)

Fig 5.3.10 TDC error fractional code generator (a) Schematic (b) Simulation waveform

The final design of TDC error fractional code generator is shown in Fig 5.3.10 (a), which is designed following with the theory of Fig 5.3.3. The CKV signal is delayed

and captured by FREF in TDC block, and the thermometer code from TDC is translated into timing information by edge detector and subtractors. Finally, a fractional code generator is used to convert the timing information into fractional code for comparison in simplified phase-domain PFD. The simulation results of TDC error fractional code generator is expressed in Fig 5.3.10 (b) with the same example as Fig 5.3.2 (b). The final output of TDC error fractional code generator is '01000000', which matches the ¼ relationship between time interval and CKV period, and the processing time for the fractional code generator is 620ps.

5.4 Simplified Phase Domain Digital Phase Frequency Detector

The simplified phase domain PFD is implemented with a TDC to calculate the phase error, a variable frequency accumulator to count the cycle numbers of DCO output, a reference retiming circuit to capture the integer and fractional information, and a digital comparator to verify the locking condition. As described in Section 5.3, the fractional detection result is generated by the TDC circuit. In Fig 5.4.1, the reference retimed signal CKR is created by capturing FREF with DCO output CKV. The hardware implementation of the variable phase estimator is explained in 5.4.2. The FCW is directly connected to the digital comparator to compare its integer part with variable phase estimator and its fractional part with TDC results. The detailed circuit implementations are analyzed in Section 5.4.1 to Section 5.4.4.

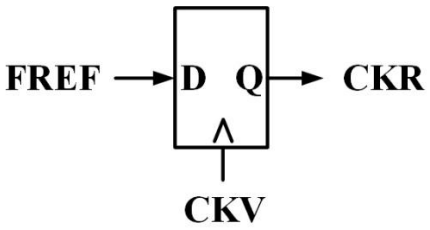


Fig 5.4.1 Reference retimed circuit

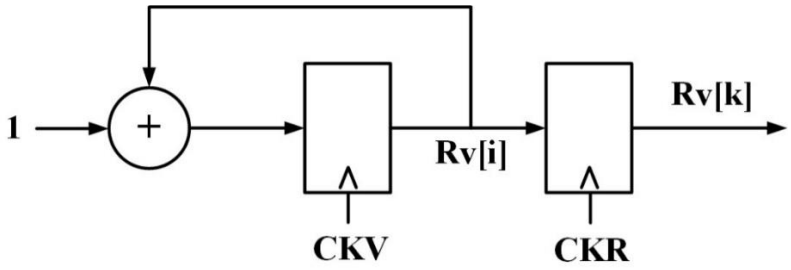
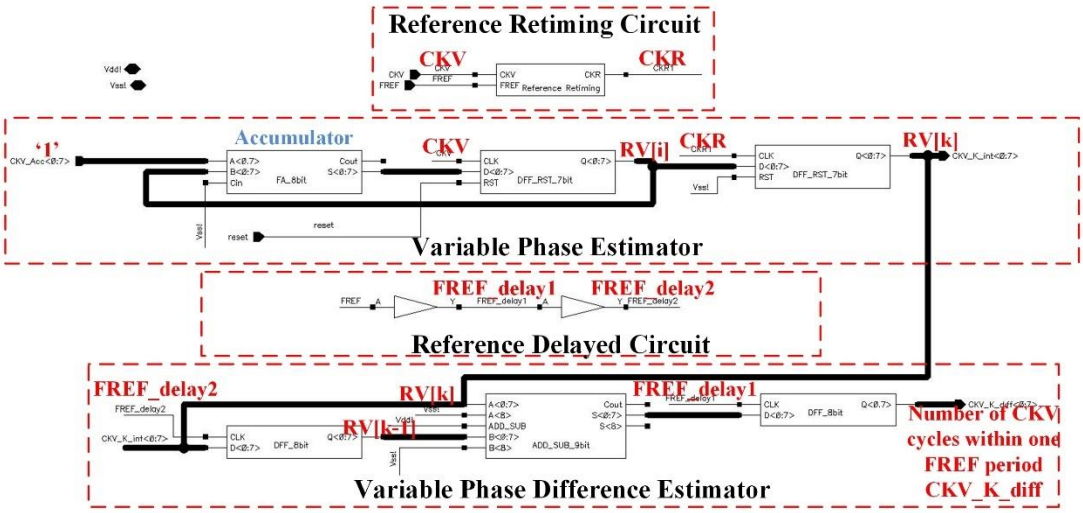
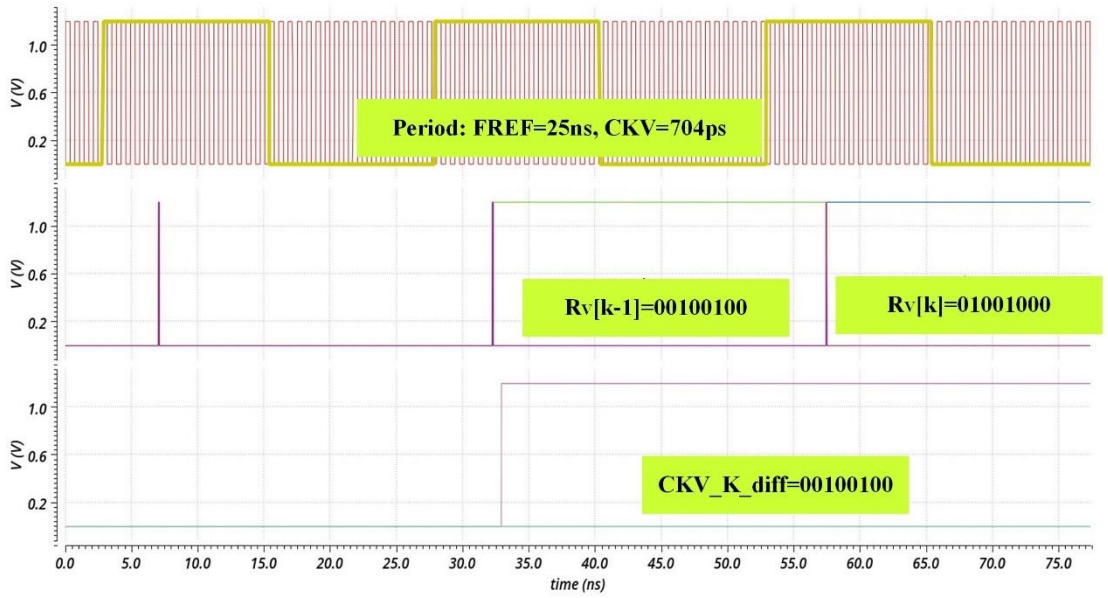


Fig 5.4.2 Hardware implementation of variable phase estimator

5.4.1 Circuit Implementation of Variable Phase Estimator



(a)



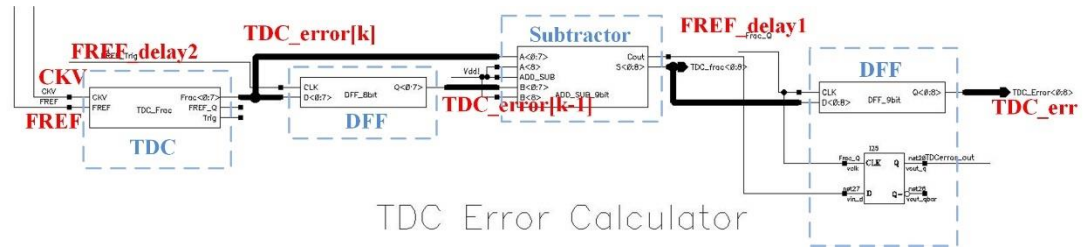
(b)

Fig 5.4.3 (a) Circuit implementation of variable phase estimator (b) Simulation result of the variable phase estimator

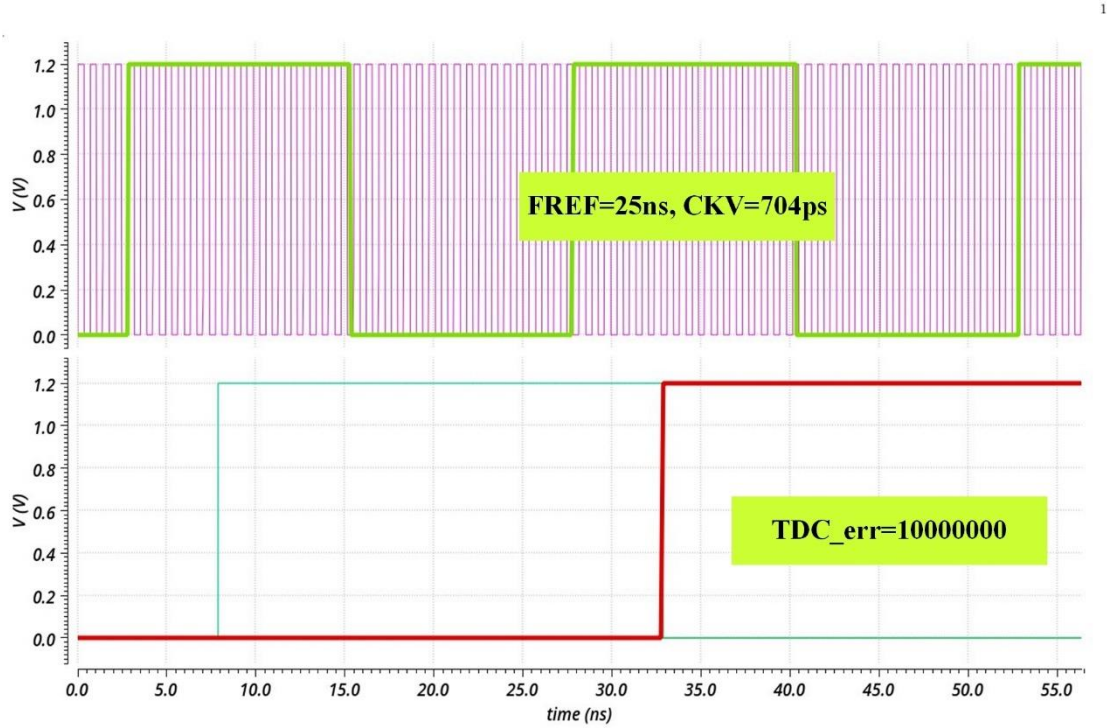
The circuit implementation of the variable phase estimator is shown in Fig 5.4.3(a). An accumulator is the first stage to count the number of cycles of CKV signal, the retimed CKR signal is used to capture the accumulator result and generates the digital code. The accumulated result $R_V[k]$ is saved by a DFF and compared with the initial result of the variable phase estimator $R_V[k-1]$ to calculate the number of CKV cycles within one FREF period CKV_K_diff, and CKV_K_diff is regarded as the measured integer data of the PLL system.

An example of FCW equals to $35\frac{1}{2}$ is explained in Fig 5.4.3(b). The CKV_diff is correctly measured as 36 with the digital code of '00100100' at this variable phase estimator stage.

5.4.2 Circuit Implementation of TDC Error Calculator



(a)



(b)

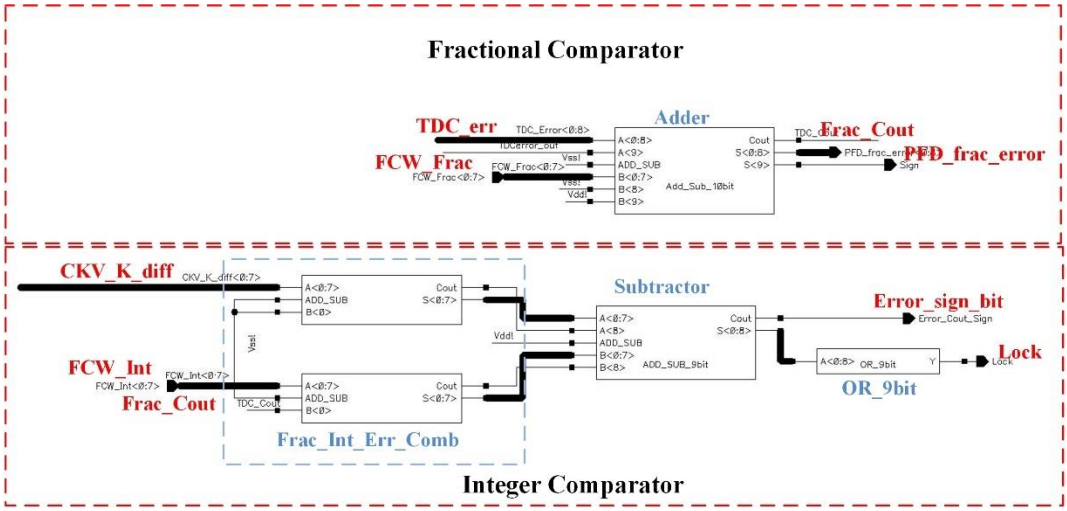
Fig 5.4.4 (a) Schematic of TDC error calculator (b) Simulation result of TDC error calculator

In Fig 5.4.4(a), the VRTDC is the first stage for TDC error calculator, which generates the time interval between the rising edge of FREF and the next rising edge of CKV. According to the analysis in Section 5.2, the calculated result is saved by a DFF and subtracted with the next calculated TDC result to generates the TDC error between two reference clock cycles TDC_err.

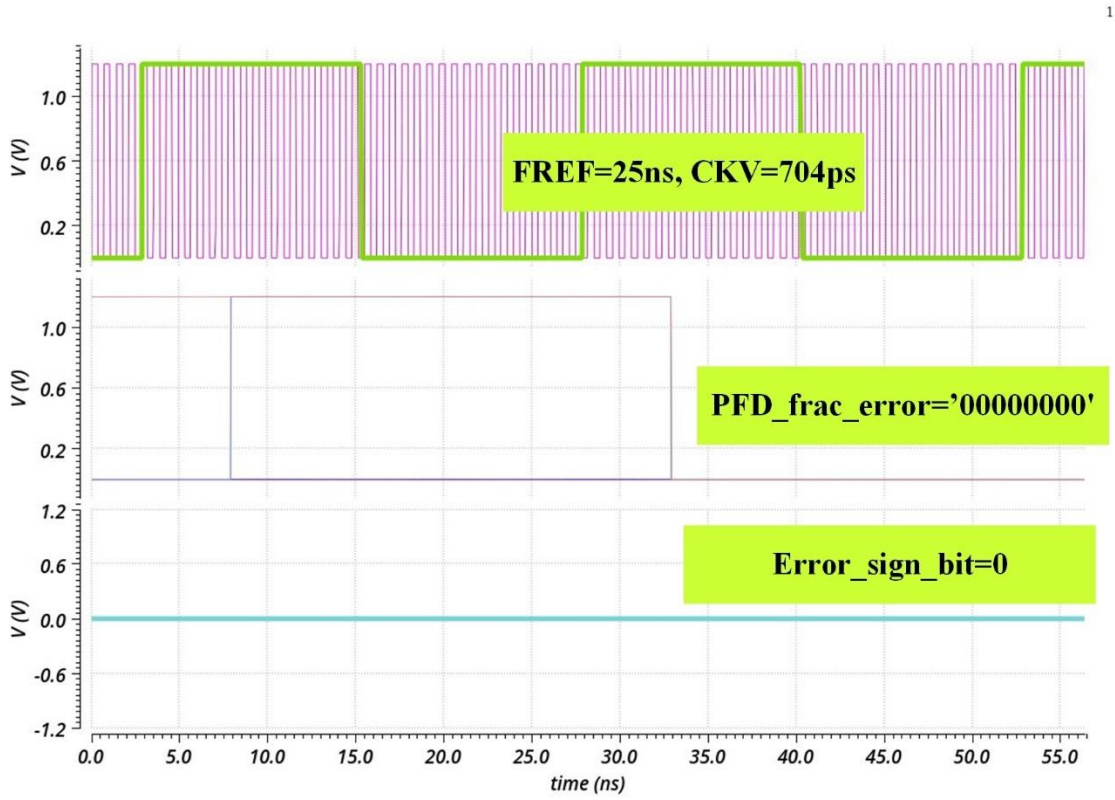
The simulation result of the same example of $T_{FREF} = 25ns$ and $T_{CKV} = 704ps$ *with* $FCW = 35\frac{1}{2}$ is tested and shown in Fig 5.4.4(b). The TDC error between

two reference cycles is calculated as $\frac{1}{2}$ with the output code of '10000000' correctly.

5.4.3 Circuit Implementation of Fractional and Integer Code Comparator



(a)



(b)

Fig 5.4.5 (a) Schematic of fractional and integer code comparator (b) Simulation results of fractional and integer combiner

As shown in Fig 5.4.5(a), the fractional error comparator compares the TDC error with the fractional input of FCW (*FCW_frac*). When *TDC_err* matches the *FCW_frac*, for example, for the case of FCW equal to $4\frac{1}{4}$ and TDC error equals to $\frac{3}{4}$, the $Frac\_Cout$ bit is triggered to '1'. Then, the $Frac\_Cout$ result is calculated with the fractional and integer error combiner (Frac_Int_Err_Comb), and subtracted with *CKV_K_diffv* to verify the PLL locking condition. When CKV is lower than the desired operating frequency, Error_sign_bit is '0', otherwise, Error_sign_bit is triggered to '1'. A 9-bit OR gate is connected after the subtractor stage to check the locking status of the system. When system is locked, the outputs from subtractor are '0's, so a logic low is created by the OR gate (*Lock=0*). When system is in calibration mode, *Lock=1*. The outputs of integer comparator are designed for controlling the DCO varactor banks through a digital loop filter.

For the case of $T_{FREF} = 25ns$ with $T_{CKV} = 704ps$ (in Fig 5.4.5(b)), the measured fractional and integer codes match the input of FCW, so there is no signal generated at the sign bit to vary the VCO varactor bank.

5.4.4 Schematic of Proposed Digital Phase Frequency Detector

As indicated in Fig 5.4.6, the variable phase estimator and TDC error calculator are operating simultaneously with the retimed reference signal. Then, the digitized results of fractional and integer parts are compared to FCW to make final decision.

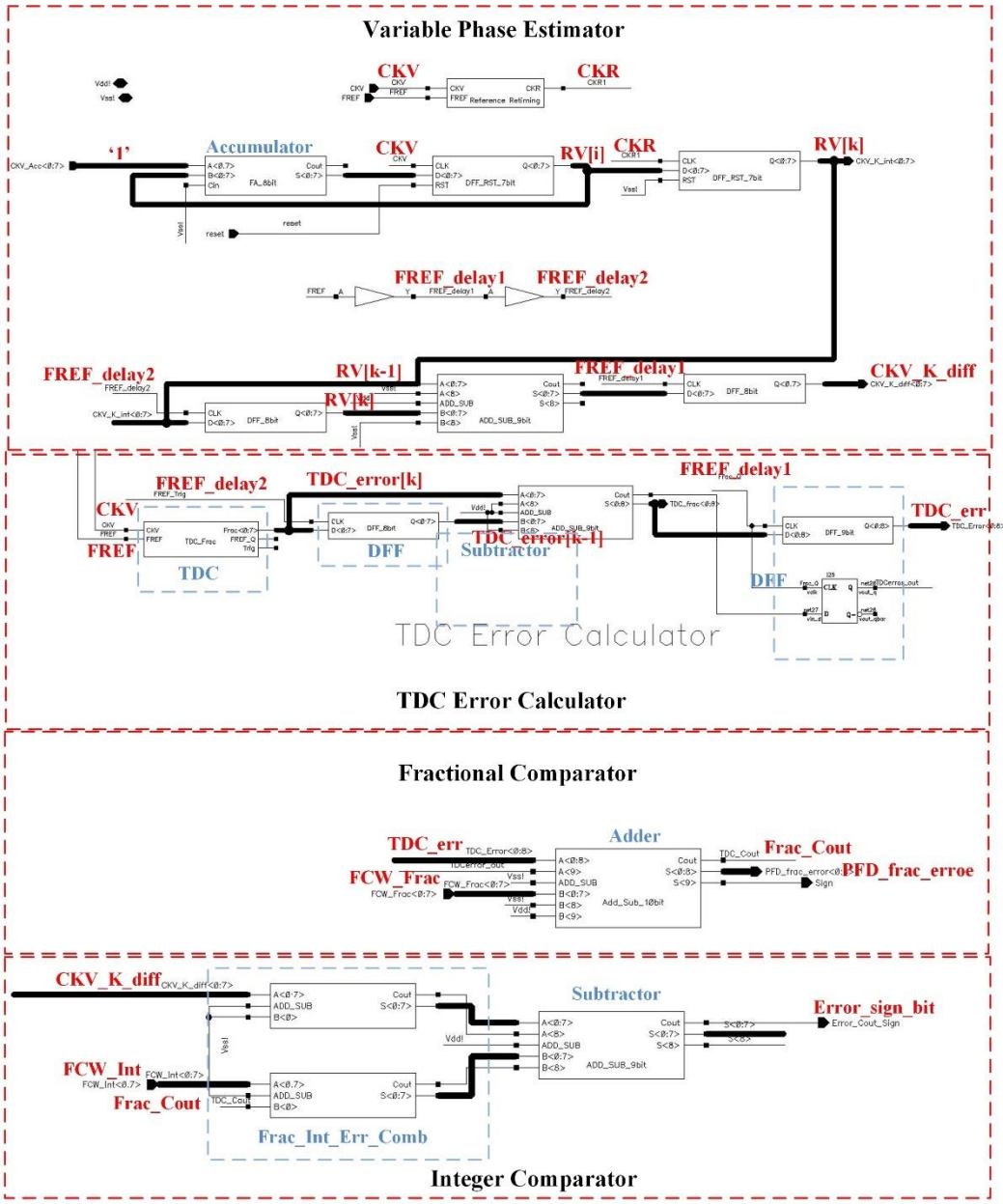


Fig 5.4.6 Schematic of proposed DPFD

5.5 Digital Loop Filter

Similar as analog loop filter, the digital loop filter is also employed in DPLL to filter out unwanted noise and passing out the desired signal to DCO inputs. In DLF design, there are no passive components (such as resistance and capacitance), and it is

used as a conjunction to deliver the phase error information from DPFD to varactor bank of DCO [73] [74].

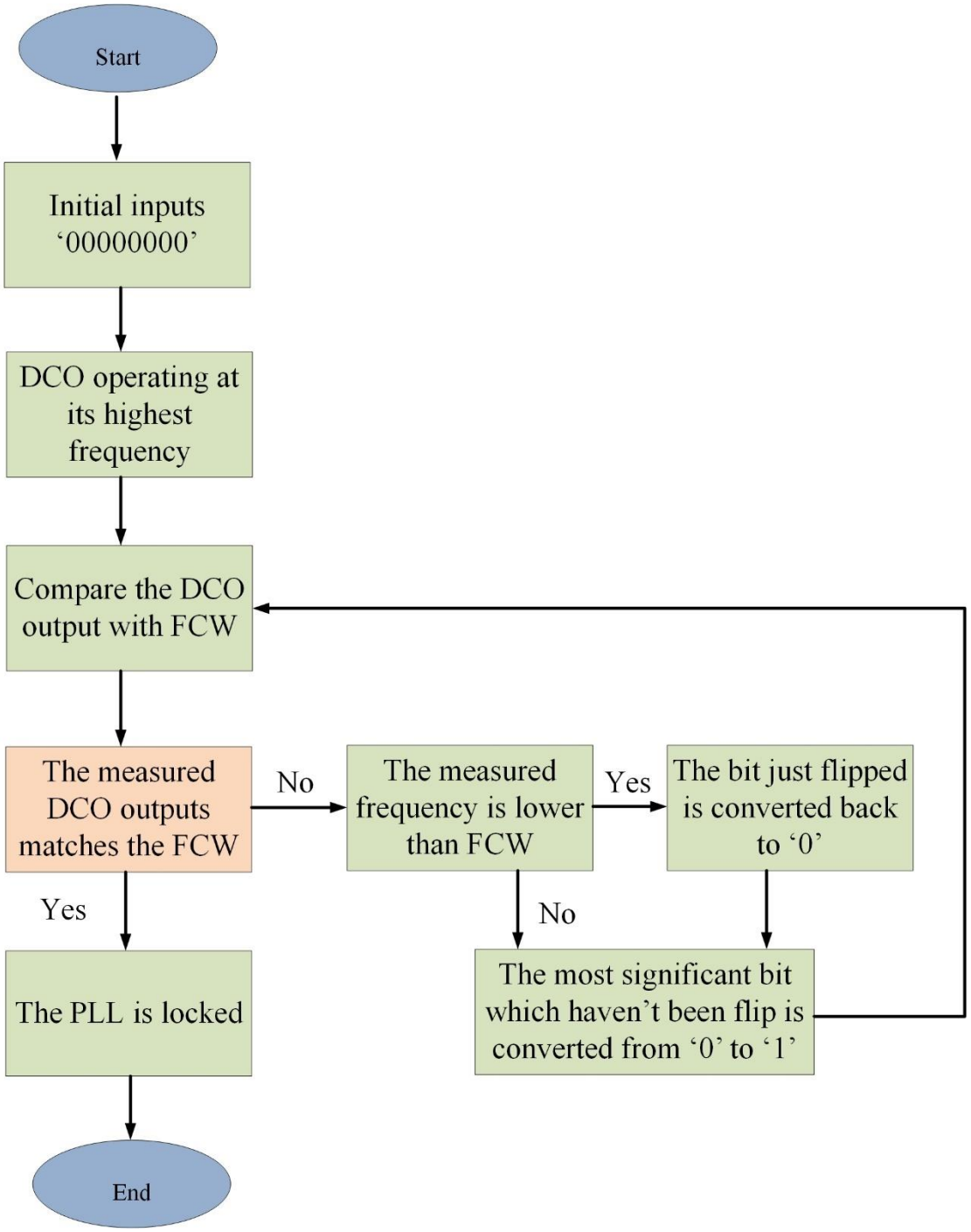
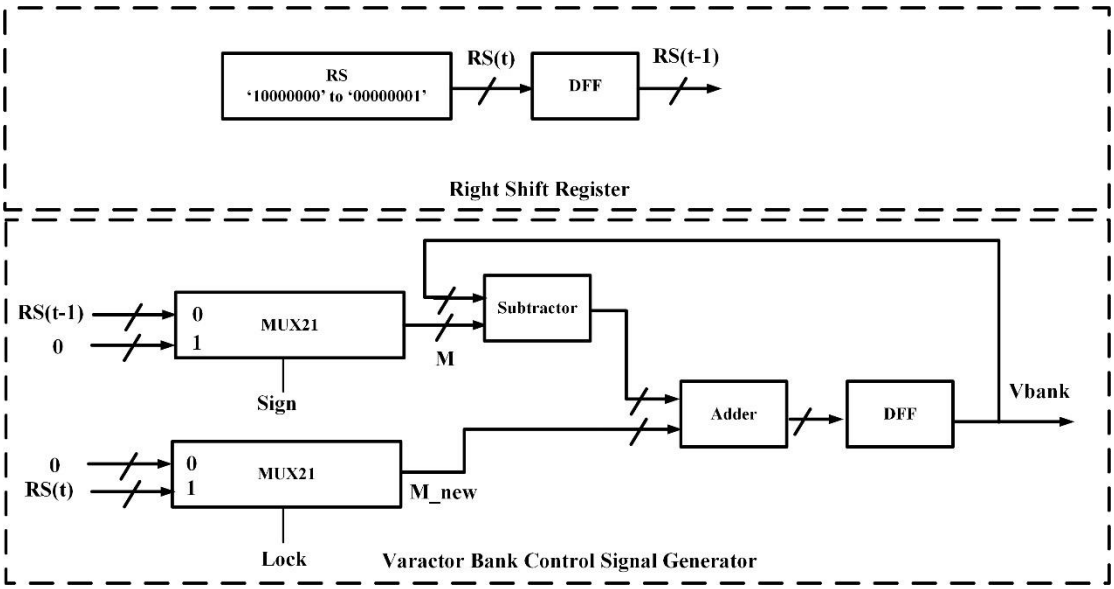


Fig 5.5.1 Flow chart of PEVBC

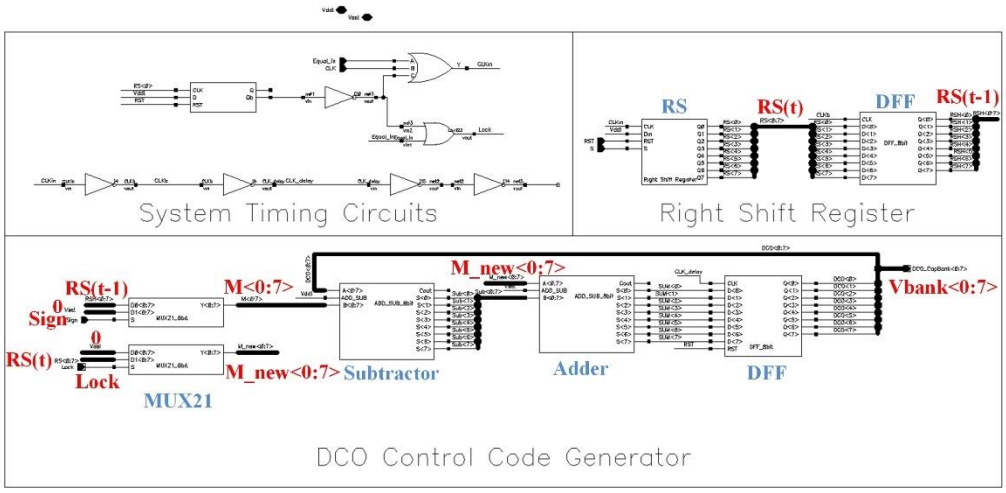
To convert the digital phase frequency detector result into digital code and control the varactor bank of DCO, a Phase Error to Varactor Bank Converter (PEVBC) circuit is needed in the proposed digital phase locked loop.

As described in Fig 5.5.1, the logic of the proposed PEVBC is as following: The initial setup of the varactor bank input is '00000000' for controlling the 8 in parallel varactors that will be discussed in Section 5.6.3, Fig 5.6.5, which stands for the highest frequency of the DCO. If the measured frequency of DCO output matches the FCW, the PEVBC keeps the current output, otherwise, the most significant bit is changed to '1' to decrease the DCO output frequency. The new frequency is measured and compared with the FCW again. If it matches FCW, the system is stable, and the adjustment is end; If the frequency is higher than FCW, the second most significant bit is converted from 0 to 1 to decrease the DCO frequency further; If the frequency is lower than FCW, the most significant bit is adjusted back to '0', and the second most significant bit is converted to 1 for further frequency test. Then, the other bit is adjusted with the same theory as the significant bit until the system is locked.

The top-level block diagram of the proposed PEVBC is shown in Fig 5.5.2 (a), and the circuit implementation in Cadence Virtuoso is expressed in Fig 5.5.2(b). A Right Shift (RS) register is used to generate the digital code *RS(t)* from '10000000' to '00000001', The new RS register output RS(t-1) is saved by a delayed system clock for further calculation.



(a)



(b)

Fig 5.5.2 (a) Top-level block diagram of PEVBC (b) Circuit implementation of PEVBC

A MUX is the first stage of the DCO control code generator, which is controlled by the sign bit from digital phase frequency detector. When the PLL system is not stable, there are two cases: the DCO frequency is higher than the FCW frequency, or it is lower than the FCW frequency. If the DCO frequency is higher, the output of the MUX is '00000000', otherwise, the output is the digital code of RS register from previous state.

A subtractor is the second stage after the MUX, and the previous DCO inputs is subtracted from the MUX outputs based on the comparison results of digital phase frequency detector stage. Then, the subtracted results is combined with either the saved RS register results or '0' based on locking condition from 'Lock' bit through an adder to generates the new control code of DCO varactor bank.

5.6 Digital Control Oscillator

A digital control oscillator is employed in DPLL to generate the desired high frequency signals [75]. Comparing with conventional VCO, it is more flexible to program by digital control words instead of varying the control voltage of the varactors.

Typically, there are two main kinds of DCOs: ring oscillator based and LC-tank based DCOs. The LC-tank DCO is more suitable in wireless communication applications because of the superior phase noise performance compared with digital ring oscillator [76] [77] [78].The main technique in conventional LC-tank DCO is adopting varactor array to vary the capacitance in order to realize the fine resolution as explained in Fig 5.6.1 and (5-6-1), where the varactor value C_{var} is decided by the digital control word D_i and parasitic capacitance C_{par} in (5-6-2).

$$f_{DCO} = \frac{1}{2\pi\sqrt{LC_{var}}} \tag{5-6-1}$$

$$C_{var} = C_{par} + \sum_{i=0}^{n} D_i \cdot C_i \tag{5-6-2}$$

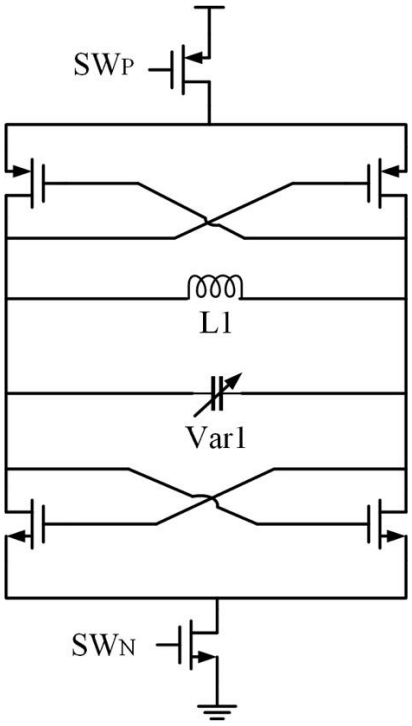


Fig 5.6.1 Schematic diagram of conventional DCO

5.6.1 Capacitor Bank and Frequency Tuning Range in Conventional DCO

For the conventional DCO in Fig 5.6.1, the relationship between the capacitance range of varactor bank and Frequency Tuning Range (FTR) is calculated in (5-6-3) to (5-6-4) below:

$$R_f = \frac{f_{max}}{f_{min}} = \frac{\frac{1}{2\pi\sqrt{LC_{var\_min}}}}{\frac{1}{2\pi\sqrt{LC_{var\_max}}}} = \sqrt{\frac{C_{var\_max}}{C_{var\_min}}} = \sqrt{\frac{C_{par}+\sum_{i=0}^{n} C_i}{C_{par}}} \quad (5\text{-}6\text{-}3)$$

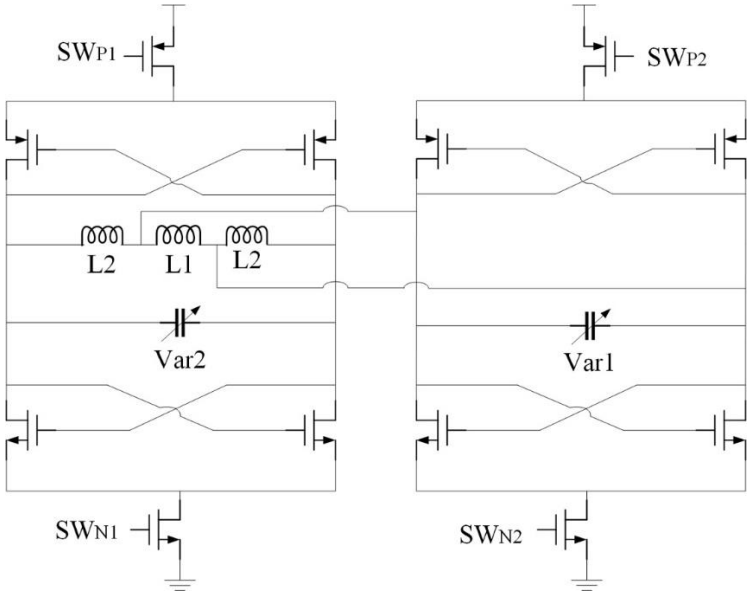
$$FTR = \frac{f_{max}-f_{min}}{\frac{f_{max}+f_{min}}{2}} \times 100\% = \frac{2(R_f-1)}{R_f+1} \times 100\% \quad (5\text{-}6\text{-}4)$$

It can be seen FTR is limited in the LC tank based DCO because the parasitic properties of varactor bank cannot be ignored [79] [80]. There is a trade-off between the FR and f_{max}, and FTR is limited by the f_{max}. For the design of multiple band frequency in 5G application, it is hard to meet the tuning range from 600MHz to 4.2GHz by single LC tank. The quad-band and multi-band LC tanks are studied to cover

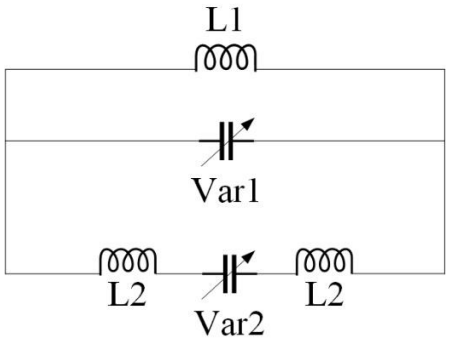
the frequency tuning range from 600MHz-930MHz, 2.4GHz-2.9GHz and 3.4-4.2GHz.

5.6.2 Quad-mode DCO

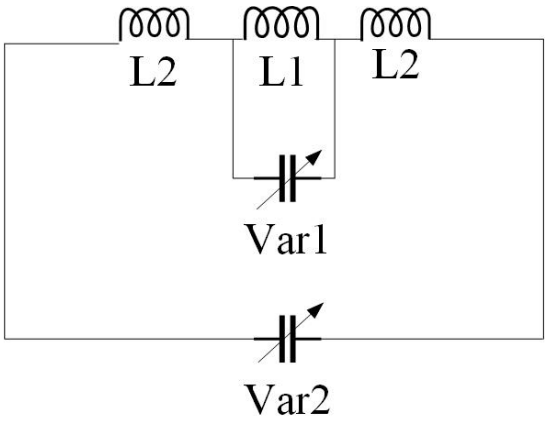
In Fig 5.6.2(a), a Quad-mode DCO consists of three inductors (L1, L2, L3) and two capacitor banks (Var1, Var2). The tuning mode is switched by alternating the two pairs of switches SW_{P1}/SW_{N1} and SW_{P2}/SW_{N2}. The circuit can be converted into two different structures as shown in Fig 5.6.2(b) and 5.6.3(c) separately [79] [80]. In structure I, SW_{P1} / SW_{N1} switches are on with SW_{P2} / SW_{N2} off, and the capacitive/inductive feature of V_{ar2} and L_2 is controlled by tuning the varactor bank V_{ar2}. While in structure-II, SW_{P2} / SW_{N2} are on with SW_{P1} / SW_{N1} off, and the capacitive/inductive feature of V_{ar1} and L_1 can also be switched by tuning V_{ar1}. In this case, four different operating modes are realized by employing two varactor banks.



(a)



(b)



(c)

Fig 5.6.2 (a) Schematic diagram of Quad-DCO (b) Equivalent circuit of Structure I (c) Equivalent circuit of Structure II

In structure I, the resonating frequency of L_1 and V_{ar1} is $f_{S1} = 1/(2\pi\sqrt{L_1 V_{ar1}})$, and the capacitive/inductive feature of V_{ar2}/L_2 branch either lower the effective inductance or higher the effective capacitance, so the output frequency of mode 1 and mode 2 are expressed as followed:

When the V_{ar2}/L_2 branch is inductive, $f_{OSC1} > f_{S1}$, and $L_2' = 2L_2 + \frac{\frac{1}{j\omega_{OSC1} Var_2}}{j\omega_{OSC1}}$. The oscillating frequency in mode 1 is expressed as:

$$f_{OSC1} = \frac{1}{2\pi\sqrt{(L_1 // L_2')Var_1}} \tag{5-6-5}$$

When the V_{ar2}/L_2 branch is capacitive, $f_{OSC2} < f_{S1}$, and the capacitance is $C_2' =$

$\frac{\frac{1}{j\omega_{OSC1}}}{(2j\omega_{OSC1}L_2+\frac{1}{j\omega_{OSC1}Var_2})}$. The oscillating frequency in mode 2 is:

$$f_{OSC2} = \frac{1}{2\pi\sqrt{L_1(Var_1+Var_2')}} \tag{5-6-6}$$

In structure II, the resonating frequency of L_2 and V_{ar2} is $f_{S2} = 1/(2\pi\sqrt{2L_2V_{ar2}})$, and the capacitive/inductive feature of V_{ar1} / L_1 branch either lower the effective inductance or higher the effective capacitance, and the oscillating frequency of mode 3 and 4 are calculated below:

When the Var_1/L_1 branch is capacitive, $f_{OSC1} > f_{S1}$, the capacitance of V_{ar1} in parallel with L_1 is $C_1' = \frac{\frac{1}{j\omega_{OSC2}}}{j\omega_{OSC2}L_1//\frac{1}{j\omega_{OSC2}Var_1}}$, and the equivalent oscillating frequency of mode 3 is:

$$f_{OSC3} = \frac{1}{2\pi\sqrt{(2L_2-\frac{1}{\omega_{OSC2}{}^2C_1'})Var_2}} \tag{5-6-7}$$

When the V_{ar1}/L_1 branch is inductive, $f_{OSC4} < f_{S1}$, the inductance for V_{ar1} and L_1 branch is $L_1' = \frac{j\omega_{OSC2}L_1//\frac{1}{j\omega_{OSC2}Var_1}}{j\omega_{OSC2}}$, and the output frequency for mode 4 is:

$$f_{OSC4} = \frac{1}{2\pi\sqrt{(2L_2+L_1')Var_2}} \tag{5-6-8}$$

To realize the wide band tuning range requirement of 5G network (600MHz to 930MHz, 2.4GHz to 2.9GHz, and 3.4GHz to 4.2GHz), the quad-mode DCO is used in this dissertation to generate the desired frequency in DPLL.

5.6.3 Implementation and Simulation of Digital Control Oscillator

The quad-mode DCO shown in Fig 5.6.3 is implemented in this dissertation to realize the frequency tuning range from 600MHz to 930MHz for low-band, and 2.4GHz

to 2.8GHz and 3.4GHz to 4.2GHz for mid-band. A channel select circuit shown in Fig 5.6.4(a) is used to select the frequency band of quad-mode DCO. As explained in Fig 5.6.4(b), when the select bit S is low, the SW_{P1} and SW_{N1} switches are on with SW_{P2} and SW_{N2} off, and the DCO is working in mid-band (2.4-2.8GHz and 3.4-4.2GHz). When S is high, SW_{P2} and SW_{N2} are on with SW_{P1} and SW_{N1} off, and the DCO is working in lower frequency band (600MHz to 930MHz).

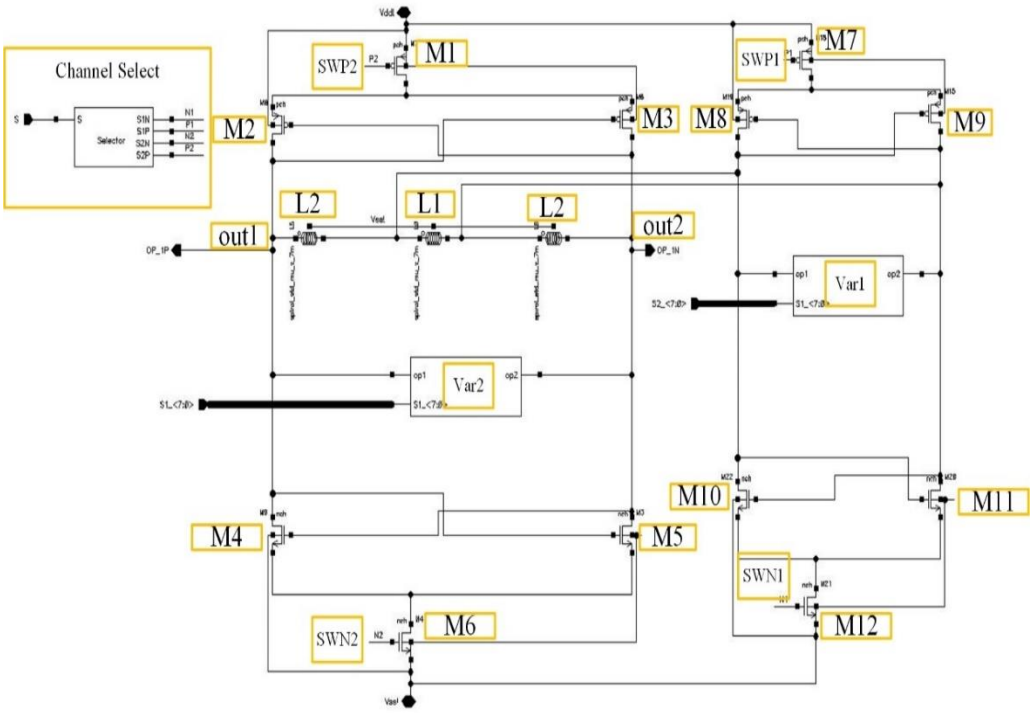
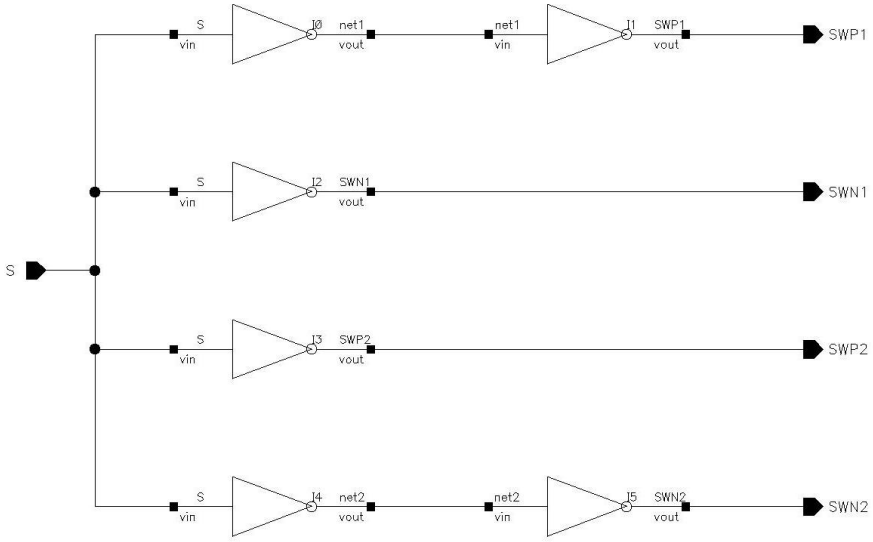
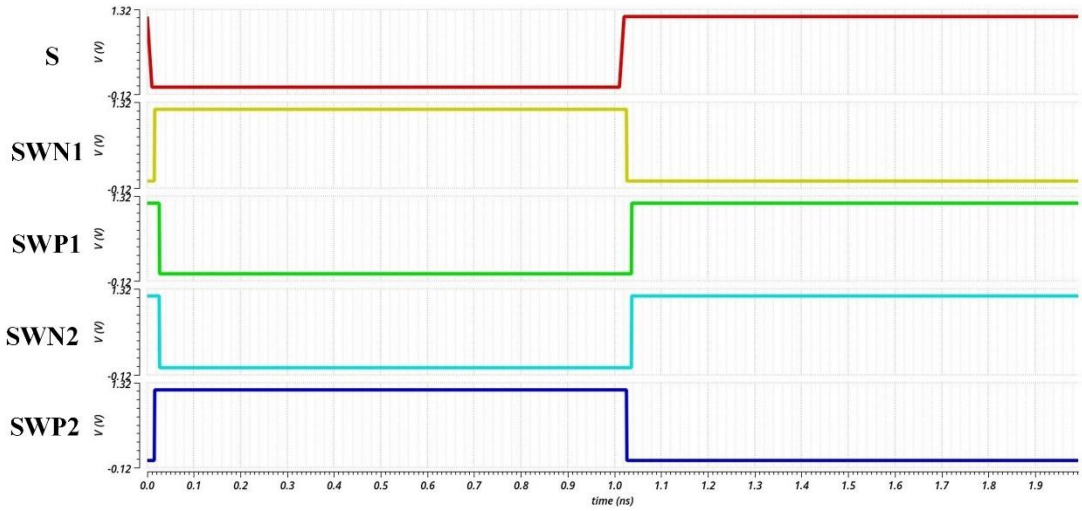


Fig 5.6.3 Schematic of quad-mode DCO



(a)



(b)

Fig 5.6.4 Logic of channel select circuit (a) Schematic (b) Simulation results

The circuit implementation of varactor banks is in Fig 5.6.5, which consists of 8 varactors. The tuning range of Var_1 is from 2.82pF to 0.02pF, and Var_2 is from 4.9pF to 0.04pF. Transistors' sizes of varactors are listed in Table 5.6.1.

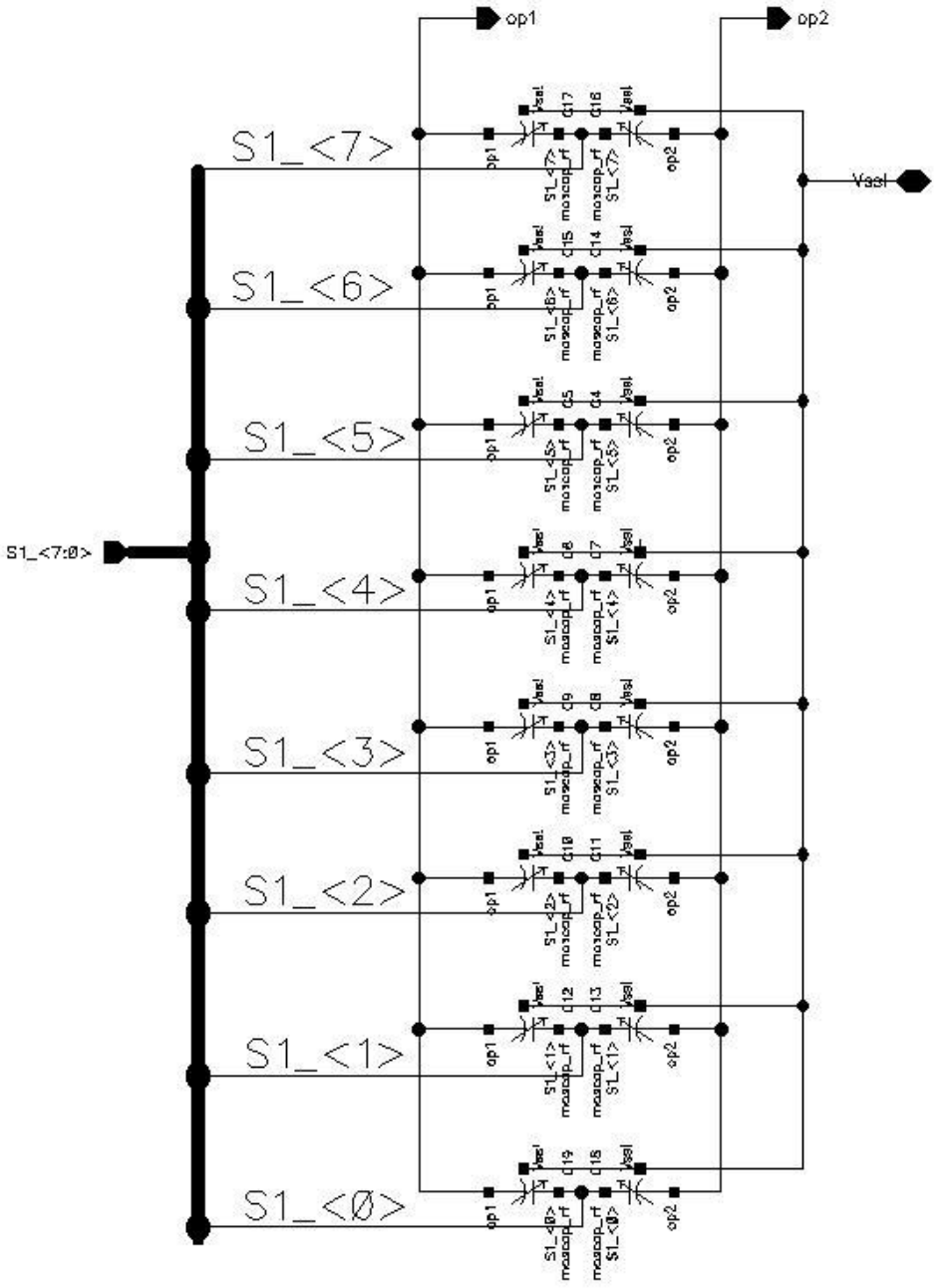


Fig 5.6.5 Schematic diagram of varactor bank

Table 5.6.1 Transistor sizes of varactor banks

Varactor bank	Width per finger (um)	Length (nm)	Finger per group	Number of Groups	Multiplier	Varactor (pF)
Var_1 20fF-2.82pF	3.2	3.2	8	2	1	2.82
	3.2	3.2	8	1	1	1.43
	3.2	3.2	4	1	1	0.71
	3.2	3.2	2	1	1	0.36
	3.2	1.6	2	1	1	0.18
	1.6	1.6	2	1	1	0.09
	1.6	0.8	2	1	1	0.04
	0.8	0.8	2	1	1	0.02
Var_2 40fF-4.9pF	2.8	3.2	8	4	1	4.9
	2.9	3.2	8	2	1	2.56
	2.9	3.2	8	1	1	1.29
	1.5	3.2	8	1	1	0.65
	1.5	1.6	8	1	1	0.32
	1.5	0.8	8	1	1	0.16
	1.4	0.4	8	1	1	0.08
	1.4	0.2	8	1	1	0.04

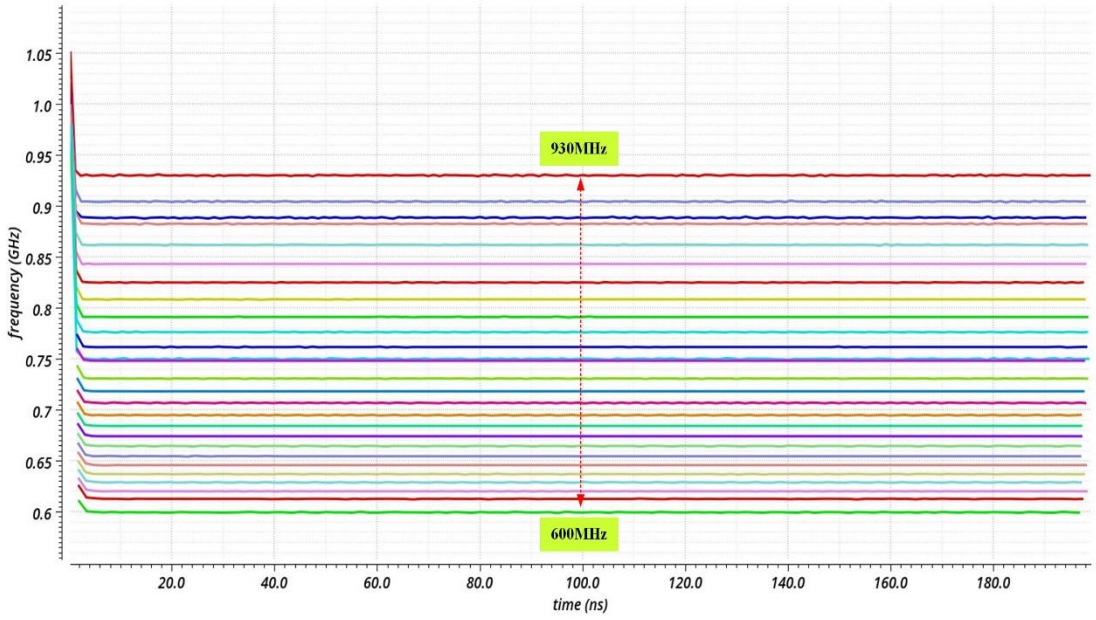
The quad-mode DCO in Fig 5.6.3 is implemented and simulated in TSMC 65nm technology, and the design tool is Cadence Virtuoso. The operating supply voltage is 1.2V. Transistor sizes are summarized in Table 5.6.2, and multiple fingers are used to increase the circuit performance based on rules of [81]. The inductors used in this design is 2nH for L_1 and 6.7nH for L_2.

Table 5.6.2 Transistor sizes of quad-DCO

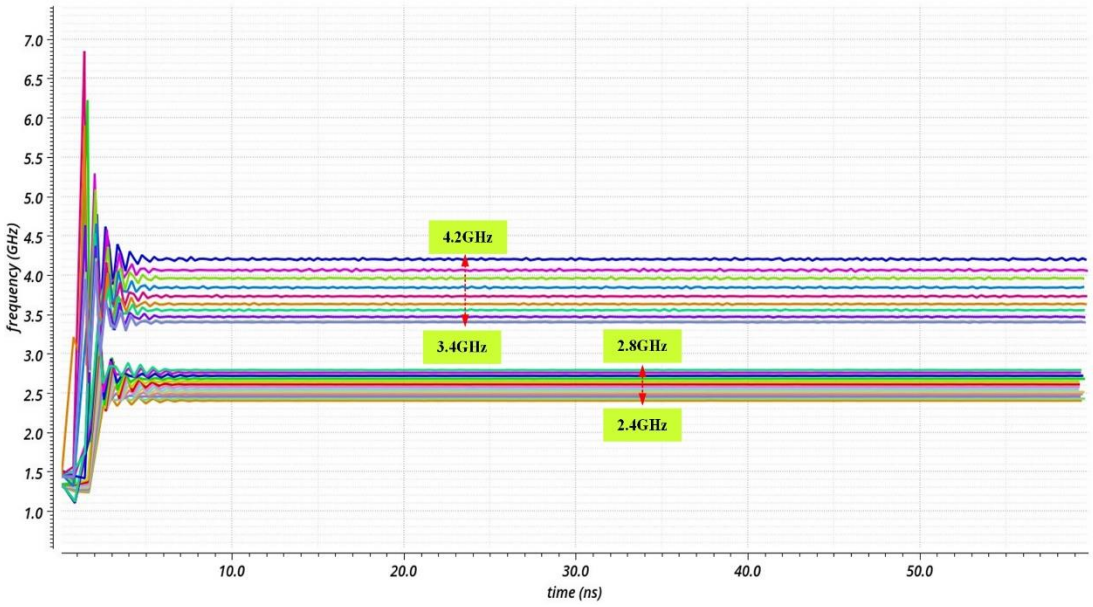
Transistor	Size (W/L)
M1	100um/130nm
M2/M3	70um/130nm
M4/M5	40um/130nm
M6	40um/130nm
M7	100um/130nm
M8/M9	70um/130nm
M10/M11	75um/130nm
M12	50um/130nm

Fig 5.6.6 (a) and (b) shows the frequency response of the quad-mode DCO operating at low-band and mid-band under different varactors. By increasing the

capacitance of varactors, the output frequency of DCO can be varied from 930MHz to 600MHz, 2.8GHz to 2.4GHz and 4.2GHz to 3.4GHz. The frequencies versus varactors plots are explained in Fig 5.6.7 (a) to (c), and the slops are relatively linear for different operating bands. The frequency resolutions for different bands are listed in Table 5.6.3, which meet the design requirement in Table 5.3.1. In Fig 5.6.8(a) to (c), the zoom-in version of transient simulation results for different structures are presented, and only the circuit operating at 3.8GHz, 2.4GHz, and 600MHz are presented for simplicity.

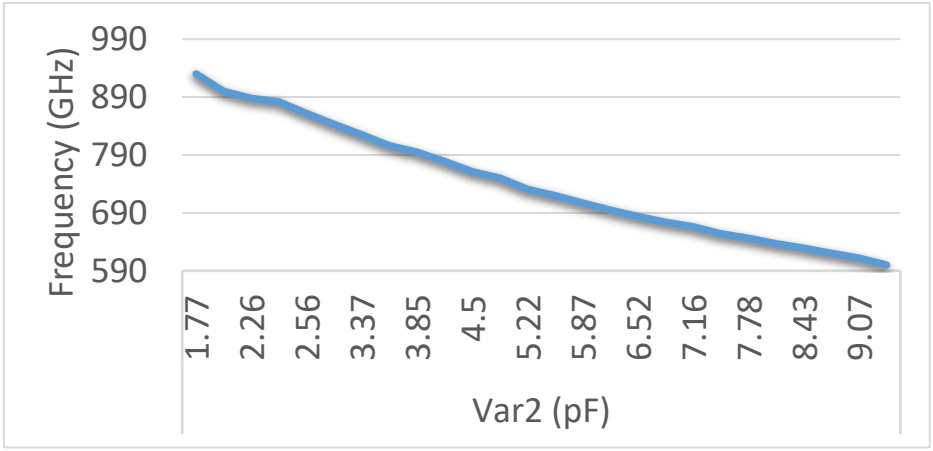


(a)

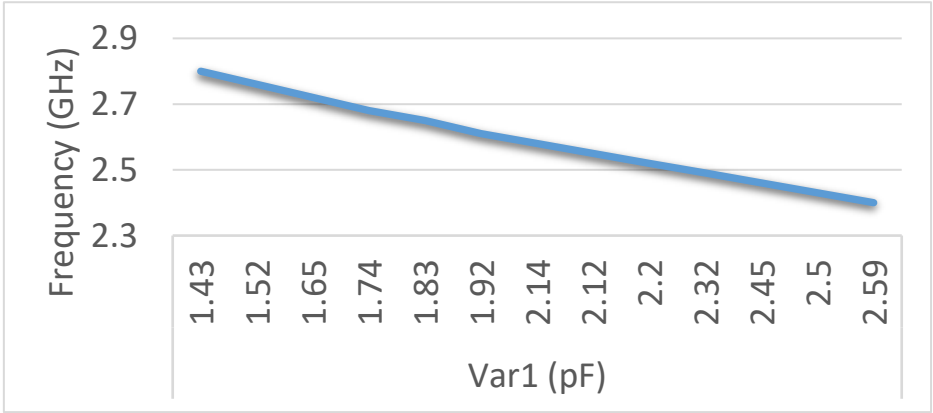


(b)

Fig 5.6.6 Simulation results of frequency response (a) Low band (b) Mid band



(a)



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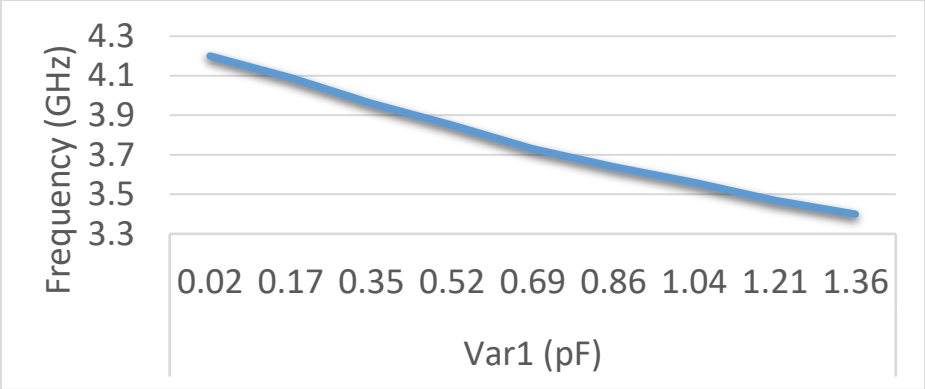
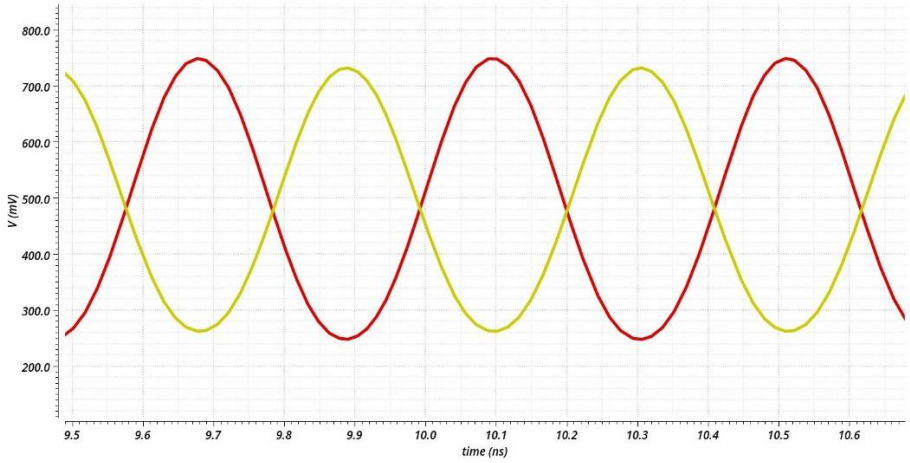


(c)

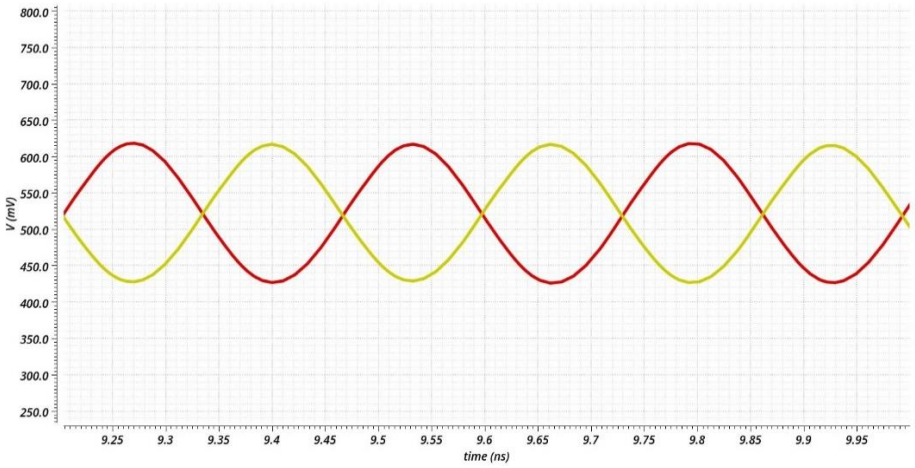
Fig 5.6.7 Frequency versus varactor plots (a) 600MHz to 930MHz band (b) 2.4GHz to 2.8GHz band (c) 3.4GHz to 4.2GHz band

Table 5.6.3 Frequency Resolution of quad-mode DCO

Varactors	Capacitance (pF)	Frequency (GHz)	Frequency Resolution (MHz/step)
Var1 off	1.77	0.93	8.25
	2.26	0.89	
	2.56	0.86	
	3.37	0.83	
	4.17	0.78	
	4.9	0.75	
	6.19	0.70	
	7.46	0.65	
	8.43	0.63	
	10	0.6	
Var2=4.9pF	2.58	2.84	100
	2.77	2.76	
	3.12	2.68	
	3.46	2.61	
	3.63	2.58	
	3.81	2.55	
	3.98	2.52	
	4.16	2.49	
	4.51	2.43	
	4.68	2.4	
Var2 off	0.02	4.2	200
	0.17	4.09	
	0.35	3.96	
	0.52	3.85	
	0.69	3.73	
	0.86	3.64	
	1.04	3.56	
	1.21	3.47	
	1.36	3.4	



(a)



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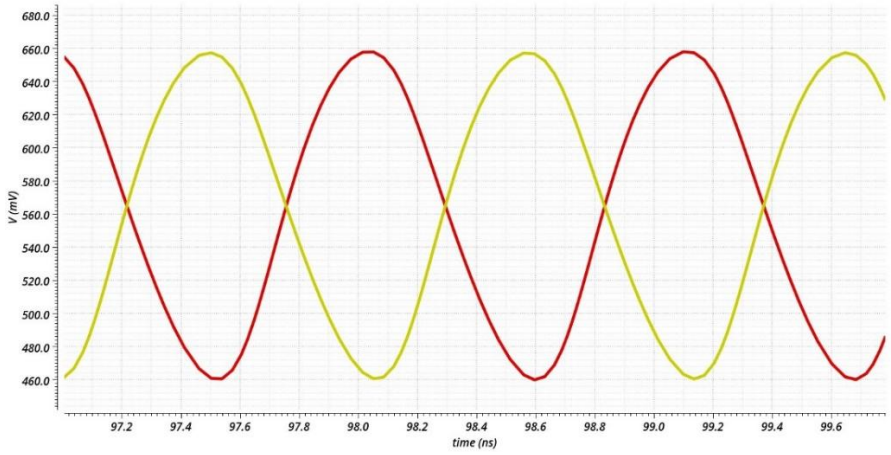


(c)

Fig 5.6.8 Transient simulation results for (a) Structure I at 3.8GHz (b) Structure

II at 2.4GHz (c) Structure III at 930MHz

Based on the simulation results, the quad-mode DCO can be used to generate the signals for low-band and mid-band. By turning on and off the switches SW_1 and SW_2, the operating frequency of DCO is varied to realize the wideband properties with relative high frequency resolution. In addition, the power consumption of the quad-mode DCO is from 5.58mW to 6.78mW.

5.7 Implementation and Simulation of Simplified Phase-Domain Phase Locked Loop

As described in Fig. 5.7.1, the proposed simplified phase-domain digital phase locked loop consists of a digital phase frequency detector to compare the phase between reference signal and DCO outputs and convert it into digital information; a digital loop filter to convert the digital code from PFD to the varactor control signals of DCO; a Channel Select (CS) circuit to process the varactor control code to certain varactor banks and a digital control oscillator to generate the differential waveforms.

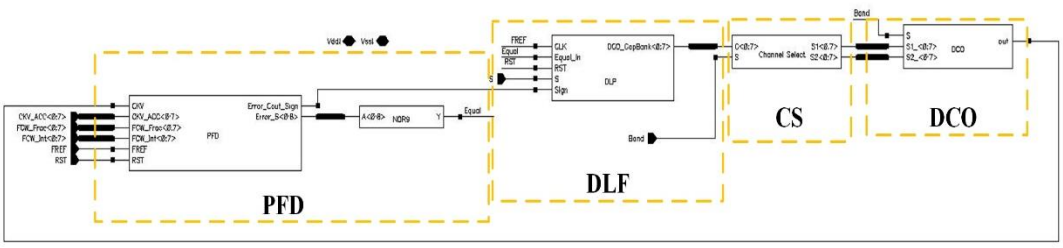


Fig 5.7.1 Schematic of Proposed Simplified Phase-Domain

The logic of channel select circuit is shown in Table 5.7.1. When S is low, the digital control code is used to control Var1, and the DCO is operating in mid-band. The inputs of Var2 are low. When S is high, the digital control code is used to control Var2, the DCO is operating in low band, and the inputs for Var1 are low. The relationship between S, control word (CW), Var1 and Var2 can be expressed as (5-7-1) and (5-7-2), and the circuit implementation of CS circuit is shown in Fig 5.7.2.

$$Var1 = \bar{S} \cdot CW \tag{5-7-1}$$

$$Var2 = S \cdot CW \tag{5-7-2}$$

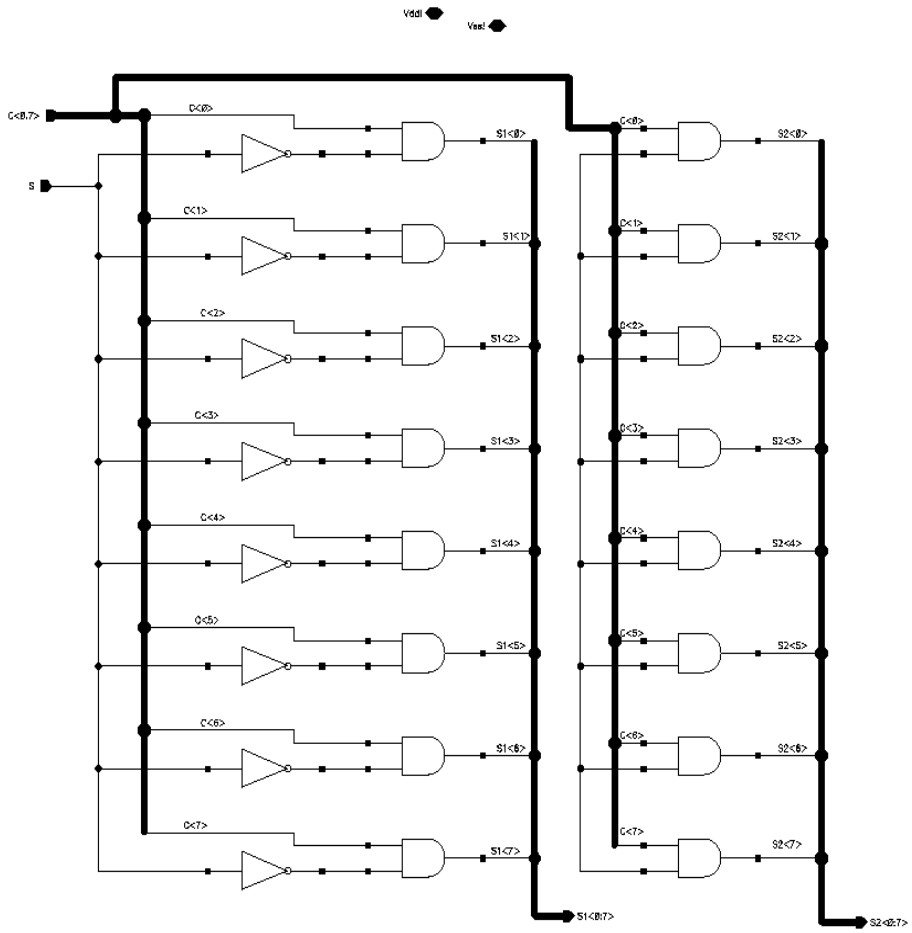
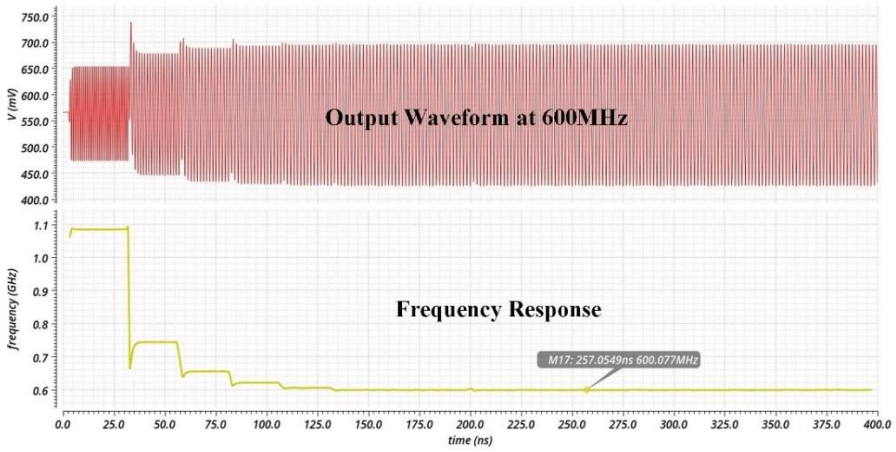


Fig 5.7.2 Circuit implementation of channel select

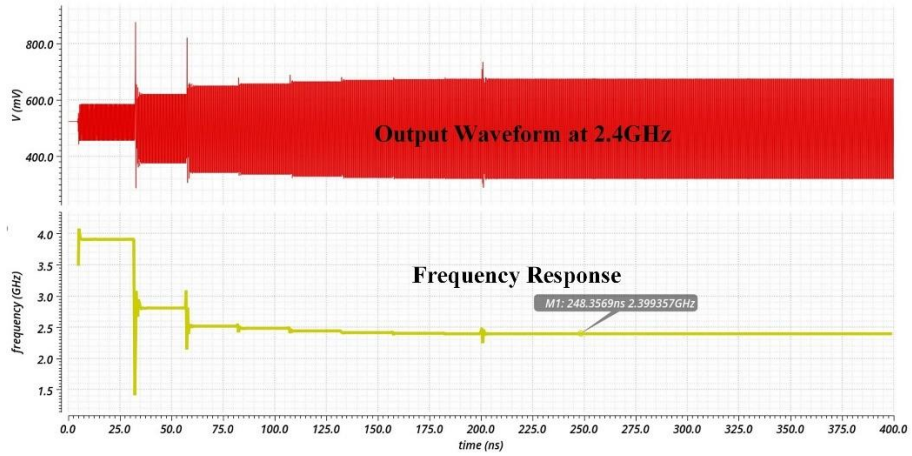
Table 5.7.1 Truth Table of Channel Select Circuit

S	DCO Control Code (CW)	Varactor 1	Varactor 2
0	**X**	**X**	**0**
1	**X**	**0**	**X**

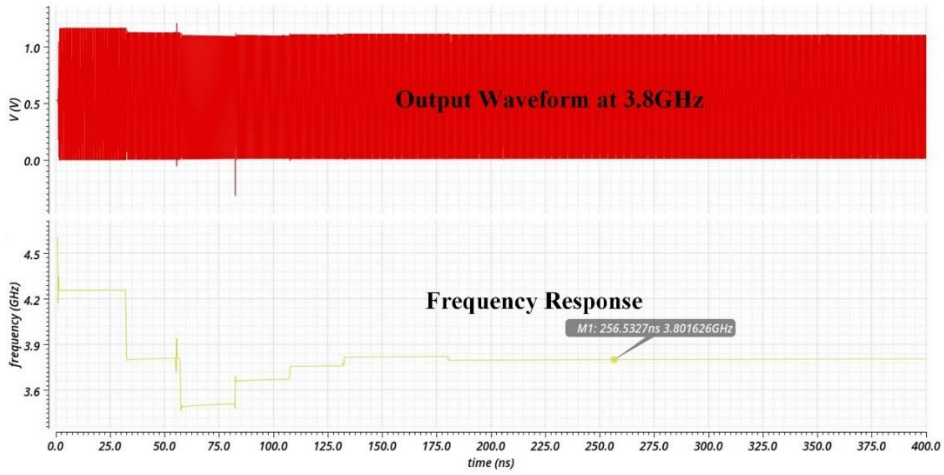
The proposed digital PLL is implemented in Cadence virtuoso software, and the power supply is 1.2V. The transient simulation results for the DPLL working in 600MHz, 2.4GHz and 3.8GHz are shown in Fig 5.7.3 (a), (b) and (c) respectively. The proposed phase-domain digital PLL calibrates the operating frequency based on the frequency control word and then stabilized at the desired frequency. The power consumptions of the circuit are 6.93mW at 600MHz, 8.53mW at 2.4GHz and 10.23mW at 3.8GHz operating frequency. The phase noise performances of the proposed digital PLL are shown in Fig 5.7.4 (a) to (d), and the PN performance is comparable with other state art designs as summarized in Table 5.7.2.



(a)

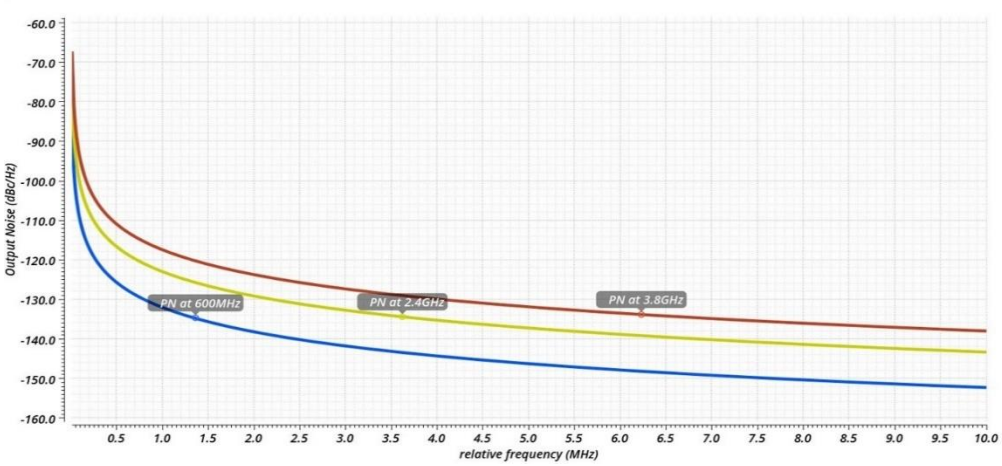


(b)

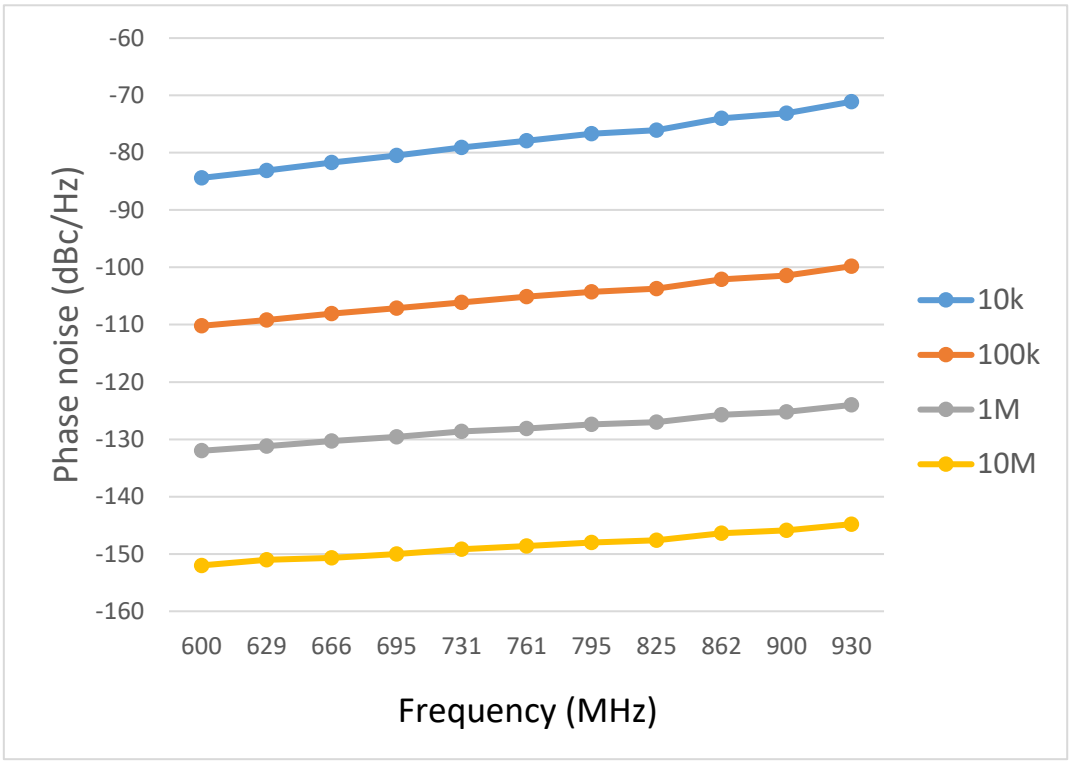


(c)

Fig 5.7.3 Transient simulation for proposed simplified phase-domain PLL (a) at 600MHz (b) at 2.4GHz (c) at 3.8GHz



(a)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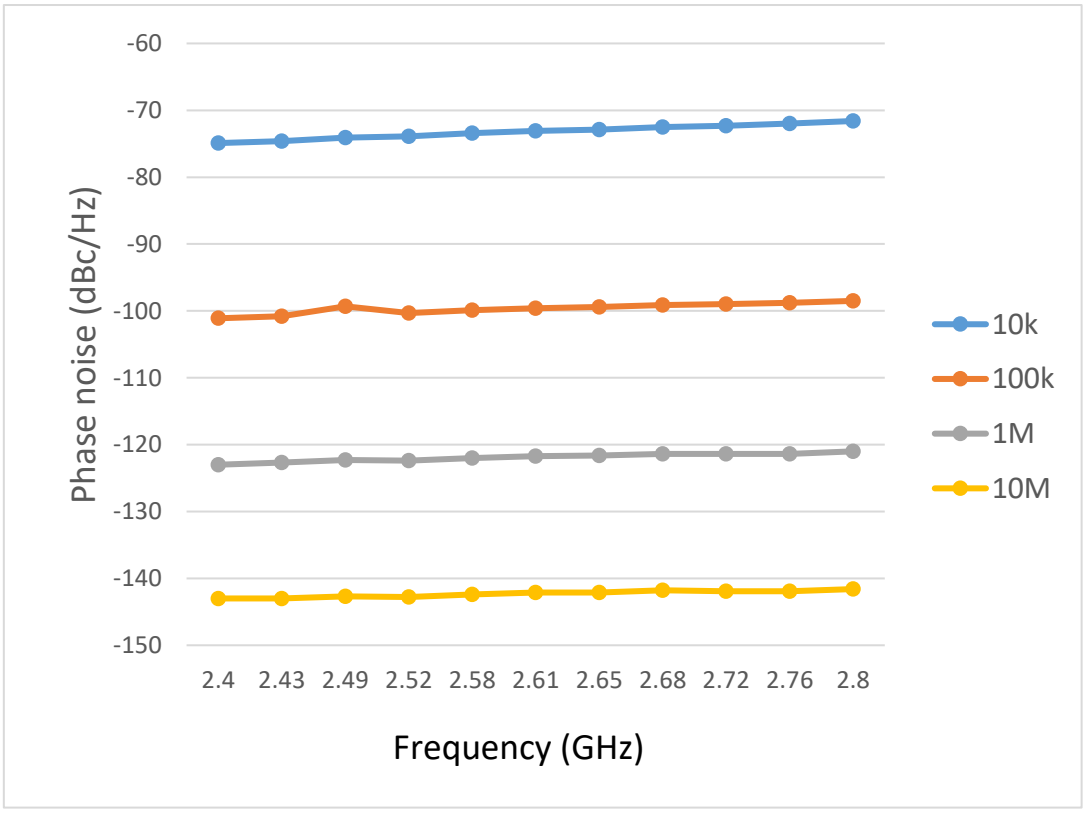
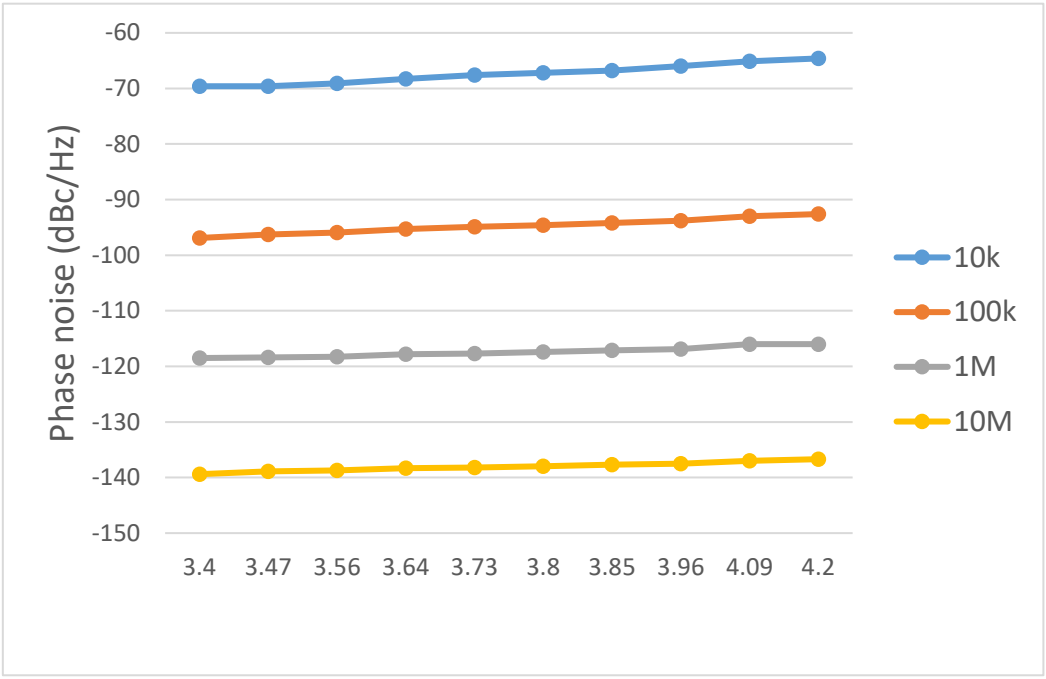
-130
-140
-150
-160
Phase noise (dBc/Hz)
600 629 666 695 731 761 795 825 862 900 930
Frequency (MHz)
10k
100k
1M
10M

(b)


-60
-70
-80
-90
-100
-110
-120
-130
-140
-150
Phase noise (dBc/Hz)
2.4 2.43 2.49 2.52 2.58 2.61 2.65 2.68 2.72 2.76 2.8
Frequency (GHz)
10k
100k
1M
10M

(c)



(d)

Fig 5.7.4 Phase noise performance of the proposed phase-domain digital PLL (a) Simulation results of the PLL operating at 600MHz, 2.4GHz and 3.8GHz (b) PN results for PLL at 600MHz to 930MHz band (c) PN results for PLL at 2.4GHz to 2.8GHz (d) PN results for PLL at 3.4 to 4.2GHz

Table 5.7.2 Phase Noise Performance Summary

	[21]	[82]	[80]	[83]	This Work
Architecture	Digital	Analog	Digital	Digital	Digital
Design Type	Fabrication	Fabrication	Schematic	Fabrication	Schematic
Process	28nm	180nm	130nm	65nm	65nm
Reference Frequency	40MHz	48MHz	45MHz	40MHz	40MHz
Operating Frequency	1.425GHz-2.125GHz	2.12-2.4GHz	880MHz-5.85GHz	2.9GHz-4GHz	600MHz-4.2GHz
Phase Noise	-164dBc/Hz @20MHz (915MHz)	-112dBc/Hz @50kHz	-110dBc/Hz @1MHz (2.8GHz)	-102dBc/Hz @50kHz	-110dBc/Hz @100kHz (600MHz) -101dBc/Hz @100kHz (2.4GHz) -97dBc/Hz @100kHz (3.4GHz)

VI. Circuit Implementation and Simulation of Proposed Quadrature Phase-Domain ADPLL with Integrated On-line Amplitude Locked Loop Calibration System

6.1 Circuit implementation and Simulation

In this dissertation, an active RC-CR phase shifter circuit is proposed to generate wide band and accurate quadrature phase signals; an integrated on-line amplitude locked loop calibration system is created to vary the pole frequency of the active RC-CR phase shifter and generate constant gain quadrature signals; a 10-transistor symmetric high-speed high-sensitivity dynamic voltage comparator is proposed to improve the accuracy and speed of the calibration system; a simplified phase-domain digital phase frequency detector architecture is proposed to reduce the detection time and avoid extra clock signal generator; a quad-mode DCO circuit is used to realize the multi-band (600MHz to 930MHz, 2.4GHz to 2.8GHz and 3.4GHz to 4.2GHz) function within one DCO circuit; a multi-band highly programmable all digital phase-domain PLL is designed to meet the requirement of 5G network..

The proposed simplified quadrature phase-domain digital PLL with integrated active amplitude detection and calibration locked loop system is created in Cadence Virtuoso software with 65nm process, and the power supply of the circuit is 1.2V. As shown in Fig 6.1.1, it consists of a simplified phase domain all digital PLL to generate the frequency based on digital frequency control codes, a pair of bias removal circuits to convert the dc offsets of differential signals from DCO to 0V for 90-degree phase

shifter inputs, and a pair of 90-degree phase shifter with integrated on-line amplitude calibration system to generate the constant gain quadrature outputs.

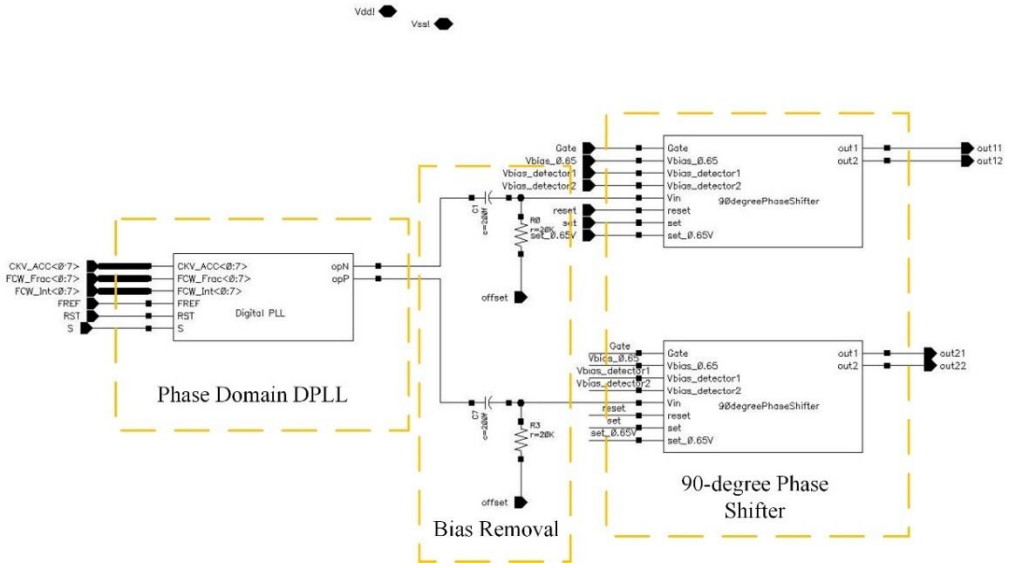
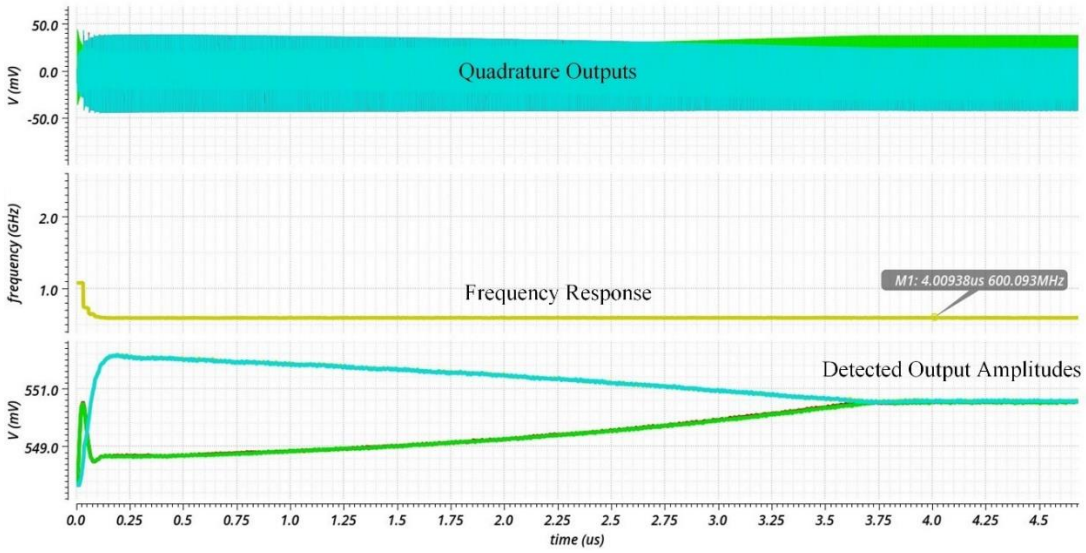
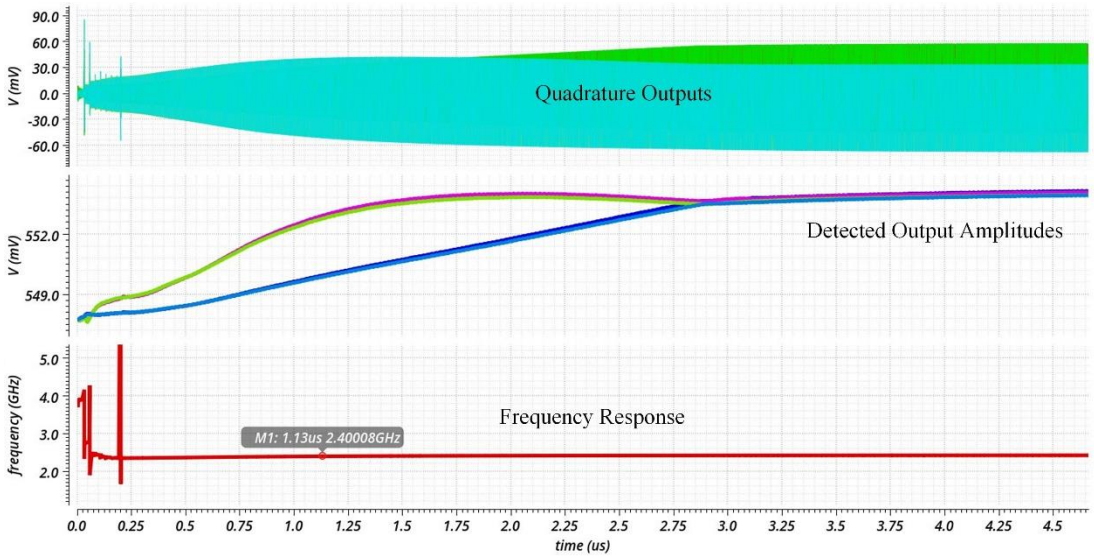


Fig 6.1.1 Circuit implementation of proposed ADPLL with 90-degree phase shifter

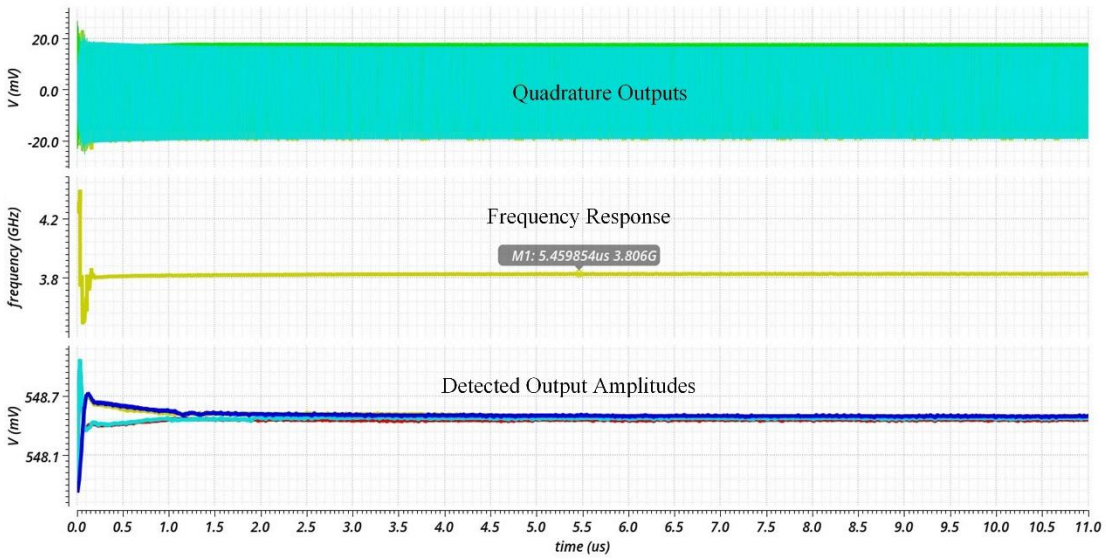
The simulation results of the proposed architecture are described in Fig 6.1.2 (a) to (c) for the cases of system operating at 600MHz, 2.4GHz and 3.8GHz respectively. In the frequency response plots, the desired frequencies are generated by the simplified phase-domain digital PLL initially, which takes about 200ns. Then, the frequency is locked for amplitude calibration. For the output amplitude plots, the amplitudes of the outputs are calibrated to constant values through the on-line amplitude locked calibration feedback system. It takes about 3.5us for circuit working at 600MHz, 3us for circuit operating at 2.4GHz and 2us for circuit at 3.8GHz. A zoom-in version of the transient simulation result for circuit operating at 2.4GHz is shown in Fig 6.1.3 (d), the amplitudes for the four quadrature outputs are calibrated to constant gain by employing the proposed active on-line amplitude locked loop calibration system.


Quadrature Outputs
V (mV)
50.0
0.0
-50.0
Frequency Response
frequency (GHz)
2.0
1.0
M1: 4.00938us 600.093MHz
Detected Output Amplitudes
V (mV)
551.0
549.0
0.0 0.25 0.5 0.75 1.0 1.25 1.5 1.75 2.0 2.25 2.5 2.75 3.0 3.25 3.5 3.75 4.0 4.25 4.5
time (us)

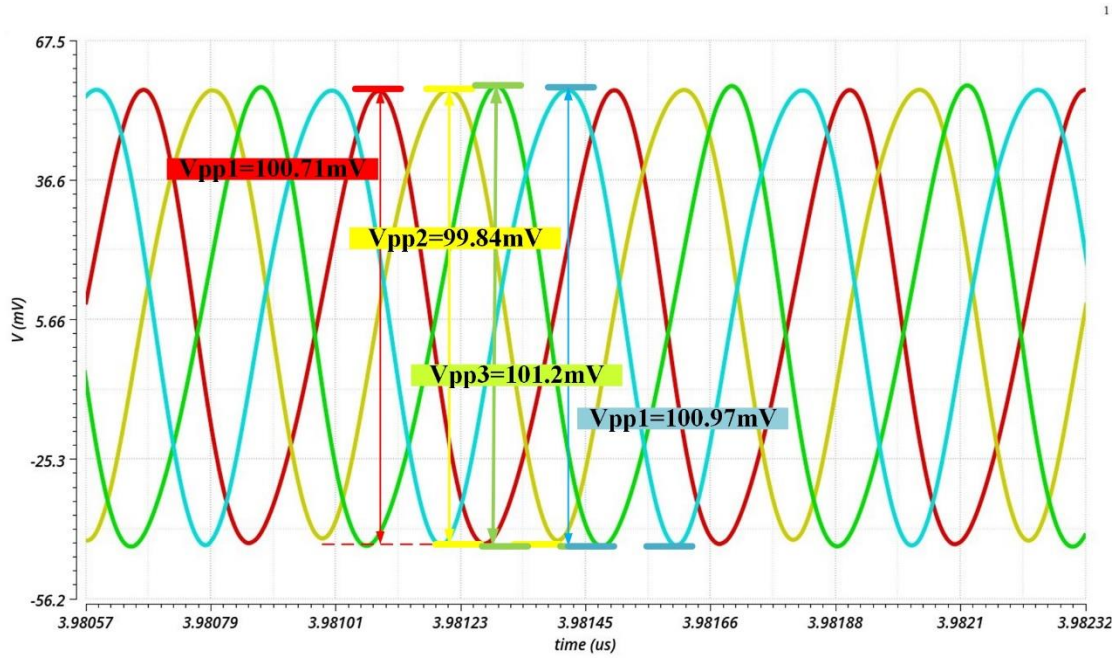
(a)


Quadrature Outputs
V (mV)
90.0
60.0
30.0
0.0
-30.0
-60.0
Detected Output Amplitudes
V (mV)
552.0
549.0
Frequency Response
frequency (GHz)
5.0
4.0
3.0
2.0
M1: 1.13us 2.40008GHz
0.0 0.25 0.5 0.75 1.0 1.25 1.5 1.75 2.0 2.25 2.5 2.75 3.0 3.25 3.5 3.75 4.0 4.25 4.5
time (us)

(b)



(c)

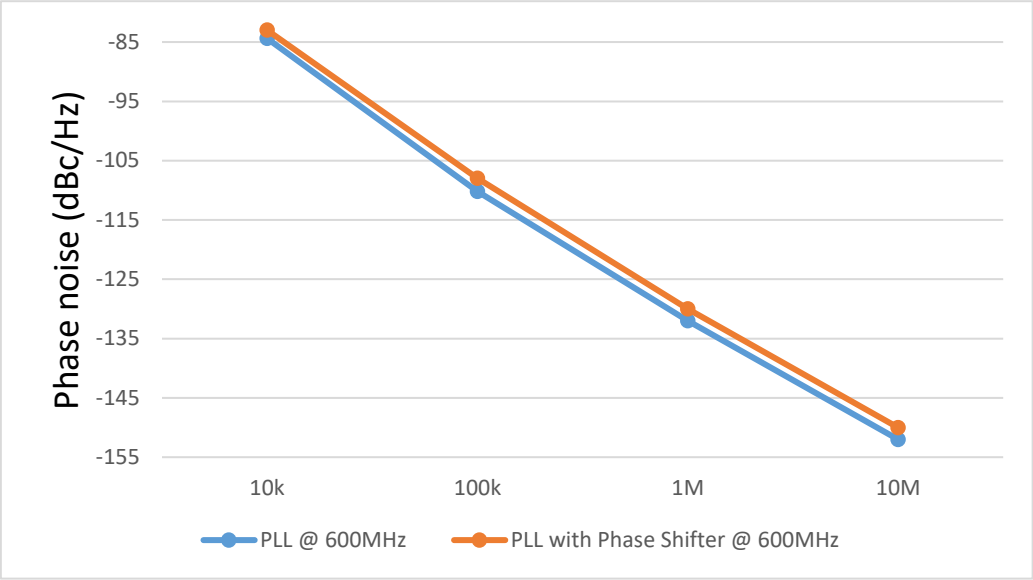


(d)

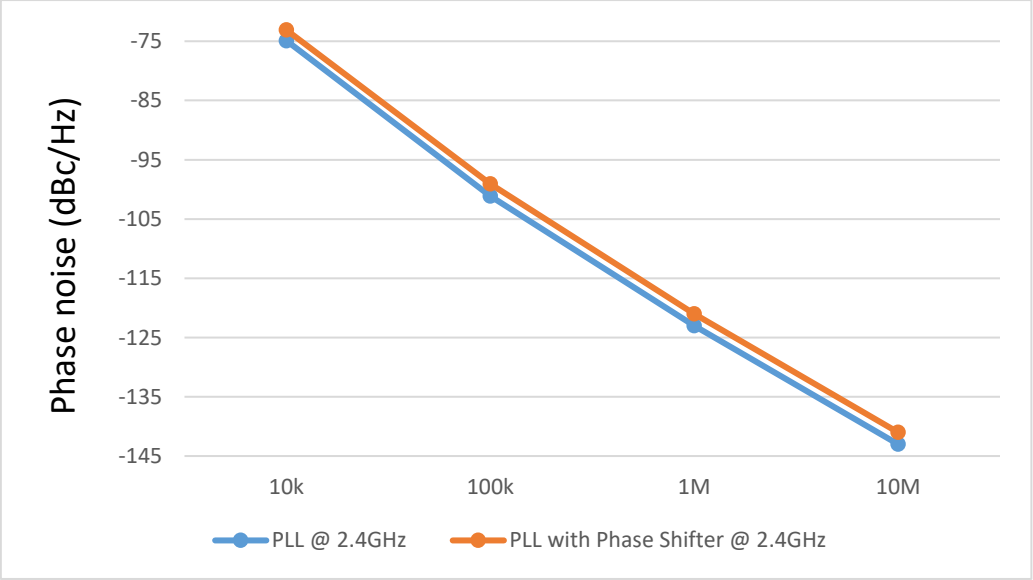
Fig 6.1.2 Transient simulation results of proposed DPLL with 90-degree phase shifter (a) Frequency at 600MHz (b) Frequency at 2.4GHz (c) Frequency at 3.8GHz (d) Zoom-in version of transient simulation result at 2.4GHz

The simulation results of phase noise performance of the phase-domain DPLL without/with integrated on-line amplitude locked loop calibration system are shown in Fig 6.1.3. The PN performance is varied slightly after adding the 90-degree phase

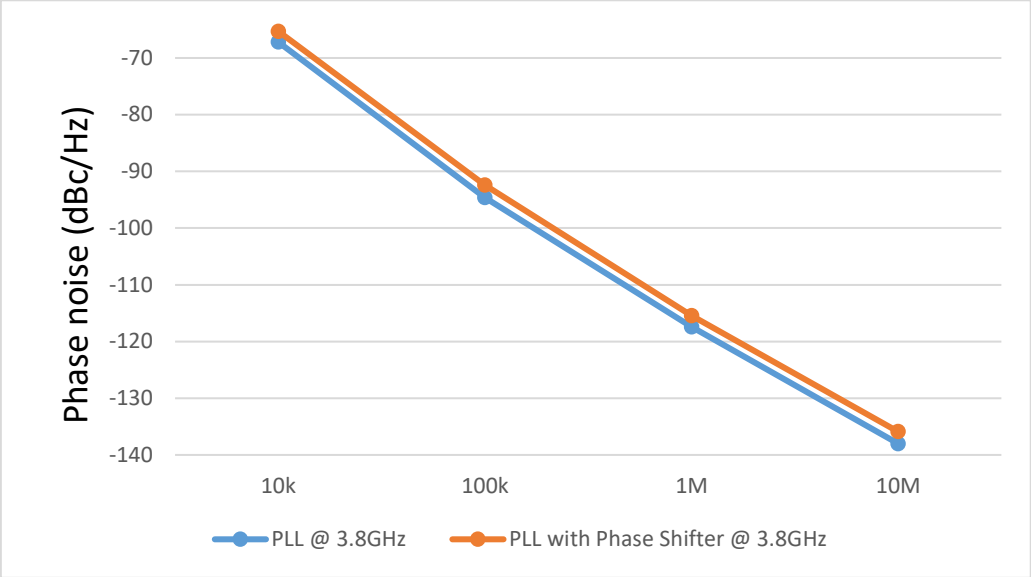
generator. In this case, the proposed integrated phase shifter system is feasible for a wide input frequency range within one integrated circuit. Besides, the 90-degree phase shifter system can be used after the PLL to generates the constant quadrature phases without varying the frequency.



(a)



(b)



(c)

Fig 6.1.3 Phase noise performance of quadrature phase-domain DPLL without/with integrated on-line amplitude calibration system (a) at 600MHz (b) at 2.4GHz (c) at 3.8GHz

6.2 Conclusion

The phase noise performances of the proposed simplified quadrature phase-domain DPLL with integrated on-line amplitude locked loop calibration system are listed in Table 6.1.1. By combining the wide band simplified phase-domain digital PLL with active RC-CR 90-degree phase shifter with on-line amplitude locked calibration system, the proposed quadrature frequency synthesizer system can be used to realize the multi-band requirement of 5G applications with simplified circuit design, relative low power consumption, fast response time, and acceptable phase noise performance.

The comparison of the proposed quadrature phase-domain digital PLL with other state-of-arts are summarized in Table 6.1.2. By employing the integrated 90-degree

phase shifter with on-line amplitude locked loop, the proposed circuit automatically generates quadrature phases within the wide frequency tuning range (600MHz to 4.2GHz), and the output gains are calibrated to constant values for the use of beamforming and image rejection purpose in transceiver system. Besides, the proposed architecture is low complexity with low phase noise, relative low power consumption and acceptable response time.

Table 6.1.1 Circuit performance of proposed quadrature DPLL

		@ 600MHz	@ 2.4GHz	@ 3.8GHz
Power Consumption (mW)		11.04	14.84	17.5
Phase Noise (dBc/Hz)	@ 10kHz	-84.1	-74.1	-66.3
	@ 100kHz	-108	-100.2	-93.4
	@ 1MHz	-130.2	-122	-116.5
	@ 10MHz	-150.9	-142	-137
Response time (us)		3.5	3	2

Table 6.1.2 Performance comparison of proposed wide band quadrature digital PLL with other state of art designs

	[80]	[21]	This Work
Process	0.13um	28nm	65nm
Design Type	Schematic	Fabrication	Schematic
Supply Voltage (V)	1.2V	1.05V	1.2V
Type	Differential	Differential	Quadrature
Operating Frequency (GHz)	0.8-1.1, 1.9-2.8, 3.2-4, 5-6	1.425-2.125	0.6-0.93, 2.4-2.8, 3.4-4.2
Resolution	3KHz@0.8-1.1GHz, 15KHz@1.9-4GHz, 30KHz@5-6GHz	-	8.25MHz@0.6-0.93GHz, 100MHz@2.4-2.8GHz, 200MHz@3.4-4.2GHz
Response Time	<1us	2us	3.5us@600MHz, 3us@2.4GHz, 2us@3.8GHz
Power Consumption	24.9mW@1GHz, 31.6mW@5.7GHz	7.4mW	11.04mW@600MHz, 14.84mW@2.4GHz, 17.5mW@3.8GHz

Phase Noise (dBc/Hz)	-116.6@1MHz offset@1GHz output, -105.6@1MHz offset@1GHz output	-164@20MHz offset	-108@100KHz offset@600MHz output, -100.2@100KHz offset@2.4GHz output, -93.4@100KHz offset@3.8GHz output

VII. Conclusion and Future Works

7.1 Conclusion

In this dissertation, an active 90-degree RC-CR phase shifter is proposed to generate quadrature outputs for image rejection and beamforming purpose, followed with an integrated on-line amplitude locked loop calibration system to compensate the gain error and output constant amplitudes. A 10-transistor symmetric low-complexity, high-speed and high-sensitivity dynamic comparator is proposed to improve the calibration system properties of speed and accuracy.

A highly programmable simplified phase-domain digital PLL is presented to deliver multi-band signals under 5G network protocol and verify the function of constant gain phase-shifter system, which eliminates the reference phase estimator to reduce detection time and extra clock generator, and single quad-mode DCO core is used to realize the multi-band function. The proposed circuit is designed for wide frequency tuning range within one integrated circuit with low circuit complexity, low phase noise performance, low power consumption and acceptable response time, which is compatible with 5G standard.

7.2 Major Contribution

- Design a varied pole active 90-degree RC-CR phase shifter to realize the wideband properties instead of the single frequency in conventional passive RC-CR architecture.

- Design a high-sensitivity high-speed dynamic comparator with parallel input clocked switches in calibration system to decrease the gain error of quadrature

outputs.

- Design a calibration system that can compensate process variation and vary the pole frequency of active RC-CR phase shifter with input signal automatically.

- Design a multi-band and simplified phase-domain digital PLL for different spectrum standard.

- Combine multi-band phase-domain digital PLL with 90-degree phase shifter circuit to realize the wideband multi phases digital PLL for 5G network.

7.3 Publications

Referenced Journal Papers

1. **X. Zhang**, S. Li, R. Siferd and S. Ren, “A 170MHz Wideband 90nm CMOS RC-CR Phase Shifter with Integrated On-Line Amplitude Locked Loop Calibration for Hartley Image Rejection Transceiver” *Circuit, System and Signal Processing*, April 2021.

2. **X. Zhang**, S. Li, R. Siferd and S. Ren, “High-sensitivity high-speed dynamic comparator with parallel input clocked switches,” *International Journal of Electronics and Communications*, July 2020.

3. H. Xue, C. R. Benedik, **X. Zhang**, S. Li and S. Ren, "Numerical Solution for Accurate Bondwire Modeling," *IEEE Transactions on Semiconductor Manufacturing*, vol. 31, no. 2, pp. 258-265, May 2018.

4. S. Li, **X. Zhang** and S. Ren, "On-chip self-calibration system for CMOS active inductor band pass filter," *AEU–International Journal of Electronics and Communications,* vol 92, Pages 64–68, August 2018

5. S. Li, **X. Zhang** and S. Ren, "High frequency unity gain buffer in 90nm CMOS technology," *Journal of Circuits, Systems, and Computers*, vol 25 Issue 7, p-1. 17p. July 2016

6. T. Moody, **S. Li** and S. Ren, "A Low Power 10-bit 850 MHz bandwidth 90nm DAC," *Journal of Circuits, Systems, and Computers.* (To be submitted)

Papers Published in Full and Official Proceedings

1. **X. Zhang**, S. Li and S. Ren, "Adjustable lumped impedance mismatching compensation circuit," 2016 *IEEE International Conference on Electron Devices and Solid-State Circuits (EDSSC)*, Hong Kong, Aug 2016, pp. 287-290.

2. **X. Zhang**, S. Li, T. Moody, H. Xue, and S. Ren, "Multi-finger MOSFET low noise amplifier performance analysis," *IEEE National Aerospace and Electronics Conference*, Dayton, OH, July 2014.

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7.4 Future Work

In this dissertation, the proposed phase-domain DPLL is not optimized. The sub-circuit performance such as TDC, variable estimator, etc. can be improved to increase the system frequency resolution, response time and power consumption. Besides, the layout of simplified phase-domain DPLL can be implemented carefully to validate the system performance.

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