Electrical design of Switched-Capacitor second-order high-Q low-pass filter with channel multiplexing

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Abstract

The aim of this thesis is to design a discrete-time second-order low-pass filter with channel multiplexing for the electronic stability control system. The purpose of this design is to study the current and noise behavior of the multiplexed discrete-time design in comparison to a single-channel continuous-time design. This work discusses the importance of a discrete-time analog filter topology over continuous time in context of integrated area, cost and complexity. It argues about the selection of a ladder-type switched-capacitor filter for the required application and presents the steps for the design from an equivalent RLC filter. It addresses the component design of the selected topology as well as the operational amplifier design. It also discusses the reasons behind the selection of the folded cascode operational amplifier topology for the design. The clocking sequence for the switched-capacitor switches as well as the channel multiplexing switches is explained. The design is verified with simulations and the results of the essential parameters describing the performance of the design are presented. These parameters include the frequency response of the design, current consumption, noise levels, total harmonic distortion of the output signal, and channel isolation between the multiplexed channels. The work is concluded with an explanation of the results and a discussion on the reasons behind out of specification results. Based on this discussion, future work as well as improvements to the existing designs are suggested.

Keywords channel-multiplexing, discrete-time low-pass filter, folded-cascode operational amplifier, ladder-filter, Switched-Capacitor

Preface

The work in this thesis has been done for Murata Electronics as part of an ongoing research project. First of all, I am thankful to Allah Almighty for giving me strength and always guiding me towards the right path. I want to express my gratitude towards my advisor, M.Sc. Tero Sillanpää for his continuous support, valuable suggestions and useful corrections in the scientific writing. I am grateful towards my supervisor, Professor Kari Halonen for introducing me to the attributes of the analog design techniques. I will also like to thank D.Sc. Lasse Aaltonen, Jouni Erkillä and other members from the ASIC design team at Murata for providing me with useful assistance whenever it was needed.
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Finally, I am grateful for the love and support of my husband through out my studies and career decisions. I am also thankful to my parents for always motivating me and arranging the finances at the right time through out my education. I would also like to thank my daughter who bring content, peace and happiness in my life.

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Reeja Iqbal

Contents

Symbols and abbreviations

Symbols

Φ	Phase
ω	Angular frequency
r	small signal resistance
σ	variance
μ	micro
μ_n	Electron mobility
μ_p	Hole mobility
p	Pico
Ω	Ohm
A	Ampere
A_{DC}	DC Gain
A_{GND}	Analog Ground
C	Capacitance
C_L	Load Capacitor
C_{ox}	Oxide capacitance
dB	decibels
F	Farad
F_S	Sampling Frequency
$Fnom$	Operating Frequency
G_m	Trans-Conductance
H	Transfer Function
Hz	Hertz
I	current
I_{out}	Output Current
I_{ref}	Reference current
k	Kilo
L	Inductor
L	Transistor length
M	Mega
M_N	n-channel MOSFET
M_P	p-channel MOSFET
m	milli
n	nano
Q	Quality factor
R	Resistance
R_{on}	On resistance

s	second or Laplace variable
T	Temperature
V	Voltage
V_{DD}	Supply Voltage
V_{DS}	Drain Source voltage
V_{GS}	Gate Source voltage
V_{in}	Input Voltage
V_{out}	Output Voltage
V_{SS}	Ground Voltage
V_T	Threshold voltage
V^3	Phase 3 Voltage
V^4	Phase 4 Voltage
z	z-domain variable

Abbreviations

AC	Alternating Current
ADAS	Advance Driver Assist System
ASIC	Application Specific Integrated Circuit
BCD	Bipolar CMOS DMOS
BW	Band-width
CMOS	Complementary Metal Oxide Semiconductor
DC	Direct Current
dps	degrees per second
ESC	Electronic Stability Control
FF	Fast Fast
FS	Fast Slow
GBW	Gain Bandwidth
GF	Global Foundaries
KCL	Kirchoff's Current Law
KVL	Kirchoff's voltage Law
MC	Monte-Carlo
MOS	Metal Oxide Semiconductor
NMOS	N-channel Metal Oxide Semiconductor
OTA	Operational Transconductance Amplifier
PMOS	P-channel Metal Oxide Semiconductor
PS	Phase Shift
PSRR	Power Supply Rejection Ratio
PVT	Process Voltage Temperature
RC	Resistive Capacitive
RLC	Resistor Inductor Capacitor
SAE	Society of Automative Engineers
SF	Slow Fast
SS	Slow Slow
SC	Switched Capacitor
THD	Total Harmonic Distortion
VDD	Supply Voltage
VSS	Ground Voltage

1 Introduction

1.1 Background

Self-driving cars have become a popular topic of research due to their enhanced safety, reduced carbon footprint, better efficiency, and reliability on the automotive industry. According to the Society of Automotive Engineers (SAE), there are six levels of vehicle autonomy ranging from zero for completely manual vehicles to five for fully autonomous driver-less vehicles [1]. As autonomous driving assumes more importance in the automobile industry, there have been significant improvements especially in the field of safety owing to Advance Driver Assist Systems (ADAS). This system is on level two of driver autonomy and requires the driver to remain alert and resume control whenever needed. The ADAS is an important step towards the realization of autonomous driving as was Electronic Stability Control (ESC) towards ADAS [2].

1.2 Motivation

Gyroscope is a device which measures and maintains the stable position of the car. Essential parts of ESC are the gyroscope and accelerometer. Accelerometer along-with gyroscope prevent the straying of the vehicle from its intended path by applying or removing the brakes to and from its wheels [3][4][5] .There are three principal axes for the rotation of an object, known as pitch, roll, and yaw axes. The pitch is the rotation of an object around transverse axis, for a car, it is the rotation from the front wheel towards the back wheel. The roll is the rotation of an object around the longitudinal axis; in other words from the left door of a vehicle towards the right. The yaw is the movement around the vertical axis; this kind of movement is likely to occur when a car is turning rapidly on a curve or slippery surface, especially on ice. The yaw movement of a vehicle is also called car skidding. The yaw rate is the measurement of an angular velocity of a vehicle around its axis of rotation; it is measured in degrees per seconds (dps). The ADAS requires the accurate yaw rate to predict the position of a car from initial speed. When the ADAS has predicted the position of the car accurately, it is able to maintain the stability of a car by keeping it on the track [6] .
Physically, the accelerometer and gyroscope are used to determine and maintain the position of a vehicle. There are two types of gyroscopes that are being used in automotive industry. In the first type of gyroscope one or two axes in the loop and it is part of the ESC system, the second type has three axes and is part of the ADAS. For a three-axes stability control of a vehicle, generally three paths are required to measure the rotation around x(roll), y(pitch), and z(yaw) axes [7].A channel is a term used to describe a path to control the rotation in this work. The exact number of paths or channels to be implemented depends on the sensing element. In this work four channels are implemented because it is easier to derive multiplexing clock for four channels instead of three. The part of application specific integrated circuit (ASIC) which measures and maintains the rotation of the car is gyroscope, there

are two controlling loops in a gyroscope, named as a primary and a secondary loop. Apart from other signals processing sections, a low pass filter is an important part of the secondary loop. Conventionally, one low pass filter is used to process one channel. This approach is simple to design, and the implementation is straightforward. However, this approach is expensive as it occupies the large silicon area on the chip. A potential solution to reduce area is to perform channel multiplexing with a single low pass filter block. Multiplexing is a method that is used to combine multiple signal paths in a single path and process it through a common resource. Multiplexing is difficult to obtain using continuous time circuitry and therefore a discrete time circuitry named as switched capacitor circuitry is implemented in this work. Noise folding is an unavoidable trait of sampling circuits. Therefore, due to sampling, the noise in the circuit increases because of noise folding to the band of interest [8]. Moreover, multiplexing requires a higher bandwidth operational amplifier, which means that the current consumption of the circuit will also increase [9].

1.3 Purpose

The aim of this thesis is to implement the electrical design of switched capacitor low pass filter with channel multiplexing for the ASIC by using the provided specifications and the equivalent continuous-time filter; while targeting reduced silicon area, smaller current consumption, and lower noise levels in the circuit. The application of this work has critical safety requirements, therefore, several other parameters, for example, functionality of the circuit at various operating frequencies, process, voltage, and temperature variation corners, requires verification according to the given specifications. This study also determines the current and noise level in the circuit while proceeding the design with the intent that all other parameters remain within predefined specifications. All the specifications together with current consumption and noise level determine the feasibility of the practical implementation of the circuit.

1.4 Scope

The scope of this work is limited to the electrical design of the filter. The layout design is out of scope from this thesis. The current consumption and noise levels are defined as targets for this work, but it is not the requirement.

1.5 Structure

The contents of the thesis are organized as follows. Chapter 2 gives the literature review and background knowledge of the design. Chapter 3 provides the already optimized specification for this design as well as the detailed steps followed for the design and development of the circuit following those specifications. Chapter 4 presents the required simulation results. Chapter 5 summarizes the work, reveals conclusions, and describes future aspects.

2 Low-pass Filters

This chapter describes different types of low pass filters and their feasibility for the application in ESC gyroscope loop. Section 2.1 describes the traditional passive low pass filters as well as active RC filters, including topologies of the Sallen-Key and transconductance-capacitor filters. Section 2.2 describes how continuous-time filters are sampled using switches and capacitors, and different topologies for the discrete-time implementation of low-pass filters. Section 2.3 provides an overall comparison of the discussed topologies and selects one to be implemented for the final design.

2.1 Continuous-Time Low Pass Filters

Low-pass filter is a device which attenuates signals higher than a certain frequency, known as the cutoff frequency. In the former times, low pass filters were implemented using resistors, capacitors and inductors. These kind of filters having no active component, e.g., transistor or operational amplifier are termed as passive filters [10] [11]. Due to the absence of these active components, the signal amplitude at the output of a passive filter is always less than the input[12] . The order of a filter is defined by the amount of attenuation it provides per decade after the cutoff frequency, i.e., gain reduction for every ten- fold increase in the signal frequency. The order of the filter is one, if the attenuation after cutoff frequency is 20dB per decade, and the order is two, if the attenuation is 40dB per decade and so on.
An inductor is a reactive component and it shows low reactance to low frequency signals, conversely, a capacitor shows high reactance to high frequency signals. Therefore, the first order passive low pass filters can be implemented as shown in Figure 1.

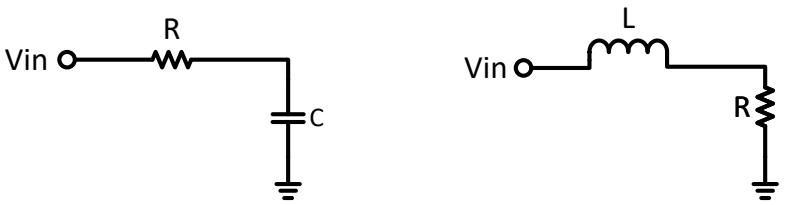

Figure 1: Passive Low Pass Filters

This passive implementation of low-pass filter especially with an inductor, has several drawbacks. In an integrated circuit, there are two main limitations for the use of an inductor, i.e., they have low quality factor because of parasitic resistance and capacitance and also the size of an inductor becomes very large for low frequency applications. Therefore, inductors are used only in radio frequency integrated circuits

and for low frequency applications they should be used only when absolutely necessary. Capacitors are preferred to be used in an integrated circuit over inductors because of the smaller size, lower cost and higher precision. It is easier to confine the electrical field in a capacitor than to control a magnetic field around an inductor coil [13]. For an integrated circuit, active filters are preferred over passive filters. Active filters are inexpensive and the response of the filter can be easily controlled by the powering part of the filter, i.e., how fast and how steep the signal moves from its pass-band to stop-band or vice versa.
There are two types of active analog filters, i.e., continuous-time and discrete-time filters. To realize a filtering transfer function in a continuous domain we need integrators, adder, and gain blocks. Based on the device used to build integrator, there are two popular types of continuous-time filter structures,i.e., $G_m - C$ filters and active-RC filters. $G_m - C$ filters are realized using transconductors while active-RC implies the use of operational amplifiers [14]. These types of filters are discussed in the following subsections.

2.1.1 Active-RC Filters

Active-RC filters has an operational amplifier(Op Amp) as its main building block, an Op Amp greatly amplifies the difference of two input signals it is receiving at its input. As a device an Op Amp shows high impedance to the signal coming at its input and low impedance at its output. To understand the working principle of these filters, one needs to understand how integration is performed with an Op Amp. Therefore, let's consider how an Op Amp works with a feedback circuit. Consider the Op Amp in both of its configurations in Figure 2. In Figure 2(a), the Op Amp is

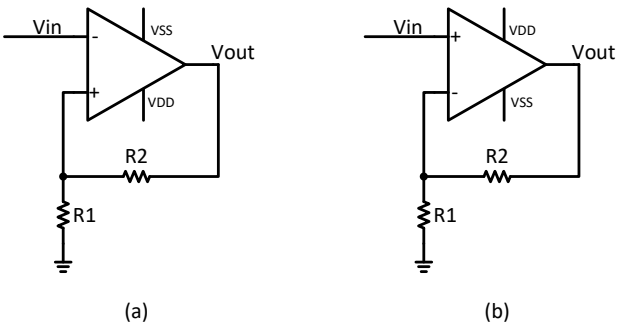

Figure 2: Op amp in positive and negative feedback configuration

connected in positive feedback configuration. If R_1 and R_2 are equal, the voltage at the positive input terminal is half of voltage at the output terminal.If input voltage is higher than the half of output voltage, the output will saturate to the negative supply rail, i.e., VSS of the Op Amp. This happens because the positive terminal tends to adjust to the change at the input by decreasing the voltage at output. As the output signal is limited by the supply voltage, the decreased voltage cannot go below the supply range. Hence output remains saturated to VSS unless V_{in} is reduced back to

VSS/2. If the voltage at input drops beyond that, the positive feedback tends to increase the output voltage and it will eventually saturate to VDD.
Next, consider the Op Amp in a negative feedback configuration as shown in Figure 2(b), here the output voltage is fed back to the negative input terminal of the Op Amp. For equal R_1 and R_2, the voltage at the negative terminal is half of the output voltage. If the input voltage at the positive terminal of the feedback is greater than the negative terminal, the negative terminal raises its voltage by increasing voltage at the output terminal till the voltage at both terminals are equal. Op Amp here is connected in the non-inverting configuration and its gain is always greater than 1 [15].

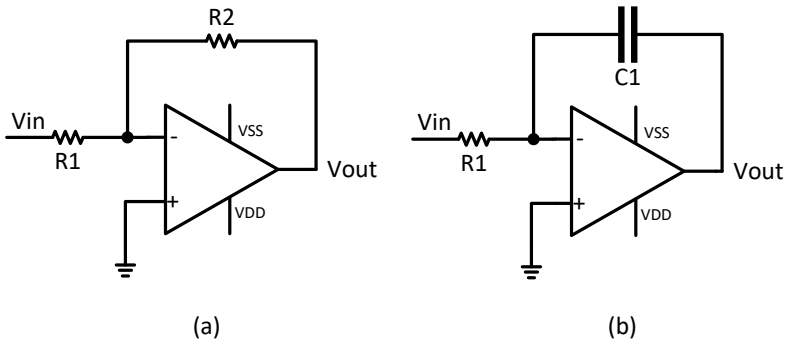

Figure 3: Inverting op amp with Gain = 1 and integrator

In the inverting configuration shown in Figure 3(a), the voltage at the negative terminal tends to be equal to ground voltage, hence, if the input voltage is rising, the output voltage decreases and thus the output voltage is 180 degrees out phase with the input voltage. The amplification of this circuit is given by the ratio of the feedback resistor to the input resistor.
In an integrator, the feedback resistor in the inverting configuration of an Op Amp is replaced by a capacitor. This is shown in Figure 3(b). To understand the integrator operation, consider a square wave being fed at the input terminal. Ideally, no current flows into the input terminal of the Op Amp. Therefore when a positive input voltage is applied to the resistor, the current flows through the capacitor and it starts charging by storing charge on its plates. This flow of current produces a negative voltage ramp at the integrator output. If the voltage at the input is negative, the current flows in the reverse direction and the capacitor gets discharged giving a negative ramp at the negative input terminal of the operational amplifier and a positive voltage ramp at the output node. Therefore, for a square wave input, output of the integrator is a triangular wave. For a triangular wave input, the output is a sine wave. For a sine wave input, the output is a cosine or 90 degrees shifted sine wave. Hence, an integrator is a first order low pass filter. For practical implementations, a resistor is added in parallel to the feedback capacitor, because at DC and low frequencies, the capacitor acts an open circuit and reduces the amount of feedback. Adding a resistor in parallel compensates for the reduced feedback. Let's consider some low pass filters implemented using operational amplifiers.

Sallen-Key low pass filter: Sallen-Key filter is a popular implementation for attaining high-Q in continuous-time filters. This topology implies positive feedback amplifier which is controlled around the cut-off frequency, if not limited by the power supply or component tolerances, very high Q values can be achieved using these filters [16]. Figure 4 shows a low-pass implementation of the Sallen-key filter. It is a

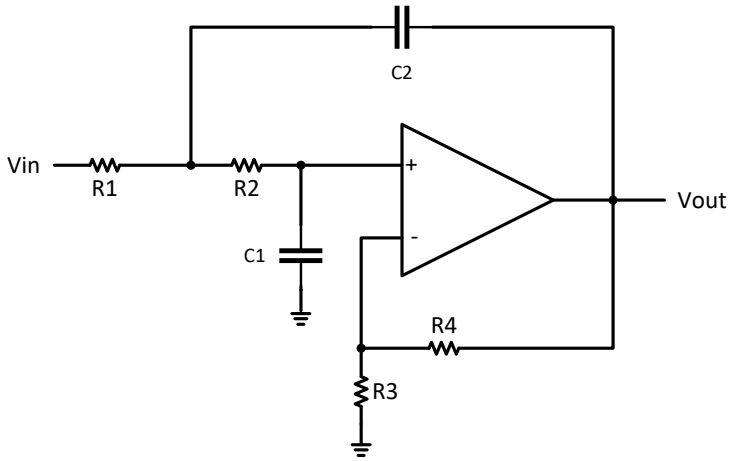

Figure 4: Sallen-Key low-pass filter

single amplifier implementation, near DC and lower frequencies, capacitors provide high impedance and the input voltage appears at the output as an amplified signal, depending on the value of gain resistors R_3 and R_4. At higher frequencies, capacitors impedance decrease as we move closer to the cutoff frequency, the amount of positive feedback increases and negative feedback tends to balance voltage level at the Op Amp input by increasing voltage at the output node. Hence, we get a peaking behaviour of the output voltage around the corner frequency. The higher is this peak, the better is the Q-value of the filter. The transfer function for this low pass filter is given by [16]:

$$H(s) = \frac{K}{s^2(R_1R_2C_1C_2) + s(R_1C_1 + R_2C_1 + R_1C_2(1-K)) + 1} \tag{1}$$

Comparing it with a standard second order frequency domain equation, i.e.,

$$H(s) = \frac{K}{\frac{s^2}{(\omega_p)^2} + \frac{1}{\omega_p Q}s + 1} \tag{2}$$

gives

$$\omega_p = \frac{1}{\sqrt{R_1R_2C_1C_2}} \tag{3}$$

$$Q = \frac{\sqrt{R_1R_2C_1C_2}}{R_1C_1 + R_2C_1 + R_1C_2(1-K)} \tag{4}$$

and

$$K = 1 + \frac{R_3}{R_4} \tag{5}$$

In this topology, the amplifier is not grounded, therefore the common mode voltage changes with the changes in the output voltage and the differential implementation of this filter is challenging.

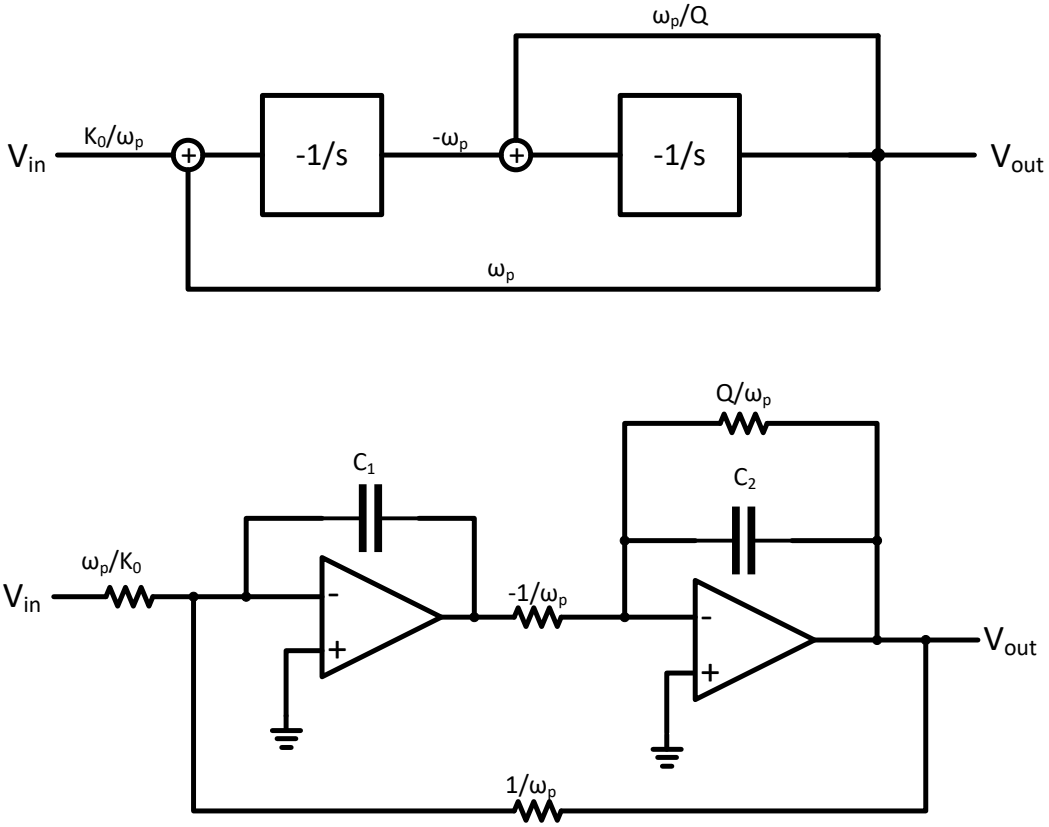

Figure 5: Tow-Thomas Biquad

Tow-Thomas Biquad: Tow-thomas biquad is a topology which implements transfer function using resistors, capacitors and Op Amps [17]. The Op Amp functions as a gain block and the co-efficients of the transfer functions are provided through the resistors and capacitors. To understand this topology, consider the transfer function:

$$\frac{V_{out}}{V_{in}} = \frac{s^2K_2 + sK_1 + K_0}{s^2J_2 + sJ_1 + J_0} \tag{6}$$

For a low-pass filter $K_2 = K_1 = 0$, rearranging the above equation for low-pass filter gives:

$$V_{out} = -\frac{1}{s}\left(\frac{\omega_p}{Q} - \omega_p\left(-\frac{1}{s}\left(\frac{K_0}{\omega_p}V_{in} + \omega_p V_{out}\right)\right)\right) \tag{7}$$

This equation and its equivalent circuit is represented in a signal flow graph as shown in Figure 5.

2.1.2 G_m-C Filters

Apart from an active-RC, the above mentioned filter topologies can also be realized using G_m-C technique. This topology applies transconductors and capacitors to perform filtering [14]. A transconductor is a circuit which takes in voltage and gives output in the form of a current which is linearly related to the input voltage. Ideally, the input and output impedance of a transconductor block is infinite. A transconductor block should have a well defined transconductance(g_m) value [18]. Consider a single ended Gm-C integrator in Figure 6.

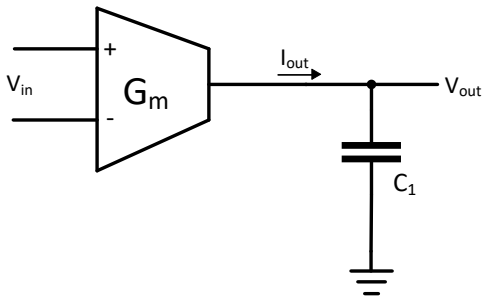

Figure 6: G_m-C Filter

Here, the output voltage is given by:

$$V_{out} = -\frac{I_{out}}{sC_L} = -\frac{G_m}{sC_L}V_{in} \tag{8}$$

Hence, the output is the integration of input voltage scaled by the transconductance of the transconductor. Unlike operational amplifier, there is no feedback involved in G_m-C technique for filter implementation. As mentioned above, the Sallen-key low-pass filter involves feedback to obtain high-Q values around corner frequencies. Therefore, this implementation is not feasible to be used with Sallen-key filter. General transfer function equation for a G_m-C based second order filter is given by:

$$\frac{V_{out}(s)}{V_{in}(s)} = \frac{s^2\frac{C_X}{C_X+C_B} + s\frac{G_{m5}}{C_X+C_B} + \frac{G_{m2}G_{m4}}{C_A(C_X+C_B)}}{s^2 + s\frac{G_{m3}}{C_X+C_B} + \frac{G_{m1}G_{m2}}{C_A(C_X+C_B)}} \tag{9}$$

For a low pass filter, C_X and G_{m5} becomes zero, and the transfer function becomes:

$$\frac{V_{out}(s)}{V_{in}(s)} = \frac{\frac{G_{m2}G_{m4}}{C_AC_B}}{s^2 + s\frac{G_{m3}}{C_B} + \frac{G_{m1}G_{m2}}{C_AC_B}} \tag{10}$$

A single-ended implementation of this transfer function is represented in Figure 7.

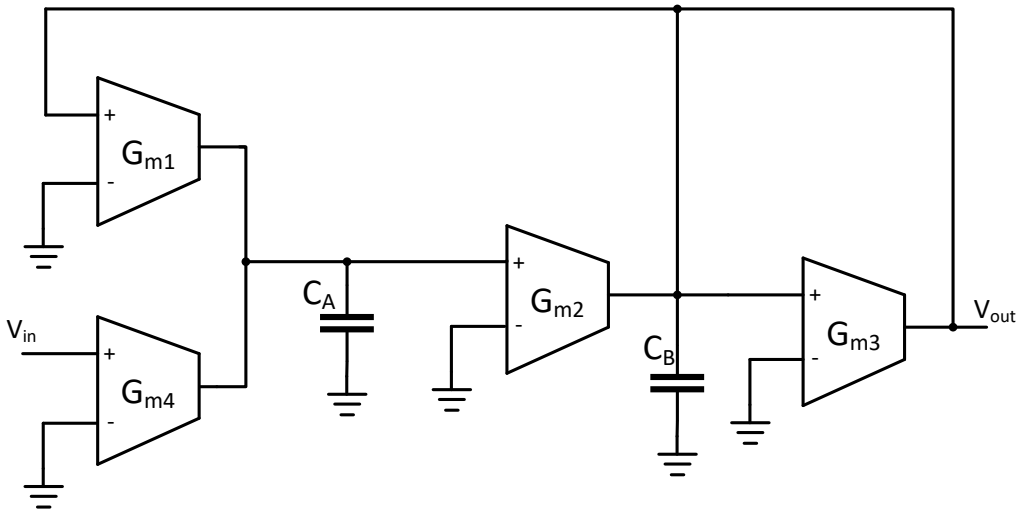

Figure 7: Second Order transfer function implementation using G_m-C topology

G_m-C based filters are generally faster but less linear as compared to their operational amplifiers counterparts. Contrarily, the filter implementation using Op Amp requires high gain-bandwidth which makes these filters slower, i.e., slew rate of these filters is high. The feedback capacitor in the active integrator gives better linearity for this circuit, whereas, the G_m-C based filters are less linear.
In order to fully-integrate these circuits on a chip using MOS technology, a high quality capacitor can be fabricated but a capacitor greater than 5pF is seldom used, in order to obtain a cutoff frequency of 23.6kHz, the resistor required for the RC-integrator would be 1.3MΩ, which would occupy a large portion of an integrated circuit. Also, the behaviour of these resistors is nonlinear in general. Therefore, a resistor not only occupies a large amount of area but it is also not very accurate. Although the capacitors are fabricated using different fabrication steps as compared to resistors, they also have the same order of individual error.
The capacitors and resistors variations are uncorrelated, the time constants achieved by them will also vary over temperature and voltage variations. Therefore, high accuracy and stability performance are difficult to achieve from active RC filters. Furthermore, if several channels needs to be filtered using these, every channel would require its own filter as it is difficult to imagine how a multiplexed signal in time domain can be filtered using single structure. Therefore, to save area and achieve multiplexing, switched capacitor filters need to be considered for the desired application. As described in the previous chapter, using switched capacitor circuit would require higher bandwidth Op Amps, leading to additional current consumption and higher noise floor due to noise aliasing resulting from the sampling nature of the circuit [13][19][20].

2.2 Discrete-time Low-pass Filters

Analog discrete-time filters implies switched-capacitors, these capacitors can be used in place of resistors in a circuit[21][22][23]. These switched capacitors provides path to the signal by sampling it at different intervals and thus approximating the behaviour of an equivalent continuous-time resistor. To understand how a switched-capacitor behaves like a resistor, consider a capacitor and two switches shown in Figure 8. The switches are switched from non-overlapping clocks and thus these two switches

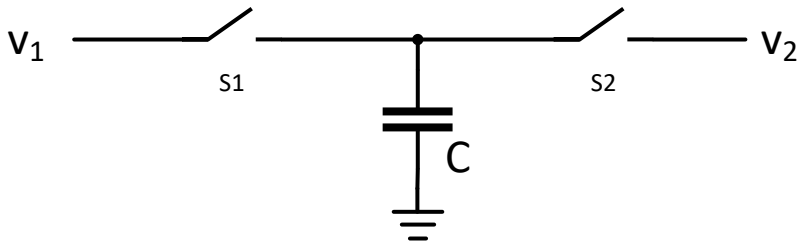

Figure 8: Switched Capacitor Circuit 1

are not closed at the same time. When transistor S1 is turned on, the capacitor is charged to the voltage v_1 in steady state, when S1 is turned off and S2 is also turned off during the non-overlapping time, the charge on the capacitor corresponds to the voltage v_1. Now, when switch S2 is turned on, the voltage on the capacitor is now v_2, due to this different voltage the charge on the capacitor changes, if v_1 is greater than v_2, the current defined as rate of change of charge is given by[24]:

$$I = \frac{C(v_1 - v_2)}{T} \tag{11}$$

where T is the time period during which S1 and S2 are turned on once. The value C/T is a constant in this equation and if we replace it with an equivalent of 1/R, we have implemented an equivalent circuit of a resistor.
The switched-capacitor equivalent resistor can also be implemented using the circuit shown in Figure 9. Here during phase 1, the capacitor is charged to the voltage v_1 - v_2, and during phase 2 the capacitor is discharged to 0. Hence, the rate of change of charge during one time period is equivalent to previous case and the circuit is behaving like a resistor of value C/T. Hence, any resistor in an integrated circuit can be replaced with a switched capacitor, resulting in more accurate time constants or equivalent resistance values as the accuracy now depends on the ratios of the capacitor and not on an individual capacitor value. Consider the integrator structure of Figure 3b, if the resistor R_1 is replaced by a switched capacitor of Figure 8, in the resulting circuit, the resulting discrete-time transfer-function is given by:

$$V_{out}(z) = -\frac{\frac{C}{C_1}}{z-1} V_{in}(z)$$

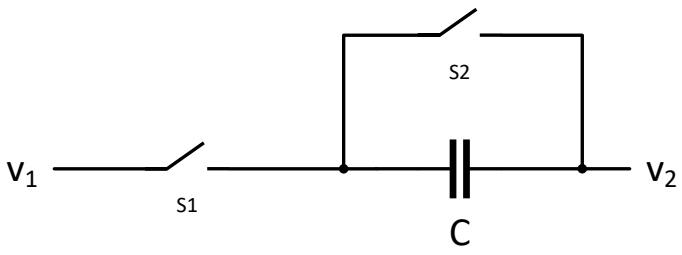

Figure 9: Switched Capacitor Circuit 2

Whereas, the s-domain transfer function of the active low-pass filter is given by:

$$H(s) = -\frac{\frac{1}{R_1 C_1}}{s}$$

For the low-pass filter implementation using switched capacitors, these topologies can be considered for implementation. First is switched capacitor bi-quad and the second topology is called switched-capacitor ladder filter.

2.2.1 Switched Capacitor Bi-quad [25]

Consider the switched capacitor shown in Figure 8, depending on the clock phase, the top plate of the capacitor is connected to the drain or source terminal of either switch S1 and S2, these terminals of the transistor have some capacitance to the substrate and this capacitance is not fixed and hence it disturbs the accuracy of the capacitance value of capacitor C. This effect is significant when the capacitor is connected to high-impedance nodes and high potential difference increases the stray capacitance values. Therefore, the capacitor is discharged to ground after each sampling phase and the effect of stray capacitance is prevented. This implementation is shown in Figure 10. Here, the numbers 1 and 2 represents the clock phase during which the transistors are switched.
Switched capacitor biquad implementation is the discrete-time implementation of the circuit shown in Figure 5. All the resistances in this circuit can be replaced by switched capacitor equivalent and the switching scheme depends on the sign of the resistor value in transfer function or signal flow graph. The switched capacitor implementation of this circuit is shown in Figure 11. The value of the integrating capacitors C_1 and C_2 remains the same, rest of the capacitance values are given as follows:

$$C_A = \frac{K_0 T}{\omega_o} \tag{12}$$

$$C_B = \omega_p T \tag{13}$$

$$C_C = \omega_p T \tag{14}$$

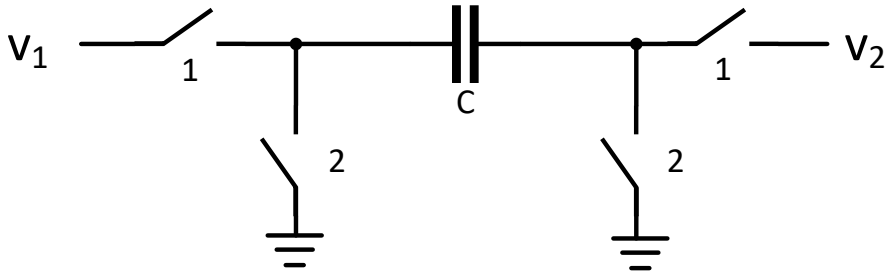

Figure 10: Switched Capacitor topology preventing capacitor value from stray capacitances

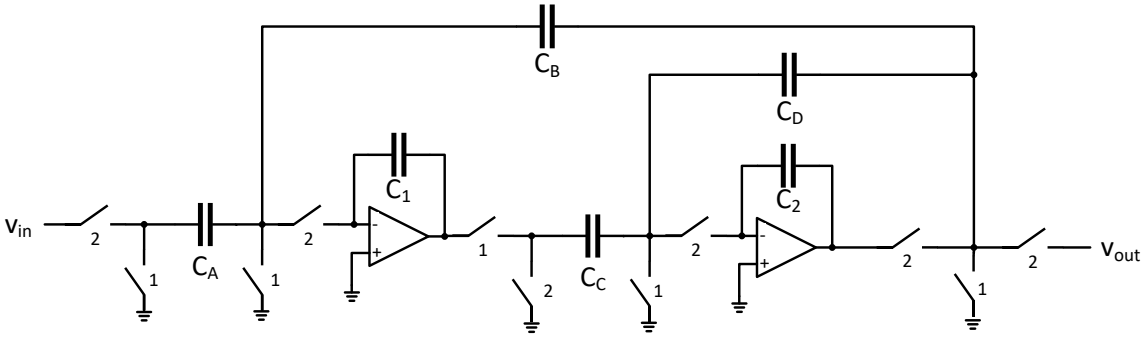

Figure 11: Implementation of a second order transfer function using switched capacitors

$$C_D = \frac{\omega_p T}{Q} \tag{15}$$

There is another possible implementation of a bi-quad filter, referring to equation 7, the relation can also be expressed as:

$$V_{out} = -\frac{1}{s}(-\omega_p)\left(-\frac{1}{s}\left(\frac{K_0}{\omega_p}V_{in} + \omega_p\left(\frac{s}{Q} + \omega_p\right)V_{out}\right)\right) \tag{16}$$

The signal flow graph, equivalent RC circuit and the switched capacitor implementation for this equation is shown in Figure 12 - Figure 14. The difference in the two biquads is the connection of C_D, which is now not a switched capacitor rather it is an integrated capacitor with its value related to Q value of the circuit, given as

$$C_D = \frac{1}{Q} \tag{17}$$

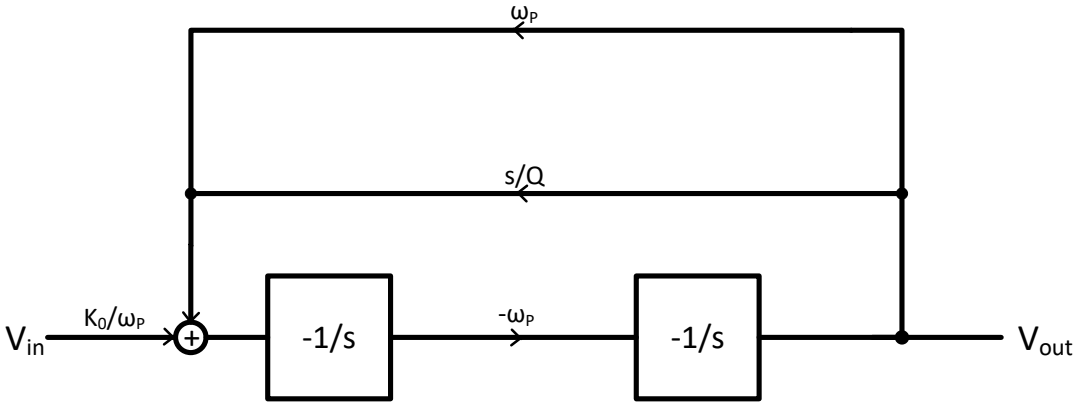

Figure 12: Signal Flow Graph

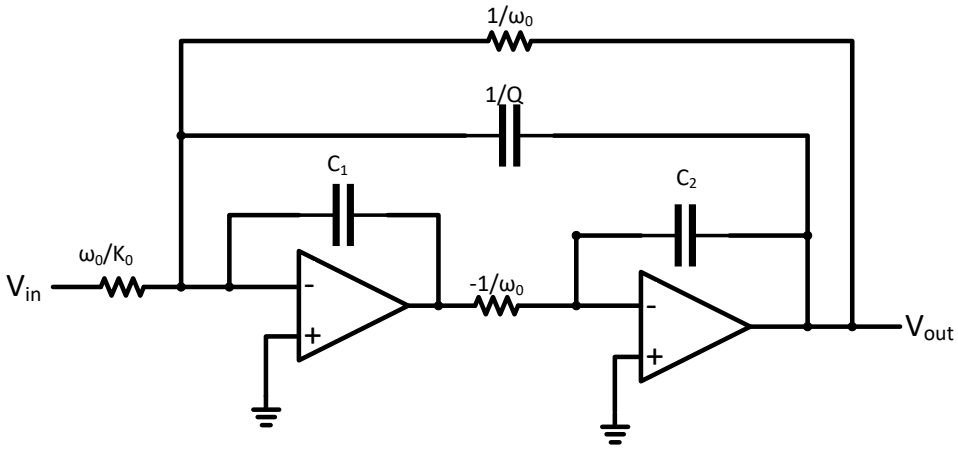

Figure 13: RC circuit for the SFG in Figure 12

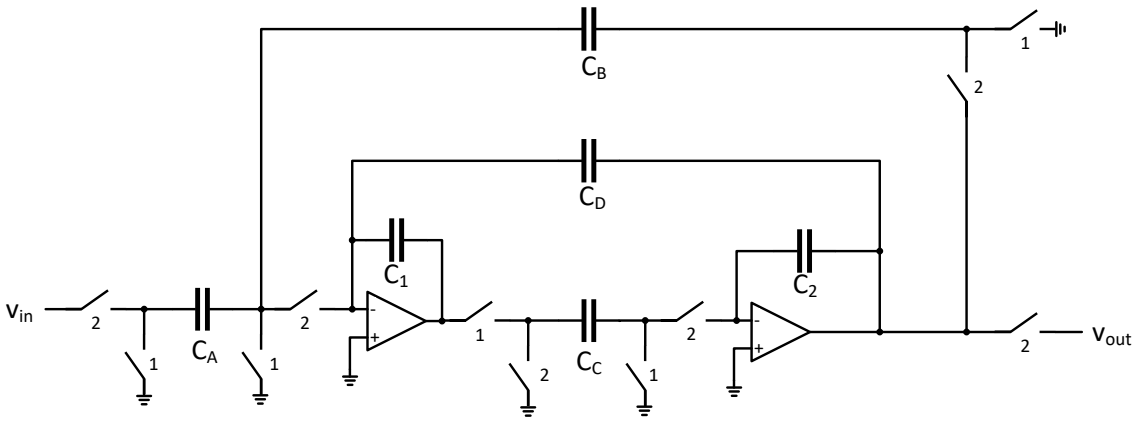

Figure 14: Switched capacitor bi-quad implementation of the SFG in Figure 12 and RC circuit in Figure 13

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To minimize area, choice of smallest capacitance defines the minimum sampling frequency for the circuit, given by C/ω_p. Therefore, the low-Q implementation of the circuit is possible using the circuit shown in Figure 11. For example, comparing equation 14 and 15, Q is defined as the ratio of capacitors C_C/C_D. In order to get Q=2 from this topology capacitor C_C and C_B are needed to be increased by a factor of 2 for the same sampling frequency. Therefore, for high-Q implementation, the circuit in Figure 14 is used in which Q value is not dependent on other capacitance values or sampling frequency. If these two circuits are compared, there are two channel specific capacitors for the low-Q implementation in the first circuit. But for high-Q implementation the number of channel specific capacitors is three. Therefore, channel multiplexing performed using this topology would require more area for high-Q requirements.

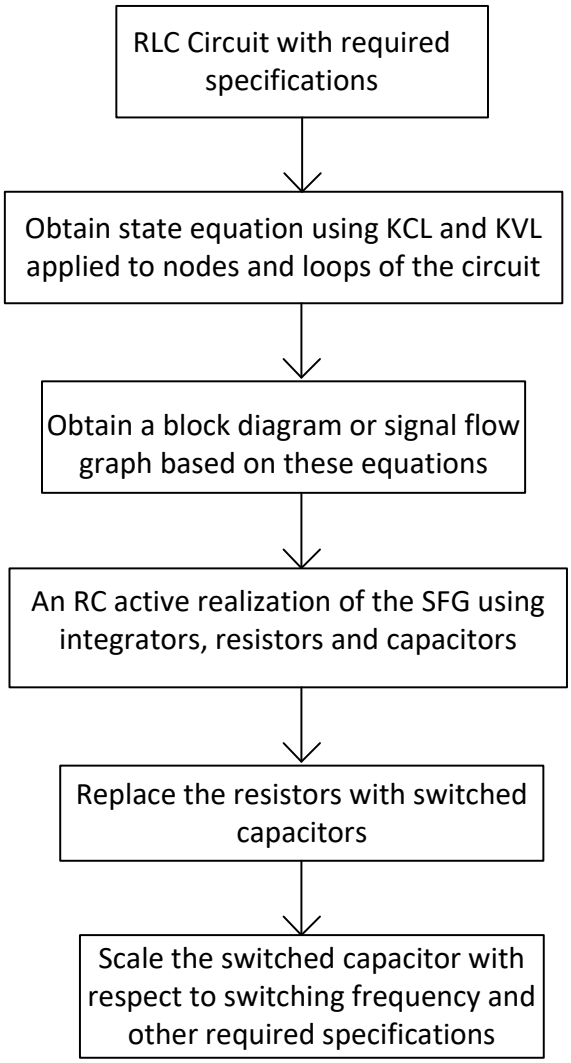

Figure 15: Design Flow for SC Ladder Circuit

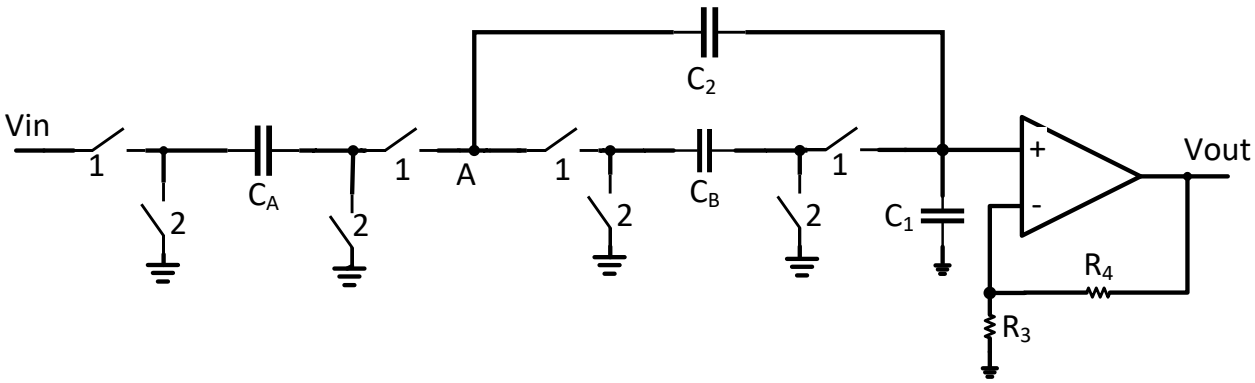

Figure 16: Switched capacitor Sallen Key Implementation of the circuit shown in Figure4

2.2.2 Switched Capacitor Ladder Filters [25]

Switched capacitor ladder filters is a widely used technology to design filters. It's concept is based on a two port device, if the input and output impedance of this device is perfectly matched at operating frequency, the device would have maximum gain. Now, if any of the elements within this port changes and the operation was already at a maximum nominal operation, the output of the circuit is going to decrease as it cannot increase from the nominal value. Hence, the sensitivity of this circuit is ideally zero when the gain is maximum. On the other hand for high-Q values switched capacitor biquads have high sensitivity and thus low stability and slight variation in any of the component values can cause the z-domain poles to move outside the unit circle and causes instability.
For sensitive applications and ease of fabrication, ladder filters are preferred over cascaded filters. This technique implies derivation of signal flow graph based on the current-voltage relationship in an equivalent passive filter. The switched capacitor filter is then derived from the signal flow graph. The design flow for switched capacitor ladder circuits is shown in Figure 15. The number of Op Amps required for this implementation depends on the order of the filter. Also, the capacitance nodes with high stray capacitance are always connected to low-impedance source which are the input and output nodes or to the virtual ground which is the input terminal of the Op Amp. Because of this stray-insensitive behaviour, this topology is used in many practical applications containing switched capacitor circuits.

2.3 Comparison

All of the topologies considered in this chapter are summarized in Table 1. Here, in this table the ✓ represent positive factor of the given topology while the × represent negative factor. Although the Sallen-Key low pass filter is implemented for continuous-time application, a switched capacitor implementation can also be acquired by replacing resistors with switched capacitors as shown in Figure 16. This implementation is sensitive to stray capacitance affect as node A is not connected to

Table 1: Comparison of all topologies for various parameters

Topology	Multiplexing	Current Consumption	Area for multiple channel	Noise
Active RC	×	✓	×	✓
Sallen-Key	×	✓	×	✓
Tow-Thomas biquad	×	✓	×	✓
G_m**-C**	×	✓	×	✓
SC biquad	✓	×	✓	×
SC ladder	✓	×	✓	×

ground neither to low impedance node during switching, this affect the accuracy of the capacitance C_2 value and hence the overall accuracy of the circuit. Hence, this topology is not considered further.
As we need to save area, channel multiplexing is implemented . The channel multiplexing is performed by placing integration capacitors equivalent to the number of channels to be multiplexed and switching them along-with the channel as shown in Figure 17. The non-overlapping phase clocks of the non-integration switched capacitors remains same. In comparison of switched capacitor biquad and ladder topology for low-pass filter, the latter one has fewer number of integrated or channel specific capacitors and is more stable structure for practical implementation. Therefore, the next chapter describes the design of switched capacitor ladder low-pass filter for the gyroscope secondary loop implementation.

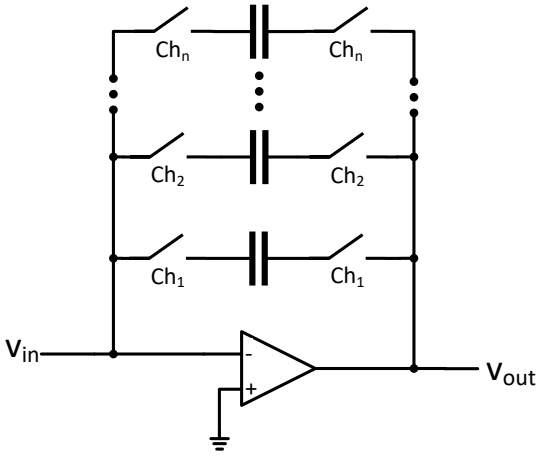

Figure 17: Channel Multiplexing

3 Modelling and Design

This chapter describes the modelling and design of switched capacitor ladder low-pass filter for the required specifications. Section 3.1 describes the requirement specifications and the target for the design. In Section 3.2, the SC low-pass filter is designed from the RLC equivalent circuit. Section 3.3 presents the multiplexed design with respect to clock cycles and the number of channels. In section 3.4, the switch and capacitor design used for the filter is listed followed by the Op Amp design in section 3.5.

3.1 Design Specifications and requirements

As described in the introduction chapter, the low-pass filter design that is to be designed for this work should be precise enough as it is intended to be used in safety critical automotive related applications. It is a requirement to multiplex and simulate second order switched-capacitor filter through an equivalent RLC while targeting lower current consumption of 1mA. The schematic of RLC prototype that needs to be modelled is shown in Figure 18. The specifications required from this RLC prototype and from its switched-capacitor equivalent as a whole is given in Table 2. The targets that are needed to be studied and achieved as close as possible are stated in Table 3.

As described, the clock sampling frequency per channel is 1.51 MHz. For multiplexing of four channels, each channel should sample once during one sampling period. And as a whole four samples would be taken per sampling period. The sampling period of each channel and their phases would be described later while implementing multiplexing to a single channel design.

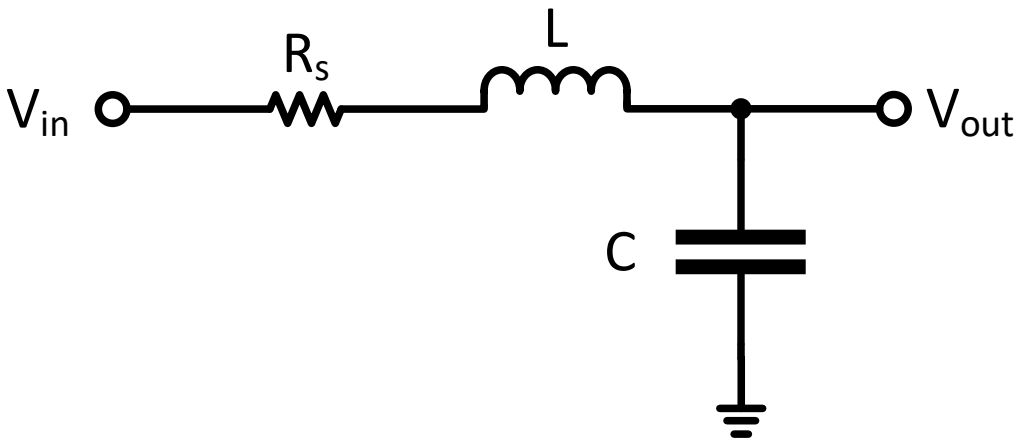

Figure 18: RLC prototype

Table 2: Design requirements

Parameter	Requirement
Pole frequency f_p	23.01kHz
Channels to be filtered	4
Q-value	5
Channel data rate	64×Fnom ± 10 % (Fnom = 23.6 kHz)
Switch on time	Half period of 512× $Fnom - nonoverlappingtime$
Supply Voltage V_{DD}	2.5 ± 0.05 V
Ground V_{SS}	$0V$
Analog Ground A_{GND}	$1.25 \pm 0.025V$
Temperature range:	$-40°C$ ... $145°C$
S-domain transfer function	Second order low pass filter $\mathrm{V}_{out}(s) = A_{dc}\frac{\omega_p^2}{s^2+\frac{\omega_p}{Q}s+\omega_p^2}V_{in}(s), \omega_p = 2\pi f_p$
Differential DC gain A_{dc}	$2(approx.6dB)$
Differential DC output offset:	
room temperature	$\pm\ 25mV$
temperature drift	$\pm\ 4.5mV$
Output Signal Range	$0.375V - 2.125V$
PSRR DC-100kHz	25 dB min
Harmonic distortion at Fnom	0.3 % at max output range
Channel Isolation	>100 dB
Transistor technology	GF 55nm BCD

Table 3: Design targets

Parameter	Target
Phase shift (PS) at f_p :	
Typical:	-86.9 degrees
Over process variation:	± 6 degrees
Over supply drift:	± 0.6 degrees
Input referred noise in signal band	500 nV/$\sqrt{Hz}$
Current consumption	1.0mA

3.2 Design

According to the required pole frequency and Q-Value, the s-domain second-order transfer function[26] can be written as:

$$H(s) = \frac{V_{out}}{V_{in}} = 2\frac{2.09 \times 10^{10}}{s^2 + 28915.2187s + 2.09 \times 10^{10}} \tag{18}$$

Comparing it with standard second-order RLC low-pass filter transfer function for R = 1:

$$H(s) = A_{dc}\frac{\frac{1}{LC}}{s^2 + \frac{R_s}{L}s + \frac{1}{LC}} \tag{19}$$

gives L = 34.58 μH and C = 1.38 μF. Writing the current and voltage equations for the voltage and current through the RLC circuit shown in Figure 18, gives:

$$I_S = -\frac{1}{sL}(V_{out} + I_s R_s - V_{in}) \tag{20}$$

$$-V_{out} = -\frac{1}{sC}(I_s) \tag{21}$$

where I_s is the current through the circuit. The signal flow graphs for these equations is drawn in Figure 19. The single-ended RC implementation for this signal flow graph is shown in Figure 20. All the resistors when replaced by switched-capacitors gives the implementation as shown in Figure 21.
Here, all the resistors with negative values have opposite clock phases in the equivalent switched-capacitors. As the sampling frequency(f_s) is 64× Fnom, the capacitor value with unity gain is R/f_s which is equal to 0.662 μF. Hence, all the unit capacitors (C_{RS}, C_{u-in}, C_{u-c} and C_u) are equal to 0.662 μF. The circuits samples the incoming signal at phase3. The output of the second integrator during phase4 of the clock

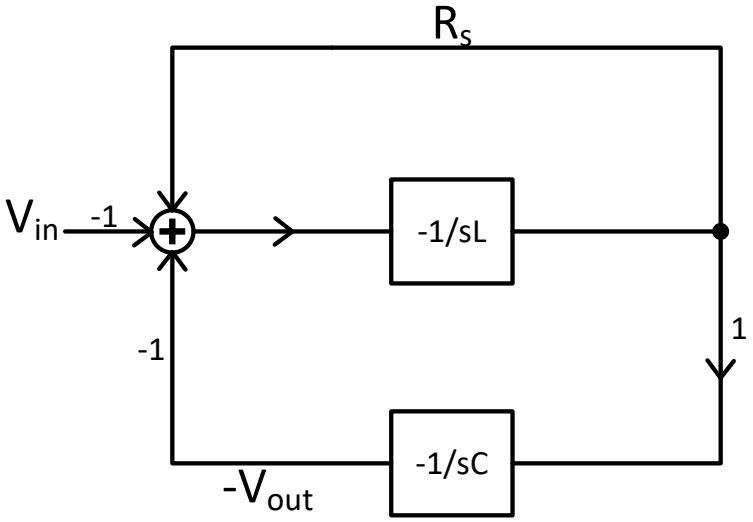

Figure 19: Signal Flow Graph

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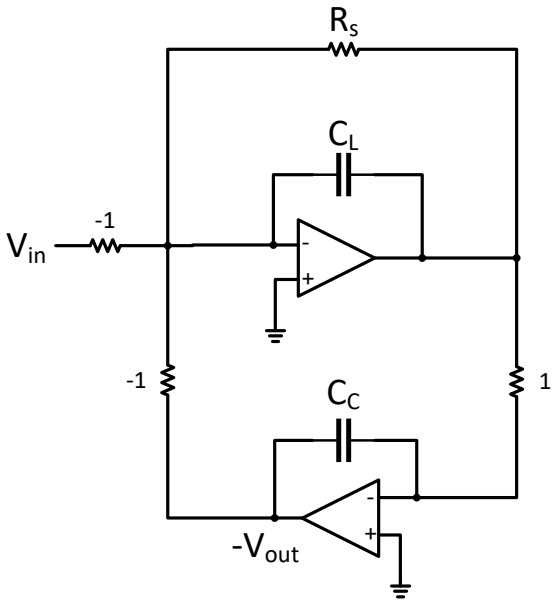

Figure 20: RC Implementation

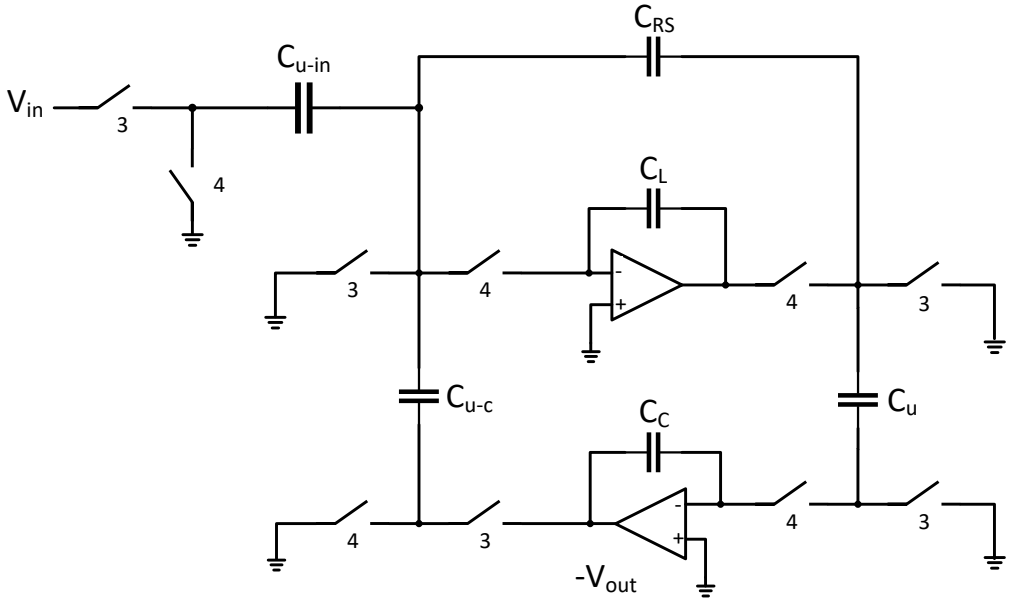

Figure 21: Switched-Capacitor Circuit.

cycle is the output of the filter. If V_1 is the voltage node at the output of the first Op Amp and V_1^4 is its output during phase clock 4. The equivalent circuit during phase 3 and phase 4 is shown in Figure 22. The z-domain transfer function for the circuit in Figure 21 can be computed using the following equations [27].

$$V_1^4 = z^{1/2} V_1^3 \tag{22}$$

$$V_{out}^4 = z^{1/2} V_{out}^3 \tag{23}$$

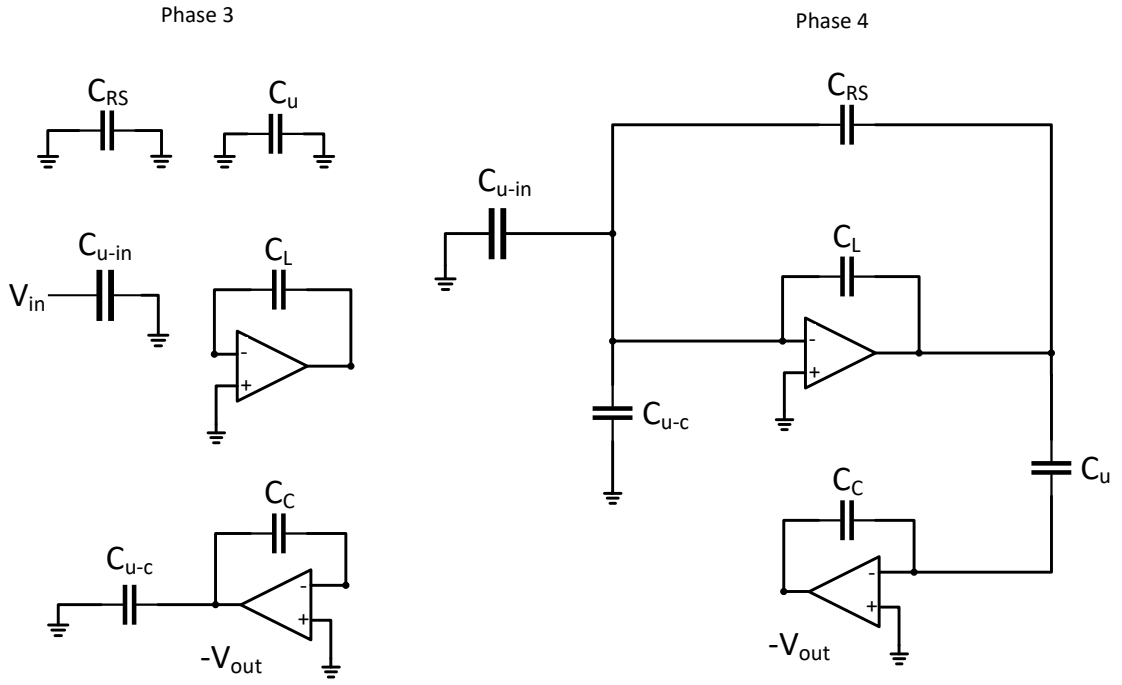

Figure 22: Equivalent Circuits during Phase 3 and Phase 4

$$-C_{u-in}z^{-1/2}V_{in} - C_{u-c}z^{-1/2}V_{out}^3 + (C_L + C_{RS})V_1^4 - C_L z^{-1/2}V_1^3 = 0 \tag{24}$$

$$C_u V_1^4 + C_c V_{out}^4 - C_c z^{-1/2}V_{out}^3 = 0 \tag{25}$$

Solving these equations for the z-domain transfer function gives,

$$H(z) = \frac{V_{out}^4}{z^{-1/2}V_{in}} = \frac{C_u C_{u-in}}{C_C C_{RS} + C_C C_L - (2C_C C_L + C_C C_{RS} - C_u C_{u-c})z^{-1} + C_C C_L z^{-2}} \tag{26}$$

Substituting the capacitance values into this transfer function and normalizing denominator constant to 1 gives:

$$H(z) = \frac{0.00899}{1 - 1.972z^{-1} + 0.981z^{-2}} \tag{27}$$

The gain in this transfer function is 1. To increase the gain by two, the capacitances C_C and C_{u-c} needs to be scaled by half. The z-domain transfer function thus becomes,

$$H(z) = \frac{0.01798}{1 - 1.972z^{-1} + 0.981z^{-2}} \tag{28}$$

In addition to that, for optimized dynamic range, the gain at the output of the first Op Amp and at the output of low-pass filter at the operating frequency should be same. The transfer function till the output of the first operational amplifier is given by:

$$H_1(z) = \frac{C_c C_{u-in} - C_c C_{u-in} z^{-1}}{C_C C_{RS} + C_C C_L - (2C_C C_L + C_C C_{RS} - C_u C_{u-c})z^{-1} + C_C C_L z^{-2}} \tag{29}$$

Table 4: Capacitor Values

Capacitor	**Unscaled Value**	**Gain Scaling**	**Maximized Dynamic Range**	**Optimized Dynamic Range**	**Scaled Value**
C_{u-in}	$0.66208\mu F$	$0.66208\mu F$	$0.66208\mu F$	$0.66208\mu F$	$0.53248pF$
C_{RS}	$0.66208\mu F$	$0.66208\mu F$	$0.062169\mu F$	$0.068386\mu F$	$55fF$
C_u	$0.66208\mu F$	$0.66208\mu F$	$0.062169\mu F$	$0.062169\mu F$	$50fF$
C_{u-c}	$0.66208\mu F$	$0.33104\mu F$	$0.33104\mu F$	$0.33104\mu F$	$0.26624pF$
C_L	$34.58\mu F$	$34.58\mu F$	$3.24706\mu F$	$3.5717\mu F$	$2.8726pF$
C_C	$1.3834\mu F$	$0.6917\mu F$	$0.6917\mu F$	$0.6917\mu F$	$0.50572pF$

When substituting the values it is given by:

$$H_1(z) = \frac{0.01878 - 0.01878z^{-1}}{1 - 1.972z^{-1} + 0.981z^{-2}} \tag{30}$$

For dynamic range optimization, scale the capacitors connected at the output of the first operational amplifier(C_L, C_{RS} and C_u) by factor of 0.01878 times of half of maximum gain. As the maximum gain of the transfer function is 20 dB, the scaling factor is thus 0.0939. The capacitor values then become 3.24706 μF, 0.062169 μF and 0.062169 μF respectively. These capacitance values gives the dynamic range optimization at 21.6KHz , to make it optimized at operating frequency of 23.6kHz, the capacitance, C_{RS} needs to be scaled further by a factor of 1.1. This also changes the values of the capacitor C_L by the same factor according to the transfer function in Equation 19 .C_u is the smallest capacitance for the required low pass filter implementation. The benefit of switched-capacitor as compared to RC circuits is that their overall performance depends on the capacitor ratios and not on the individual capacitor values. Therefore, all capacitor values can be scaled by the same factor. The lowest capacitance values available for the fabrication technology is 50fF. The value of the smallest capacitance affects the noise performance of the circuit. The noise performance is inversely proportional to this value, lower the capacitance value higher is the noise. Moreover the ratio of the largest capacitance to the smallest, affects the matching of these components. At this point, all other capacitance including integration capacitors are scaled by 50fF/0.062169μF to minimize area. The overall scaling factor is thus $8.04265\times\ 10^{-7}$. The unscaled (initial capacitor values) and scaled capacitor values are given in Table 4. The noise performance of the circuit as well as the capacitor mismatch results would be shown in later sections.

3.3 Clock Signals and Multiplexing

This section describes how the required number of channels are multiplexed for the required sampling frequency. The single stage channel multiplexed schematic is shown

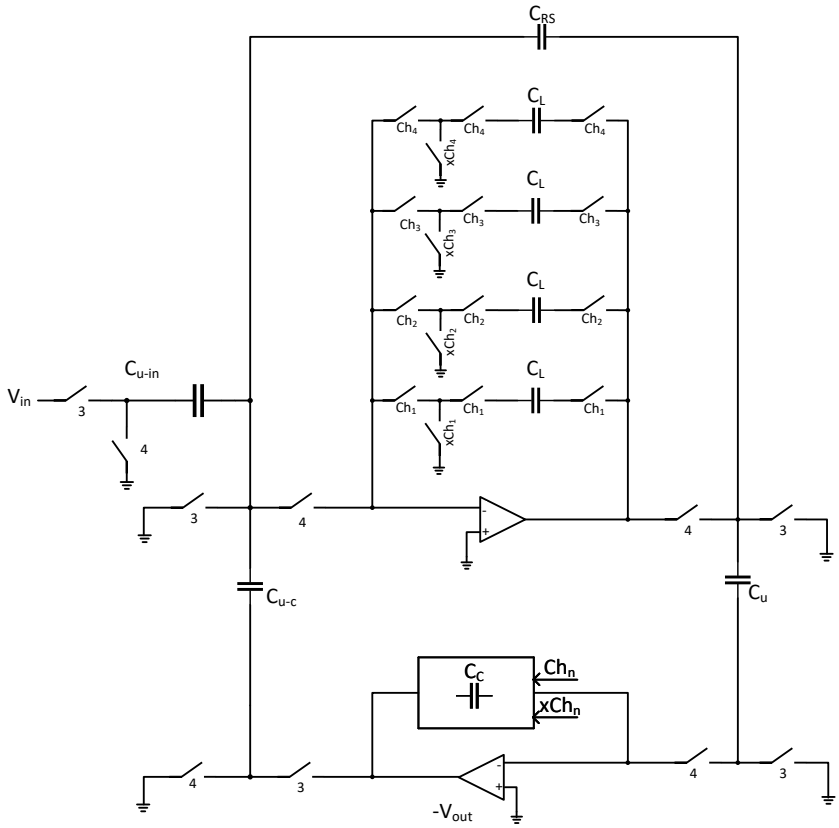

Figure 23: Full single ended schematic depicting channel multiplexing for the first stage of the filter, multiplexing for Capacitor C_C is also similar to the first stage capacitor C_L.

in Figure 23. The channel multiplexing is performed by providing de-multiplexed path for the integration capacitors. The operational amplifier performs integration to the signal separated by the switches Chn and xChn, where n is the number of channels that are required to be multiplexed. "Chn" switches provide the integration path to the specific channel signal. "xChn" switches hold the capacitor charge against ground when the channel is turned off. Therefore, the Chn and xChn switches needs to be non-overlapping. Just like the phase3 and phase 4 clocks of the low pass filter needs to be non-overlapping to prevent charge leaking[28]. The two extra switches Ch and xCh in contrast to the scheme shown in Figrue 17, helps in improving channel isolation or crosstalk when combined with a reset switch connecting input and output of the Op Amp[32]. The full schematic with the reset switch is shown in Figure 40.

For the carrier frequency of 23.6kHz and sampling frequency of 64× Fnom, one phase of single channel switched capacitor filter is switched 64 times during Fnom. Fnom is thus the carrier frequency for the sampling. When multiplexing is applied to this filter, the number of channels are increased. The overall switch-on interval for

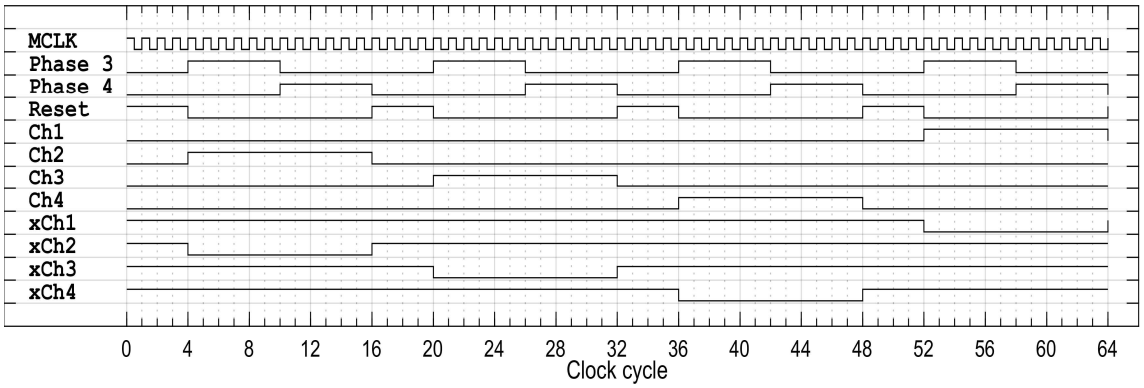

Figure 24: Clocking Sequence

one phase decreases because of the non-overlapping time but the sampling frequency per channel remains same. The maximum oscillation that can be obtained within the ASIC is 100MHz. This information was provided in advance. The highest multiple of carrier frequency that can be obtained on ASIC is 4096× Fnom (approx. 96.66 MHz). The switching is distributed according to half period of the master clock cycle. The clocking sequence is shown in Figure 24. Here, one clock cycle is equivalent to the one period of master clock. The 64 clock cycles are equivalent to one sampling interval i.e 1/(64× Fnom). The multiplexing is performed within this one sampling interval. It is not easy to see the non-overlapping time in Figure 24 as the figure is showing one complete sampling period but there is 2ns of non-overlapping time between Phase3, Phase 4 and Reset switches as shown in Figure 25.
A sampling interval starts with a reset phase. In this phase, the output of the operational amplifiers of the circuit is connected to the input. As a result, we have the zero offset at the Op Amp's input nodes. After reset phase, channel two is turned on and after a minor delay, the phase3 clocks samples the input signal. After non-overlapping time between phase 3 and phase 4, the switches for phase 4 are turned on. After phase 4 the channel goes off. The xCh switch is turned on to hold the charge and then reset is performed again before next channel is turned on. The clock signals and their characteristics are described in Table 5. Figure 26 depicts the

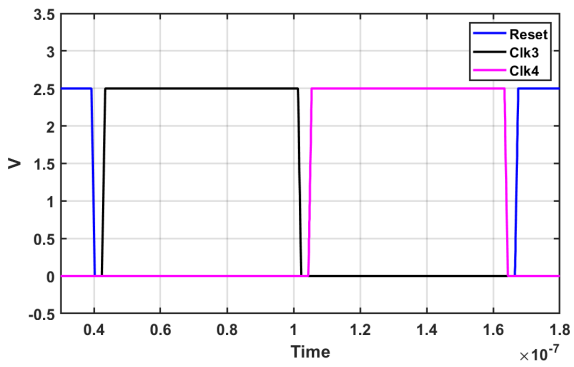

Figure 25: Non-overlapping time

Table 5: Clock Signals

Clock name	Period	Delay	Pulse Width
Reset	16/(4096× Fnom)	1 ns	3.6/(4096× Fnom)
3	16/(4096× Fnom)	4/(4096× Fnom) + 1 ns	5.6/(4096× Fnom)
4	16/(4096× Fnom)	10/(4096× Fnom) + 1 ns	5.6/(4096× Fnom)
Ch_1	64/(4096× Fnom)	52/(4096× Fnom)	11.8/(4096× Fnom)
Ch_2	64/(4096× Fnom)	4/(4096× Fnom)	11.8/(4096× Fnom)
Ch_3	64/(4096× Fnom)	20/(4096× Fnom)	11.8/(4096× Fnom)
Ch_4	64/(4096× Fnom)	36/(4096× Fnom)	11.8/(4096× Fnom)
xCh_1	64/(4096× Fnom)	0	51.8/(4096× Fnom)
xCh_2	64/(4096× Fnom)	16/(4096× Fnom)	51.8/(4096× Fnom)
xCh_3	64/(4096× Fnom)	32/(4096× Fnom)	51.8/(4096× Fnom)
xCh_4	64/(4096× Fnom)	48/(4096× Fnom)	51.8/(4096× Fnom)

definition of delay, pulse width and period of the signal. The rise and fall time for all of these clock signals is 1ns.

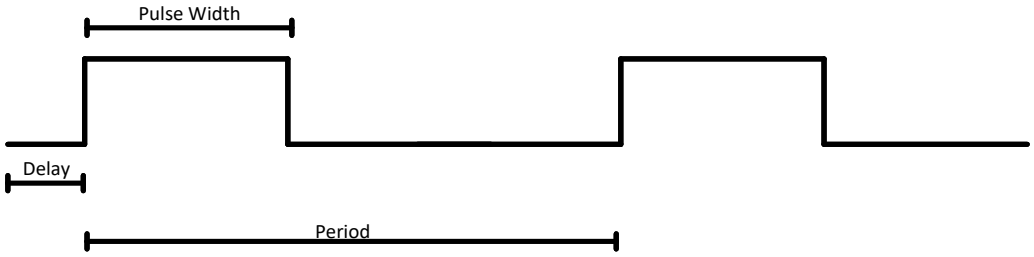

Figure 26: Timing Definition

3.4 Component design

Apart from Op Amp, switches and capacitors are important part of switched-capacitor circuits.

3.4.1 Switch design [25]

A simple MOSFET in its unit form can always be used as a switch. When the voltage at the gate terminal of the transistor goes high. The current starts to flow between the drain and source terminal due to the potential difference between them. For an NMOS transistor this gate to source voltage needs to be positive while for a PMOS

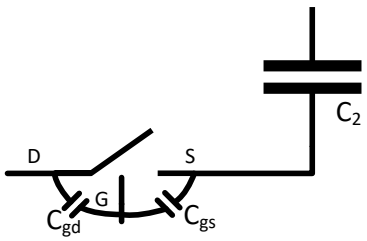

Figure 27: Parasitic Capacitances of the transistor

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the gate to source voltage should be negative for the switch to be turned on. This gate signal is coming from the clock source and is 2.5V. Thus, the transistor can be assumed to be operating in the linear region and the current equation for this region is given by:

$$i_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(2(V_{GS} - V_T)V_{DS} - {V_{DS}}^2) \tag{31}$$

where μ_n is the mobility of electrons and C_{ox} is the capacitance of the oxide material. These are the process dependent parameters. The resistance to this current when $V_{GS} - V_T$ is greater than V_{DS} is called the on- resistance of the transistor and is given by:

$$R_{on} = \frac{1}{2k(V_{GS} - V_T)} \tag{32}$$

where,

$$k = \frac{1}{2}\mu_n C_{ox}\frac{W}{L} \tag{33}$$

In a real switch, during the switching transient, there are capacitive currents coming from the parasitic capacitances of the device. The main source of these noise currents are capacitances C_{gd} and C_{gs}. In the switched-capacitor applications, there are capacitors connected to one or both terminal of the transistor. Therefore, the C_{gd} and C_{gs} form a capacitor divider with the switched capacitors as shown in Figure 27. If the capacitor C_2 is of the order of 1pF and the C_{gs} is 10fF, then for the gate on voltage of 2.5V, this clock signal would be divided by 100 and would contain a clock-feedthrough noise of 25mV. Similarly, if the source terminal of the transistor is connected to a virtual ground node, and C_2 is the feedback capacitor for an integrator. A charge equivalent to C_{gs} times 2.5V = 25fC can enter C_2 and cause an output voltage step of 25mV. Hence, in order to minimize these transient affects, a transmission gate can be used as a switch. The on-resistance of this CMOS switch is the parallel equivalent of both NMOS and PMOS. The schematic for this switch is shown in Figure 28.

Thus this switch has lower voltage drop and increased dynamic range as smaller signal can be passed through it. A transmission gate consists on both NMOS and

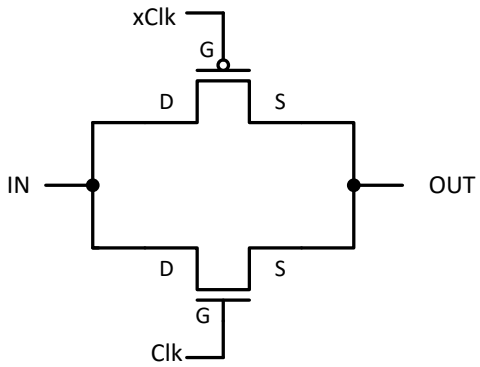

Figure 28: Transmission Gate Implementation

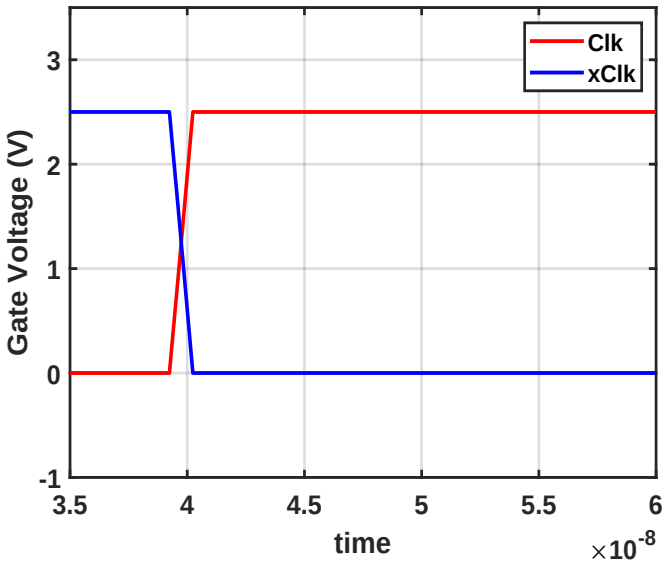

Figure 29: Gate Signals for the TG transistors

PMOS transistors. The clock signals applied to these NMOS and PMOS transistors are complementary as shown in Figure 29. The complementary gate signals can be achieved through an inverter, connected to the gate of the PMOS transistor. The incoming control signal is connected to the gate of NMOS transistor directly and to the gate of PMOS transistor through an inverter. When the control signal is high both PMOS and NMOS are turned on and the transmission gate is conducting else it is not conducting. The equivalent resistance of a transmission gate is lower compared to the individual transistor resistance because of the parallel connection. Therefore, the gate signals for the transmission gate is complementary. Moreover, this type of switch can conduct in both directions depending on the voltage polarity at its drain and source terminals. As a rule of thumb, a good switch-on resistance along-with the largest capacitance in the circuit makes the time constant equal to 1/7th of the sampling time. Switch on-resistance has a direct impact on the gain and phase shift

at the filter output. In the requirement specifications shown in the table above, the phase shift at the pole frequency has some limitation. As a target, the phase shift should not exceed 6 degrees over process variation. The main contributors to the phase shift in this circuit are transmission gate on-resistance and the bandwidth of the operational amplifier. To study the impact of the switch-on resistance, the circuit was simulated with ideal components and ideal Op Amp model. The switches used in this study were ideal. The switch resistance was varied and the phase shift from the nominal ideal cases was observed. The result of this study is shown in Figure 30.

Table 6: On Resistance

Number of fingers (m)	R_{on}	**5-sigma** R_{on}	**5-sigma Phase-shift**
3	3.5kΩ	4.6kΩ	1.2 degrees
4	2.7kΩ	3.45kΩ	0.2 degrees

Table 7: Transmission gate design

Transistor	**Width**	**Length**	**Number of fingers(m)**
NMOS	400nm	560nm	4
PMOS	1.4μm	560nm	4

For the optimized design process of the transmission gate, first of all the PMOS and NMOS transistors that were to be used in the design were selected. The selected transistors are Global Foundaries 55nm triple-well 6 terminal NMOS and the corresponding PMOS. The reason for using these transistors was their triple well structure. The bulk of these transistors is less noisy and as noise is one of the main factors in the performance of switched-capacitor circuits. This would help in minimizing the bulk noise affect in the ASIC. Next, the minimum width

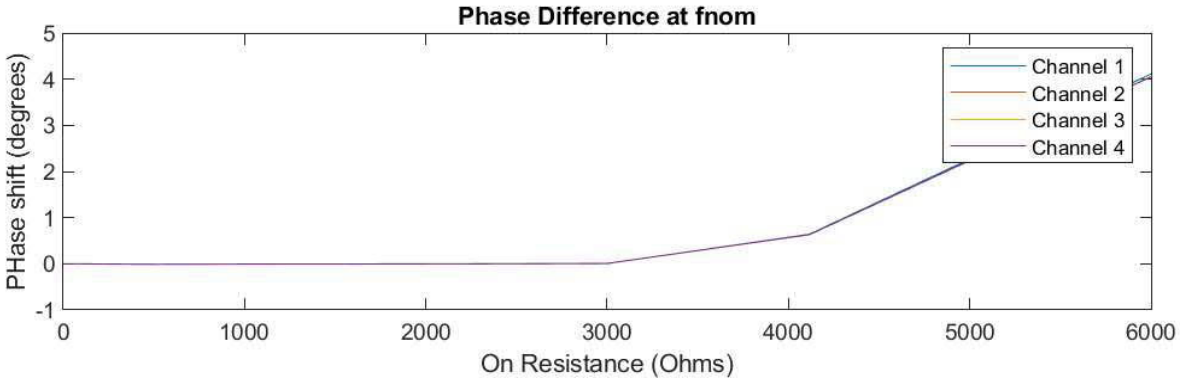

Figure 30: Phase Shift caused due to TG resistance

NMOS transistor was selected for the NMOS part of the transmission gate and the corresponding PMOS was 3.5 times wider than the NMOS. The PMOS transistor is usually 2.5 times wider than the NMOS transistor in the complementary structures. The reason for this is the mobility of holes which is 2.5 times slower than the mobility of the electrons. Here, the PMOS is 3.5 times wider because through simulations, it was found that this ratio gives a flat resistance across a large part of the operating voltage. This is the basic cell of the transmission gate and it has the resistance of 9kΩ. The resistance was then varied by changing the number of fingers and hence the width of the transistors.
From Figure 30, it can be seen that there is no significant difference in the phase shift when the switch on resistance is around 3kΩ and 4kΩ. Further, the Monte-Carlo simulation was performed for m=3 and m=4 and the 5 sigma variation for the on-resistance was calculated. The on-resistance value for these number of fingers and the corresponding 5-sigma values are summarized in Table 6.
Phase shift is also affected by the bandwidth of the operational amplifier and the mismatch in the capacitors. Out of the 6 degrees phase shift that we can have in the worst case, if m is chosen as 4, their is more margin for the phase shift caused by the mismatch and bandwidth of the Op Amp. Therefore, the switch design is summarized in Table 7 for lesser phase shift allowed because of the on-resistance.

3.4.2 Capacitor design

For a constant distance between the capacitor plates for the technology, i.e., d, the capacitor dimensions for the capacitor values shown in Table 4 are calculated and computed in Table 8. Capacitor mismatch also has an affect on the phase shift of the

Table 8: Capacitor design

Capacitor	**Width**	**Length**
Cu_{in}	16.963μm	16.963μm
Cu_c	11.93μm	11.93μm
Cu	5.021μm	5.021μm
C_{rs}	5.28μm	5.28μm
C_c	16.525μm	16.525μm
C_L	39.7μm	39.7μm

design. To study this affect, Monte-Carlo simulations were performed and 5-sigma variation for the phase shift because of mismatch was observed. The Monte-Carlo simulation result of this simulation are shown in Figure 31.

3.5 Operational Amplifier design [28]

Operational amplifier or an an Op Amp, is an active component of any switched capacitor circuit, ideally it is a voltage controlled voltage source which means that

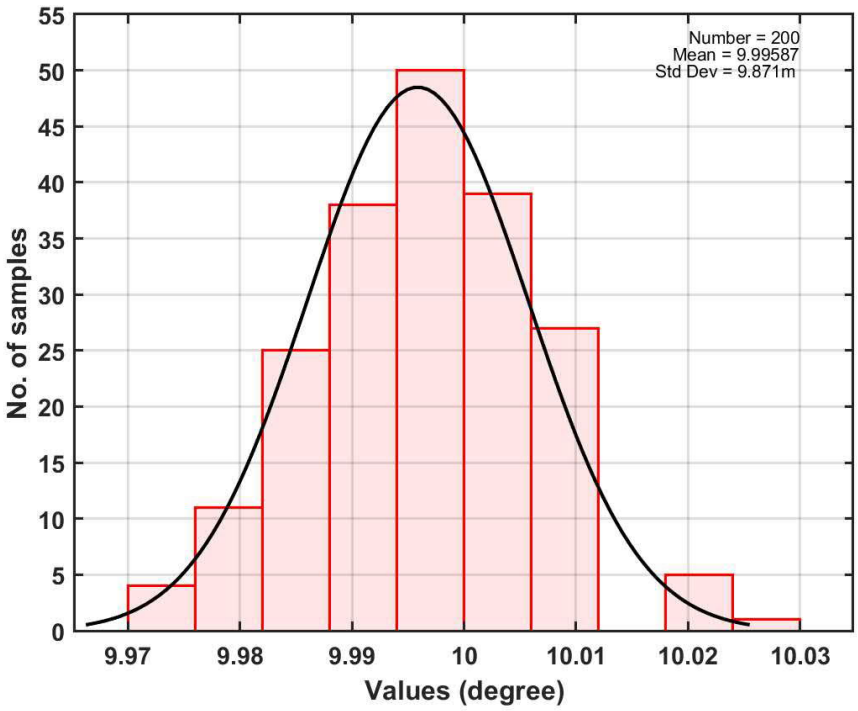

Figure 31: Monte Carlo Simulation results for Phase Shift due to Capacitor Mismatch in the TG

.

the output voltage of an op-amp depends on the change of the voltage at its input terminal. Moreover ideally, an Op Amp has infinite voltage gain, infinite bandwidth, infinite input resistance and zero output resistance. Practically, the Op Amps have finite gain which is highest for the low frequency signals. The carrier mobility and stray capacitance effect increases at higher frequencies. As a result, the gain decreases at higher frequencies. This limits the bandwidth of the Op Amp. Bandwidth is defined as the range of input signal frequency for which the output is greater than 0dB or unity. There is also a slew rate limitation for a real Op Amp. The slew rate is defined as the rate of change of output signal level of the Op Amp with respect to the change in input voltage. It is measured in V/s. For a large step at the input, the output will follow the input voltage slowly. The maximum rate of input change that an amplifier can follow is called it's slew rate.
The low-pass filter is required to be implemented in differential form, for this purpose it requires a fully- differential Op Amp. A fully-differential amplifier has differential outputs whereas a standard operational amplifier has single ended output. For a fully differential amplifier a common-mode circuitry is needed to set the common mode voltage of the amplifier to a predefined level. Conventionally, this is at the middle of the maximum available supply range. Whereas, for a standard single ended operational amplifier, the output voltage level is the same as input signal. This is the reason behind increased dynamic range of the fully differential amplifier. A

fully-differential system has inherited rejection to the external noise source. The noise or signal that appears at the input of the Op Amp as common mode signal is fully rejected by the differential Op Amp. This is the reason behind immunity of the fully differential amplifiers against common mode noise signals. Moreover, in comparison to the single-ended differential amplifier, fully differential op amps have increased dynamic range because the output signal is differential in contrast to the single-ended output signal.
Two types of operational amplifiers were considered to be implemented in the switched-capacitor circuit, i.e., the miller compensated two stage Op Amp and the folded cascode Op Amp. These amplifiers are discussed and compared in context of the low-pass filter Op Amp design in the later sections.

3.5.1 Two stage Miller Compensated Op Amp

As the name implies, a two stage amplifier consists of two stages, i.e., a differential amplifier stage and a gain stage. The overall gain of the amplifier consists on the gain of these two stages. Typically, the first stage is a differential input single ended output amplifier while the second stage is the common-source amplifier. The second stage has an active load. The circuitry is shown in Figure 32.

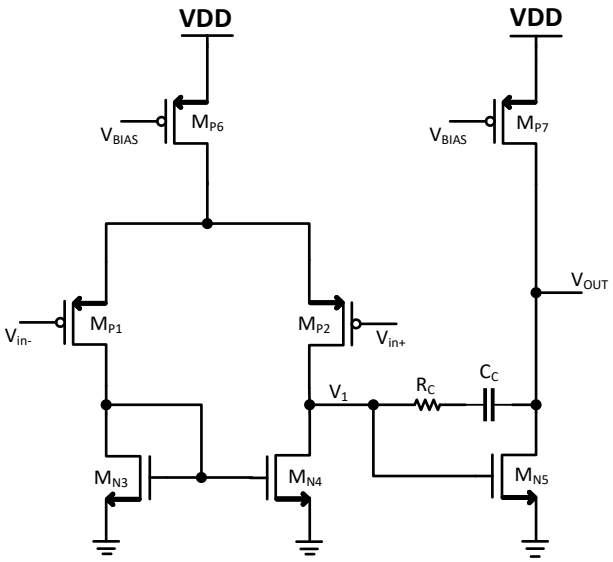

Figure 32: Two Stage Miller Compensated Operational Amplifier

It has the p-channel devices for the input differential pair formed by the transistors M_{P1} and M_{P2}, whereas the n-channel M_{N3} and M_{N4} is the active load for this stage. Common source gain stage is formed by the n-channel M_{N5} with M_{P7} acting as an active load for this stage. Transistor M_{P6} is the current mirror biasing transistor for the differential stage. Here, the Op Amp is implemented using complementary devices for both the gain stages. C_C and R_c provides the dominant pole compensation and lead compensation respectively. To understand these compensations, consider

the small signal equivalent model for the Op Amp in Figure 33.
Here, V_1 is the single ended output from the first stage of the Op Amp. R_1 and C_1 is the output resistance and capacitance of the first stage. Similarly, R_2 and C_2 is the resistance and capacitance at the output node. The transfer function for the dominant pole compensation alone can be written as:

$$\frac{V_{out}}{V_{in}} = \frac{g_{m1}g_{m5}R_1R_2(1 - \frac{sC_c}{g_{m5}})}{1 + sa + s^2b} \tag{34}$$

where

$$a = g_{m5}R_1R_2C_c + R_1(C_1 + C_c) + R_2(C_2 + C_c) \tag{35}$$

$$b = R_1R_2(C_1C_2 + C_1C_c + C_2C_c) \tag{36}$$

Solving the transfer function for the first and second pole(ω_{p1} and ω_{p2} respectively) gives,

$$\omega_{p1} = \frac{1}{g_{m5}R_1R_2C_c} \tag{37}$$

and

$$\omega_{p2} \simeq \frac{g_{m5}}{C_1 + C_2} \tag{38}$$

and a zero at

$$\omega_{z1} = \frac{-g_{m5}}{C_c} \tag{39}$$

Whereas without the compensation capacitor, the transfer function for the small signal model would give two poles defined by the capacitors C_1 and C_2. As these capacitance values are defined approximated by the gate to source capacitance of transistor M_{N5} and load capacitance. In the magnitude bode plot of the two pole transfer function, the gain decreases with the slope of 20 dB/decade after first pole and after the second pole it decreases with 40 db/decade. Also, there is a phase shift of 180 degrees after the second pole. The phase margin of the transfer function is measured as the difference of phase between the unity gain frequency and 180 degrees. The more difference there is the more stable is the Op Amp in negative

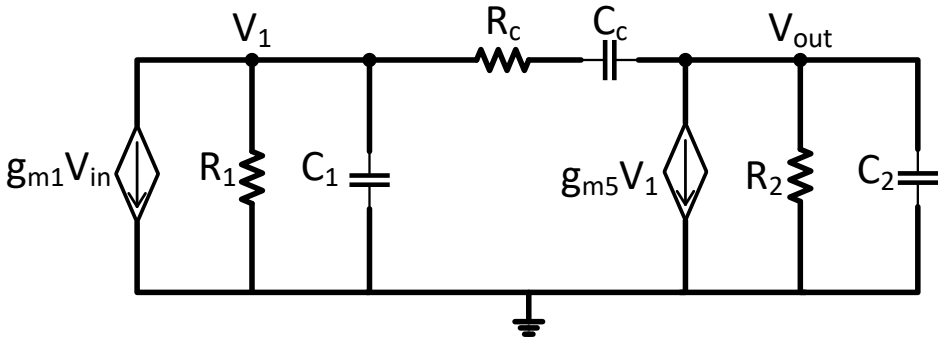

Figure 33: Small Signal Model for the op amp in Figure 32

feedback configuration. As the small change in the load capacitance value in the feedback can affect the phase and if the feedback becomes positive that makes the Op Amp unstable. Without compensation, the two poles are very close to each other and the phase margin is very low any parasitic pole or an additional capacitor in the feedback can decrease the phase margin further. From the above relations, we can see that first pole of the system depends on the transconductance g_m of the common-source drive transistor. Thus, the pole is moved to the lower frequency which decreases the 3-dB bandwidth of the system but increase the phase margin and stability. For the lead compensation, an additional pole and modified zero is introduced to the transfer function. In equation 34 the zero is now given as:

$$\omega_{z1} = \frac{-1}{C_c(\frac{1}{g_{m5}} - R_C)} \tag{40}$$

Choosing the value of R_C to be greater than $1/g_{m5}$ moves this right half plane zero to left half plane zero. It cancels the affect of ω_{p2} if the load capacitance is known and to increase the phase margin further as discussed above select R_C even greater than that to move this zero at a frequency slightly higher than the unity gain frequency. The compensation is an important part of op-amp design if the op-amp is intended to be used in the feedback configuration. One important thing to consider here is the type of devices used for input differential stage and common source stage, they are always used in complementary manner.
The choice of whether to use p-channel or n-channel devices as the input stage transistors and the complementary device for the common source stage depends on several trade-offs. For a high frequency applications, the above mentioned configuration is preferred as it increases the transconductance of the second stage and the second pole and unity gain frequency of the op amp is dependent on the transconductance of the second stage. Also p-channel transistors have less 1/f noise than the n-channel devices because 1/f is mainly caused when carriers (electrons or holes) of a device are trapped in the surface states and holes have less tendency to get trapped in the surface states than electrons. When the resistive loads are meant to be driven, an output buffer stage is added to the above mentioned topology. This decreases the output impedance of the Op Amp. If no resistive load is required to be driven, the output node can have higher impedance. One of the Op Amps which have high output impedance node is the folded cascode Op Amp described in the next section.

3.5.2 Folded Cascode Op Amp

Folded cascode Op Amp is the type of op-amp commonly referred as operational transconductance amplifier (OTA) because of the ratio of the output current to the input voltage. This amplifier topology has a very high impedance output node while the other nodes in the circuit are low impedance and hence these amplifiers have higher speed. The low impedance nodes within the op-amp can result in reduced voltage signals at them but the current signals can be large. Moreover, these amplifiers do not require additional compensation mechanism for stability as the compensation for them comes from the load capacitance. The Op Amp becomes more

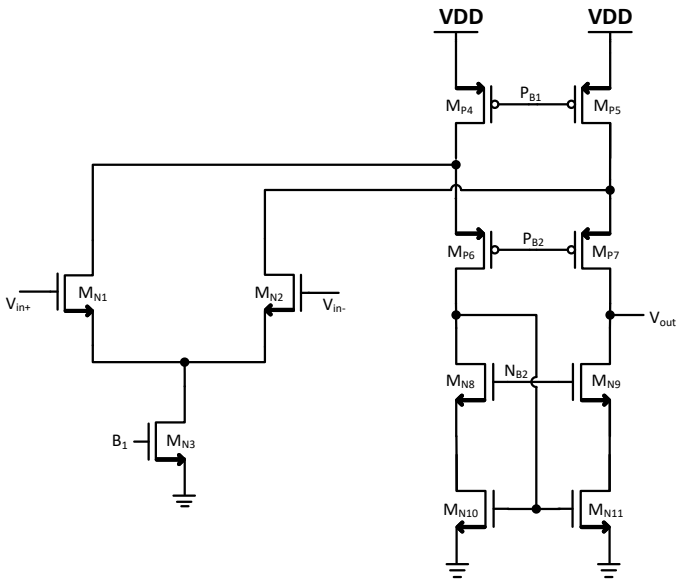

Figure 34: Folded cascode Operational Amplifier

stable as the load capacitance increases but its speed decreases. In these amplifiers, cascode transistors opposite in channel type to the input differential pair follows the input differential pair. These Op Amps uses wide-swing current mirrors rather than the conventional current mirror. With the conventional current mirror it is difficult to obtain large output swing and high gain because of the their lower output impedance. The wide swing current mirror provide better gain and higher output signal swing. The main idea in wide swing current mirrors is to bias the transistors M_{N10} and M_{N11} with lowest bias voltage which prevents them from operating the transistors in the triode region. The transistor M_{N10} and M_{N8} provides diode connection for the current mirroring through transistors M_{N9} and M_{N11}. The circuit for the folded cascode op-amp is shown in Figure 34.

The structure consists on n-channel MOS device for the input differential pair and the complementary p-channel device for the cascode. Transistor M_{N3} provides tail current for the differential pair. Depending on the input voltage signal the current through either of M_{N1} or M_{N2} starts to increase or decreases. For higher V_{in+}, M_{N1} turns on and the gate voltage starts to increase, and near the positive peak or maximum V_{in+}, the transistor is operating near the edge of the saturation region (for saturation Vds $\geq$ Veff) and eventually enters into the triode region at the peak. Now when V_{in-} becomes greater it takes some time for the transistor M_{N1} to come out of the triode region. To make sure that the transistor channels always have some current flowing, the current through the transistors M_{P4} and M_{P5} is kept euqal or higher than the current through M_{N3}. The small signal model for this op amp is shown in Figure 34. All nodes except the output nodes are low impedance nodes. It is assumed that in this case almost all of the input current flows to the output through different paths. Usually, all the capacitance values except the output capacitance are very small. Therefore, the pole or zero caused by them are at frequencies higher

than the unity gain frequency defined by the load capacitance. Hence, the small signal transfer function for this topology is defined as follows,

$$\frac{V_{out}}{V_{in}} = \frac{g_{m1}R_{out}}{1 + sC_LR_{out}} \tag{41}$$

where R_{out} is the impedance seen at the output node and it value can be computed as:

$$R_{out} = (g_{m9}r_{ds9}r_{ds11})||(g_{m7}r_{ds7}(r_{ds2}||r_{ds5})) \tag{42}$$

which is a high value. Both of these operational amplifiers topologies are compared in Table 9.

Table 9: Operational Amplifier topologies comparison

Feature	**Two Stage Op-amp**	**Folded Cascode Op-amp**
Output Swing	more	less
Gain Bandwidth	Depends on C_C	Depends on C_L
Usual load	Resistive	Purely Capacitive
Power Consumption	more	less

The load for the low pass filter is purely capacitive and power consumption is one of the important target of this design. Therefore, the selected topology for the low-pass filter Op Amp design is the folded cascode Op Amp.

3.5.3 Folded Cascode Op Amp Design

As mentioned in the previous section, the compensation in the folded cascode op-amp is provided by the load capacitor, higher value of the load capacitor makes the operational amplifier more stable in the feedback configuration. If the value of the load capacitor is very small that it becomes comparable to the other internal capacitance values, then an additional capacitance is required at the output node for compensation. For the low-pass filter, total load capacitance is 1pF, which is the load capacitance for the second operational amplifier in Figure 23. Whereas for the first stage the output capacitance including the external probing capacitance values used for testing is 250fF. The total current consumption of the folded cascode op-amp depends on the tail current flowing through the transistor M_{N3} and the current through transistors M_{N10} and M_{N11}. Therefore, for better power consumption, the current through both of the operational amplifiers should be different depending on their load capacitance values. Therefore, both of the operational amplifiers are required to be designed separately. To estimate minimum bandwidth requirement for this design, consider the plot shown in Figure 35.Here the independent variables are bandwidth and on-resistance, by varying the independent variable, dependent parameter i.e., phase is observed. As described previously, the total phase shift of the

filter depends on the transmission gate on resistance, the mismatch in the capacitors and the bandwidth of the operational amplifier. Assuming that the phase variation due to capacitor mismatch is independent of the on resistance of the transmission gate and bandwidth of the amplifier. On the other hand, the switch-on resistance and bandwidth of the amplifier are linearly dependent on each other. The maximum variation in the output phase that can be tolerated according to the specifications is thus given by:

$$\sqrt{(\sigma_{R_{on}} + \sigma_{BW})^2 + (\sigma_{C_{MM}})^2} = 5.7 \tag{43}$$

Where σ_{R_on}, σ_{BW} and σ_{C_MM} correspond to 5-sigma variation in the phase due to R_{on}, BW and capacitor mismatch respectively. Referring to Figure 31, the 5 sigma variation due to capacitor mismatch is 0.049(0.49%). 0.49% of the total phase shift is 2.8 degrees. The remaining phase shift variation that we can have from R_{on} and BW given by equation 43 is 4.96 degrees. Using ideal models for TG and Op Amp, simulations are performed varying R_{on} and BW independently and the Phase shift from nominal is observed, the results are plotted in Figure 35.
In section 3.4.1, it is reported that the phase shift due to the selected transmission gate is 0.2 degrees. The remaining phase shift that we should get from the operational amplifier is 4.7 degrees. From Figure 35. it can be seen that against 4.7 degrees the BW of the operational amplifier should be atleast 14MHz. For ideal Op Amp the minimum bandwidth that should be available considering slewing and switch settling into account should be 1.875 times of 14MHz. Therefore, the minimum BW that should be considered for the design should be 26.25MHz. For the Op Amp the unity gain frequency, i.e., the frequency of the dominant pole needs to be considered. As a rule of thumb, this frequency should be 3 times of the minimum required BW. Therefore, the GBW for the operational amplifier design is 78MHz. The GBW and

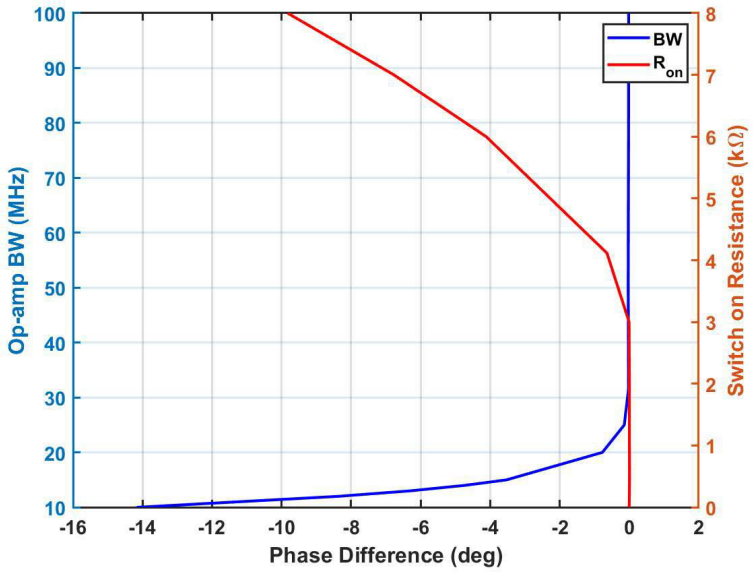

Figure 35: Phase shift due to switch on resistance and BW

the load capacitor value gives the transonductance value for the input transistor.

$$g_{m_{N1}} = GBW \times C_L \tag{44}$$

For constant I_D,

$$g_m = \frac{2I_D}{(V_{GS} - V_{th})} \tag{45}$$

Therefore,

$$I_{D_{N1}} = \frac{g_{m_{N1}}(V_{GS} - V_{th})}{2} \tag{46}$$

For the GF 55nm BCD technologies the factor k'_n and k'_p for the transistors under consideration are approximately found to be

$$k'_N = \mu_N C_{ox} \simeq 120\mu A/V^2 \tag{47}$$

$$k'_P = \mu_P C_{ox} \simeq 40\mu A/V^2 \tag{48}$$

The bias current for the input transistors depends on the slewrate (SR) requirement of the Op Amp design. The slew rate comes from by maximizing the rate of change of output signal.

$$SR = max\left(\frac{dV_{out}(t)}{dt}\right) = \omega_o V_{op} \tag{49}$$

where V_{op} is the maximum voltage of the output signal i.e 2.125V and ω_o is the carrier frequency i.e.23600. As the Op Amp is being designed for the switched capacitor application, the output is taken during phase4 of the clock cycle described in the section above. As a rule of thumb, atleast 20% of the phase 3 time should be considered for slewing. This defines minimum available slew rate as:

$$SR = \omega_o V_{op} \times \frac{t_{rep}}{0.2t_{on}} \tag{50}$$

where t_{rep} is one sampling period i.e. 64xF_nom and t_{on} is 0.0579μs. They give the minimum slew rate of 18V/μs. Therefore, for the load capacitance of 1pF, the tail current for the differential pair should be greater than 18μA. For the tail current of 20μA, the size of the input differential pair transistors M_{N1} and M_{N2} is given by:

$$\left(\frac{W}{L}\right)_1 = \left(\frac{W}{L}\right)_2 = \frac{GBW^2 C_L^2}{k'_N I_{M_{N3}}} \tag{51}$$

which is 100 approx., and this size of input differential pair transistor gives the width to length ratio of the tail transistor M_{N3} as 450. This increases the transistor dimensions which increases the parasitic capacitance and can affect the stability of the operational amplifier at lower load capacitance values. Moreover, if one of the input differential transistor starts to operate in the triode region or turns off close to the rail, it will take some time for the transistors parasitics to get charged and transistor to turn on, this will slow down the operational amplifier function.

Therefore, for faster and stable design the tail current of the design is increased to 200μA. For this tail current the size of the transistors M_{N1} and M_{N2} is 10. Transistor M_{N3} size is given by minimum input common mode level [33].

$$\left(\frac{W}{L}\right)_3 = \frac{2 \times I_{M_{N3}}}{k'_N \left(V_{in}(min) - V_{SS} - \sqrt{I_{M_{N3}} k'_N (W/L)_1}\right)} \tag{52}$$

The current through the transistors M_{P4} and M_{P5} is kept 1.2 times higher than the current through the input differential pair. At the maximum input signal to keep the transistors in saturation the maximum voltage drop would appear at the transistors M_{P4}, M_{P5}, M_{P6} and M_{P7} transistors. At this worst case, the voltage drop should not exceed more than 0.375V from the rails. It is a good practice to have more voltage drop at the transistors M_{P4} and M_{P5}, to keep the transconductance of the transistors M_{P6} and M_{P7} high and thus have more gain at the output. To encounter for the approximate values of the k'_n and k'_p, the design on paper was done for the output range of 250mV from positive supply rail and 200mV from the negative supply rail. The voltage drop for the M_{P4} and M_{P5} is reserved for 200mV and 50mV for M_{P6} and M_{P7} transistors. The dimension for M_{P4} and M_{P5} are given by maximum input common mode level [33].

$$\left(\frac{W}{L}\right)_4 = \left(\frac{W}{L}\right)_5 = \frac{2 \times 1.2 \times I_{M_{N1}}}{k'_p V_{SD}^2} \tag{53}$$

Similarly for the lower transistors M_{N8}, M_{N9}, M_{N10} and M_{N11}, the size depends on the output range from the negative supply rail. Out of 200mV of this range, 150mV

Table 10: Transistor Dimensions of the op amp design for two stages of the filter

	1st Stage Op amp $C_L = 0.25pF, GBW = 65MHz$		**2nd Stage Op amp** $C_L = 1pF, GBW = 78MHz$	
Transistor	**Length**	**Width**	**Length**	**Width**
M_{N1}	$1\mu m$	$60\mu m$	$1\mu m$	$40\mu m$
M_{N2}	$1\mu m$	$7\mu m$	$1\mu m$	$10\mu m$
M_{N3}	$1\mu m$	$7\mu m$	$1\mu m$	$10\mu m$
M_{P4}	$1\mu m$	$200\mu m$	$1\mu m$	$160\mu m$
M_{P5}	$1\mu m$	$200\mu m$	$1\mu m$	$160\mu m$
M_{P6}	$0.33\mu m$	$900\mu m$	$0.33\mu m$	$900\mu m$
M_{P7}	$0.33\mu m$	$900\mu m$	$0.33\mu m$	$900\mu m$
M_{N8}	$1\mu m$	$800\mu m$	$1\mu m$	$800\mu m$
M_{N9}	$1\mu m$	$800\mu m$	$1\mu m$	$800\mu m$
M_{N10}	$1\mu m$	$80\mu m$	$1\mu m$	$80\mu m$
M_{N11}	$1\mu m$	$80\mu m$	$1\mu m$	$80\mu m$

is meant to be dropped across transistor M_{N8} and M_{N9} and the rest of the 50mV as V_{DS} of transistors M_{N10} and M_{N11}. It is given by minimum output voltage level [33].

$$\left(\frac{W}{L}\right)_7 = \left(\frac{W}{L}\right)_8 = \frac{2 \times 1.2 \times I_{M_{N1}}}{k'_n V_{DS}^2} \tag{54}$$

The final transistor dimensions for this Op Amp design are shown in Table 10. The same design implementation for both of the Op Amps gives the total current consumption for the low-pass filter to be 950μA. This is within the target, but as the load capacitor for the first stage op amp is lower, the design is further optimized by designing another operational amplifier for the GBW of 65MHz and load capacitance of 250fF. Both of the design are summarized in the table 10. Here, the length of the output cascode transistors M_{P6} and M_{P7} in an op amp is kept smaller than the rest of the lengths to have higher transconductance and hence the higher gain.

3.5.4 Biasing Circuit

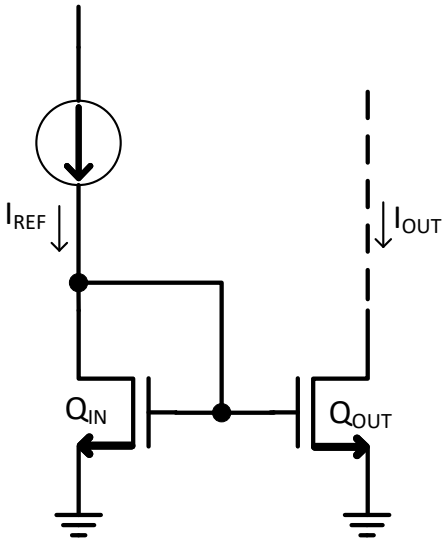

Figure 36: Current Mirror

On an integrated circuit, there are different circuits which employ the external supply to maintain the operation of different blocks present on the chip. These circuits include biasing circuits, reference circuits and regulators. The biasing circuit usually provides a biasing voltage for the gate of a transistor in such a way that the operating point of the transistor is maintained. The biasing circuit is sensitive to temperature and process variations. On the other hand, the reference circuit is such a circuit which does not vary with temperature and process variation and keeps a constant reference for current or voltage. This reference is usually maintained through a bandgap voltage reference which remains constant. For practical implementation, the biasing circuit is placed in close proximity to the circuit that needs to be biased

to minimize the affect of noise and component mismatch. For the Op Amp above the biasing circuit is designed from the 5μA reference current. It exercises the current mirrors to create biasing voltages for the operational amplifier transistors. A basic current mirror for N and P-channel devices is shown in Figure 36. Here the input current I_{ref} is converted into voltage trough a diode connected transistor Q_{in}. As both Q_{in} and Q_{out} has the same gate voltage, if the dimension of these transistors are also same, the same current will flow as I_{out} through the transistor Q_{out}. As the diode connected transistor is in saturation, both currents can be related to each other using drain current equation for the same gate voltage of the transistor giving:

$$I_{out} = \frac{(W/L)_{out}}{(W/L)_{in}} I_{ref} \tag{55}$$

Therefore, if the length of both transistors is same, I_{out} depends on the width ratio of both of the transistors. The biasing circuit along-with the operational amplifier is shown in Figure 37. The tail current transistor M_{N3} and PMOS load current transistors M_{P4} and M_{P5} are biased based on the current required for them as described in Table 10 in the previous section, as well as considering that the gate voltage of these transistors should keep them operating in the saturation region. For instance, to keep the transistor M_{N3} in saturation , voltage B_1 should be biased in such a manner that the drain voltage of the transistor is greater than the difference of the voltage at B_1 and V_{th} . Similarly the cascode transistors M_{P6}, M_{P7} and cascode load transistors M_{N8}, M_{N9} are biased by making sure that the gate voltage for these transistors is atleast greater than the $V_{GS} + 2V_{th}$ by cascoding three transistors with the same length cascoded in the biasing circuit. It is equivalent to increasing the length of the transistor while keeping the width constant to obtain higher biaising voltage. For a differential Op Amp, the biasing of the transistors M_{N10} and M_{N11} is performed through a common mode feedback circuit described in the next section. Transistor dimension for the biasing circuits of both of the amplifiers are shown in

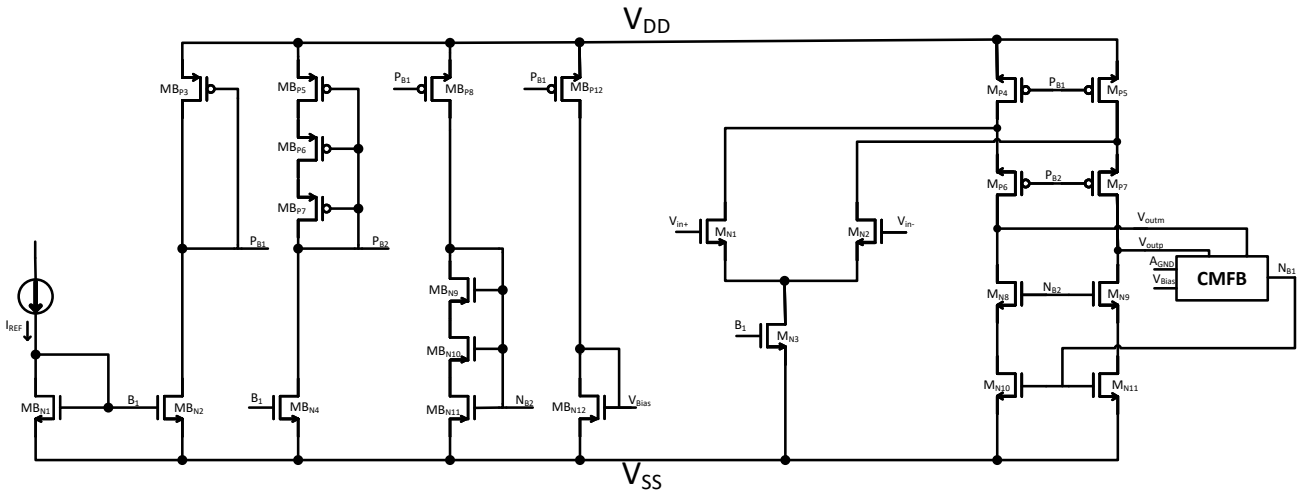

Figure 37: Biasing Circuit with the fully differential implementation of the Op Amp

Table 11: Op Amp Biasing Circuit Transistor Dimensions

	1st Stage Op Amp $C_L = 0.25pF, GBW = 65MHz$		**2nd Stage Op Amp** $C_L = 1pF, GBW = 78MHz$	
Transistor	**Length**	**Width**	**Length**	**Width**
MB_{N1}	$1\mu m$	$2\mu m$	$1\mu m$	$1\mu m$
MB_{N2}	$1\mu m$	$3.6\mu m$	$1\mu m$	$2.4\mu m$
MB_{P3}	$1\mu m$	$10\mu m$	$1\mu m$	$10\mu m$
MB_{N4}	$1\mu m$	$3.75\mu m$	$1\mu m$	$2.5\mu m$
MB_{P5}	$1\mu m$	$1\mu m$	$1\mu m$	$1\mu m$
MB_{P6}	$1\mu m$	$1\mu m$	$0.33\mu m$	$1\mu m$
MB_{P7}	$1\mu m$	$1\mu m$	$0.33\mu m$	$1\mu m$
MB_{P8}	$1\mu m$	$10\mu m$	$1\mu m$	$10\mu m$
MB_{N9}	$1\mu m$	$2\mu m$	$1\mu m$	$2\mu m$
MB_{N10}	$1\mu m$	$2\mu m$	$1\mu m$	$2\mu m$
MB_{N11}	$1\mu m$	$2\mu m$	$1\mu m$	$2\mu m$
MB_{P12}	$1\mu m$	$12.9\mu m$	$1\mu m$	8.8µm
MB_{N13}	$1\mu m$	$8\mu m$	1μm	8μm

the Table 11.

3.5.5 Common mode feedback

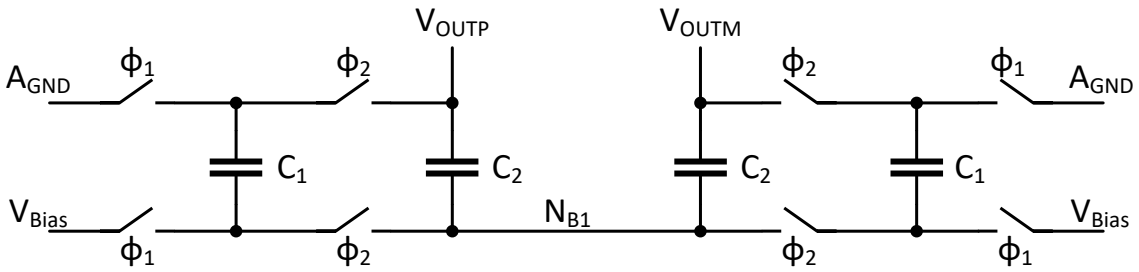

Figure 38: Switched Capacitor Common Mode Feedback

The topology shown in Figure 34 is for the single-ended folded cascode operational amplifier. The low-pass filter is implemented in the fully differential form which requires fully-differential Op Amps. Fully differential Op Amps have common-mode feedback which is meant to keep the output node at the specified common mode voltage which is usually the middle of the supply range. The purpose of common-mode feedback circuit and it's implementation is described in detail in this subsection.

A common mode feedback circuit senses the common mode voltage at the output of the differential operational amplifier, compares it with a reference voltage and feedbacks the correcting common mode signal. This results in a corrected common mode level at the output. There are two types of common mode feedback circuits, i.e., continuous-time circuit and switched-capacitor based discrete-time circuits. The switched-capacitor topology is used usually for the switched-capacitor circuits as the discrete-time circuit can cause clock feed-through glitches in the continuous-time circuits. The circuit implemented for the design the Op Amps design of this thesis is shown in Figure 38.Here, V_{Bias} is the voltage difference between the desired common mode voltage which is 1.25 (equivalent to AGND) NB1 which is the desired bias voltage for the Op Amp transistors, M_{N10} and M_{N11}. Capacitor C_2 is a fixed capacitor connected to each output of the Op Amp. The V_{bias} was determined through simulations using ideal CMFB. It is basically a voltage controlled current source in the feedback configuration. For equal capacitors C_2, if both of the output terminals are fully differential and there is no common mode signal the node NB1 is maintained at the center of the supply range, i.e., 1.25V. During phase 2, this DC voltage across C_2 appears across C_1. If there is any difference in N_{B1} because of change in Voutp or Voutm, it is compensated by charge transfer through C_1 during phase2 of the clock. The clocking is set such that the clocks complete their cycle once during each phase of the clock phases ck3 and ck4 described in the section 3.3. The switches are realized using transmission gates to keep the switch resistances constant and fast operation. The transmission gate dimension for the CMFB as well as the capacitor values for both amplifiers are shown in Table 12 and Table 13.

Table 12: Common mode feedback transmission gate

Transistor	**Width**	**Length**	**Number of fingers(m)**
NMOS	400nm	560nm	1
PMOS	1.4μm	560nm	1

Table 13: Common mode feedback Capacitors

Capacitor	**Op Amp stage 1**	**Op Amp stage 2**
C_2	200fF	75f
C_1	446fF	177fF

3.6 Final fully differential schematic

The fully differential schematic with multiplexed channel is shown in Figure 40. The channel demultiplexer implemented with ideal switches for the analyses and simulations is shown in Figure 39.

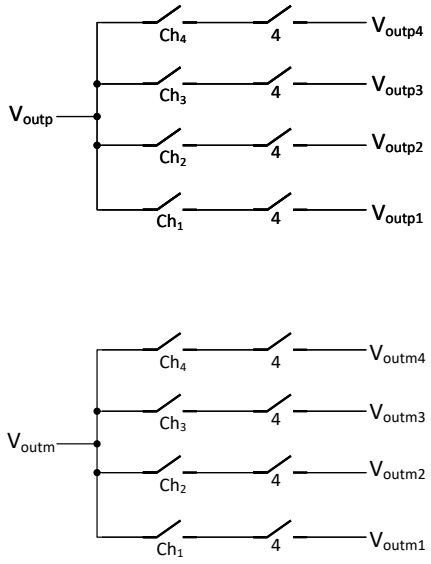

Figure 39: Demultiplexer Implemented with ideal switches for simulation purposes

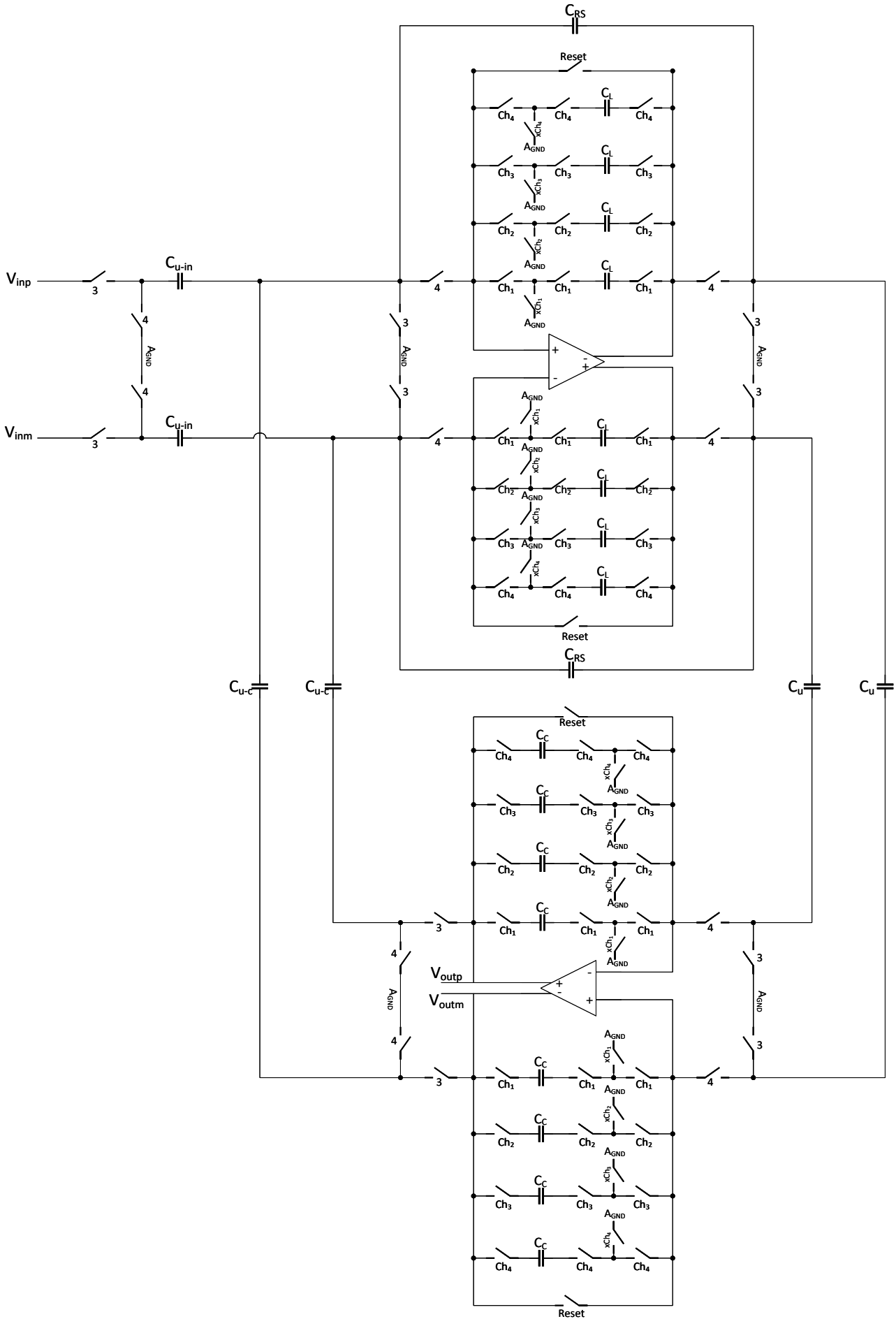

Figure 40: Full schematic with the channel multiplexing

4 Simulation Results

This chapter describes the simulation results obtained using Cadence tools. The first section compares the transfer function of the transistor level design with the reference transfer function, thus comparing the Q value and the DC gain. Section 4.2 shows the harmonic distortion of the output waveform at nominal frequency. Section 4.3 constitutes of the power supply rejection ratio (PSRR) results. Section 4.4 shows the channel isolation between different channels of the low pass filter. Section 4.5 represents the input referred noise in the signal band for the design while the final section 4.6 shows the current consumption in nominal as well as process voltage temperature (PVT) corners.

4.1 Transfer function

The transfer function for all outputs of the filter from the output is obtained using the period steady state analysis in cadence virtuoso. This analysis computes the steady state response of a periodic circuit at a fundamental frequency which is 23.6kHz in our case. The results are shown Figure 41 and Figure 42 in comparison to the z-domain transfer function computed in the previous section and plotted in matlab using the calculated co-efficients for the required Q-value, and center frequency. Note that the plots are done through MATLAB and it plots phase difference from 180 degree for the phase plot therefore, the negative phase is plotted as Phase value - 180. Figure 41 shows the magnitude comparison while Figure 42 shows the phase comparison as a whole and around the fnom frequency as well. Moreover, monte carlo and PVT simulations were also performed for one output and phase and they are shown in Figure 43 and Figure 44 respectively. The phase and magnitude variation described in the Figure 41 - Figure 44 are summarized in the Table 14. The phase shift of the signal at the Fnom frequency is targeted to be ±6 degrees over process variations and 0.6 degrees over supply variations the Table 14 summarizes the results for the phase shift at 23600 Hz.

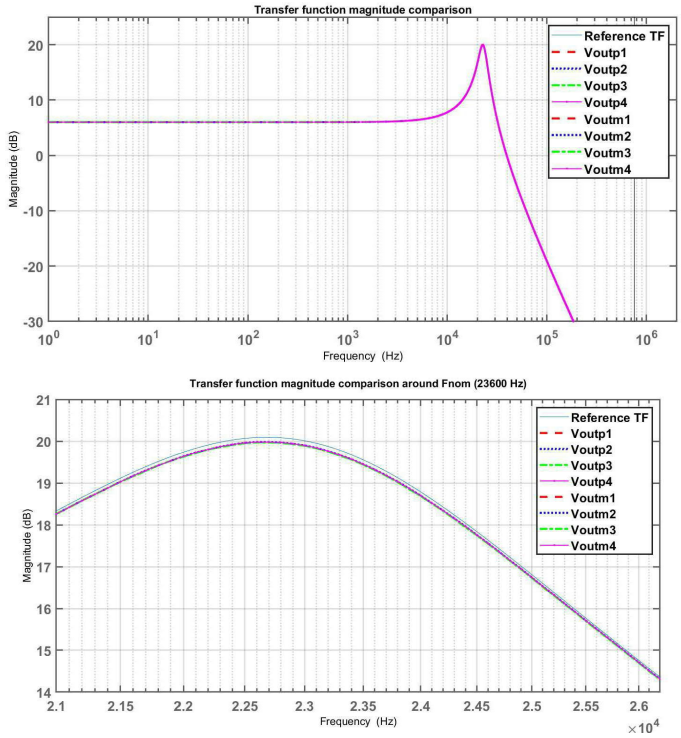

Figure 41: (top to bottom) Full Scale Magnitude response and the response around Fnom for all outputs

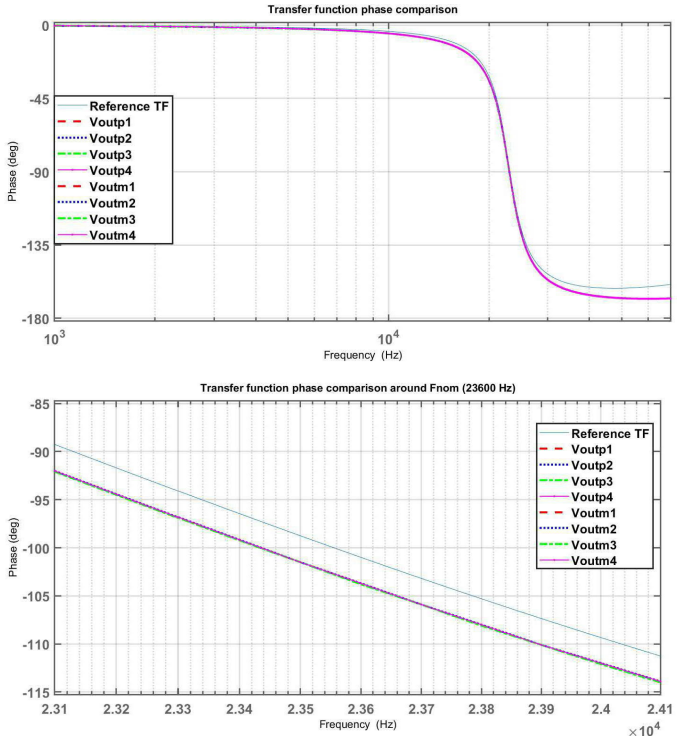

Figure 42: (top to bottom) Full Scale Phase response and the response around Fnom for all outputs

Table 14: Phase Shift values at each output

Corner	**Voutp1**	**Voutp2**	**Voutp3**	**Voutp4**	**Voutm1**	**Voutm2**	**Voutm3**	**Voutm4**
Nominal	-103.8	-103.7	-103.8	-103.7	76.24	76.3	76.24	76.3
$V_{DD} = 2.45V$	-103.6	-103.6	-103.6	-103.6	76.42	76.41	76.42	76.41
$V_{DD} = 2.55V$	-101	-101	-101	-101	78.97	79.04	78.97	79.04
Cold	-103.5	-103.4	-103.5	-103.4	76.84	76.59	76.84	76.59
Hot	-104.1	-104.1	-104.1	-104.1	75.9	75.93	75.9	75.93
FF	-103.9	-103.8	-103.9	-103.8	76.12	79.06	76.12	79.06
FF Cold	-100.8	-100.9	-100.8	-100.9	79.22	75.93	79.22	75.93
FF Hot	-103.8	-103.8	-103.8	-103.8	76.18	76.17	76.18	76.17
FS	-101	-101.2	-101	-101.2	79	78.79	79	78.79
FS Cold	-103.8	-103.8	-103.8	-103.8	76.22	76.19	76.22	76.19
FS Hot	-103.8	-103.8	-103.8	-103.8	76.24	76.21	76.24	76.21
SF	-100.7	-100.9	-100.7	-100.7	79.25	79.05	79.25	79.05
SF Cold	-103.3	-103.3	-103.3	-103.3	76.74	76.70	76.74	76.70
SF Hot	-104.2	-104.2	-104.2	-104.2	75.75	75.8	75.75	75.8
SS	-100	-100.3	-100	-100.3	80	79.72	80	79.72
SS Cold	-103	-102.9	-103	-102.9	76.98	77.09	76.98	77.09
SS Hot	-103.7	-103.7	-103.7	-103.7	76.35	76.33	76.35	76.33
Mean	-103.734	-103.723	-103.734	-103.725	-	-	-	-
5σ **value**	0.725	0.77	0.736	0.686	-	-	-	-

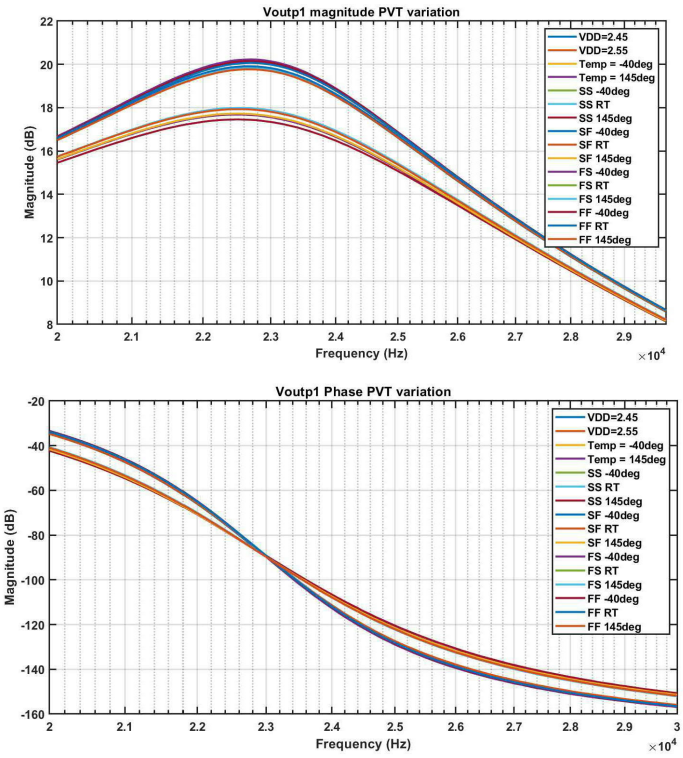

Figure 43: (top to bottom)PVT simulations for magnitude and phase response around Fnom

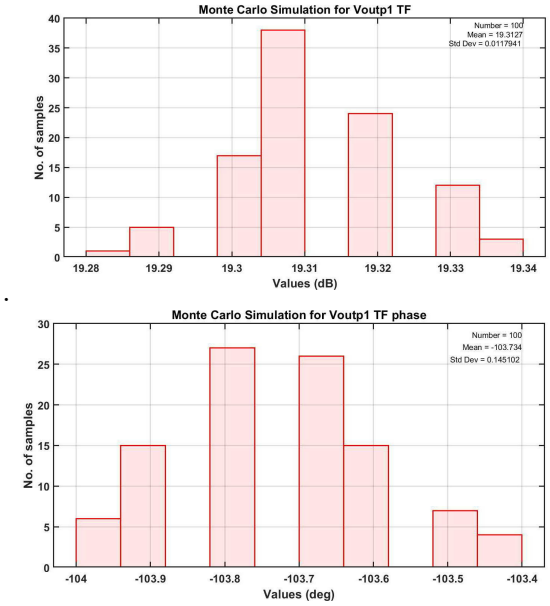

Figure 44: (top to bottom)MC simulations for magnitude and phase variation around Fnom

4.2 Total harmonic distortion

Harmonic distortion of a signal is defined as the ratio of total signal component except the fundamental component to the fundamental signal component. It is the power of the fundamental frequency power compared to the other powers in the frequency spectrum [29]. The harmonic distortion of an ideal pure sine-wave is 0. This section shows the total harmonic distortion of the de-multiplexed single ended output waveform. According to the design requirements total harmonic distortion at nominal frequency should not be greater than 0.3 % when the signal is maximum i.e., 2.125V, because the signal has maximum distortion when it is close to the supply rail. Table 15 shows the PVT simulation results for the THD for all of the output signals while Table 16 shows the Monte-Carlo simulation result i.e the mean value for the total harmonic distortion values in all of the output signals as well as the 5-sigma variation value.

Table 15: PVT Simulations for the total harmonic distortion in percentage

Corner	**Voutp1**	**Voutp2**	**Voutp3**	**Voutp4**	**Voutm1**	**Voutm2**	**Voutm3**	**Voutm4**
Nominal	0.2075	0.2058	0.2069	0.2061	0.2166	0.215	0.215	0.2161
$-40°$	0.2455	0.2425	0.2447	0.2439	0.2532	0.2501	0.2513	0.2521
$145°$	0.1398	0.1357	0.1408	0.1354	0.1511	0.1468	0.1506	0.1478
FF	0.2391	0.2361	0.2374	0.2363	0.2483	0.2460	0.2461	0.2469
FF $-40°$	0.2834	0.2804	0.2825	0.2819	0.2918	0.2895	0.2905	0.2915
FF $125°$	0.1256	0.1189	0.1257	0.1186	0.1385	0.1327	0.1376	0.1335
SS	0.1899	0.190	0.1897	0.190	0.1994	0.1987	0.1975	0.2001
SS $-40°$	0.2236	0.2222	0.2232	0.2231	0.2304	0.2283	0.2288	0.2303
SS $125°$	0.1546	0.1535	0.1553	0.1522	0.1647	0.1633	0.1642	0.1635
SF	0.1957	0.1948	0.1956	0.1942	0.2057	0.2045	0.2043	0.2050
SF $-40°$	0.2231	0.2209	0.2223	0.2220	0.2311	0.2285	0.2291	0.2305
SF $125°$	0.1516	0.1498	0.1534	0.149	0.1628	0.1605	0.163	0.1606
FS	0.2074	0.2057	0.2068	0.2066	0.2158	0.214	0.214	0.2159
FS $-40°$	0.2430	0.2403	0.2417	0.2412	0.250	0.247	0.2477	0.2489
FS $125°$	0.1369	0.1354	0.138	0.1345	0.1474	0.1452	0.1472	0.146
V_{DD} = 2.45V	0.2049	0.2037	0.2052	0.2045	0.2138	0.2127	0.2131	0.2144
V_{DD} = 2.55V	0.2149	0.2126	0.2137	0.2131	0.2236	0.2212	0.2213	0.2226

Table 16: Monte-Carlo Simulations for the total harmonic distortion in percentage

	Voutp1	**Voutp2**	**Voutp3**	**Voutp4**	**Voutm1**	**Voutm2**	**Voutm3**	**Voutm4**
Mean	0.2075	0.2058	0.2069	0.2059	0.2166	0.2151	0.2151	0.2161
5-sigma variation	0.00329	0.00317	0.00351	0.00362	0.00293	0.00283	0.00312	0.00302

4.3 Power Supply Rejection Ratio [30]

Power Supply Rejection Ratio (PSRR) is a factor which determines how effectively a circuit rejects the variations coming from the power supply. It is defined as ratio of the gain of the signal coming at the output from the power supply to the gain of the signal at the output coming from the input. The power supply node for our circuit is the V_{DD} and there are several paths for this signal to travel to the output. If the incoming signal follows the differential path with opposite phase, it would be cancelled because of the differential nature of the circuit. But there could be some signals which because of the path they take are not totally opposite in phase, these signals specially at high frequency can cause poor PSRR. The PSRR was simulated by introducing a signal at the V_{DD} and observing the transfer function at the output and comparing it with the signal gain coming from the input. According to the requirements the PSRR at 100kHZ should be atleast 25dB. PSRR over different process corners is shown in Figure 45. The simulation results for PSRR at 100kHz

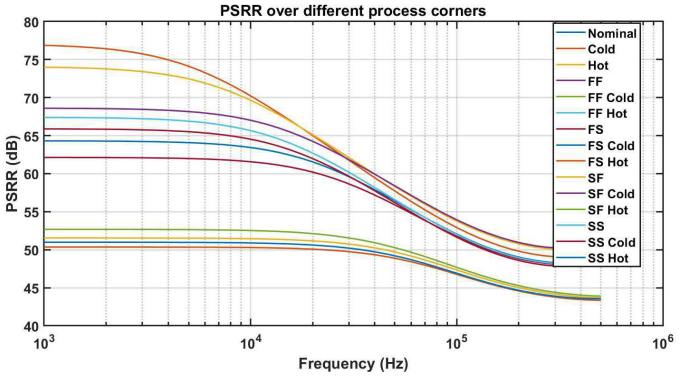

Figure 45: PVT simulation for PSRR

Table 17: PSRR at 100kHz

Corner	PSRR at 100kHz	Corner	PSRR at 100kHz
Nominal	52.95 dB	**Cold**	52.92 dB
Hot	47.34 dB	**FF**	51.99 dB
FF Cold	51.65 dB	**FF Hot**	46.91 dB
SS	53.04 dB	**SS Cold**	54.66 dB
SS Hot	47.78 dB	**SF**	53.76 dB
SF Cold	53.94 dB	**SF Hot**	47.69 dB
FS	51.77 dB	**FS Cold**	52.05 dB
FS Hot	46.77 dB		

under different process corners are compiled in Table 17. The PSRR dependency on mismatch using Monte-Carlo simulation was not analyzed. Based on the good

values for PSRR for nominal and corner simulations, Monte-Carlo simulation results are expected to be within specification also.

4.4 Channel Isolation

For the multiplexed channels, the isolation among them is an important parameter. For the low pass filter, poor channel isolation can affect the accuracy measurement for the gyroscope. Channel isolation is defined by the amount of signal in one channel affecting the signal in the other channels. A channel is considered on when it is transmitting a full scale signal while it is considered off when there is no AC signal and the input of the channels are at AGND DC level. Channel isolation for one channel is measured by keeping only one channel on at a time and keeping other channels closed. Now, the level of signal observed through fourier analysis in other channels in comparison to when all channels were closed is the signal leaking from the on channel. For the requirements given for the design, the channel isolation should be greater than 100dB meaning that the signal leaked from one channel to the other should be atleast 100dB attenuated. Referring to the clock and channel signals, the channels are turned on in the following sequence 2341234... it is observed through the simulations that when a certain channel is transmitting a full scale signal it affects the isolation to of the channel which is to be turned on next according to the switching scheme shown in the previous chapter in Figure 24 , therefore the isolation of the channel which is to transmit next is the most critical. Consider the

Table 18: Channel Crosstalk

Channel	**Channel Isolation level**
pCh1	131.2 dB
pCh3	94.62 dB
pCh4	130.2 dB
mCh1	134.7 dB
mCh3	94.54 dB
mCh4	132.3 dB

case when only channel 2 is transmitting, the channel isolation simulations were performed for the very first time and the signal was attenuated more than 100dB in all the channels except the next channel i.e. channel3 in which the signal level was attenuated by about 85 dB. The first thing that was considered as the root cause was the charge leakage from one integrating capacitor (of channel 2) to the next integrating capacitor (of channel 3), this was investigated by connecting an ideal switch in series with the next channel integration capacitor so that when the switch is turned off the ideal switch provides ideal isolation to the charge transfer, this improved the channel isolation to upto 103 dB attenuation. Another factor affecting the channel isolation realized later in the design process was the mismatch in the operational amplifier design. The initial design of the operational amplifier used the number of fingers to obtain the correct transistor widths but later when the

multiplier factor was used it improved the matching and also the Channel isolation was improved from 85 dB to around 94 dB. There is still room for improving the matching in the operational amplifier design which is believed to improve the channel isolation further. The final channel isolation simulation results, when only channel 2 is transmitting, are summarized in Table 18.

4.5 Noise simualtions

There are two types of noise in an electric circuit, white noise and a thermal noise which is defined for a resistor by the following equation:

$$V_{n-res} = \sqrt{4kTR} \tag{56}$$

where T the temperature in Kelvin. For a switch and capacitor having resistance R and capacitance C respectively, the corner frequency for the thermal noise is given by 1/nRC where n is the number of switches connected with the capacitor. For the sampling frequency of F_S due to the nyquist criterion, the noise at the multiples of F_S is aliased to the base band, therefore the noise F_S is the combination of white noise and aliased noise. Decreasing the on resistance decreases the thermal noise but it increases the white noise and when combined with the aliased noise the total noise comes to the same level therefore in switched capacitor circuits, the noise depends on the value of the minimum capacitor in a circuit, the lower is the capacitance value the higher is the noise factor[25]. For the specified Q-value the values of capacitors in our circuit is fixed but if the minimum capacitance value can be increased this would improve the noise characteristic of the design. According to the design targets the input referred noise level for the design should be at-least $500nV/\sqrt{Hz}$ in the signal band of interest (i.e 23300-23900). The input referred noise curves for different process corners are shown in Figure 46. The noise around Fnom is shown in Figure

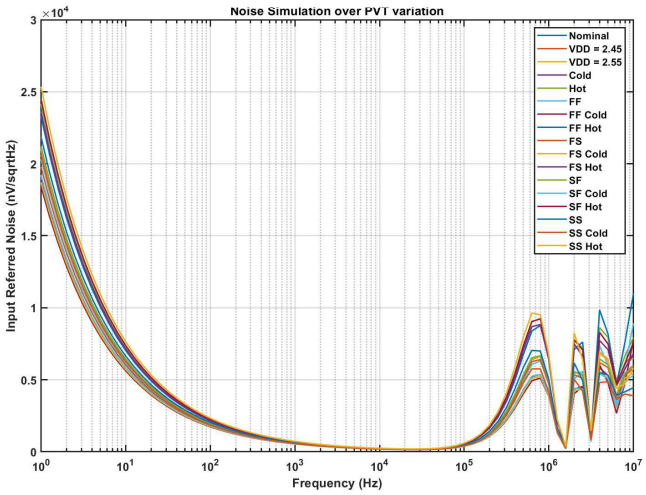

Figure 46: Full Scale input referred noise

47. Table 19 summarizes the PVT and MC simulations results for the input referred noise.

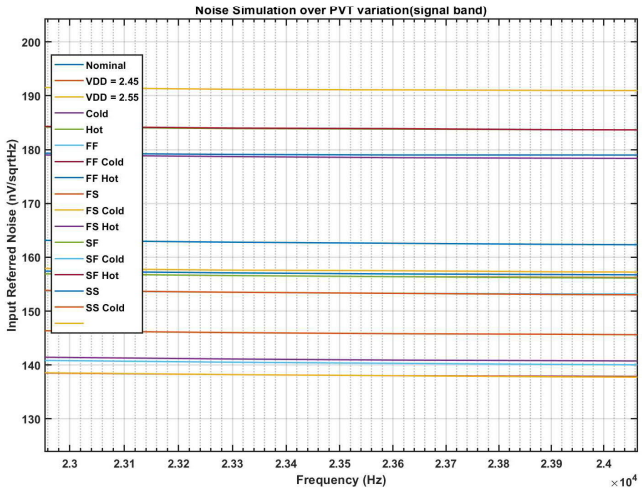

Figure 47: Input referred noise around Fnom

Table 19: Noise simulation results (nV/sqrtHz)

Corner	at 23300 Hz	at 23600 Hz	at 23900 Hz
Nominal	157.1	156.9	156.8
$V_{DD} = 2.45V$	156.6	156.4	156.9
$V_{DD} = 2.55V$	157.6	157.5	157.3
Cold	141.1	141.2	141.3
Hot	183.9	183.8	183.7
FF	153.5	153.3	153.2
FF Cold	138.2	138	137.9
FF Hot	179.1	179	179
SS	162.8	162.6	162.4
SS Cold	146	145.8	145.7
SS Hot	191.2	191.1	191
SF	156.6	156.4	156.2
SF Cold	140.5	140.3	140.1
SF Hot	184	183.9	183.7
FS	153.5	153.3	153.1
FS Cold	138.2	138	137.8
FS Hot	178.7	178.5	178.4
Mean	157.1	156.9	156.79
5-sigma variation	0.21	0.197	0.123

4.6 Current Consumption

The total current consumption for the low pass filter is targeted to be less than 1mA. The main source of current consumption in the design are the operational amplifiers. As the sum of the tail current and the PMOS current sources of the cascode stage of both operational amplifier is 400μA and 440 μA, the total current consumption Table 20 summarizes the MC and PVT simulation results for the current consumption.

Table 20: Current Consumption

Corner	**Current Consumption**
Nominal	844.3 μA
Cold	842.4 μA
Hot	846.3 μA
FF	844 μA
FF Cold	841.7 μA
FF Hot	846.3 μA
SS	845.1 μA
SS Cold	843.4 μA
SS Hot	847 μA
SF	849.2 μA
SF Cold	848.2 μA
SF Hot	850.2 μA
FS	840.6 μA
FS Cold	837.8 μA
FS Hot	843.6 μA
$V_{DD} = 2.45V$	842.8 μA
$V_{DD} = 2.55V$	845.8 μA
MC Mean	844.3 uμA
5-sigma variation	83.15 pA

5 Summary and Conclusion

This thesis presented the transistor level design of the second-order switched-capacitor ladder type low-pass filter with the channel multiplexing. The design was performed using GF 55nm technology. The crux of the thesis was to study the topology in comparison to the already existing equivalent continuous-time design in terms of area, current consumption and noise performance. The layout for the design was out of scope for this work but chapter 2 discusses the area reduction in discrete-time designs in comparison to the continuous time-designs and the significance of the ladder filter topology for this purpose. There were two types of specifications provided for this design, i.e., the requirement and the target. Chapter 3 describes how the design was carried out step by step keeping them in consideration and the final results are shown in Chapter 4. The design was verified to be functional at various process and voltage corners. The key specifications that were defined for this design versus the final values for these parameter of the design are summarized in Table 21. The table also

Table 21: Targets and Requirements versus Results

Parameter	**Specification**	**Result**
PSRR at 100kHz	$\geq$ 25 dB	52.95 dB
THD	$\leq$ 0.3%	0.21%
Channel Isolation	$\geq$ 100 dB	94.5dB
Phase shift at Fnom (target)	$\pm 6.6 degrees$	6.6 degrees
Input Referred Noise (target)	$\leq$ 500nV/$\sqrt{Hz}$	$\leq$ 184nV/$\sqrt{Hz}$
Current Consumption (target)	$\leq$ 1mA	0.844mA

depicts the successful design of the topology meeting most of the specifications. Over the course of this work, various improvements were made to the first version of the functional design which includes the improvement of the matching of the transistors in the Op Amp design as well as the separate design for the Op Amps of the two stages of the filter. This improved the noise level, channel isolation level and the current consumption of the design respectively. The table also shows that the final channel isolation level achieved is not according to the specifications. This parameter was studied further and various parameters (which includes the affect from CMFB SC circuit, transmission gate leakage and the matching of the transistors in the Op Amp design) that could affect the channel isolation were studied by replacing them with ideal designs in the circuit and seeing the affect. The CMFB SC circuit and transmission gate leakage was ruled out but better matching of the op amp transistors improved the results. The further investigation of this deviation as well as the layout and post layout results for the essential parameters are left for future work. Moreover, the clock generator circuit was also studied for this work but due to the complexity and non feasibility of getting these signals from the digital part on ASIC, the subject is left out to be studied as future work.

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