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Reduction of the contact resistance by doping in pentacene few monolayers thin film transistors and self-assembled nanocrystals

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The authors study the contact resistance of gold-pentacene interface by applying the transmission-line method to a few monolayers thick pentacene films in thin film transistor geometry. It was found that tetrafluorotetracyanoquinodimethane (F_4TCNQ) doping reduces the contact resistance by more than a factor of 20. In addition, a significant improvement of the conductance of pentacene nanocrystals self-assembled on 10 nm gap Au nanojunction devices by F_4TCNQ doping is observed. The result demonstrates the importance of doping on the performance of organic electronic devices from 10 nm scale up to 100 μm scale. © *2007 American Institute of Physics*. [DOI: 10.1063/1.2738382]

The charge injection at the metal-organic semiconductor interface is an important arena for the optimization of the performances of organic electronic devices[1] such as an organic thin film transistor (TFT). The injection at the metal-semiconductor interface and the contact resistance can predominate over the channel resistance especially when the size of the device is reduced. It has been reported that doping is effective to reduce the contact resistance.[2,3] Similar doping-induced reduction of the contact resistance is also observed in inorganic semiconductor devices.[4] However, the exact mechanisms are expected to differ since the diffusion length of the electronic transport is in the order of 1 nm and is smaller than in inorganic semiconductors. In fact, organic TFTs can operate even when the channel thickness is decreased to a few monolayers[5,6] (MLs) and when the channel length is in the 10 nm range.[7] In this work, to explore the charge-injection mechanism at the interface between pentacene (PC) and metals, we study the contact resistance of undoped and tetrafluorotetracyanoquinodimethane (F_4TCNQ) doped PC channels in TFT geometry and in self-assembled PC nanocrystals bridging a 10 nm gap.[8] The results demonstrate that the doping by F_4TCNQ improves the device performance significantly.

To measure the contact resistance R_c of PC TFT, we apply the transmission-line method.[9,10] Here, by measuring the total resistance R_{tot} of several TFTs with various channel lengths L and fixed width W, R_c is evaluated from R_{tot} at L equal to zero extrapolated from the relation between R_{tot} and L. For this purpose, four PC TFTs with nominal L's of 20, 50, 75, and 200 μm and with W of 110 μm are simultaneously fabricated (see the inset of Fig. 1) and electrically characterized *in situ*. TFTs are fabricated on a heavily *p*-doped silicon wafer covered by 150 nm thermal oxide. The substrate serves as the gate electrode. First, we pattern five 200 μm square contact pads along one line by photolithography, thermal evaporation, and lift-off. The contact pads consist of a 200-nm-thick Au and a 10-nm-thick Ti sticking layer. Next, we pattern a resist mask opening across the metal pads where the PC film is to be deposited. We adopt a double-layer resist in order to eliminate the parasitic conduction through the PC outside the resist opening. L's are defined by the separations between the contact pads. W is defined by the width of the resist opening.

For the manufacturing of the nanojunction, two Au electrodes separated by an ~10 nm gap are prepared by an angle evaporation of the metal masked by a sharp and insulating vertical step.[8] The gap size can be controlled by adjusting the difference between the step height and the deposited metal thickness [Fig. 3(a)].

PC is deposited at a rate of 0.04–0.06 ML/min at a pressure of $\sim 10^{-8}$ mbar. The rate is monitored by a water-cooled quartz microbalance that was calibrated by thickness measurements using a tapping-mode atomic-force microscope. The *in situ* electrical characterization of the devices is performed via electrical feedthroughs attached to the vacuum chamber. For the TFTs, a total of 6–7 MLs of PC are deposited in several steps. TFTs are also characterized at each

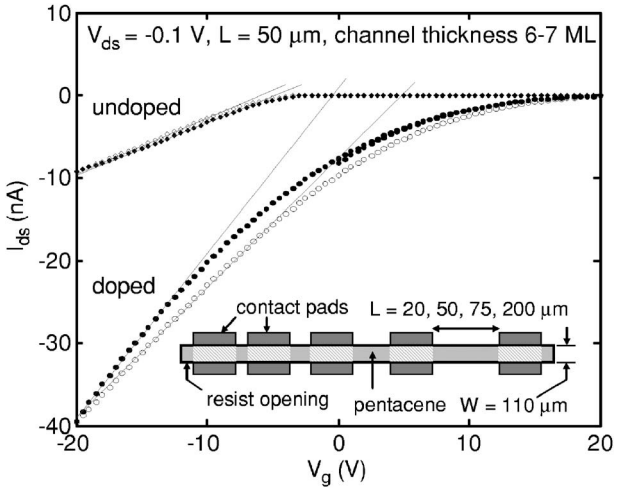

FIG. 1. Transfer characteristics of pentacene thin film transistors with 6–7-MLs-thick channels. The results of an undoped and a F_4TCNQ doped device having 50 μm channel lengths are shown. V_{ds} equal to −0.1 V is applied while cyclically varying the gate bias V_g between ±20 V. The filled (empty) symbols indicate the result observed when the gate bias V_g is increased (decreased). The lines are linear fit of the characteristics at high negative V_g for both scanning directions. The inset shows the device geometry: four devices with channel lengths of 20, 50, 75, and 200 μm are fabricated at the same time by depositing the pentacene film through the resist opening.

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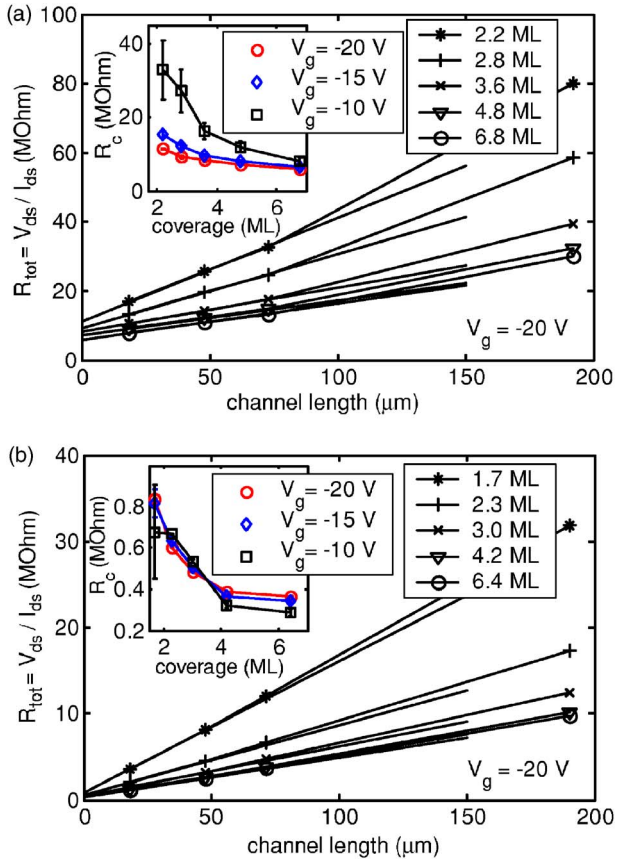

FIG. 2. (Color online) Total resistance R_{tot} vs channel length L for the undoped (a) and F_4TCNQ doped PC TFTs (b) measured at V_g=−20 V for various channel thicknesses. The relation between the contact resistance R_c and the channel thickness for both cases is shown in the insets for three gate biases. R_c is evaluated by extrapolating the relation R_{tot} vs L to L=0. The error bars indicate the difference between the values determined from the up and down scans of V_g.

intermediate film thicknesses T. The 10 nm channel device is fabricated by depositing a total of ~6 MLs PC on the Au nanojunctions. We found that minimizing the air exposure of the sample surface prior to the PC deposition is essential to fabricate working devices. Therefore, the nanojunction device is transferred to the PC deposition chamber within 10 min after Au electrode deposition. For TFT devices, the sample is cleaned by an oxygen plasma for 30 s and is transferred to the PC deposition chamber within 15 min.

The doped PC TFTs are fabricated by depositing 1.5±0.5% F_4TCNQ mixture of PC. The doping content was calibrated from the hole concentration p divided by dopant activation ratio η equal to 0.1±0.02. p is given by $C_{ox}\Delta V_{th}/e$, where C_{ox} is the oxide capacitance equal to 2.4×10^{-8} F cm^{-2}, and ΔV_{th} is the shift of the threshold gate bias voltage of the doped PC TFT from that of the undoped PC device obtained from the comparison of the transfer characteristics (Fig. 1). η is evaluated in a separate measurement.[11] We confirm from the transfer characteristics that the on/off ratio of the drain-source current is above 10^3 at this doping concentration.[12] For the doped PC nanojunction, F_4TCNQ is coevaporated with PC at a 3% ratio using two separate crucibles.

Figure 2(a) shows the relation between R_{tot} and L of undoped PC TFTs for different channel thicknesses h at V_g equal to −20 V and at a fixed drain-source voltage V_{ds} equal to −0.1 V. We verified that the relation between V_{ds} and I_{ds} is linear for V_{ds} equal to −0.1 V. We found that R_{tot} increases proportionally to L below 80 μm. Therefore, using the data in this L range, we evaluate R_c. The result is summarized in the inset of Fig. 2(a) for three gate bias voltages. The error bars indicate the difference of R_c due to the hysteresis of the drain current between up and down sweeps of V_g. The decrease of R_c with the increase of h is attributed to the increased uniformity of the PC coverage at the edge of Au contacts. This is confirmed by scanning electron microscopy (SEM) observation of the devices with different PC coverages. We note that at fixed h, R_c decreases with increasing negative V_g. This indicates that the barrier lowering by the the gate electric field at the contact is essential for the efficient injection of charges to the TFT channel, in agreement with Ref. 13. We found that R_c reaches a minimum value of 7 MΩ for the thickest channel device and with V_g equal to −20 V. This value is eight times higher than the reported values.[9,10] We ascribe this result to a factor of 10 thinner h's of our devices. We note that this R_c is about 80% of the total resistance at L equal to 20 μm. The observation underlines the importance of R_c on the organic TFT performance.

Next we discuss the results of F_4TCNQ doped PC TFTs [Fig. 2(b)]. In the inset we summarize R_c evaluated in the way described above. We found that the F_4TCNQ doping significantly decreases R_c; the smallest R_c of 0.3 MΩ is observed for the device with the thickest h at V_g equal to −10 V. This value is a factor of 20 smaller than in the undoped case. The resulting R_c is 30% of R_{tot} for the 20 μm channel, showing the importance of doping to improve the performance of PC TFTs.[14] These are ascribed to the barrier lowering at the Au-PC interface by the Coulomb potential of the ionized dopants. We note that, in contrast to the undoped TFTs, the R_c of the F_4TCNQ doped TFTs depends on V_g only weakly. This indicates that the doping significantly modifies the local potential profile at the interface, irrespectively to V_g. However, the ionized dopants hardly affects the mobility μ of the channel; we evaluate μ of undoped and doped PC TFTs from the transfer characteristics after eliminating the influence of R_c. We found that doped and undoped TFTs have the same μ equal to 0.35±0.05 cm^2/(V s).

A detailed inspection of the data indicates a slight increase of R_c for V_g below −10 V. This may be related to a decrease of the density of states (DOS) of the PC channel at the Fermi energy as a consequence of an upward shift of PC states with V_g relative to the electronic states of the metal. Such a nonmonotonical DOS in doped organic semiconductor films has been observed recently.[15] On the other hand, the holes in the PC channel can partially screen the impurity potential. This effect counteracts the barrier lowering effect and consequently the width of the interface barrier and R_c increase at large $|V_g|$. However, the screening property of the holes, limited by the hoppinglike conduction in organic semiconductors, has not been clarified yet.

Finally, we discuss two-terminal I-V of 10 nm channel PC. We found that PC molecules deposited on a 10 nm gap nanojunction self-assemble as flake like islands. These nanocrystals bridge the 10 nm gap electrically and enable electrical transport measurements [Fig. 3(a)].[8] From the SEM, we found that the width of the channel is ~0.1 μm in total. In Fig. 3 we also show typical I-V of undoped and F_4TCNQ doped PC nanocrystals measured *in situ* [Fig. 3(b)] and in ambient air [Fig. 3(c)]. The undoped PC shows a highly insulating, back-to-back Schottky behavior. When 3% of

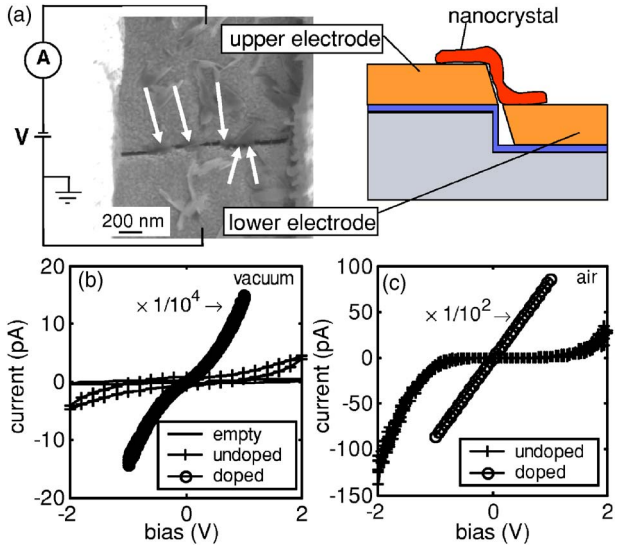

FIG. 3. (Color online) (a) SEM image of F_4TCNQ doped self-assembled PC nanocrystals deposited on a 10 nm gap Au nanojunction. The arrows indicate the nanocrystals that bridge the gap. A schematic cross section of the device along the vertical direction is also shown (right). In the measurements, a positive bias is applied to the upper electrode. The lower panel shows *I-V* of undoped and doped PC nanocrystals measured in vacuum (b) and in air (c). In (b), *I-V* of the nanojunction before the nanocrystal deposition denoted as empty is also shown.

F_4TCNQ is doped to the PC, the rectifying *I-V* is converted to a nearly linear characteristic. At the same time, the conductance increased by factors of 10^5 and 10^3, respectively, for the *in situ* and for the air-exposed case. The results indicate that the co-deposited F4TCNQ molecules intermix with PC. In contrast, the deposition of a uniform layer of F4TCNQ on top of preformed pentacene nanocrystals did not reveal any of the described effects. These are consistent to the observations that, at zero V_g, the undoped TFTs are off while the F_4TCNQ doped TFTs are on, as shown in Fig. 1. R_c measurements of PC in TFT geometry indicate that, when the channel length is below 10 μm, R_c is more than 80% of R_{tot}. Therefore, the improvement of the conductance of the 10 nm channel PC is ascribed to the decrease of the contact resistance between Au electrodes of the nanojunction and PC nanocrystals. In fact, the zero-bias resistance of PC nanocrystals equal to ~60 MΩ is of the same order of magnitude as the estimated contact resistance equal to 10 MΩ of a doped PC TFT with similar channel width of ~0.1 μm [see Fig. 3(a)]. The increased current of the undoped PC in air is likely due to the barrier lowering by hole doping induced by the combination of moisture and/or oxygen with light.[16] However, this unintentional doping process is not sufficient to achieve an ohmic contact.

In conclusion, we found that the contact resistance between gold and pentacene is decreased by a factor of ~20 by doping with F_4TCNQ in TFTs, while converting the initially rectifying *I-V* of self-assembled nanocrystals to highly conducting and approximately linear characteristics. This demonstrates the importance of the doping to improve the organic TFT performance for 10 nm to ~100 μm channel length. The V_g and the channel thickness dependence of the R_c indicate a significant influence of the F_4TCNQ molecules on the charge-injection processes at the PC-Au interface. To elucidate the microscopic mechanism, further research including the temperature dependence of the transport characteristics is underway.

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