UNIVERSITÀ DEGLI STUDI DI NAPOLI
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PH.D. THESIS

IN

INFORMATION TECHNOLOGY AND ELECTRICAL ENGINEERING

IMPEDANCE SPECTROSCOPY FOR INTERFACE CHARACTERIZATION IN SEMICONDUCTOR DEVICES

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List of Abbreviations

AC	Alternate current
Cd	Cadmium
CdTe	Cadmium Telluride
C-f	Capacitance-frequency
CIGS	Copper indium gallium selenide
C-V	Capacitance-Voltage
DC	Direct current
DUT	Device under test
ETL	Electron Transport Layer
GaAs	Gallium arsenide
GaN	Gallium nitride
G	Graphene
HTL	Hole Transport Layer
IS	Impedance Spectroscopy
I-V	Current-Voltage
MOS	Metal-Oxide-Semiconductor
MS	Metal-Semiconductor
PSC	Perovskite solar cell
RC	Resistance-Capacitance
SBD	Schottky barrier diode
Si	Silicon
SiC	Silicon carbide
SiO_2	Silicon dioxide
WF	Work function

Introduction

1.1 Motivations

The hardest challenge in semiconductor device characterization consists in the understanding of the device internal physics and working principles by accessing only external connections. Depending on the specific type of the considered device, several and different physical parameters can be investigated. Many of them depend on the interfaces between different materials, which are the preferential location of lattice defects. The double objective of *(i)* isolating the contribution of each interface from the overall electrical behavior and *(ii)* detecting and characterizing interface defects will be addressed in this work.
The main focus will be on solar cells, with a particular hint on Schottky based solar cells. A Schottky interface can be characterized by the barrier height and the metal work function, which are both associated to the capacitance exhibited by the junction. Separating the junction capacitance from the externally measurable impedance is of former importance to correctly calculate Schottky barrier properties. Nevertheless, the capacitance is influenced by lattice defects. From here the necessity of detecting interface defects and, then, decoupling the contribution of the different interfaces existing in the device. These aims have always been a great challenge, that is why numerous techniques can be found in the literature. Among them, impedance spectroscopy is highly reliable and effective, giving both detailed information about microscopic mechanisms occurring at interfaces, and macroscopic information for lumped circuit representation. This analysis is usually performed in the reverse bias operating region since

some parameters, such as barrier height and metal work function can be extracted in this region. Howbeit, many significant information can be achieved by exploring the forward bias region, where solar cells performance is usually evaluated, i.e., between short-circuit and open-circuit conditions. Even if the analysis in forward bias region allows the investigation of a variety of phenomena, such as carrier injection phenomena, the outcomes are sometimes quite critical to interpret.
The study of interface properties by means of impedance spectroscopy and C-V analysis, extended to the forward bias operating region, is the main topic of this thesis.

1.2 Interface characterization techniques

Interface physics influence the overall macroscopic behavior of electronic devices. The importance of separating the contribution corresponding to each interface is due to the fact that each of them gives a contribution, as discussed previously. Unfortunately, interfaces are inside the device and cannot be accessed from the device terminals. The challenge is to extract interface contributions by means of non-destructive and non-invasive methods, allowing the understanding of the underlying physics.
The most widely exploited characterization techniques rely on the measurements of current, charge and capacitance. Current techniques [5]-[6] are based on the calculation of the area underlying the current versus time curve, i.e., the charge emitted by defects/traps. These measurements are performed as a function of the temperature because of the temperature dependence of defects properties. Capacitance techniques, or more in general, impedance/admittance measurements, are particularly appropriate for interface properties characterization. If a small voltage is applied to the DUT, the variation of charge determines a small signal capacitance which is sensitive to carrier capture and emission processes caused by defect/trap states. Several variants have been employed, such as

capacitance versus voltage measurements, impedance spectroscopy, deep level transient spectroscopy, photocapacitance measurements. Capacitance-voltage profiling exploits the fact that in a p-n or M-S junction the reverse bias space region width is strictly related to the applied voltage. This technique has been also employed in MOS structures, allowing the extraction of substrate doping concentration and gate oxide thickness [7]-[9]. The effect of oxide traps on MOS capacitance has also been studied [10]-[12]. The comparison between high and low frequency capacitance at the same gate voltage allows the extraction of traps distribution at the Si/SiO_2 interface [13]-[16]. This is because traps cannot follow high frequency variation, hence they do not influence high frequency capacitance. On the other hand, if the frequency is low enough that all the traps can respond to the stimulus, the low frequency capacitance incorporates the contribution of all existing traps. Traps distribution is also extracted using capacitance technique for MOSFET structures [18]-[21].

C-V measurements are extensively used in devices embedding interfaces with a very high density of traps, as it is the case for the SiO_2/SiC interface in SiC MOSFETs [19]-[21]. In Schottky structures, the capacitance analysis has also been used, providing detailed information about the metal properties and the band bending existing at the Schottky interface [22]-[26]. Schottky barrier diodes, SBDs, working principle is based on the barrier height at the MS interface [4], Φ_B. Almost all studies investigate Schottky devices capacitance uniquely in reverse bias, that only allows the extraction of Φ_B and WF [31]-[34]. Considering exclusively the reverse bias range of the capacitance narrows the set of information and it doesn't allow information about defects and their properties. At this purpose, forward bias capacitance is a valuable source of information [34]. Moreover, capacitance-voltage in the forward bias region highlights that the SBD capacitance differs from that expected at a first order analysis [35]. Many experiments show that the capacitance is not monotonically increasing, with a peak at low forward voltage and no exhaustive explanations can be found in the literature, even though some papers exist. In [36], the

interface state density of a Schottky diode is extracted using forward capacitance, while in [37] the same procedure is employed on organic Schottky diodes. Sometimes, an additional peak is seen at higher forward bias [38]-[39]. In the following of this thesis it will be shown that such additional peaks give significant information about the spatial uniformity of deposition processes.

1.3 Thesis outline

The thesis is organized as follows.
Chapter 2 presents the impedance spectroscopy technique and its applications. In this chapter, the impedance data representation in the form of Nyquist plots is also shown. From such plots it is possible to extract electrical equivalent circuit with lumped elements. An automatic procedure is presented which is suited for multilayer structures and has the advantage to combine information deriving from impedance spectroscopy and C-V experimental data. C-V curves are then exploited, both in reverse and forward bias operation region.

The impedance spectroscopy technique and the capacitance analysis have been applied in different fields. The subsequent chapters show the results obtained for different applications. In **Chapter 3** the application of the technique on power devices is presented. More in detail, SiC MOSFETs are characterized in terms of C-V curves and numerical model. A TCAD model is realized using the commercial environment Sentaurus TCAD Workbench. The model is calibrated aligning numerical and experimental C-V curves obtained in different configuration. **Chapter 4** dwells on achievements obtained on perovskite solar cells. On such devices, Nyquist plots are presented, and electrical equivalent circuit is extracted. By looking the impedance data in terms of equivalent circuit it is possible to easily extract some physical parameters, thus characterizing and comparing different perovskite solar cells technologies. **Chapter 5** presents results on Schottky solar cells. The

impedance data collected on Graphene-Silicon solar cells with different contact technologies allowed solar cells characterization. More in detail, by applying the automatic procedure to collected impedance data it is possible to separate the contact contribution from the overall impedance, selecting the specific contact technology most suitable for the analyzed solar cell. Graphene-silicon solar cells are also studied using capacitance curves. The analysis of such curves in forward bias highlighted the existence of multiple peaks. This circumstance is associated to interface spatial non-uniformity. The explanation of multiple capacitance peaks is given through extensive numerical and experimental data. A TCAD model is presented in this chapter. This model is calibrated with experimental data, extracting interface properties. Conclusions are then drawn.

Chapter 2: Impedance spectroscopy

The aim of this Chapter is to discuss impedance spectroscopy (IS), its representation in the form of Nyquist plots and its application. Section 2.1 describes the fundamentals of the characterization technique and the Nyquist plots obtained from impedance data. These plots can be interpreted in terms of an electrical equivalent circuit. This relation is described starting with simple RC pair circuit. The features of more complex configurations are then shown in detail. An automatic procedure developed to extract the equivalent circuit from impedance spectroscopy data is also reported. The presented procedure has the advantage to cross the information deriving from impedance spectroscopy data, represented in the form of Nyquist plot, with C-V experimental data, adding physical constraints to the extracting procedure.

In Section 2.2, the capacitance extracted from impedance measurements is analyzed; in particular, C-V curves are analyzed in reverse bias region and in forward bias region. The importance of forward bias capacitance in giving information about interface defects is pointed out. The influence of interface defects properties on capacitance profiles is also discussed.

2.1 Impedance spectroscopy technique

Performance of solar cells are usually estimated by measuring conversion efficiency, series and shunt resistances, built-in voltage and so on. These parameters are commonly measured using DC techniques. DC current-voltage techniques allows the measurement of the mentioned parameters and their study with varying reverse and forward bias or temperature, in both illumination and dark condition. However, these techniques cannot detect some important parameters such as interface quality and transition capacitance. It is necessary to adopt AC techniques to identify those parameters. Impedance spectroscopy is one of the most assessed frequency domain technique for decoupling the different physical processes existing at the various interfaces in the

solar cell. This electrical characterization is a non-destructive technique that can be used in dark or in illumination condition, if the considered device is photosensitive.
Impedance spectroscopy is performed by applying to the device under test a DC bias with a small AC voltage perturbation superimposed. The DC bias determines the stationary condition while by varying the frequency of the AC signal the perturbation is varied. Thus, this method permits the complete device characterization in the established working condition by differentiating the existing physical phenomena with different time constants. This means that different physical processes taking place at different frequencies can be identified using IS analysis. By performing and analyzing a single measurement, it is possible to gain knowledge on multiple physical phenomena. At this aim, a detailed analysis of the impedance spectroscopy data is needed. This analysis can be carried out by means of an equivalent electrical model allowing the extraction of the desired physical parameters and the correlation of impedance data with physical mechanisms.

Impedance spectroscopy has been adopted as characterization technique in various application fields. There are two main types of impedance spectroscopy: electrochemical impedance spectroscopy (EIS) and everything else. The EIS addresses all the measurements and analysis in all the material where ionic conduction predominates, such as solid and liquid electrolytes. In the electrochemical systems, IS has been applied to Dye sensitized solar cells (DSCs) [40] to study electronic and ionic processes. In this application, high frequency behavior of electrochemical impedance spectroscopy data is associated to charge transfer at front electrode while intermediate/low frequency region is attributed to electron transport in the region of the mesoscopic semiconductor oxide film and at the back surface. Electrochemical IS is a steady-state technique very suited to investigate DSCs as it allows the characterization of electron transport process, back reaction, and charge transfer. This technique also unravels the aging phenomena, giving information on the reason beside them.

Another electrochemical application of IS concerns the organic solar cells [41]. In this application the organic solar cell capacitance is studied. It has been stated that if a remarkable displacement exists in the capacitance between dark and under illumination condition, this is ascribable to a band displacement under illumination condition. This

result has been interpreted with the existence of surface states, limiting the performance of the solar cells.

Also, batteries and solid-liquid interfaces have been studied using impedance spectroscopy. In batteries [42], EIS results allow the identification of the kinetics of Li transport in Lithium titanium oxide (LTO) as well as in the solid-electrolyte interphase. Considering EIS data, it is possible to extract some fundamental parameters for battery characterization such as charge transfer resistance, intercalation capacitance and chemical diffusion coefficient, showing how charge transport is affected by biphasic behavior of the active material chosen. Electrochemical IS has been applied also to ionic liquids in solid-liquid interfaces [43] in order to have a qualitative evaluation of capacitance of these systems and extract electrochemical properties, such as electrolyte resistance.

Even if in literature various electrochemical applications are reported, there is still scarcity of works related to other category of materials. These materials can be classified as dielectric material where electronic conduction is the dominating conduction mechanism, such as solid-state devices.

In [44], CdTe solar cells are characterized by means of impedance spectroscopy under illumination condition. Impedance data are always analyzed in terms of equivalent electrical circuit. Other types of solar cells have been studied using this AC method too, such as GaAs/Ge solar cells. The analysis of impedance data of these cells, both in illumination and dark conditions [45], shows the increase of capacitance and the decrease of resistance under illumination compared to dark condition. Similar study has been performed also on CIGS solar cells [46], obtaining some important parameters, such as minority carrier lifetime and back contact resistance. The properties of *pin* silicon solar cells have been investigated using the IS technique[47]. These data allow the estimation of different layers properties independently, using an equivalent circuit model suited to explain the role of the different solar cell components. IS developed most for silicon based solar cells because of three main factors. The first one is because silicon solar cells are the conventional solar cells and new developed solar cells performance are always compared to silicon solar cells as reference. The second reason is related to the high stability of this type of solar cells together with their low cost and high performance. The last reason

concerns the material itself. Silicon has a homogenous property, without any grain boundary in its lattice network. In literature various impedance model have been proposed for silicon solar cells characterization. These mathematical models have been based on the experimental impedance data obtained. Knowing the solar cell structure make possible to choose the most suited model for the device under test. Selecting the proper model is the sometimes difficult and non-immediate. The conventional procedure relies on the study of the recombination and resistive losses taking place in the solar cells. If from one side this discussion can allow the decoupling of the different physical processes and the analysis of relaxation time of the solar cells, on the other hand it requires a lot of theoretical analysis to be carried out. In this thesis, the model chosen for the automatic procedure extraction is immediate and intuitive. The model considered assumes that each interface existing in the device can be electrically described as a RC parallel pair. This means that a device embedding *n* interface can be modelled as the series of the *n* RC parallel pairs.This can be considered acceptable because this is a one-dimensional problem and no relevant lateral interactions exist, since it has been assumed that all the important phenomena are taking place in the vertical dimension of the device.

2.1.1 Nyquist representation

Impedance data collected by means of impedance spectroscopy can be visualized in terms of Nyquist plots. In these graphs, the x-axis shows the real part of the impedance, Z_{RE}, while the imaginary part of the impedance, Z_{IM}, is depicted on the y-axis, as shown in Figure 2.1. Each reported curve has been obtained for a certain DC bias, while each point on the curve has been acquired for a certain AC voltage frequency.

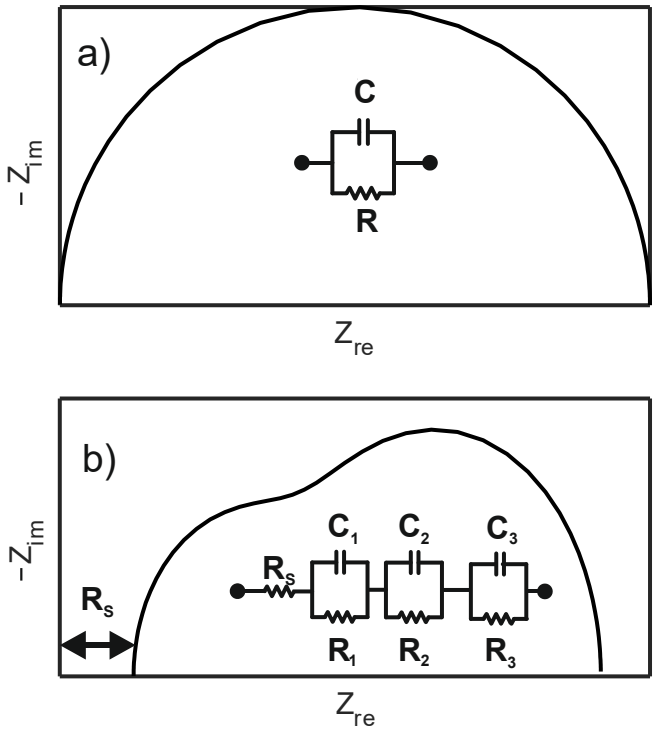


Figure 2.1 *Nyquist plots (a) corresponding to a single RC pair or (b) to a three RC pairs with a series resistance.*

By visual inspection, it is possible to quickly detect some circuit characteristics and non-idealities. It is well known that, if a single RC network is considered, the Nyquist plot is a semi-circular locus of points (see Figure 2.1a). In this case the total impedance is:

$$Z_{TOT} = Z_{RE} + Z_{IM} = \frac{R(1 - j\omega RC)}{1 + \omega^2 R^2 C^2} \tag{2.1}$$

If multiple RC networks are considered, the analysis becomes more complex, as well as the associated Nyquist plot, as reported in Figure 2.1b. In the case of a circuit with a series resistance, R_S, and *n* parallel RC pairs in series, the total impedance can be always defined as the sum of Z_{RE} and Z_{IM} contributions, defined as:

$$Z_{RE} = R_S + \sum_{i=1}^{n} \frac{R_i}{1 + \omega^2 R_i^2 C_i^2} \tag{2.2}$$

$$Z_{IM} = j\omega \sum_{i=1}^{n} \frac{R_i C_i}{1 + \omega^2 R_i^2 C_i^2} \tag{2.3}$$

In order to fully exploits this method advantages, Nyquist plots can be reconducted to an equivalent circuit configuration where each element corresponds to a physical parameter. Typically, the more the Nyquist plot shape differs from the semi-circular shape, the more the total impedance of a sample cannot be due to a single RC network. Complex Nyquist plots are very common specially if we think that each interface in a device can be modelled with a single RC circuit. As preannounced, the extraction procedure presented in following Section models the total impedance of the structure as a series of parallel RC networks plus a series resistance. The knowledge of the physical structure of the device can give an immediate feedback on the suitable number of RC pairs needed in the equivalent circuit schematic. On the other hand, there's no guarantee that each interface gives a significant contribution to the total impedance in the chosen range of frequency. Moreover, the extracted RC parameters are not constant with the DC bias voltage, since they describe voltage dependent physical mechanisms. This means that the extraction procedure has to be carried out at all DC biases at which IS has been performed. Results consistency is the requirement to develop an extraction procedure with physical meaning.

2.1.2 Automatic procedure for equivalent circuit extraction

The developed automatic procedure allows the extraction of equivalent electrical configuration from impedance spectra. The first aspect to investigate while studying a Nyquist plot is the number of RC pairs involved. The minimum number of RC pairs in the equivalent circuit is established to one or two RC networks by checking the Nyquist plot aspect ratio, defined as the maximum of Z_{RE} divided by

the maximum of Z_{IM}. Considering that the aspect ratio of a semi-circular Nyquist plot is 2, the minimum number of RC pairs is set to one if the aspect ratio is nearly 2, it is set to two otherwise. The maximum number of RC pairs is here set to five, suitable for the most physical structures of interest.

The series resistance, R_S, is evaluated according to (2.2), by considering that if the angular frequency meets the condition $\omega >> 1/(R^2C^2)$ the value of Z_{RE} is exactly R_S, which corresponds to the minimum value of Z_{RE}.

The proposed procedure performs a least-squares fit between the impedance experimental data and the impedance evaluated from the equivalent circuit. This step is performed simultaneously for different circuit configurations (i.e. the circuit schematic with all allowed number of RC pairs). Hence an initial guess for RC parameters involved is needed for each equivalent circuit configuration. To this purpose, initial values for capacitances, C_i, are calculated by evaluating the mean value of the capacitance in the experimental C-f data:

$$C_i = \frac{1}{n\Delta F}\int C(f)df \tag{2.3}$$

where $\Delta F = (f_{max} - f_{min})$ is the considered frequency range and $i = 1, .., n$.

For what it concerns resistance initial guess, R_i, the main constraint is that the sum of all resistances of RC pairs existing in the equivalent circuit must be equal to the diameter, D, of Nyquist plot, as follows

$$\sum_{i=1}^{n} R_i = D \tag{2.4}$$

where D is defined as

$$D = Z_{RE}(\omega_{max}) - Z_{RE}(\omega_{min}) \tag{2.5}$$

with $\omega_{max} = 2\pi f_{max}$ and $\omega_{min} = 2\pi f_{min}$.

Moreover, resistances are evenly spaced by a constant value Δ, according to the following recursive formulation

$$R_1 = \Delta$$
$$R_i = R_{i-1} + \Delta \tag{2.6}$$

By applying (2.6) to (2.4), Δ can be expressed as

$$\Delta = \frac{2D}{n(n+1)} \tag{2.7}$$

where *n* is the number of the RC pairs considered.

This procedure is performed for each DC bias and it is fully automated, thus avoiding visual inspection of experimental Nyquist plots.

A double step approach is adopted to precisely extract equivalent circuit parameters. A first least-squares fit is performed on the real part of the impedance, returning a second guess for the RC parameters involved. Intermediate results are provided as initial values to a second least squares fit on the imaginary part of the impedance. As mentioned before, the procedure extracts RC pairs for all the circuit configurations. If it could be found a unique circuit configuration providing the minimum mean relative error (MRE) with respect to experimental data for all available V_{DC} values, then this is the selected configuration. Otherwise, the two configurations giving the lower mean MRE in the V_{DC} range are considered, subsequently the behavior of both equivalent circuit configurations is compared to the behavior of the experimental C−V curves. Finally, the circuit configuration providing the minimum mean relative error with respect to experimental C-V data is selected.

It is important to notice that the experimental C−V curve is related to the overall capacitance of the measured structure. This means that to compare the experimental C−V curve to the equivalent circuit behavior, an equivalent total capacitance, C_{eq}, has to be introduced as

$$C_{eq} = \frac{Y_{IM}}{\omega} \tag{2.8}$$

where Y_{IM} is the imaginary part of the total equivalent circuit admittance.

Since C−V curves are function of the frequency and C-f curves are function of DC bias, the proposed procedure allows to cross information on the DC bias and frequency.

The proposed procedure has been tested on numerical and experimental data. The test on numerical data is included in this Section, while the experimental data results are shown in the application Sections. The total impedance of the schematic in Figure 2.2 has been calculated using Spice commercial circuit simulation environment. The number of RC networks in the equivalent circuit is returned from the procedure presented above, without giving any constraint.

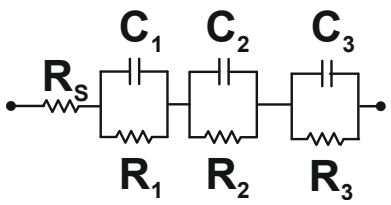


Figure 2.2 *Schematic of the numerically analysed circuit.*

Extracted results are presented in Figure 2.3 in terms of Nyquist plot along with input data, showing a perfect match between the curves. Actual and extracted RC network values are proposed in Table1, for comparison. As can be seen, R_1, R_2, C_1, C_2 and R_S coincides, while on R_3 and C_3 there is a small error. In the third column of Table1, values coming from mere least squares fit on the complex impedance are reported. This fit has been performed by assigning the value of the series resistance and the number of RC pairs, which would be not known in real experimental data; the initial values for all other resistances are set equal to D divided by N. For what concerns capacitances, initial values have been assigned in the order of magnitude of the values set in the circuit of Figure. 2.2. It has to be noticed that these steps should be performed for each DC bias and that the number of RC pairs is not available as well as the order of magnitude of all the capacitance. Even though much more information than those

actually available have been provided, the pure analytic fit extracts values, for both R and C, which are very far from the targets.

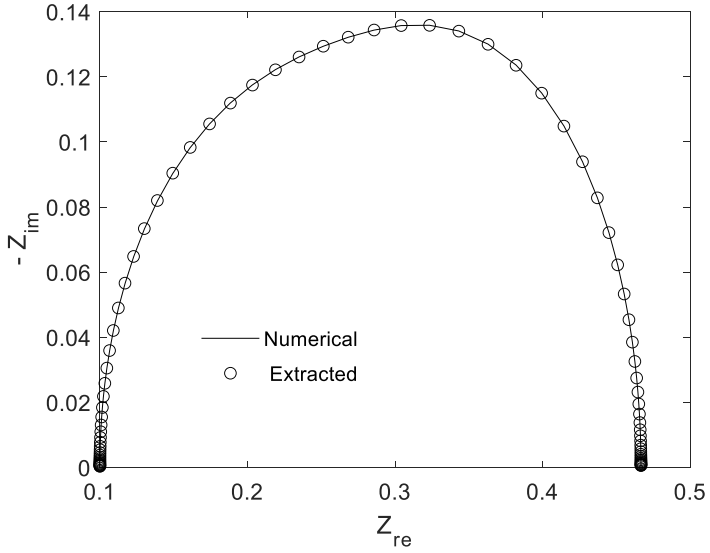


Figure 2.3. *Nyquist plots comparison of curves originating from schematic of Figure 2.2, and from the extracted equivalent circuit through the proposed procedure.*

TABLE I.

Electrical parameter	***Numerical***	***Procedure***	***Fit***
R_1 [Ω]	0.20	0.20	0.12
R_2 [Ω]	0.10	0.10	0.12
R_3 [Ω]	0.06	0.07	0.12
C_1 [mF]	1.00	1.00	9.00
C_2 [mF]	2.00	2.00	9.00
C_3 [mF]	$6.67 \cdot 10^{-1}$	$6.26 \cdot 10^{-1}$	0.1
R_S [Ω]	0.10	0.10	0.10

2.2 Capacitance – voltage curves

This Section offers a detailed overview of the capacitance behavior with a varying DC voltage applied. These curves are obtained from IS when AC small signal frequency is fixed, and DC bias is swept. It is important to notice that these curves are generally analyzed only in the reverse bias region although the forward bias operating region can unravel some junction properties.

2.2.1 Reverse bias region

In Schottky diodes, the reverse bias capacitance [48]:

$$C = \sqrt{\frac{q\epsilon_S N_D}{2(V_{bi} + V - V_T)}} \tag{2.10}$$

where $q=1.6\cdot10^{-19}$ C is the electron charge, ε_S is the silicon dielectric constant, V_{bi} is the built-in voltage, V_T is the thermal voltage and N_D is the substrate donor doping density.

It is of common opinion that capacitance vs voltage curves can give an insight into the device physics, especially if we consider MS interface. It is possible to extract from these curves the built-in voltage of the junction, according to [48]:

$$\frac{1}{C^2} = \frac{2}{(2\epsilon_S N_D)}(V_{bi} - V) \tag{2.11}$$

and the barrier height as:

$$\phi_B = V_{bi} + \frac{kT}{q}\ln\left(\frac{N_C}{N_D}\right) \tag{2.12}$$

From the barrier height, it is possible to calculate the metal work function as the sum of barrier height and semiconductor electron affinity, χ:

$$WF = \phi_B + \chi \tag{2.13}$$

Generally, capacitance-voltage curves are observed only in reverse bias, where (2.11) -(2.13) strictly holds.

2.2.2 Forward bias region

The forward capacitance model of a single junction is discussed in Subsection A, where it is also considered the influence of interface defects. The case of non-uniform interface properties is presented in Subsection B.

A. Single junction

In general, the capacitance across two terminals of an electronic device can be obtained by impedance measurements performed by means of an impedance analyser. To interpret experimental results, a physical model describing the specific device must be adopted. Since the global impedance cannot be easily attributed to physical model parameters, a proper extraction procedure must be implemented.

Consider, for instance, forward capacitance measurements performed on a diode which embeds a single junction.

For a given DC bias, the instrument forces a small AC voltage at the terminals and measures the flowing current. As result, the device admittance *Y* is provided as output [49], expressed as:

$$Y = G_P + jB \tag{2.14}$$

where the real part, G_P, is the conductance and the imaginary part, B, is the susceptance.

In other words, the DUT is considered equivalent, in terms of impedance, to a simple RC pair as depicted in Figure 2.4a, where the resistance R_P is given by:

$$R_P = \frac{1}{G_P} \tag{2.15}$$

and the capacitance between two terminals is associated to the quantity C_P expressed as:

$$C_P = \frac{B}{\omega} \tag{2.16}$$

where $\omega = 2\pi f$ is the angular frequency and f is the operating frequency. If we assume that this capacitance is associated to the junction, C_P should behave like the junction capacitance.

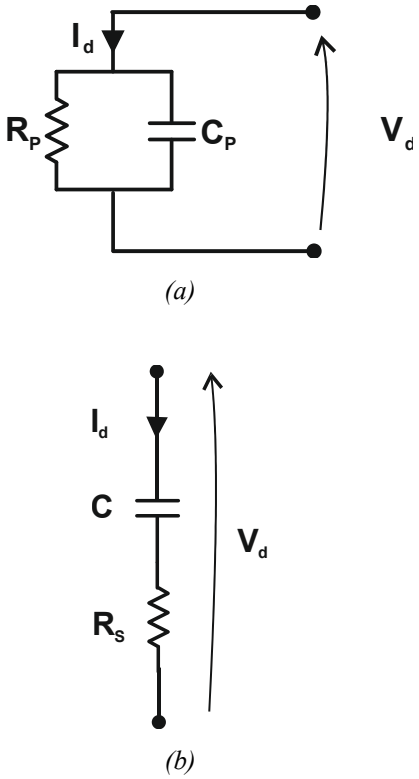


Figure 2.4. *a) Circuit configuration consisting of a single RC pair. b) Circuit configuration consisting in the series of a capacitance, C, and a resistance, R_S.*

As it is widely known, the p-n junction capacitance C is the sum of two components:

$$C = C_j + C_d \tag{2.17}$$

where C_j is the junction capacitance and C_d is the diffusion capacitance. In forward bias, the diode capacitance is mostly ascribable to the diffusion capacitance. The diffusion capacitance can be derived as:

$$C_d = \frac{\tau I_d}{V_T} \tag{2.19}$$

where τ is the minority carrier lifetime and I_d is the forward current across the device. More in detail, the diode current can be expressed as:

$$I_d = I_S \left[\exp\left(\frac{V}{nV_T}\right) - 1 \right] \tag{2.20}$$

According to this model, the capacitance C increases exponentially.

This result seems in contrast with experimental data, as we will see in Chapter 5. A possible explanation is that the model of Figure 2.4a is too simplified because it neglects the unavoidable series resistance. Considering such resistance, the circuit of Figure 2.4b is obtained, where the parallel resistance R_P is omitted, since it is expected to be much higher than R_S. Consequently, in the impedance measurements, the capacitance at the terminals, C_P, provided by the impedance analyzer cannot be directly interpreted as the diode capacitance C.

Nevertheless, the quantity given as junctions capacitance, in nearly all analyses that can be found in the literature, is C_P because it is the standard output given by impedance analysers.

Consequently, it is of paramount importance to give a proper interpretation of C_P, as function of the physical parameters of the model. Since the models in Figure 2.4 a and b describe the same device, the capacitance C_P and the conductance G_P can be reconducted to C and R_S following these formulas:

$$G_P = \frac{1}{R_S} \frac{(\omega R_S C)^2}{1 + (\omega R_S C)^2}$$

$$C_P = \frac{C}{1 + (\omega R_S C)^2} \tag{2.17}$$

From (2.17), it comes that C_P is strongly influenced by R_S and, of course, by C.

It can be found that C_P exhibits a peculiar behaviour, reaching a peak as the forward biased junction starts to inject minority carriers.

The increase of R_S moves the peak towards lower voltages. This is evident from Figure 2.5 which shows C_P and C with increasing R_S. As can be seen Rs affects the height and the position of the peak appearing in Cp.

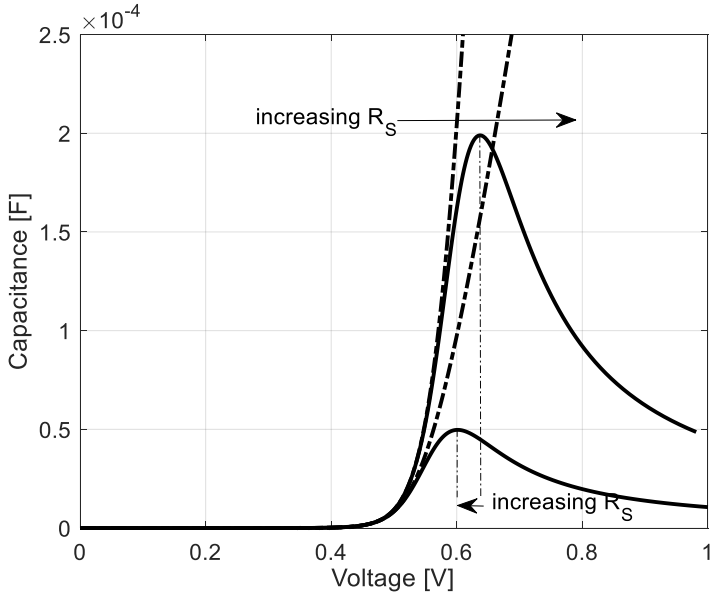


Figure. 2.5. *C-V curves obtained from circuit configuration of Figure 2.4a and Figure 2.4b. The dashed curves represent C, while the other curves are C_P. Series capacitance tends to angle due to R_S increase. Parallel capacitance shift towards lower voltages with increasing R_S as can be seen from peak position. In this graph the series resistance values are R_{S1} = 4 mΩ, R_{S2} = 8 mΩ.*

In order to find an analytical expression of the peak height, it is necessary to derive the C_P expression with respect to the voltage and find where the derivates is equal to zero:

$$\frac{dC_P}{dV} = \frac{d}{dV}\left(\frac{C}{1+(\omega R_S C)^2}\right) = 0 \tag{2.21}$$

where

$$\frac{dC}{dV} = \frac{dC_d}{dV} + \frac{dC_j}{dV} \approx \frac{dC_d}{dV} \tag{2.22}$$

Assuming that C_d is given by

$$C_d = \frac{\tau}{V_T} I_S \left[\exp\left(\frac{V_j}{nV_T}\right) - 1 \right] \approx \frac{\tau}{V_T} I_S \exp\left(\frac{V_j}{nV_T}\right) \tag{2.23}$$

Developing (2.17), the following expression occurs:

$$\frac{d\mathrm{C}}{dV}\left(\frac{1-\omega^2 {R_S}^2 C^2}{\left(1+\omega^2 {R_S}^2 C^2\right)^2}\right) = 0 \tag{2.24}$$

In this equation:

$$\frac{d\mathrm{C}}{dV} > 0 \tag{2.25}$$

Because C has been considered equal to C_d which follows an exponential law. The unique condition to satisfy the (2.24) is to zero the expression in the parenthesis. This leads to the following condition:

$$C = \frac{1}{\omega R_S} \tag{2.26}$$

Substituting this value of C in (2.17), the expression of the peak is found:

$$C_{P\max} = \frac{1}{2\omega R_S} \tag{2.27}$$

The analytical expression of peak is found, revealing that the higher or lower value of the peak at a certain frequency is only regulated by R_S value. In Figure 2.5, it can be seen that for a series resistance value which doubles, the peak height reduces at ¼ the starting value.

Found the expression of the peak height, the expression of peak position in the voltage range must be established. At this purpose, it is possible to define the voltage across the diode as the sum of the voltage across the junction and the voltage drop on the series resistance:

$$V = V_j + R_S I_S \exp\left(\frac{V_j}{nV_T}\right) \tag{2.28}$$

In the maximum point, the (2.26) can be substituting in the (2.23), obtaining the following equation:

$$\frac{1}{\omega R_S} = \frac{\tau}{V_T} \exp\left(\frac{V_j}{nV_T}\right) \tag{2.29}$$

From this equation, it is possible to find the expression of the junction voltage at the maximum point:

$$V_j = nV_T \ln\left(\frac{V_T}{I_S R_S \omega \tau}\right) \tag{2.30}$$

The voltage at which peak occurs, V_P, is defined by substituting (2.30) in (2.28):

$$V_P = nV_T \ln\left(\frac{V_T}{I_S R_S \omega \tau}\right) + I_S R_S \exp\left(\ln\left(\frac{V_T}{I_S R_S \omega \tau}\right)\right) \tag{2.31}$$

$$V_P = nV_T \ln\left(\frac{V_T}{I_S R_S \omega\tau}\right) + \left(\frac{V_T}{\omega\tau}\right) = A\ln\left(\frac{B}{I_S R_S}\right) + B \tag{2.32}$$

$$A = nV_T; B = \frac{V_T}{\omega\tau}; \tag{2.33}$$

Deriving (2.32) with respect to the I_S and R_S it is possible to perform a sensitivity analysis on the effect of these parameters on the voltage on which peak occurs. The following expression can be written:

$$\frac{\partial V_P}{\partial I_S} = -\frac{A}{I_S}\cdot\frac{I_S}{V_P} = -\frac{A}{A\ln\left(\frac{B}{I_S R_S}\right) + B} \tag{2.34}$$

$$\frac{\partial V_P}{\partial R_S}\cdot\frac{R_S}{V_P} = -\frac{A}{R_S}\cdot\frac{R_S}{V_P} = -\frac{A}{A\ln\left(\frac{B}{I_S R_S}\right) + B} \tag{2.35}$$

Considering equations (2.34) and (2.35), it can be asserted that both the parameters I_S and R_S play an important role in V_P behaviour. However, V_P depends on defects concentration since I_S depends on defects concentration.

The I_S effect on V_P seems stronger than R_S one. This can be explained by thinking that the two parameters have the same sensibility, hence, the parameter with the greater relative variation causes the greater variation of V_P. The current can change of orders of magnitude, while the series resistance can change of decades. This means that both I_S and R_S modify the peak position, but a more prominent peak shift arises in case of a I_S variation.

In Figure 2.6, the influence of I_S on C and C_P is shown. It can be seen that for a higher I_S value, C moves toward left and diode starts conducting at a lower voltage compared to the curve corresponding to a lower I_S. Also C_P behaviour is influenced by I_S, and more precisely the capacitance peak moves toward left with respect to the curve with a lower I_S. Considering Figure 2.5. and Figure 2.6, it is possible to notice

that R_S impacts the peak height and slightly the peak position, while Is strongly impacts the peak position.

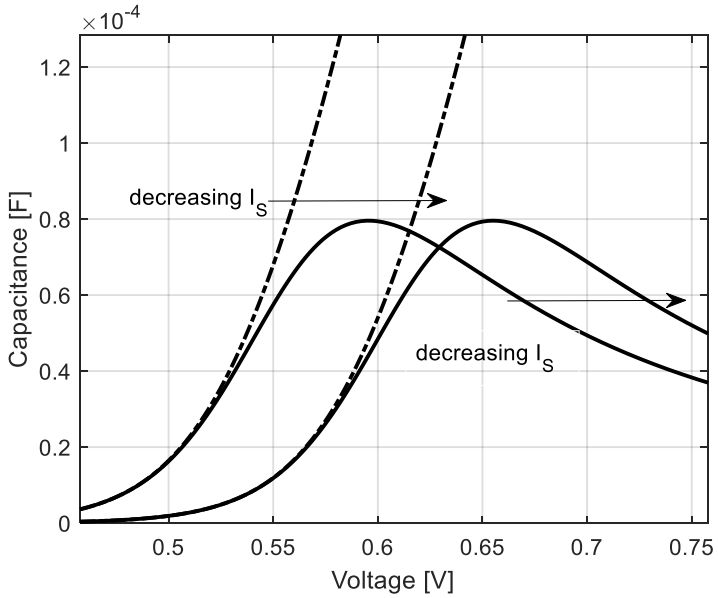


Figure 2.6. *I_S influence on C and C_P curves. Both curves shift toward left with increasing I_S. The two curves are obtained for I_{S1} =1·10^{-10} A, I_{S1} =1·10^{-9}A.*

Forward capacitance is not only influenced by intrinsic properties of a device. Also extrinsic features can modify capacitance behavior, and more precisely peak position. The most impacting factor relies on defects in the device under test. As it is widely known, defects and traps in a MS interface can dramatically influence the diodes physical behaviour and hence the resulting capacitance results modified with varying applied voltage. A detailed study on the influence of defects properties on the forward bias C-V curve is needed in order to gain a better insight in the device physics. In the following part of this Section, some traps properties are taken into account and their effects on C-V curves are highlighted. Three types of traps are considered in this study: fixed charge defects, acceptor and donor traps. A trap can be defined as a defect in the bandgap which behaves as a generation or a recombination centre (G-R centre) [50][1]. Each centre can be occupied

by an electron or a hole or otherwise it can be vacant. While fixed charges are always occupied, this is not the case for acceptor and donor traps. These latter are charged as a hole when occupied or are neutral if not occupied. Vice versa acceptor traps are charged as an electron if occupied or neutral if vacant.
The energetic distribution of traps, TD, is defined as follows:

$$TD = C_0 \exp\left(-\left|\frac{E - E_0}{E_S}\right|\right) \tag{2.36}$$

where C_0 is the traps concentration, E_0 is the central energy level, E_S is the lateral width and E is the energy [51].

- In first case, only **fixed charge traps** are considered. In Figure 2.7, the comparison between C-V curves obtained for structure without any defect and structure with fixed charge is shown. Structure considered is n-type silicon substrate, $N_D = 5 \cdot 10^{15}$ cm^{-3}, with a top layer of metal, WF = 4.8 eV. From Figure 2.7, it can be noticed that fixed charge traps existence shifts the forward bias capacitance peak towards lower voltages. The capacitance peak obtained for the structure without defects occurs at $V_{P1} = 0.46$ V, while the peak occurs for $V_{P2} = 0.23$ V for the structure with a fixed charge concentration equal to $5 \cdot 10^{15}$ cm^{-3}. This result can be better understood if it is also considered the shift occurring in the I-V curve of the two structures. The parameter that undergoes the most substantial change with fixed charge is the saturation current, as can be seen in Table II. As the fixed charge concentration increases also I_S increases. This is in agreement with analysis performed previously, where it has been stated that increasing I_S the capacitance curve shifts toward left and its peak occurs for a lower voltage.

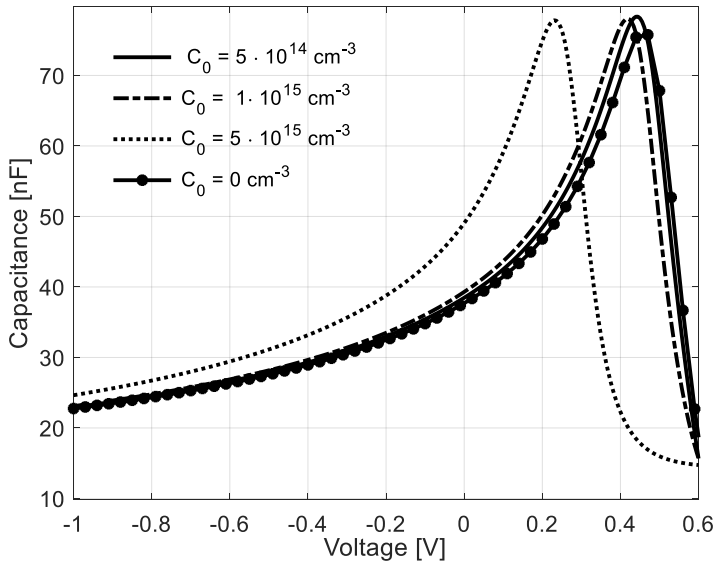


Figure 2.7. *C-V curves obtained from the same structure with different fixed charge traps concentration.*

Table II*. Saturation current corresponding to different fixed charge concentration values considered.*

Fixed Charge concentration [cm^{-3}]	I_S [A]
0	$3.9 \cdot 10^{-15}$
$5 \cdot 10^{14}$	$4.0 \cdot 10^{-15}$
10^{15}	$2.4 \cdot 10^{-14}$
$5 \cdot 10^{15}$	$3.0 \cdot 10^{-11}$

- If only **donor type traps** are considered, the C-V curve modifies as shown in Figure 2.8. The peak in forward bias slightly moves toward higher voltage as the donor concentration increases. Also, the peak intensity results modified, more precisely the higher is the traps concertation, the higher is the peak value. In this case, donor traps considered are located at an energetic level E_0 = 0.3 eV from conduction band and the traps

distribution has a width E_S = 0.2 eV. The main effect of donor traps existence is the enhancement of the capacitance peak in forward bias.

- If only **acceptors type traps** are considered in the device structure, the C-V curve shows the same trend of Figure 2.8. Even if only acceptor traps exist in the MS structure, the main effect in C-V curve behaviour is related to the peak height. This outcome is similar to the effect of R_S on capacitance curve, Figure 2.5. Donors or acceptors traps affects the peak height and they only marginally shift the peak position.

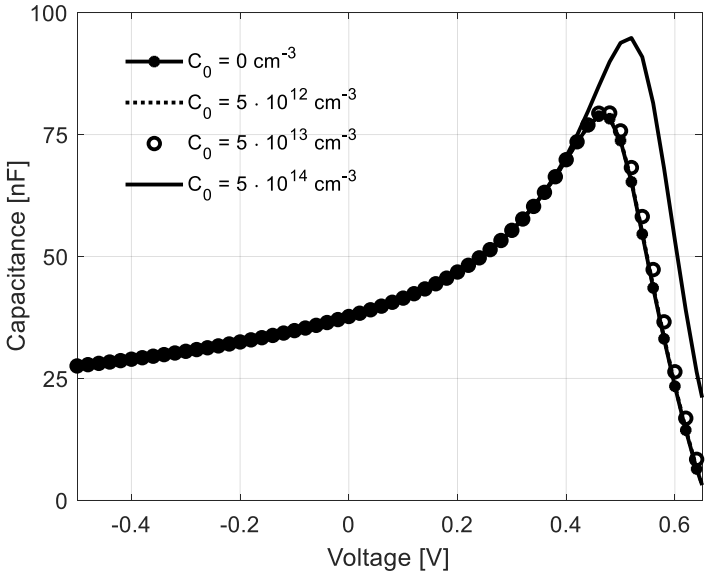
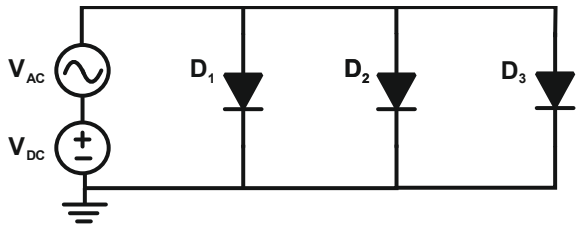


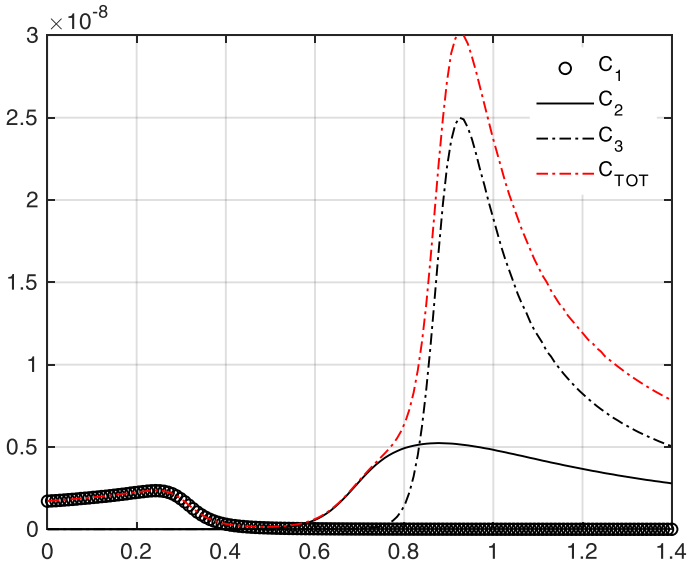
Figure 2.8. *C-V curves behaviour with donor traps concentration.*

B. Multiple interfaces

The focus of this Section is on the forward bias capacitance behavior in the case of a device under test embedding several interfaces in its design. More in detail, a particular hint is on the additional peak in the capacitance behavior which is sometimes obtained in measured data. To explain this phenomenon, it is necessary to do one step back and consider that in the case of multiple interfaces, the resulting capacitance curve is given by the superposition of all the existing interfaces contributions. From the circuit configuration obtained in LTSpice, Figure 2.9a, where three SBDs with different knee voltages are connected in parallel between them, it is clear that the total capacitance curve is exactly the sum of the three diodes capacitances. The C-V curve has been obtained imposing on the parallel a DC voltage sweep in the rage [0,1.4] V and an AC signal superimposed with a frequency f = 1 kHz. In Figure 2.9b, the curve with continuous line is correspondent to capacitance obtained if only diode D_1 is considered, the curve with markers is relative to diode D_2, while the dashed curve is relative to diode D_3. The resulting capacitance shows an additional peak in forward bias. This result is obvious if we think in terms of lumped elements. The objective in this Section is to show that if we consider an interface with a defects distribution which is different in a limited portion, then we can model such interface as two different interfaces connected in parallel. This is possible because, as seen in previous Section, defects can modify the value of capacitance peak and the voltage at which this peak occurs. Thus, an interface with non-uniform properties in terms of defects concentration has a capacitance deriving from the superposition of the different behaving portion of the device, i.e., the interface parts with the same defects properties.



(a)



(b)

Figure 2.9.a) Circuit schematic realized in LTSpice software; b) C-V curves obtained from considered schematic.

To validate this assessment, the case of non-uniform MS interface is taken into account. A test structure has been developed in Sentaurus TCAD [51], Figure 2.10. This structure is composed of a n-type silicon substrate and a metal top layer. The MS interface has different physical properties in different interface part. More in detail, there is a uniform defect concentration at the MS interface, except for a limited interface portion, where a different defects concentration has been locally assigned. More in detail, the MS interface predominant defects distribution is $C_0 = 5 \cdot 10^{11}$ cm^{-3} (assigned to the wider region,

region #2), while to a limited part of the interface has been assigned a different defects concentration equal to $C_0 = 5 \cdot 10^{15}$ cm^{-3} (region #1). The width W of region #1 has been varied, keeping the total width constant, to investigate the resulting effects on the C-V curve. Depending on the ratio between the two portions of the interface, the resulting capacitance enhances or lessen the two existing peaks, as can be seen in Figure 2.11. The dotted curve shows capacitance due to structure of Figure 2.10 with a uniform fixed charge concentration $C_0 = 5 \cdot 10^{15} cm^{-3}$, which is shifted toward lower voltage, as seen in Subsection A. In the same graph, the dashed curve is the resulting capacitance with a fixed charge concentration $C_0 = 5 \cdot 10^{11}$ cm^{-3}, while the other curves have been obtained assigning the ratio of the two different MS interface parts. More precisely, the second peak is more prominent if the zone with defects concentration causing such peak is wider.

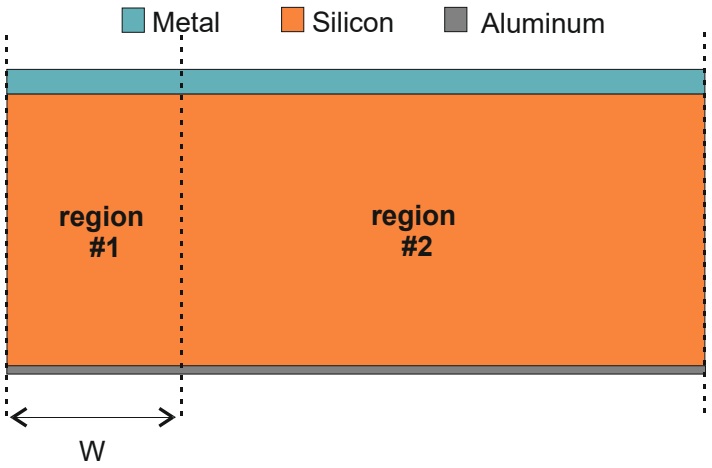


Figure 2.10. *Numerical structure developed. The structure consists of a n-type silicon substrate with a metal layer on its top. The traps concentration has been assigned non locally uniform at the MS interface. The predominant part of the interface has a traps concentration of $C_0 = 5 \cdot 10^{11}$ cm^{-3}, while the other part has a traps concentration of $C_0 = 5 \cdot 10^{15}$ cm^{-3}. The total width of the structure is keep constant to 1.4 µm.*

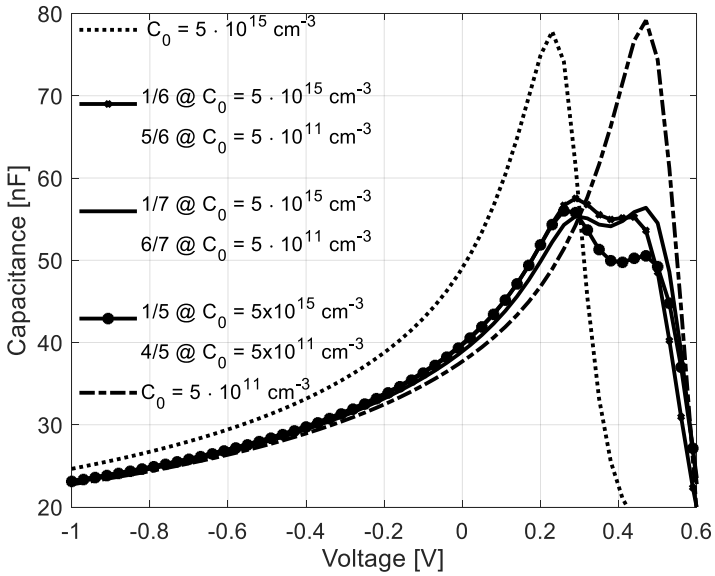


Figure 2.11. *C-V curves obtained from structure of Figure2.10.*

This means that considering the structure of Figure 2.10 and supposing an uneven distribution of that trap concentration at the MS interface, a double peak capacitance profiling should arise. In this case, in region #1(with a W = 0.28μm) C_0 was set to $5 \cdot 10^{15}$ cm^{-3}, while in region #2 C_0 was $5 \cdot 10^{11}$ cm^{-3}. The behavior of the device has been numerically evaluated in the Synopsys Sentaurus environment; results are shown in Figure 2.12. In this figure, the dotted line is referred to the capacitance of the device if only region #1 is considered, while the dashed line is related to the capacitance of device if only region #2 is taken into account. The entire device capacitance is the superposition of the capacitances deriving from the two mentioned part, line in Figure 2.12. This means that the capacitance of the entire device behaves like the two parallel connected capacitances since it overlaps the sum of the two capacitances relative to region #1 and region #2.
This discussion suggests that the existence of multiple peaks in the measured capacitance is linked to some issues in the fabrication process, leading to non-uniform properties of the interfaces.

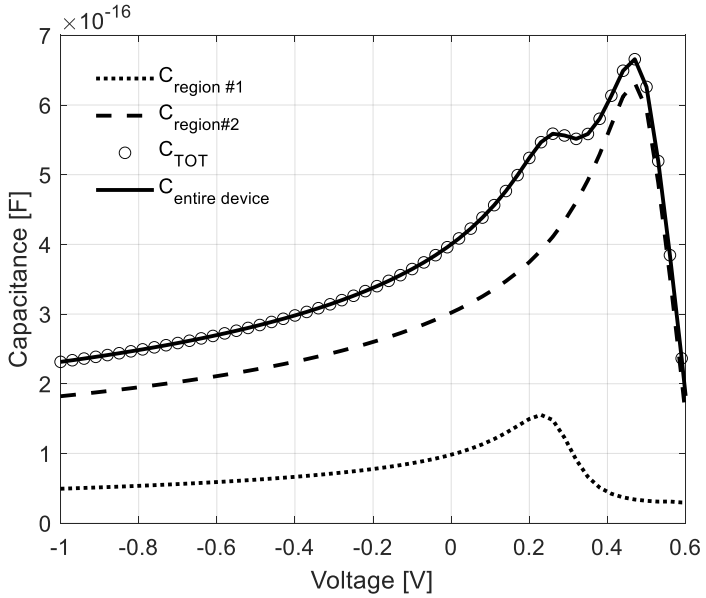


Figure 2.12. *Capacitance behavior obtained for a structure sized 1/5 of the total structure with a $C_0 = 5 \cdot 10^{15}$ cm^{-3} (dotted line), for a structure sized 4/5 of the total structure with a $C_0 = 5 \cdot 10^{11}$ cm^{-3}. The full line is the capacitance obtained for the entire structure with 1/5 and 4/5 of it having traps properties respectively $C_0 = 5 \cdot 10^{15}$ cm^{-3} and $C_0 = 5 \cdot 10^{11}$ cm^{-3}.*

Chapter 3: SiC MOSFETs

This Chapter describes the methodologies and the approaches exploited to *(i)* characterize power SiC MOSFETs and *(ii)* perform electrical simulations obtaining a calibrated model to explain (iii) experimental results.

The reduction of the trap density at the SiC/SiO_2 interface of a SiC MOSFET is still an open issue for the next generations development. Since TCAD simulations are one of the most powerful tools adopted in the field of power semiconductor devices, in this Chapter the guidelines for the calibration of the TCAD model are defined from the point of view of the interface traps modeling. This Chapter is divided in three main Sections. In the first Section, the analysis approach is adopted to investigate the effect of the interface traps from theoretical, numerical and experimental point of view. Therefore, after a brief recall of the SiC/SiO_2 trap distribution in modern SiC MOS structures, the details of the TCAD model of the reference cell are reported. To correctly simulate the C-V curve of a SiC MOSFET it is mandatory to keep into account the time duration of the measurement and the derivative over the time. In Section 3.2.2, the developed mixed-mode simulation approach is reported in order to accurately simulate the C-V curve. The focus of the third Section is the analysis of the effect of the SiC/SiO_2 interface traps on the C-V curve from the numerical point of view, with the scope of understanding some anomalous results coming from the experimental C-V curves. The experimental setup is detailed as well in this Section. The numerical analysis of the traps effect on the C-V curve allows to improve the interpretation of the experimental C-V curves.

3.1 SiC MOSFETs

Silicon carbide power devices, such as SiC metal-oxide-semiconductor field effect transistor, are replacing the silicon devices in many high-power electronics applications [52]. SiC has attracted great interest because of the superior performance of this material,

compared to Si. It has a wide bandgap, a high electron mobility, and an excellent thermal conductivity [53]. Even if great effort has been spent for the development of SiC technology there are some issues still open such as threshold voltage hysteresis and high traps density at the SiC/SiO_2 interface. Typically, the density of states at the SiC/SiO_2 interface is two order of magnitude higher than that of the Si/SiO_2 interface [54], [55]. The effects of a high density of traps at the interface are several, since they affect the channel mobility, the threshold voltage stability and they cause a higher leakage current [56]. The hysteresis effect arising in transfer characteristics is another known issue for the development of SiC MOSFET devices and it is detrimental for the performance of power applications, since the threshold voltage is different for MOSFET turn-on or turn-off [57]. Despite the large literature, the origin of the interface traps variability is not completely clear and different analysis report for different phenomena leading the formation of the interface traps [56], [58]-[60]. The main contribution to the interface traps formation are due to: the higher number of carbon atoms at the SiC/SiO_2 interface, compared to the Si/SiO_2 one, and the near-interfacial oxide traps [56], [59], [60]. The characterization of the trap distribution requires advanced interface characterization techniques that do not allow an easy estimation of the trap distribution of the interface traps [56]. From this point of view, C-V measurements are very helpful, but they have to be supported by TCAD simulations. These latter are challenging for SiC MOSFET devices because of the complexity of the trap distribution and their process variability. Therefore, in this thesis the input data for the calibration of the SiC MOSFET TCAD model are provided by the capacitance-voltage characterization results. TCAD simulators are a consolidated tool for the development of power semiconductor devices and an accurate model of the device is mandatory to carry out predictable simulations. With the aid of TCAD simulators, the development of the SiC MOSFET led to high performance devices for various current and voltage ratings [61]. The aim of this Chapter is the analysis of the SiC/SiO_2 interface traps effects on the SiC MOSFET C-V curve by means of TCAD simulations, with the aim of supporting the interpretation of the experimental C-V curves. The numerical results have been adopted to explain some unexpected behavior of the experimental C-V curves of two commercial devices. The combination

of the numerical and the experimental results, allowed the analysis of the influence of the interface trap levels on the C-V curve in a real device.

3.2 Analysis approach

SiC MOSFETs characterization has been carried out using a detailed analysis approach. Such procedure relies on the development of a reliable TCAD simulation framework together with detailed C-V measurements.

3.2.1 The SiC/SiO_2 interface in SiC MOSFETs

SiC is gradually replacing silicon for high power electronics applications, because of material intrinsic properties, such as wide bandgap, high electron mobility and good thermal conductivity. Another important advantage of SiC is the possibility to grow SiO_2 oxide layer by simple thermal oxidation [62]. Despite of these characteristics, the first generations of SiC MOSFETs did not replace the Si switching devices on the market. The reason of this misleading expectation is the high density of traps distribution at SiC/SiO_2 interface. Hence, this interface is a key point for device reliability and performances degradation. This is a critical issue especially for MOSFET devices, where important parameters, such as channel mobility and threshold voltage, quickly degrade and modify due to interface traps. In addition to the effects on the channel mobility, the SiC/SiO_2 interface traps lead to the threshold voltage hysteresis effect [63], [64], related to the trapping and de-trapping phenomena. The main difference between Si and SiC is the presence of C atoms at the boundary between SiC and SiO_2. The carbon atoms do not contribute to the oxide formation, leading to the formation of two dominating sources of electrically active defects: carbon atoms and near-interfacial oxide traps [56]. More in detail, carbon atoms organize as sp2-clusters and as graphite-like clusters. The main effect of the interface imperfections is the arising of interface state levels all over the forbidden gap at the interface. Even if great effort has been put into the improvement of the SiC/SiO_2 interface, the state-of-the-art devices are still far from a satisfactory quality level. Therefore, a large number of

works in literature focus on the improvement of the interface states through a careful adjustment of the oxidation process of the SiC. The reference oxidation process is the dry one and the effect of the nitridation annealing process is reported. More in detail, the state profiles of nitridation in NO or N_2O are reported. Measurements are carried out by the conventional high-low method. It is clear as the adoption of a nitridation annealing process strongly reduces the interface states density. On the other hand, the nitridation annealing process leads to the presence of a high concentration near the conduction band of very fast interface states. These fast states can respond to a probe frequency of 100 MHz up to frequencies higher than 1 GHz. This introduces a relevant inaccuracy in the characterization of the interface states density when low frequency probes are adopted. The adoption of the annealing in NO or N_2O leads to the accumulation of nitrogen at the SiC/SiO_2 interface. However, a direct link between the carbon clusters and the interface state density is not established and the very high density of interface states close to the conduction band is still not understood [65]. Despite the progress in SiC MOSFET technology, the density of SiC/SiO_2 interface states is still higher than Si/SiO_2 interface by two orders of magnitude [54], [55]. An important point is that SiC/SiO_2 interface states properties are not known a priori but they are dependent on all of the processes affecting the SiC/SiO_2 interface states and device structure. An effort to reduce interface defects density is mandatory. A common approach to reduce the trap density is the partial passivation of interface states which is achieved through some treatments such as nitridation [65], [66], [67], or oxidation in N_2O gas [67]. The SiC/SiO_2 interface states density (D_{it}) distribution depends on technological steps. However, data coming from literature [60], [65], [69]-[71], show as for a n-type 4H-SiC MOS structure, the trap level distribution has a peak in the proximity of the conduction band and exponentially decreases toward the bandgap center, with peak value in the range of (10^{13} - 10^{14}) traps/cm^2 at an energy level which is 0.2 eV under the conduction band. For a p-type 4H-SiC MOS structure the distribution of interface state density has a peak at an energy level which is 0.2 eV from the valence band, with a concentration that varies from (10^{12} - 10^{13}) traps/cm^2. Moreover, the interface states in the proximity of the conduction band are very fast and high frequency characterization are required to investigate their density [68], [69].

3.2.2 Simulated structure

A sketch of the SiC MOSFET TCAD model is reported in Figure3.1 [72]. The reference structure is a vertical 1200 V SiC MOSFET, with a design compatible with the electrical performances of 1200 rated commercial devices. The simulations presented in following part of this Chapter are all based on this device structure. Simulations have been carried out by means of the commercial TCAD simulator Sentaurus TCAD [73]. The structure is composed by a planar SiC MOSFET, with a shielding region to suppress parasitic BJT effects under fast dV/dt transient. The channel region has been made by using a constant doping concentration and all the doping concentrations are reported in Figure3.1, together with the distances of the different areas of the device. In principle, a rigorous TCAD electro-thermal simulation should carefully keep into account for the geometrical features of the device. A 3D elementary cell should be adopted to the correctly estimate the temperature distribution in the structure [74]. Since in this analysis it is assumed that a stripe approach is adopted for the active area design of the device, the adiabatic conditions can be assumed for the 2D elementary cell on the lateral borders. The focus is the modeling of the traps at the SiC/SiO_2 interface, therefore the C-V curves are evaluated by adopting the standard conduction models (Arora [75] for mobility and Scharfetter [77] for lifetime in terms of equations, while the specific parameters for the SiC are from [76]). As reported in the previous Section, the traps composition at the channel interface is very complex for the SiC MOSFET and this strongly affects the threshold voltage behavior of the device. The situation is even more complicate when temperature changes in the device. The strong temperature dependence of the electron emission rate by traps can lead to a strong variation of the threshold voltage, that can become relevant in events such as the short circuit [72], [76]. Therefore, a careful modeling of the SiC/SiO_2 interface is kept into account for the TCAD model.

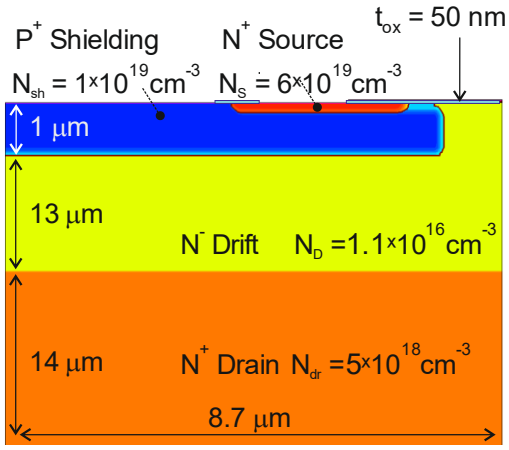


***Figure 3.1**. TCAD model of the SiC MOSFET adopted in this Chapter. The structure is not to scale.*

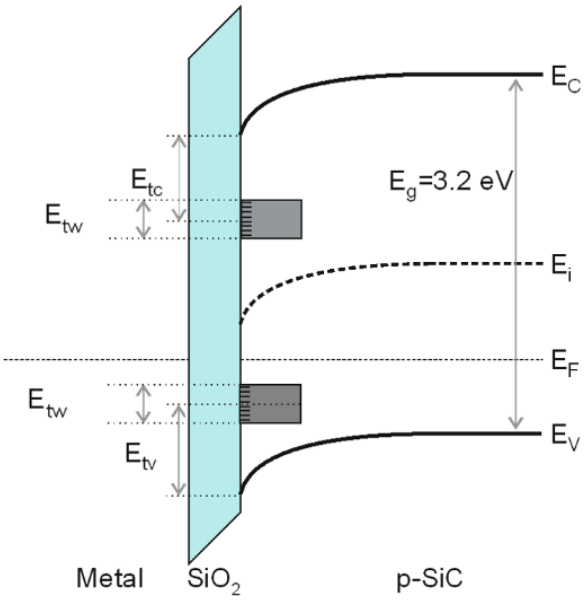


***Figure 3.2.** Band diagram of the simulated structure.*

In Figure 3.2 the detail of the band diagram at the interface, is reported. The analysis takes into account the trap levels close to the Valence and those close to Conduction band. Data from literature report

that the traps can occupy different positions in the forbidden gap of the SiC substrate and their position strongly depends on the technological steps needed to process the device, as seen in previous Section. Therefore, a simplified approach for the TCAD model calibration of the SiC MOSFET device is here presented. The aim is to evaluate the effect of the traps at the SiC/SiO_2 interface, this is the reason why traps levels have been added to the TCAD model and their effect on the carriers dynamics is kept into account. More in detail, both the acceptor and donor type traps have been considered for the modeling of the interface traps. The former type is uncharged when unoccupied and they carry the charge of one electron when fully occupied, while the latter are uncharged when unoccupied and they carry the charge of one hole when fully occupied [73], as seen in Chapter 2. The situation depicted for a SiC device cannot be modeled with a single trap level in the forbidden gap, but a complex trap distribution has to be defined to model what occurs in real SiC MOSFET devices. Therefore, to keep into account a complex distribution of the traps at the SiC/SiO_2 interface, traps in the SiC side have been modeled with two kind of possible bands: for traps located in the proximity of the conduction band, the distance between the trap band center and the conduction band is called E_{TC}; for traps located in the proximity of the valence band, the distance between the trap band center and the valence band is called E_{TV}. The width of the trap band is named E_{TW}. Finally, the concentration of the trap at the interface (C_{it}) is calculated as the product of the E_{TW} parameter and N_0, the concentration of traps per area and per energy (N_0 is given in $V^{-1}cm^{-2}$).

3.2.3 Simulation framework

In Figure 3.3a, it is shown the TCAD framework developed to emulate experimental C-V setup and to investigate the effect of SiO_2/SiC interface traps on the C-V curve measurement.

Typically, a voltage ramp is applied to the DUT to measure the capacitance. The capacitance measurement is carried out by adding a small sinusoidal signal to the DC voltage and the current signal is measured to evaluate the impedance of the device, as seen in previous Chapter. In Figure 3.3a the connection of the MOSFET under test with the C-V tracer is reported. Here V_{GEN} keeps into account both the static

component of the applied voltage and the small signal generator used to measure the impedance at a specific DC voltage.

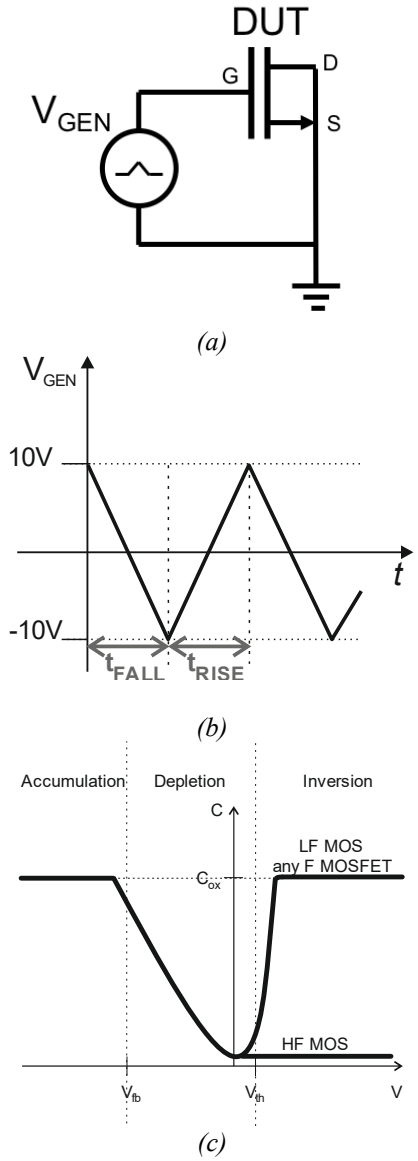


Figure 3.3. *TCAD framework for the simulation of the dynamic C-V curve. (a) Schematic of the circuit used for the simulation of the C-V experimental setup. b) Voltage waveform generated by V_{GEN} in (a). (c) a typical C-V curve of a MOSFET structure.*

Since the Drain and the Source of the DUT are connected to ground, no static current flows into the device. In Figure 3.3b the waveform of V_{GEN} is presented. It is a triangular waveform that varies linearly between -10 V and 10 V and the duration of the voltage ramp-up or ramp-down can be varied by changing the measurement time. The duration of the ramp-down is defined as t_{FALL}, while the duration of the ramp-up is called t_{RISE}. Typically, t_{FALL} and t_{RISE} values are chosen in a way that the C-V measurement can be considered quasi-stationary. This means that the time constant of trapping and de-trapping process existing in the MOSFET structure is assumed to be negligible compared to the period of the V_{GEN} signal (T). This latter can be defined as the sum of t_{FALL} and t_{RISE} ($T = t_{FALL} + t_{RISE}$). In Figure 3.3c an example of the quasi-stationary C-V curve of a generic MOSFET is reported. In accumulation region the capacitance contribution is mainly due to the oxide capacitance (C_{OX}). When the gate voltage is increased, the channel region depletes and the more the voltage increases, the more the depletion region increases. The increase of the depletion region leads to the reduction of C_G, the measured capacitance. On the other hand, when the inversion occurs in the channel region, the channel forms and the majority carriers act as an equivalent plate of the gate capacitor. At the SiC/SiO_2 interface above the JFET region the accumulation of electrons occurs. Therefore, the Gate capacitance becomes C_{OX}.

It has to be mentioned that the C-V curve of a MOS transistor is different from the one of a MOS structure in inversion condition. More in detail, when the Gate voltage applied to a SiC MOS brings the structure in inversion condition, because of the very low thermal carrier generation in the depletion region, the inversion charge (Q_{INV}) can follow the applied AC variation only for infinitely low frequency. This implies that the C-V curve in inversion condition is different for low or high frequency in a MOS structure. On the other hand, in a MOS transistor device the carriers to follow the AC variation come from the Source and Drain region that provide the carriers for the channel region. Therefore, the high and low frequency C-V curve in inversion condition is the same in MOS structures [78]. In this work, the t_{FALL} and the t_{RISE} parameters are changed to investigate the effect of the ramp slope on the measured C-V curves. The simulation framework keeps into

account for the C-V curve dependence on the period of V_{GEN} driving signal by using the combination of the transient and the AC quasi-stationary simulations. More in detail, by means of a transient simulation the V_{GEN} voltage have been varied accordingly to the waveform in Figure 3.3b. To carry out the C-V curve, the AC analysis is performed at any pre-defined time step. In this way, the AC analysis keeps into account for the carrier's distribution at the specific time instant. This aspect is crucial, since, depending on the t_{RISE} and t_{FALL} values, the carrier distribution over the device can change for the same V_{GEN} value, in presence of traps. The simulation approach allows to keep into account for the eventuality of the time constant related to the traps dynamics is comparable or higher than the derivative slope of the rising-up or rising-down of the V_{GEN}. All of the analyses have been carried out assuming $t_{RISE} = t_{FALL}$. The effect of fixed charge has been kept into account as well. The aforementioned framework allows to analyze the C-V curve dependence over both the dv/dt of the applied voltage and the traps properties. Therefore, the TCAD model trap properties are varied and the effect on the C-V curve is investigated.

3.3 Experimental and numerical results

In the first part of this paragraph the experimental setup is presented. In the second Subsection the method to calibrate the TCAD model of a SiC MOSFET in terms of the trap distribution at the SiC/SiO_2 interface is reported. First, an extensive analysis of the effect of the concentration (C_{it}), the capture cross sections (σ_n and σ_p), the energy level and the type of the interface traps on the C-V curve shape is carried out. In the second part the experimental results are reported, together with all of the measurements details. Finally, starting from the numerical results, the experimental results are commented.

3.3.1 Numerical results

An extensive analysis of the effect of the interface traps on the C-V curve of a SiC MOSFET has been carried out. All the numerical analyses have been performed adopting the simulation framework presented in the previous Section. Simulations have been carried out for T = 300K. Basically, in absence of both fixed charge and traps at the

SiC/SiO_2 interface, the C-V curve of a SiC MOSFET mainly depends on the design, the SiC material and doping profile of the elementary cell. The first analysis has been the evaluation of the effect of the fixed charge at the SiC/SiO_2 interface. In Figure 3.4 the C-V curves of the SiC MOSFET structure is reported for two fixed charge values. Since the fixed charge is positive, the structure with a higher value of fixed charge shifts to the left the C-V curve, without any warping of it [4].
The Gate voltage variation labeled "d" identifies the voltage variation between the two points of the C-V plot where the capacitance has the value $C_{REF} = 0.8 \times C_{OX} + 0.2 \times C_{Gmin}$, where C_{Gmin} is the minimum C_G value. Confirmed that the only effect of the fixed charges is the shift of the C-V curve, next investigation of the trap effects has been the evaluation of the trap effect on the C-V curve when only one type of trap is considered. The trap band position has been changed over the whole forbidden gap. The carriers dynamic introduced by the traps depends on the capture cross section of both electrons (σ_n) and holes (σ_p), therefore this parameter has been kept into account as well. An extensive analysis carrying out the presence of trap bands at the SiC/SiO_2 interface effects has been performed by means of TCAD simulations. In the following, the most relevant results are reported. In Figure 3.5 the numerical C-V curves are reported for six remarkable acceptor trap band levels, together with the C-V curve in absence of traps. For all the numerical C-V curves presented in this Chapter it is assumed that the trap band has a constant state level energy, with a width $E_{TW} = 0.1$ eV.

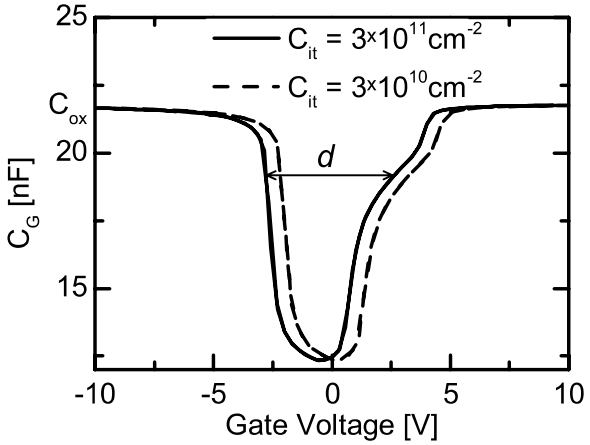


Figure 3.4. Numerical C-V curve for two fixed charge densities the SiC/SiO_2 interface with a temperature *T=300K.*

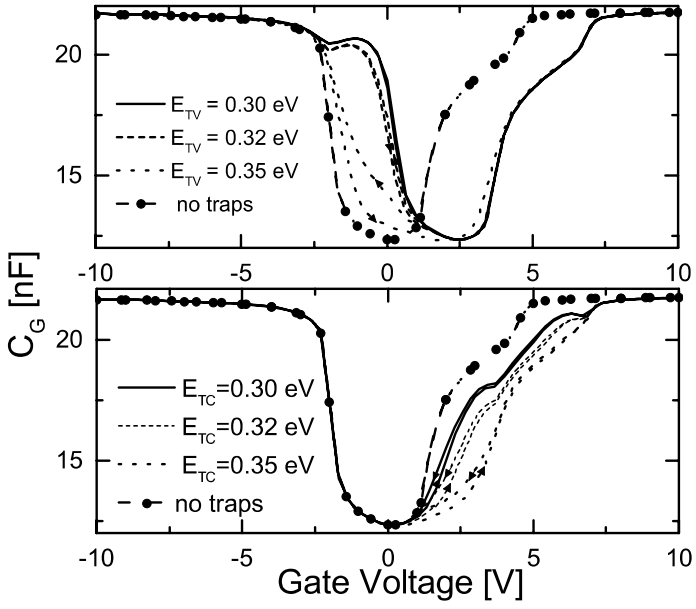


Figure 3.5. *Numerical C-V curves traced when one donors trap band is assumed, with the E_{TC} or E_{TV} changing. The C-V curve without traps is reported as well. $\sigma_n = \sigma_p = 1 \cdot 10^{-16}$ cm², $C_{it} = 1 \cdot 10^{12}$ cm^{-2}, $E_{TW} = 0.1$ eV and $t_{RISE} = t_{FALL} = 1$ ms, T=300K.*

These results show that the effect of the acceptor type traps is the modification of the C-V curve on the left side ($V_G < 2.5$ V) and the overall curve is shifted to the right, when the trap band is close to the valence band. More in detail, the more the trap band moves toward the Fermi level (E_i), the more the width of the C-V curve increases, as expected from theory [80]. For example, for $E_{TV} = 0.35$ eV, the C-V curve extension, for $C_G = 20$ nF, is 8.5 V, while the C-V curve extension for the structure without the traps is 6.2 V. Moreover, the presence of traps at the interface leads to a different C-V curve when the voltage changes from -10 V to 10 V or changes in the opposite side, this effect is more visible for $E_{TV} = 0.35$ eV. The shift occurs even for $E_{TC} = 0.3$ eV, $E_{TC} = 0.32$ eV and $E_{TC} = 0.35$ eV. This effect can be addressed as a hysteresis effect. More detailed analysis concerning the hysteresis behavior will be presented in the following of this Chapter. From results in Figure 3.5, the more the E_{TV} distance increases, the more the hysteresis effect increases. On the other hand, when the Acceptor like trap band is close to the conduction band, the C-V curve is shifted to the left and it extends on the right side ($V_G > -2.5$V). The more the distance from the conduction band increases, the more the C-V curve moves to the right for $V_G > -2.5$ V. Again, the C-V curve is different when the V_G varies from -10 V to 10 V, therefore a hysteresis effect arises again. The C-V curve without traps never shows a hysteresis effect, for any t_{RISE} and t_{FALL} value. In Figure 3.6 the same analysis has been carried out for donor type traps. The first effect of the donor type traps is the shift of the curve on left side, compared to the C-V curve without traps. The C-V curves increase their extension in presence of traps, as for the acceptor analysis. The effect on the capacitance given by the existence of donor traps is similar to acceptor traps effect. When the trap band is close to the valence band, the C-V curve is modified on the left side, while when the trap band is close to the conduction band, the C-V curve is modified on the right side. The hysteresis effect occurs for $E_{TV} = 0.35$ eV, $E_{TC} = 0.3$ eV, $E_{TC} = 0.32$ eV and $E_{TC} = 0.35$ eV. Therefore, it can be concluded that the presence of the traps changes the shape of the C-V curve and the involved area does not depend on the type of trap, but it is dependent on the distance of the trap band from both the valence band and the conduction band.

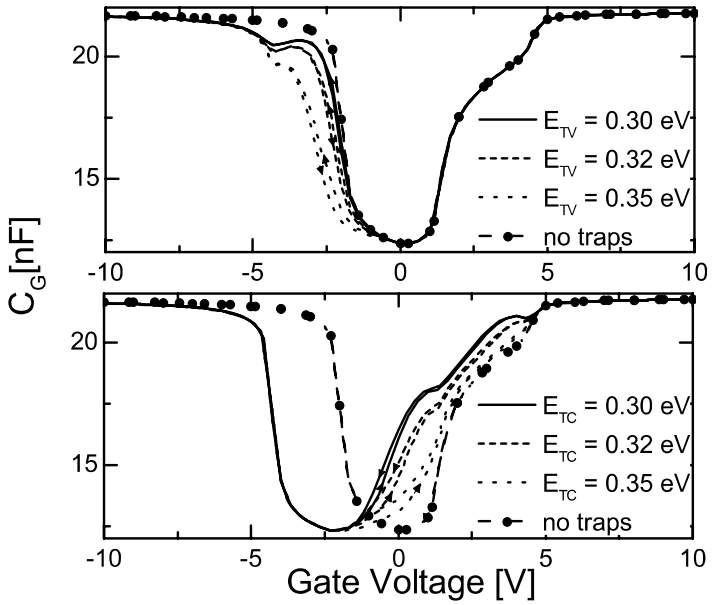


***Figure 3.6**. Numerical C-V curves traced when one donor trap band is assumed, with the E_{TC} or E_{TV} changing. The C-V curve without traps is reported as well. $\sigma_n = \sigma_p = 1 \cdot 10^{-16}$ cm^2, $C_{it} = 1 \cdot 10^{12}$ cm^{-2}, $E_{TW} = 0.1$ eV and $t_{RISE} = t_{FALL} = 1$ ms, $T = 300$K.*

The combined effect of the presence of band traps close to both the valence and conduction band has been investigated. In Figure 3.7 the numerical C-V curves are reported for two conditions: 1) acceptor type trap bands are considered close to both the valence and the conduction band, with $E_{TC} = E_{TV} = 0.35$ eV; 2) donor type trap bands are considered close to both the valence and the conduction band, with $E_{TC} = E_{TV} = 0.3$ eV. For both plots, four C-V curves are reported: 1) the one without traps; 2) the one where only the trap band close to the conduction band is kept into account; 3) the one where only the trap band close to the valence band is kept into account; 4) the one where both the trap bands are kept into account. Results show that the C-V curves warping can be considered as the superposition of the effects of the single trap bands. An example is reported for the donors C-V curves. If a fixed capacitance level, the same slope of the C-V curve and the

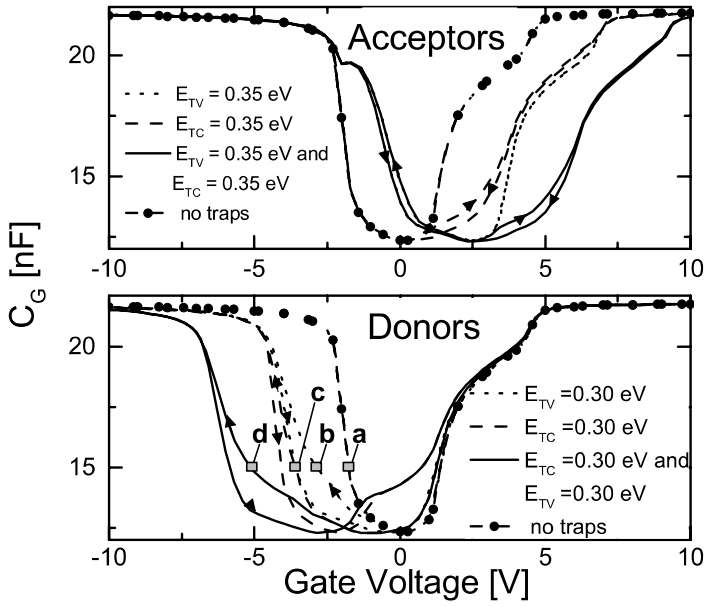


Figure 3.7. *Numerical C-V curves when two trap bands with the same trap type, one close to the valence band and one close to the conduction band, are considered.* $C_{it} = 2 \cdot 10^{12}$ *cm*$^{-2}$, $E_{TW} = 0.1$ *eV*, $t_{RISE} = t_{FALL} = 1$ *ms*, $\sigma_n = \sigma_p = 1 \cdot 10^{-18}$ *cm*^{2}, *T = 300K.*

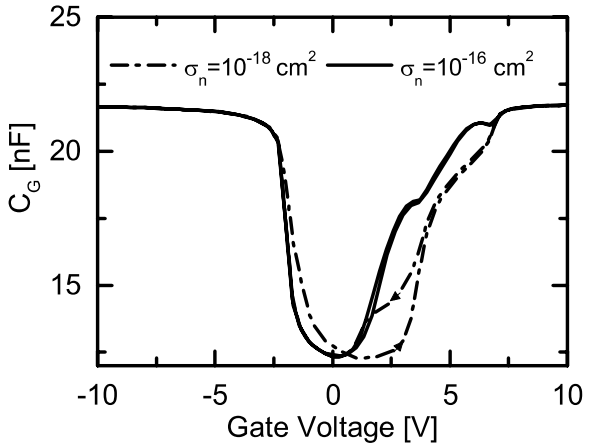


Fig 3.8. *Numerical C-V curves dependence on the interface traps capture cross Section.* $E_{TC} = 0.3$ *eV*, $C_{it} = 1 \cdot 10^{12}$ *cm*$^{-2}$, $E_{TW} = 0.1$ *eV*, $t_{RISE} = t_{FALL} = 1$ *ms and traps are considered is the acceptor type. T = 300 K.*

same sweep direction is considered, then the voltage variation between the C-V curve without traps and the one with both trap bands is sum of the voltage variation between the C-V curve without traps and the one with the trap band close to the conduction band and the voltage variation between the C-V curve without the traps and the one with the trap band close to the valence band. As an example, in Figure 3.7 for donor type traps, the distance between the C-V curve without the traps and the one with both trap bands at C_G = 15 nF can be evaluated by:

$$V_G(a) - V_G(d) = 2 \cdot V_G(a) - V_G(b) - V_G(c) \qquad (3.1)$$

This equation is valid for any capacitance level of the C-V curve. The hysteresis effect occurs on both side of the C-V curve, with an extension that depends on the capture cross section and t_{RISE}. The comparison of the aforementioned C-V curves with the one without traps shows a very large extension in presence of both the trap bands (e.g. for the "donors" curve the C-V curve extension, at C_G = 20 nF, is 9.8V, while the C-V curve extension for the structure without the traps is 6.2 V). Traps shift the C-V curve and such shift is toward right for acceptor type and toward the left for the donor.

As mentioned before, the capture cross section of both electrons and holes is kept constant for all the previous results, therefore the effect of the capture cross section has been further investigated. In general, $\sigma_n \neq \sigma_p$, however simulation results show that the shape of the C-V curve depends only on the value of the lowest between the σ_n and σ_p. Therefore, the analysis has been carried out by assuming $\sigma_n = \sigma_p$. In Figure 3.8 the C-V curve is reported for acceptor type traps close to the conduction band (E_{TC} = 0.3 eV) for two different values of capture cross section. Basically, the value of the capture cross section affects both the shape of the C-V curve and the extension of the hysteresis effect (it is assumed that electrons and holes have the same capture cross section). More in detail, the more the capture cross section decreases, the more the hysteresis effect increases. It has been pointed out that the effect of the capture cross section is correlated to the t_{RISE} and t_{FALL} values. The C-V curve is dependent on the slope of the voltage applied over the time and for a fixed t_{RISE} and t_{FALL}, it can be found a combination of the capture cross section value that gives the same shape of the C-V curve.

Therefore, the more the capture cross section is low, the more the t_{RISE} and t_{FALL} have to be increased to the exhibit the same shape of the C-V curve.

As a last result coming from the numerical analysis, the C-V curve does not change any more its shape when the distance from the trap band and the conduction or valence band becomes higher than about 0.5 eV. This is valid for a capture cross section $\sigma_n=\sigma_p= 1\cdot10^{-16}$ cm^2. This is aligned to the experimental results coming from [66], [81], where it is demonstrated as traps close to the valence or conduction bands are defined fast, while those close to the mid-bandgap are defined slow. This is in accordance with numerical results, since the hysteresis effect occurs when the time constant of the traps is comparable to the slope of the applied voltage coming from the C-V tracer.

3.3.2 Experimental results

Capacitance measurements have been carried out using a Solartron 1260 impedance analyzer [79], and the setup schematic is shown in Figure 3.9. The voltage applied to the DUT has two components: a DC voltage value on which a small signal AC signal is superimposed [80]. In Figure 3.10, the waveform of the total voltage applied on the device is shown. The DC voltage ramps up by steps and each step has a duration of the integration time to evaluate the capacitance. More in detail, t_{RISE} is the time for the sweep from -10 V to 10 V or 20 V, while t_{FALL} is the time to sweep from 20 V or 10 V to -10 V. All the C-V curve have been measured with $t_{FALL} = t_{RISE} = 300$ s.

Measurements have been performed at room temperature, with an AC voltage amplitude of 100 mV, a frequency of 1 MHz and a DC bias sweeping from -10 V and 10 V or 20 V (positive sweep) and vice versa (negative sweep).

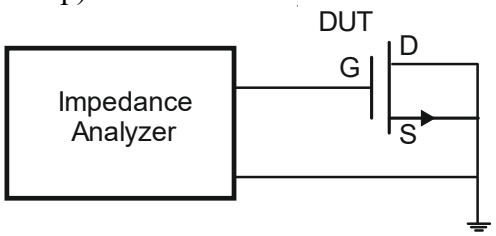


Figure 3.9. *Experimental setup for the C-V measurements.*

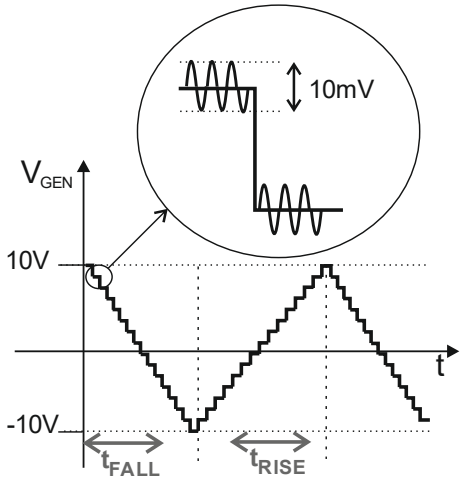


Figure 3.10. *Driving signal applied to the gate of the MOSFET during the impedance measurement.*

The lowest negative Gate voltage is due to the limit suggested by the datasheet of the DUT. The upper limit of the Gate voltage depends on the shape of the C-V curve of the specific DUT. As discussed in the previous Sections, the shape of the C-V curve depends on the voltage sweep direction and the slope of the voltage ramps. Therefore, depending on the measurements, the C-V curve has been measured over one or more periods of the waveform in Figure 3.3b. Two commercials SiC MOSFETs have been characterized by the measurement of the C-V curve and some relevant aspect have been observed. In Figure 3.11, the experimental C-V curve of the device Cree CMF20120 is reported. Two voltage sweeps have been performed in the range [-10, 20] V, with a voltage step of 0.3 V. The arrows direction indicates the voltage sweep direction. As a first comment to the experimental curve, the hysteresis effect occurs, but only for a part of the C-V curve. More in detail, the C-V curve exhibits a hysteresis effect for $V_G > -0.9$ V, while it suddenly disappears for lower voltage. This aspect is not compatible with the effect of fixed charges, while it is compatible with the numerical results reported in the previous Section since the hysteresis effect occurs only on one side of the C-V curve. The experimental C-V curve for $V_G < 5$ V shows a shape that is compatible with the curves reported in Figure 3.5-3.8. More in detail, the trap types that are

compatible with the C-V curve shape are acceptors or donors close to the conduction band. From the numerical results in Figure 3.5, Figure 3.6, Figure 3.7 and Figure 3.9 it is visible as the C-V curve hysteresis arises depending on the trap levels properties. The TCAD model is not calibrated, but it allows to claim that trap levels close to the conduction band affect the right hand side of the C-V curve, while the trap levels close to the valence band affect the left hand side of the C-V curve. Therefore, the numerical results show that the hysteresis effect in any part of the C-V curve is affected by the interface trap levels, as the experimental C-V curves show. In Figure 3.12, the experimental C-V curves are shown for Cree SiC power MOSFET C2M0080120D.

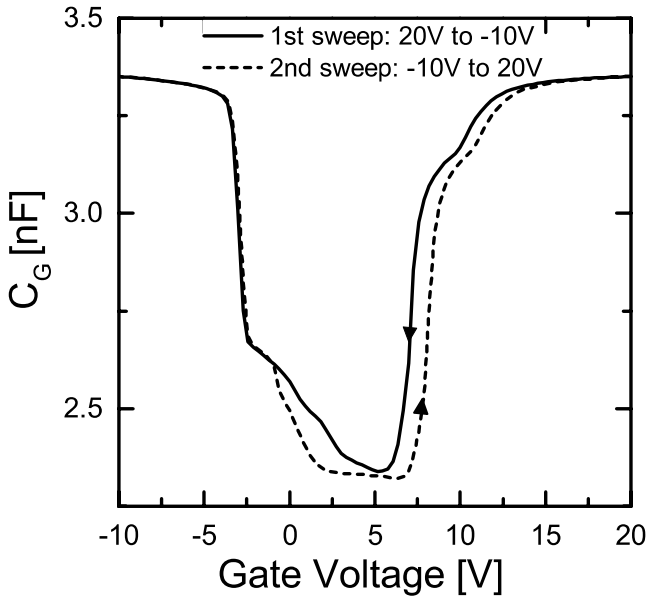


Figure 3.11. *Experimental C-V curves of the commercial SiC power MOSFET, Cree CMF20120. T=300K*

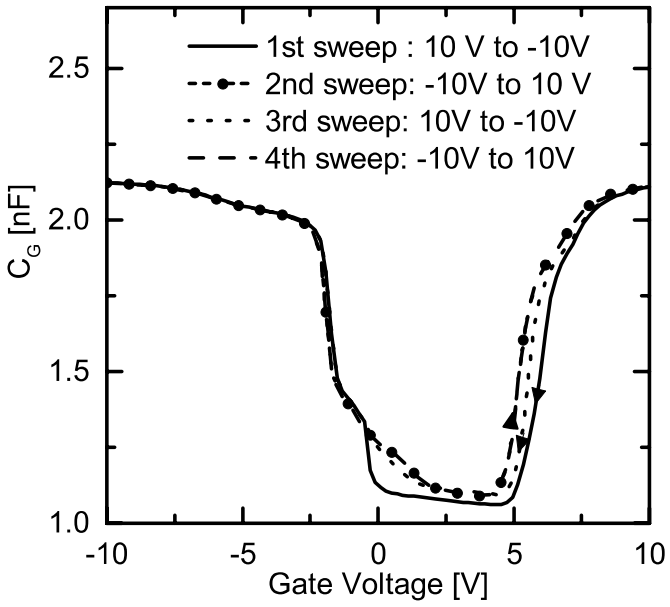


Fig 3.12. *Experimental C-V curves of the commercial SiC power MOSFET, Cree C2M0080120D. T=300K.*

For this device family two periods of the triangular waveform have been adopted to measure the C-V curve. This means that two sweeps are positive and two are negative. As expected from results in Figure 3.11, the hysteresis effect occurs only for V_G higher than a specific voltage (V_G > -0.3 V). The discussion reported for the previous Figure stands also for this Figure. However, an additional effect is visible: the shape of the negative slope sweeps depends on the number of sweeps. More in detail, while the second and the fourth sweeps are identical, the third one is closer to the second one compared to the first one. The difference between the first and the third sweep is not only of the distance to respect to the C-V curve of the second sweep, but the shape changes as well.

3.3.3 TCAD calibration approach

Theoretical and experimental evidences [56], [58]-[60], [65]-[69] highlight as the origin and the distribution of the traps at the SiC/SiO_2 interface is complex and its full experimental characterization requires specific measurement instruments. Moreover, the trap

distribution has a strong dependence on the specific technology adopted to made SiC MOSFET devices. The aim of this Subsection is the analysis of the effect of the SiC/SiO_2 interface traps on the C-V curve by means of TCAD simulations, with the scope of supporting the interpretation of the experimental C-V curves of a SiC MOSFET. It is assumed that the structure of the elementary cell is known in terms of design and doping profiles. From the numerical results, it has been shown that the shape of the C-V curve without traps does not change with the variation of the fixed charge. The only effect is the translation of the C-V curve, with a shift that depends on the sign and the value of the fixed charge. Therefore, from the numerical calculation of the C-V curve of the SiC MOSFET elementary cell without traps at the SiC/SiO_2 interface, it is possible to evaluate the minimum extension of the C-V curve (labelled "d"). When the traps are present at the interface, the extension of the C-V curve increases, and part of the C-V curve is warped. As shown in the previous Sections, depending on the trap type and the position of the trap band, the warping of the C-V curve changes. Moreover, an additive effect occurs when more than one trap band is considered at the SiC/SiO_2 interface. Therefore, a support to the comprehension of the interface trap properties effect on the experimental C-V curve shape of a SiC MOSFET can be carried out by following steps:

- Measurement of the C-V curve of the DUT at ambient temperature.
- Definition of the SiC MOSFET elementary cell in terms of materials, geometries, and doping profiles.
- Numerical calculation of the C-V curve without traps at the SiC/SiO_2 interface as the reference curve.
- Fitting of the SiC/SiO_2 interface traps of the TCAD model by fitting the experimental C-V curves, acting on both the fixed charge value (to keep into account for the translation) and the type, number and extension of multiple trap bands in forbidden bandgap of the SiC/SiO_2 interface.

In the following part of this Section, the calibration of the TCAD model on experimental data obtained from commercial device is presented. The TCAD model of the structure under test must consider

the complexity of a planar SiC MOSFET device structure. More in detail, the SiC/SiO_2 interface above the JFET region has different properties, compared to the channel region. This is due to the different technological processes adopted to obtain these regions. The novelty of the proposed TCAD model is the non-uniform modeling of the SiC/SiO_2 interface in terms of the traps distribution. More in detail, the SiC/SiO_2 interface is divided in two regions: 1) the region above the channel, region #1 in Figure 3.13 and 2) the region above the N-Drift, region #2 in Figure 3.13. This approach allows to model separately the interface properties. In a real device it is expected that the interface properties have a smooth spatial variation and the proposed approach is a realistic approximation, thus improving the accuracy of the TCAD model. In the following part, TCAD calibration results are shown for the two modelling approaches: the uniform interface approach (1 zone)

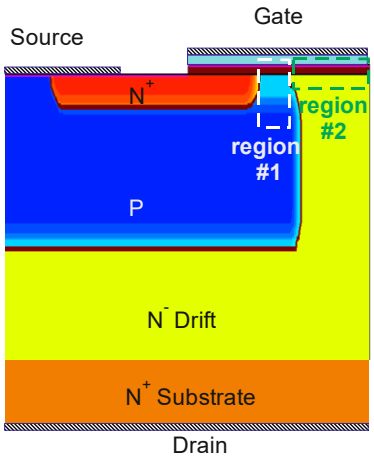


Figure 3.13. *Sketch of the TCAD structure (details as shown in Figure 3.1). It is highlighted the two different interface zones considered (region#1 and region #2).*

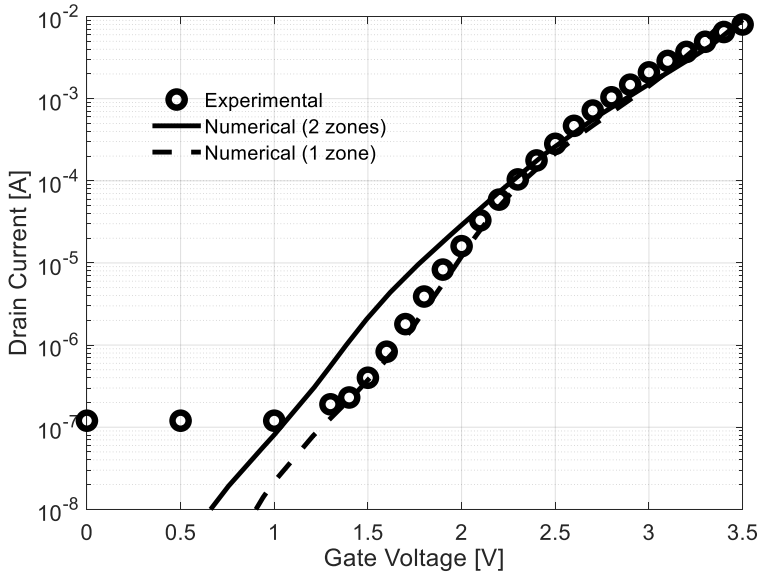


Figure 3.14. *Experimental I_D-V_{GS} curve (marker) and numerical C-V curves obtained with 1 zone approach (dashed) and 2 zones approach (line).*

and the non-uniform interface modelling (2 zones). In Figure 3.14, the experimental I_D-V_{GS} curve at ambient temperature is shown, together with the curves obtained from numerical single zone model and double zones model. Since the TCAD model was calibrated in terms of traps at the SiC/SiO_2 interface, the leakage current at $V_{GS} = 0$ V was not calibrated (the leakage current is due to bulk effects that are not kept into account in this context). As can be seen, the two numerical curves show similar results. In Figure 3.15 the numerical and experimental C-V curves are reported. It is clear that the numerical C-V curve of the structure with uniform trap distribution doesn't properly fit the experimental curve, even if the I_D-V_{GS} curve is matched, Figure 3.14. More in detail, the numerical C-V curve when the distribution is uniform matches the experimental curve for a voltage higher than the threshold voltage, where the capacitance is mainly due to the depletion of the Body region of the device and the SiC/SiO_2 interface above the JFET region is in accumulation. If the numerical double zone model is considered, a good matching among the curves is visible in all the

voltage range. The calibration was achieved by an iterative approach, acting on the traps distribution level and traps concentration. The starting guess for the iterative procedure comes from the literature available for MOS structures [65]. In Figure 3.16 the SiC/SiO_2 interface state density is reported for the two interface regions (A-B and B-C). While the interface traps above the channel region (A-B region) are acceptors, with a peak close to the conduction band, the interface traps above the JFET region are composed by both acceptor type and donor type. This aspect is a novelty compared to the state-of-the-art knowledge about the trap distribution in a SiC MOSFET structure. The latter has a more complex design compared to the standard MOS structure adopted for the SiC/SiO_2 interface characterization. In Table III the interface properties obtained from the calibration procedure are reported.

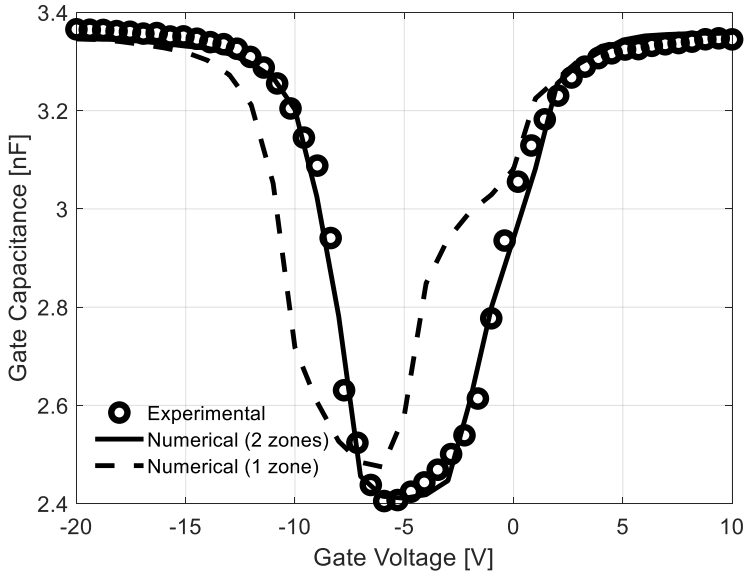


Figure 3.15. *Experimental C-V curve (marker) and numerical C-V curves obtained with 1 zone approach (dashed) and 2 zones approach (line)*

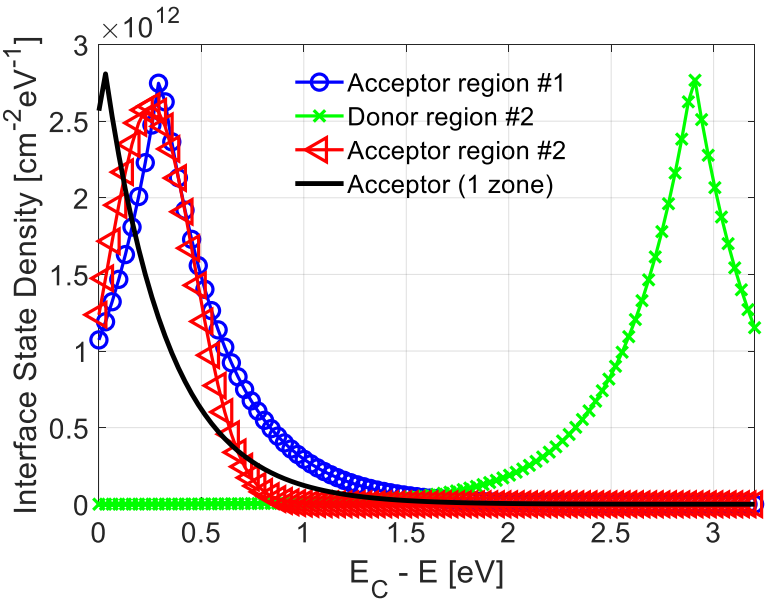


Figure 3.16. *SiC/SiO₂ interface state density in the bandgap and traps type for the two TCAD models. These properties have been obtained from calibration procedure*

Table III – Fixed charge and electron capture cross sections of the trap distributions in Figure 3.16.

	Region #1 (2 zones model)	Region #2 (2 zones model)	Uniform (1 zone model)
Fixed charge concentration [cm^{-2}]	$3.65 \cdot 10^{12}$	$2.2 \cdot 10^{12}$	$3.5 \cdot 10^{12}$
Capture cross section electrons (Acceptor) [cm^2]	$1 \cdot 10^{-18}$	$3 \cdot 10^{-18}$	$1 \cdot 10^{-17}$
Capture cross section electrons (Donor) [cm^2]	-	$1 \cdot 10^{-12}$	-

Chapter 4: Perovskite solar cells

This Chapter summarizes the results obtained applying impedance spectroscopy technique on perovskite solar cells. The Nyquist plots are analyzed, and an equivalent circuit is extracted using the procedure of Section 2.1.2. In the first part a brief introduction to perovskite solar cells is given, explaining the interest in this technology, Section 4.1, and its working principles, Section 4.1.1.
Section 4.2 is aimed at explaining the experimental data collected, the parameters extracted using the mentioned procedure and their physical meaning.

4.1 Perovskite solar cells

Perovskite solar cells are a new class of solar cells used for solar energy harvesting. These cells represent an efficient and promising alternative to silicon based solar cells. They have emerged in recent past years among all other technologies due to the record of a stable efficiency around 10% [82], obtaining new efficiency records in very short time. PSCs raised an efficiency greater than 23% in 2018 [83], attaining a better efficiency than state of the art CIGS, CdTe and polycrystalline Si thin film solar cells. Last year a stable perovskite solar cell has been developed with an efficiency record of 24.8%[84], Figure 4.1. This raise in the efficiency has been possible due to significant intrinsic optical and electronic properties of the perovskite in absorbing solar light. These excellent optoelectronic properties range from a high absorption coefficient to long electron/hole diffusion lengths, high charge carrier mobility and suitable bandgap. Furthermore, PSCs are a cost-effective technology due to the process low-temperature and less technological steps required with respect to conventional counterpart. The perovskite materials can be processed as a liquid-solution using relative low-cost materials and methods.

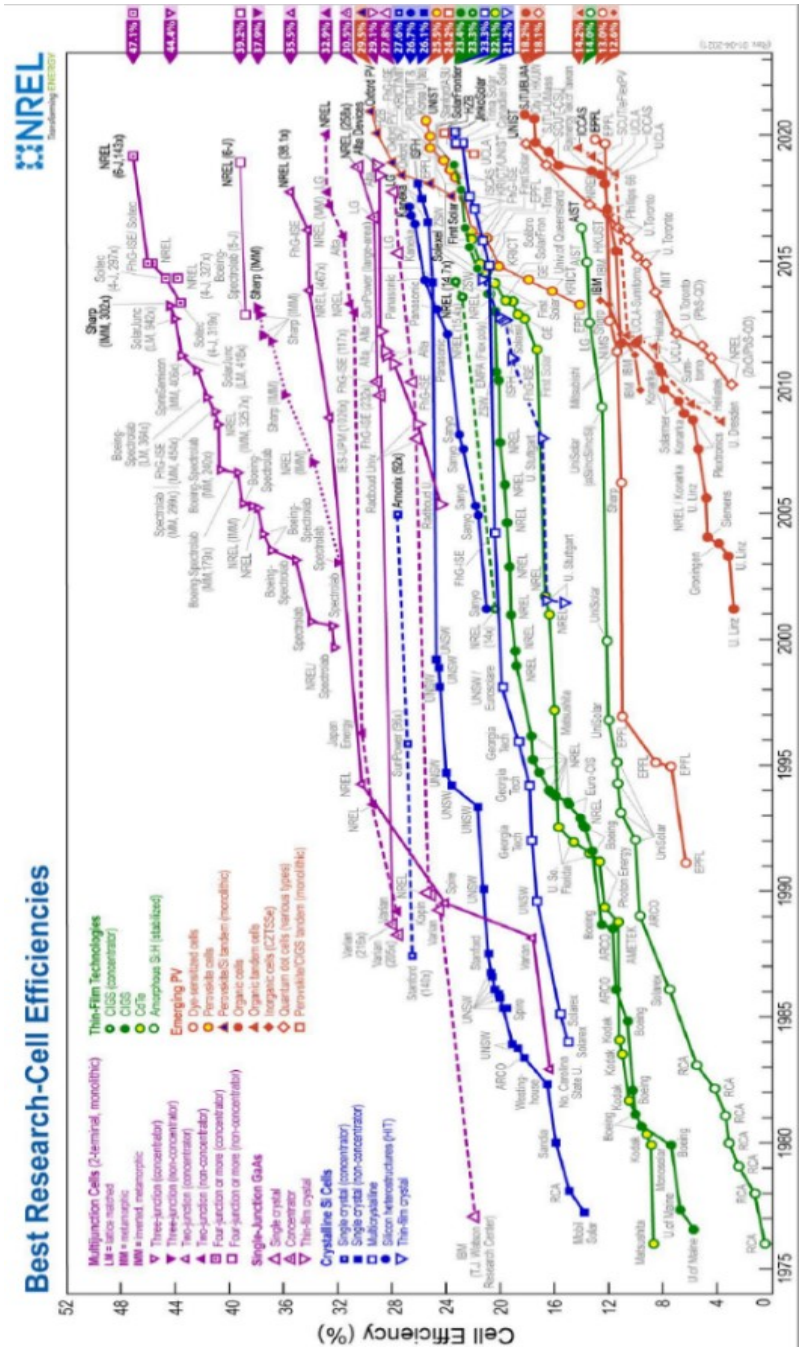


***Figure 4.1**. Chart of the highest confirmed efficiency for solar cells, plotted from 1976 to present days[83].*

4.1.1 Working principles

The physical basic structure of a perovskite solar cells consists of a perovskite layer involved in light absorption interposed between two conducting layers. More in general two main architectures exist for this technology: mesoporous and planar heterojunction. In both configurations, a layer of perovskite is included between a layer for electron transport (ETL) and another one who serves for hole transport (HTL). Hence, these transporting layers are fundamental for the efficiency of the solar cell. Charge transporting layers have the role of extracting photogenerated charges from the perovskite layer and let these charges to be collected at the corresponding electrode.
In this technology, the perovskite layer is assumed to be intrinsic and initially it is free of charge carriers. Perovskites can have different bandgap values depending on the particular composite adopted for the structure, Figure.4.2. In this figure, metal halide perovskite optical properties are presented. Metal halide compounds are semiconductor material with the general chemical formula AMX_3, where A are represented by monovalent cations, M are metal cations and X are halide cations. Very much attention has been directed to this compounds class because it is possible to change the energy bandgap by properly tuning different A, M or X ions. The energy bandgap variation has been widely studied both in experimental[86]-[88] and numerical case[89]-[98].

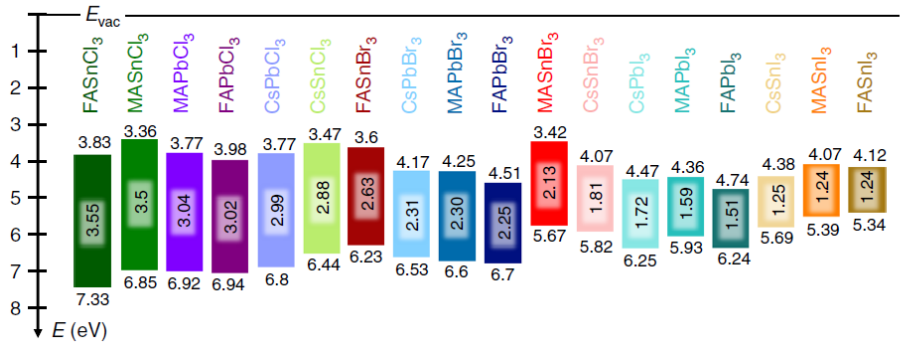


Figure 4.2. *Schematic energy level diagram of 18 halide perovskites. Different compounds are sorted in order of decreasing bandgap energy[85].*

However, in perovskite solar cells the transporting layers have to be heavily doped to form an ohmic contact with the corresponding electrodes. Generally, an accurate choice of charge transporting layers is made in order they match energy levels of Conduction or Valence band of the perovskite layer. In addition, they should ensure high efficiency in charge transport and accurate charge selectivity. For these reasons they have to exhibit high conductivity and good charge mobility.

The photons absorption in PSCs takes place in the perovskite layer and deals with free carrier generation. This last sentence can be explained from the various study published [99]-[101] reporting a small exciton binding energy for the perovskite active layer. This means that perovskite solar cells absorbing mechanism is different from that of organic solar cells, which implicate a large exciton lifetime[102]. In PSCs the mechanism of photogenerated charge separation can be ascribable either to an electron current injected in the ETL or a hole injection current flowing in the HTL. In fact, the electrons photogenerated near the perovskite/HTL interface should diffuse through the entire perovskite layer to reach the ETL/perovskite interface and be collected by ETL. This means that such free electrons have a high recombination probability during their path. Same consideration can be concluded for photogenerated holes near the ETL/perovskite interface. In some studies, it has been found that electron and hole injection mechanisms take place in the same timescale [103]. Perovskite material has a large photoinduced dielectric constant, thus reducing the Coulomb attraction existing between carriers and facilitating ambipolar current through an effective charge separation [104]. This mechanisms has been deeply studied measuring electron beam induced current in PSCs cross section [105], allowing the determination of where the current is generated. The current is higher in regions adjacent to the interface between selective contacts and perovskite, meaning an efficient electron and hole extraction at such interfaces. This indicates that perovskite allows the ambipolar transport and has a high diffusion length for both electrons and holes[103],[106]. Even if perovskite allows the charge separation and collection in a very effective way, selective contacts play a crucial role in the realization of a stable and high efficient solar cell with low recombination [107].

The stability of a perovskite solar cell is affected by mechanisms existing at the interfaces. Since this mechanisms are still not plenty understood, to achieve high performance it is necessary to optimize the active layer thickness and morphology or to exploit highly doped selective contacts with improved conductivity [108]. Another important aspect in determining the efficiency of these solar cells is related to the hysteresis arising in the I-V curve. In PSCs the shape of the measured I-V curve both in illumination and in dark conditions strongly depends on the voltage sweep applied and the scanning direction of such sweep. This problem imposes severe difficulty in the determination of PSCs efficiency [109],[110]. The origin of such phenomenon has been widely investigated from the scientific community. Some possible causes are the existence of surface traps in perovskite, the field modulated trapping/de-trapping processes, ferroelectric effect or ionic moved under applied voltage [109],[111]-[113].

PSCs are nanoscale device and the thickness and morphology of each layer strongly influence recombination and open circuit voltage, V_{OC}, which are key parameter for a solar cell. Some analyses reports that dominant recombination mechanism in these solar cells is related to non-radiative trap-assisted recombination [114]-[116]. In case of only radiative recombination the limit for V_{OC} is established around 1.33V [117]. The existence of non-radiative loss reduces however this limit to 1.1V. An important concern is the reduction of non-radiative recombination. This can be achieved by reducing defects in the perovskite and by improving interface quality between selective contacts and perovskite [118].

4.2 Experimental curves and results

In this Section, experimental impedance data are presented. These data are analyzed through equivalent electrical circuit and physical parameters are extracted using the procedure of Section 2.2.1.

4.2.1 Nyquist plots

IS technique has been applied on PSCs with the aim of characterizing such solar cells under stable working conditions. For this reason, the measurement time has been reduced as much as possible,

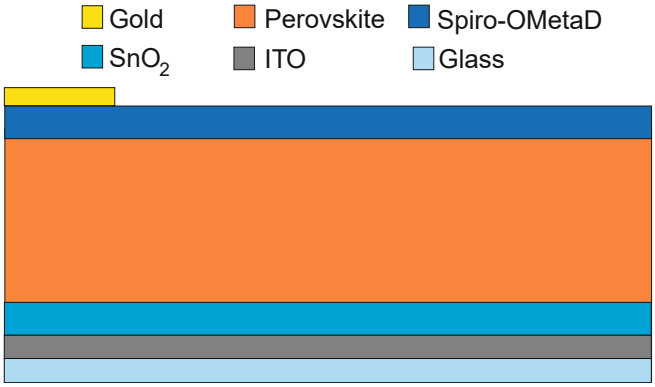
neglecting the increment of integration time or of the number of cycles which is a procedure to avoid noise in IS. Stability is a major concern in PSCs and long measurements can affect stability and lead to solar cells degradation. Nevertheless this latter is enhanced under illumination [119], it is important to perform IS under illumination condition to record change in perovskite material in such condition[120][121]. However comparative analysis between several samples can be done even at an illumination condition lower than the standard 1sun. PSCs stability can be investigated by performing I-V measurement before and after IS under illumination condition.

To increase stability during IS measurements it is necessary to have a controlled temperature and a device encapsulated. Both these conditions have been implemented in the following experimental measurements.

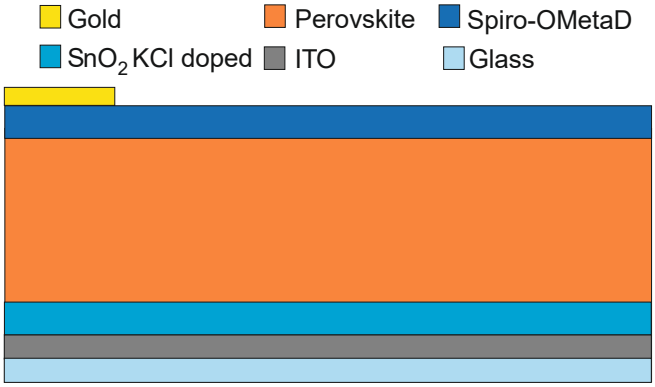
The frequency range starts from the highest frequency and span to the lowest frequency with a logarithmic sweep. In the following data, frequency range is [0.1 Hz, 1 MHz].

Unfortunately, in literature it is often compared impedance spectra only for a unique bias voltage, typically V_{OC}. This is not a right protocol since the characterization must be done in all the bias range because of the different Fermi level split. Carriers density is strongly affected by Fermi level position and several important parameters, such as recombination rate or conductivity, strongly depend on carriers density. In the following spectra, DC bias is swept from -0.2 V to 1 V.

The structures under test are presented in Figure 4.3. PSCs are processed on commercially available glass substrate with already ITO an SNO_2 layer embedded. ITO is a transparent conductive oxide while SNO_2 behaves as electron transport material. The hole transport material is given by Spiro-OMetaD. The perovskite used in both solar cells is $CH_3NH_3PbI_3$ which exhibit an energy bandgap of 1.55eV. The different between cell #1, Figure 4.3a, and cell #2, Figure 4.3b, lies in the doping of the ETL material which is performed only in cell #2.



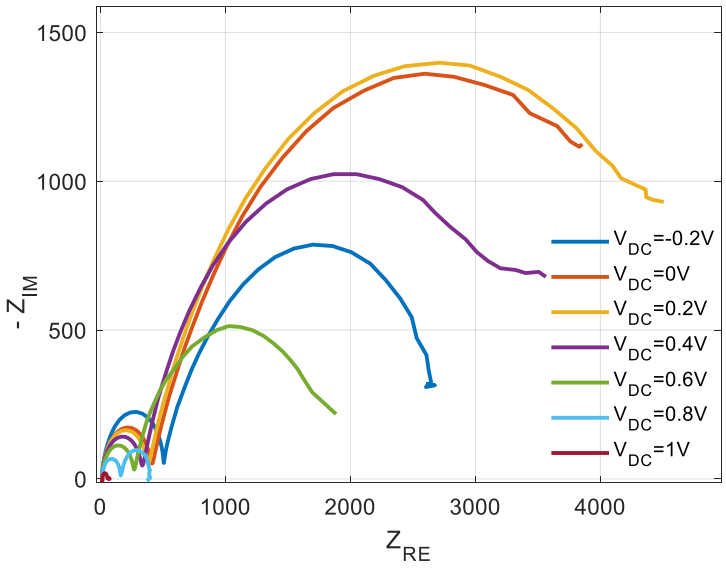
(a)



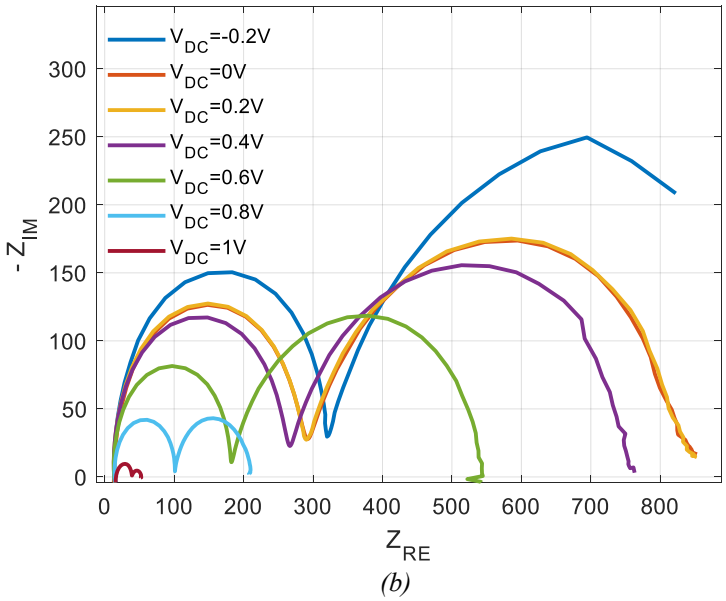
(b)

Figure 4.3. Perovskite solar cells analyzed in this Section. a) Cell #1 is formed by Au/Spiro/Pero/SnO_2/ITO and b) Cell #2 is Au/Spiro/Pero/SnO_2/ITO with a doped ETL layer.

Impedance spectra for both cell #1 and cell #2 are shown in Figure 4.4. These data have been acquired under an illumination of 1 sun. Same impedance spectra have been obtained under dark condition and are presented in Figure 4.5. It is possible to notice that the main difference between dark and illuminated condition in the impedance spectra is the presence of two semi-circular shape in illumination condition. The analysis of these data will be performed in following Subsection.



(a)



(b)

Figure 4.4. *Nyquist plots under an illumination of 1 sun of a) cell #1 and b) cell #2.*

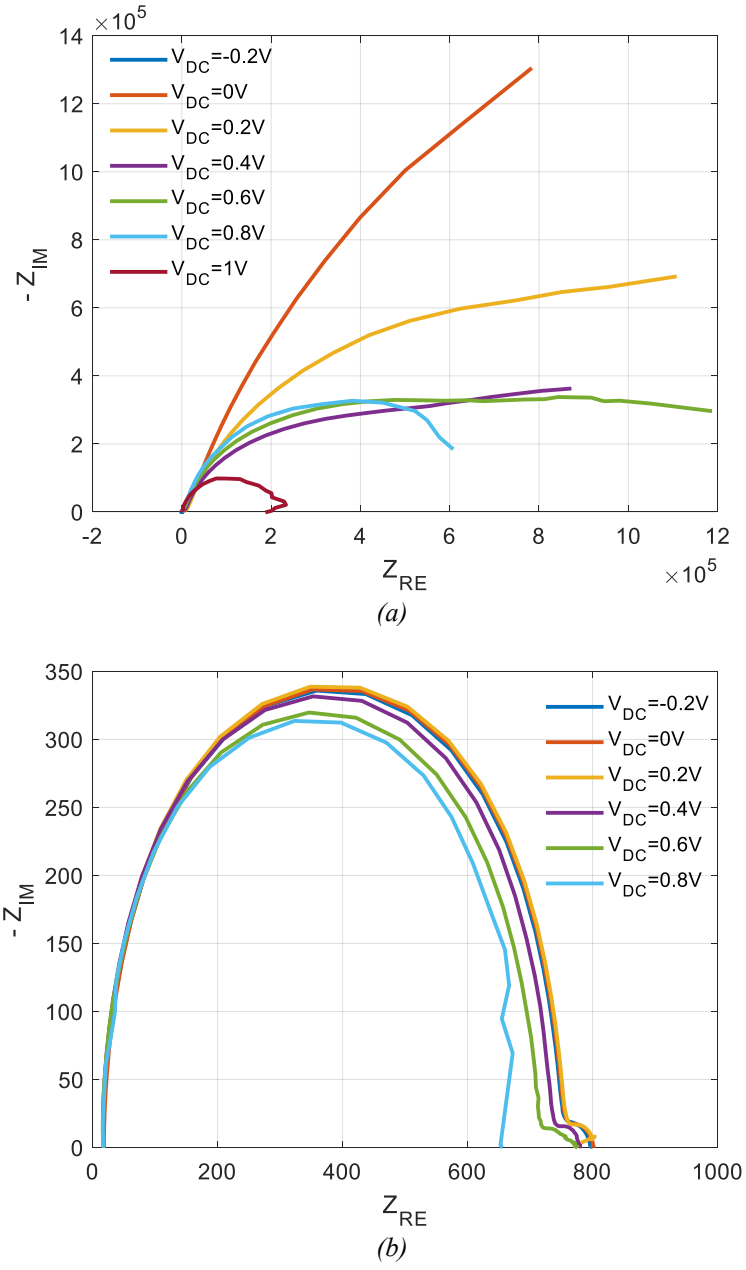


Figure 4.5. *Nyquist plots obtained in dark condition for a) cell #1 and b) cell #2.*

4.2.2 Extracted parameters

From the previous impedance data, it is possible to extract some physical parameters in order to compare the two PSCs considered. The interpretation of these data has been performed by using an equivalent electrical circuit. The specific model adopted in this case has been chosen among the numerous configuration available in literature [122]. The circuit configuration is constituted by the series of two RC pairs and a resistance, Figure 4.6. A first RC pair takes into account for the behavior of the PSC in the low frequency domain, while the other emulates the high frequency AC response of the structure.

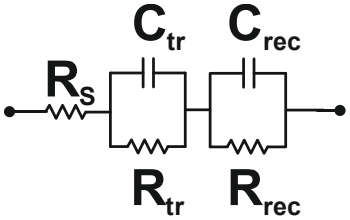


Figure 4.6. Equivalent electrical circuit employed for the analysis of the PSCs impedance data.

The high frequency arc in impedance spectra is usually attributed to the electron/hole transporting in ETL/HTL and charge transfer at the interface perovskite/HTL and ETL/perovskite[123]. It is possible to refer to such resistance as R_{tr}. The low frequency RC pair is related to perovskite active layer and the resistance is referred to as R_{rec}. The following expression have been found in literature for these value[123]:

$$R_{tr} = \frac{L}{A\sigma} \tag{4.1}$$

where A is the active area, σ is the conductivity and L is the perovskite layer thickness.

$$R_{rec} = \frac{1}{A}\left(\frac{\delta j_{rec}}{\delta V}\right)^{-1} \tag{4.2}$$

where j_{rec} is the recombination current density. From these parameters the diffusion length can be calculated as:

$$L_d = \left(\frac{R_{rec}}{R_{tr}}\right)^{\frac{1}{2}} L \tag{4.3}$$

The recombination resistance values obtained in the considered case are presented in Figure 4.7.

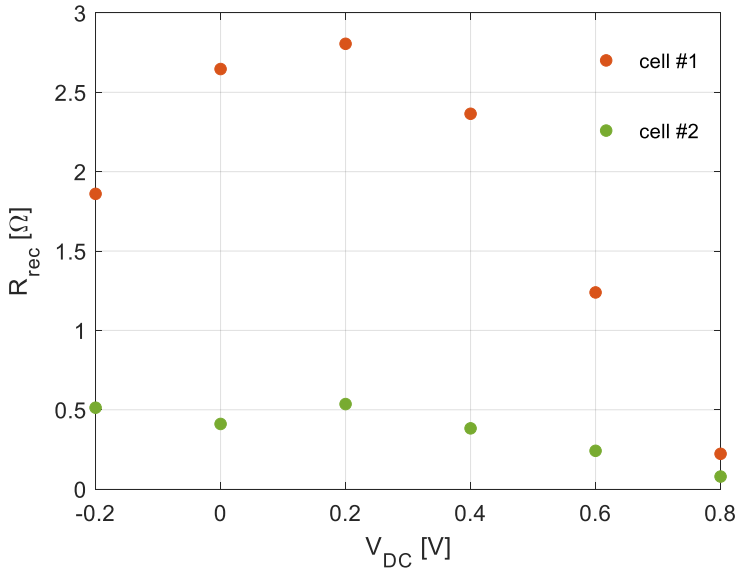


Figure 4.7 *R_{rec} behavior with applied bias for cell #1 (orange dots) and cell #2 (green dots).*

The lower value obtained for all the DC bias range for cell #2 means that higher recombination current occurs in this structure compared to the other one. This parameter allows the characterization of perovskite layer. The values obtained for the diffusion length are reported in Figure 4.8.

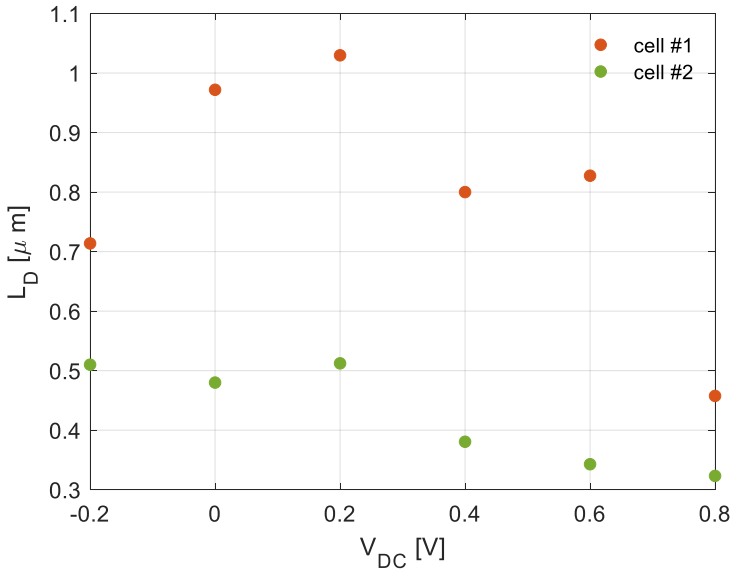


Figure 4.8. *Diffusion length obtained for cell #1 (orange dots) and cell #2(green dots).*

The higher value is obtained for cell #1, which has not undergone the doping of SnO_2. This analysis seems to suggest that ETL doping process has induced some problems in perovskite morphology or crystallinity.

Chapter 5: Schottky solar cells

In this Chapter, impedance spectroscopy technique has been applied to Schottky solar cells. In the first part a brief introduction to Schottky solar cells is given, with a major focus on Graphene-Silicon solar cells, Section 5.1, and their working principles, Section 5.1.2. Section 5.2 is aimed at explaining the experimental data collected, the parameters extracted and their physical meaning. The Nyquist plots are analyzed and an equivalent circuit configuration is extracted using the procedure of Section 2.1.2. Two different front contact technologies are compared using this approach. It is shown that standard contact technology, made of gold contact, gives rise to strongly distorted impedance spectra and that such a distortion is due to the contact resistance. Conversely, in the case of new contact technology, made of graphite contact, the impedance spectra are extremely regular, as expected for ohmic behaving contacts. In Section 5.3 experimental C-V curves are shown for different frequencies. The multiple peak behavior, explored in Chapter 2, is found also in experimental capacitance profiling. In this Section the modelling of the Graphene-Silicon solar cell using Sentaurus TCAD environment is presented, together with the calibration procedure between numerical and experimental data.

5.1 Schottky solar cells: Graphene-Silicon cells

Schottky solar cells have been studied and exploited starting from second half of past century [124]. This type of solar cell is very attractive because it has the great advantage to be a low cost and easy fabricable solution compared to conventional silicon solar cells. Nevertheless, to form a Schottky junction there is the need of a metal layer with a proper thickness. This condition has the huge drawback of absorbing part of the solar radiation which will not take part in the solar conversion process. To overcome this problem, new materials have been exploited as metal layer. Graphene material has attracted the

scientific community attention because of its both electrical and optical properties [125]-[130]. This material has a very high carrier mobility and at the same time it is optically transparent. For these reasons, graphene has immediately become a promise for new generation of Schottky solar cells. In one decade, G/Si solar cells experienced a noticeable efficiency improvement, achieving an efficiency of 15.6% in 2015[131]. These solar cells are processed at low temperature with respect to conventional solar cells, and the cost of the materials is lower. Even if they represent a potentially cheaper alternative to conventional solar cells, they are not appropriate to large scale production caused to some problems that still affect this technology, such as low stability in conventional condition operations and still low efficiency. The latter is the most important aspect to improve. The conventional G/Si solar cell structure is composed by a Si substrate with a G layer on the top, the back contact is in Al while the front contact is in Ag or Au. The efficiency can be improved by performing chemical doping, by improving the contact technology, by depositing anti-reflection coating or by passivating the G/Si interface. The chemical doping process can improve some aspect of the G/Si solar cell. The first factor is the enhancement of the Φ_B at the Schottky interface formed between G and Si[132]. The second improvement is represented by the reduction of the sheet resistance of the G material[133]. If an anti-reflection coating is inserted in the solar cells structure, the light reflection will be reduced and the light will also be trapped by several internal reflection in the structure. Several types of anti-reflection coating have been used in literature, such as TiO_2 [131], graphene oxide[134] and colloidal antireflection coatings[135]. Also contact technology plays an important role in determining the efficiency, as already stated in literature[136][26]. The surface passivation is another important factor to consider while improving efficiency. The quality of the active interface boosts the performance of the overall device. In the case of G/Si solar cell the active interface is forming between G and Si. Such interface has a high number of defects. More in detail, there are an important number of dangling bonds which behaves as recombination centre for the photogenerated carriers[137]. This latter is not the only drawback of a high defects density at the G/Si, since the Fermi level pinning can occurs due to defects and it can results in a higher saturation current and lower V_{OC} value[138].

5.1.1 Working principles

Schottky barriers diodes embed a metal-semiconductor interface so that SBDs working principle is based on the barrier existing at such interface [139]. The Schottky barrier model is shown in Figure 5.1. If the metal and the semiconductor are not in contact, the band diagram is similar to that of the upper part in Figure 5.1. Conversely, when there is contact between the two material the band diagram starts to bend, as shown in the lower part of Figure 5.1. The band diagram of Figure 5.1 assumes that there is not an interfacial layer between metal and semiconductor. Depending on the height of Φ_B, the first order SBDs behaviour can be exploited. The barrier height is certainly affected by the metal work function and semiconductor electronic affinity, as seen in Section 2.2.1. The energy difference between the vacuum energy level (E_{vac}) and the Fermi level (E_F) can be defined as the work function. The energy difference between the upper edge of the conduction band and the vacuum energy is the electron affinity of the semiconductor. After the contact between the metal and semiconductor material, the ideal barrier height, Φ_B, can be calculated as:

$$\phi_B = WF - \chi \tag{5.1}$$

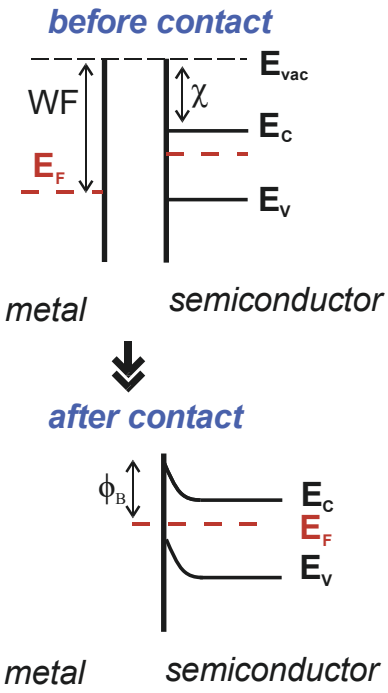


Figure 5.1. *Band diagram of a Schottky interface before contact and after intimate contact.*

According to this theory, the barrier height exclusively depends on work function of the metal and semiconductor electron affinity. It seems easy to vary the height of the Schottky barrier by simply changing the work function of the metal, and hence the specific metal used in the device structure. On the other hand, the Schottky barrier height is sometimes unvaried by changing metal (and work function). Experimentally it is found that the barrier height for some semiconductors, such as Ge, Si and GaAs results difficult to vary by modifying the metal work function[140]. This latter is attributed to Fermi level pinning in the semiconductor, which consists in the pinning of this energy level due to imperfection or surface states at the contact formation. In reality, barrier height is not influenced only by metal work function and electron affinity, but it is also depending on surface states and defects/traps [141]. Barrier height also weakly depends on substrate doping due to image force barrier lowering [142][143].

If a metal-n type semiconductor is considered, the conduction mechanisms are the followings, Figure 5.2. Depending on the substrate doping, the main conduction mechanisms is different. If the substrate is lightly doped, the currents flow mechanism is the thermionic emission, Figure5.2a [144]. If the substrate doping is intermediate, the main mechanism is the thermionic field emission, where carriers are thermally excited to an energetic level where the barrier is enough narrow for tunnelling [145], [146]. If the doping level is high, then the barrier results sufficiently narrow at or near the upper conduction band edge and electrons flows because of tunnel mechanism.

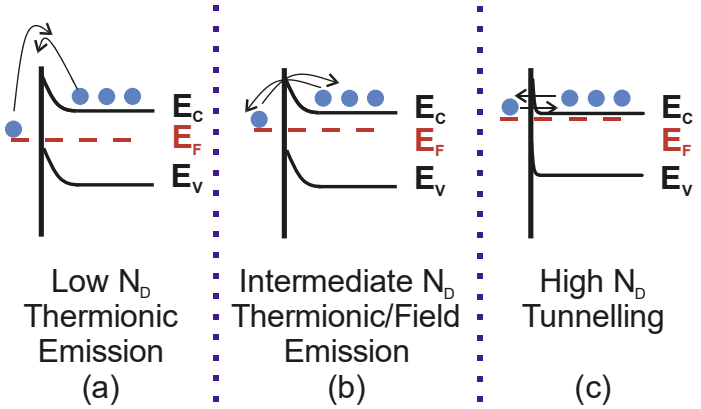


Figure 5.2. *Current mechanisms existing across the Schottky interface for different type of semiconductor doping.*

5.2 Impedance data: experimental curves and results

In this Section, experimental curves obtained on G/Si solar cells are shown. Impedance data are interpreted in terms of electrical equivalent circuit and results are used to characterize a new contact technology for G based solar cells. This new technology exploits a graphitic glue to form the top contact, instead of gold. The performance of solar cells made by means of both above mentioned contacts are compared and interpreted. The extracted circuit configurations for the two different types of solar cells allows to isolate, from the global impedance, the contributions given by the Schottky interface (G/Si

interface) and that of contact-graphene interface (gold–graphene in one case, or graphitic glue–graphene in the other case). The knowledge of these contributions allowed the extraction of the barrier height forming at the Schottky interface, the work function of the graphene and the contact resistance.

5.2.1 Experimental Nyquist plots

Measurement setup used to collect impedance data consists in a 1260 Solartron Impedance Analyzer. The frequency was swept from 1 Hz to 63.5 kHz with a logarithmic sweep, while DC bias was scanned from −1 V to 0.5 V. These measurements were performed on two types of solar cells. The processing of the solar cells is briefly summarized in the following. Multi layers graphene films were grown by CVD of ethanol on Cu substrates at 1070 °C [147]. The flow chart reported in Figure 5.3 shows the cells fabrication process. The starting substrates were commercial n-type Si wafers, 1 Ω cm, with a thermal SiO_2 layer (300 nm) on both sides. The wafers were patterned through HF etching of SiO_2, and an active area of 0.76 cm^2 was obtained. The back contact was realized by evaporating Al on the back side of the wafer. The graphene films were transferred onto the cells by a cyclododecane (CD)-supported transfer [148]. Two kinds of top contacts were realized. The first was made by standard gold deposition by e-gun evaporation; the second was obtained through a colloidal graphitic glue, spread over the graphene outside the active area.

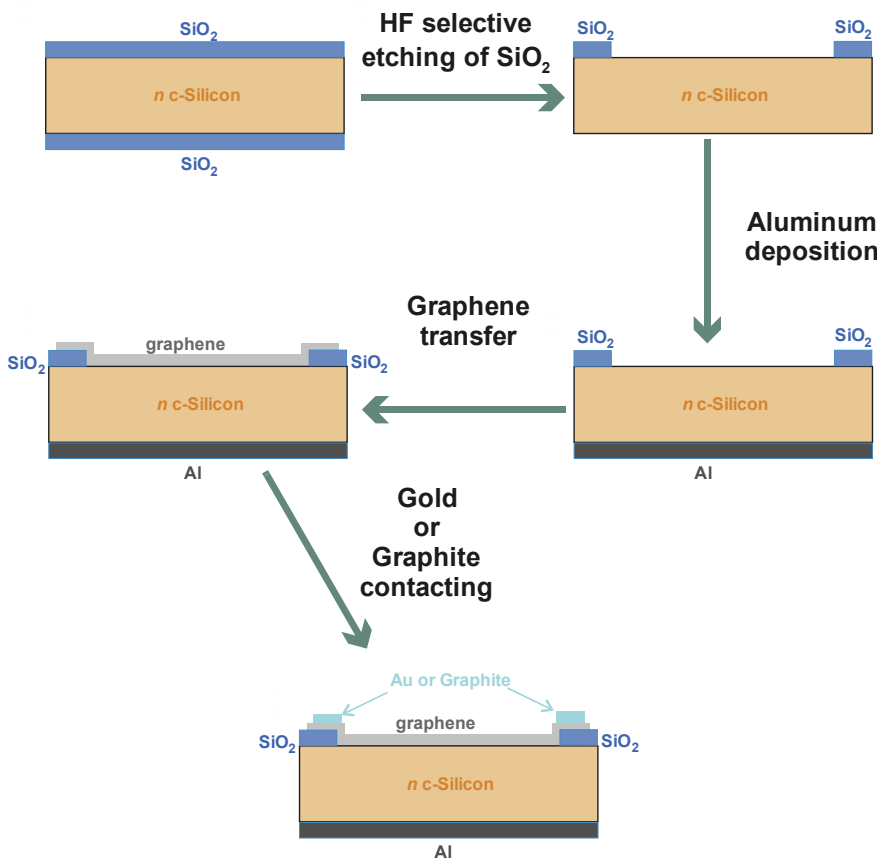


***Figure 5.3**. Schematic diagram of graphene-silicon (G/n-Si) solar cell fabrication*

Explained the two consider structures, it is possible to better understand Nyquist plots and their difference in the impedance data collected. In Figure 5.4a, Nyquist plots for the solar cell with gold contact (Au/G/Si/Al) are shown. These Nyquist plots shapes are very different from the semi-circular shape that should be observed if only the Schottky interface was dominating the AC behaviour. This means that the measured impedance is the result of the contribution of multiple reactive behaviours, rising from the various existing interfaces in the considered device. Adopting the automated procedure explained in Section 2.1.2, the equivalent circuit configuration of Figure 5.4b was extracted from the experimental data of Figure 5.4a. As an example, in Figure 5.4c, d, the Nyquist plots achieved by means of the above-

mentioned circuit representation are compared with the experiments corresponding to the DC bias of 0.1 V. As we can see, there is an almost perfect overlap between experiments and model, for both real and imaginary part of the impedance. This means that the circuit configuration extracted from the automated procedure, which contains 4 lumped resistance and 3 lumped capacitors, is suitable to model the impedance in the whole frequency range and for all considered DC biases. The complete Nyquist plot achieved by composing the real and imaginary parts, compared with the experiments, is reported on Figure 5.4e. Equally good results were achieved in the whole range of DC biases. The lumped parameters, resistances and capacitances, making the circuit model suitable in the complete bias range, are shown in Figure 5.5 a, b, respectively. The values of such parameters, along with the corresponding circuit model, allow to quantify the role of each interface in the overall behaviour. Indeed, with reference to Figure 5.5a, C_j can be attributed to the graphene–silicon interface; in fact, for negative bias, the typical dependence on the width of the depletion region can be recognized, while, for positive bias, the decreasing of C_j can be attributed to carrier injection phenomena. The other two capacitances, C_{Au} and C_{Al}, model the gold–graphene interface and the aluminium-silicon interface. In principle, these two capacitances cannot be distinguished each other, however, in this thesis, it is proposed that the highest is ascribable to the gold–graphene interface. This assumption is confirmed by looking at the behaviour of the corresponding resistance values, R_{Au} and R_{Al}. More in detail, the decreasing of R_{Au} and R_j for positive DC bias is coherent with the nature of the junction. In fact, they are differential resistances and they start decreasing if the junction is injecting carriers. Conversely, R_{Al} slightly increases when the DC bias is positive because the aluminium–silicon junction is reversed biased.

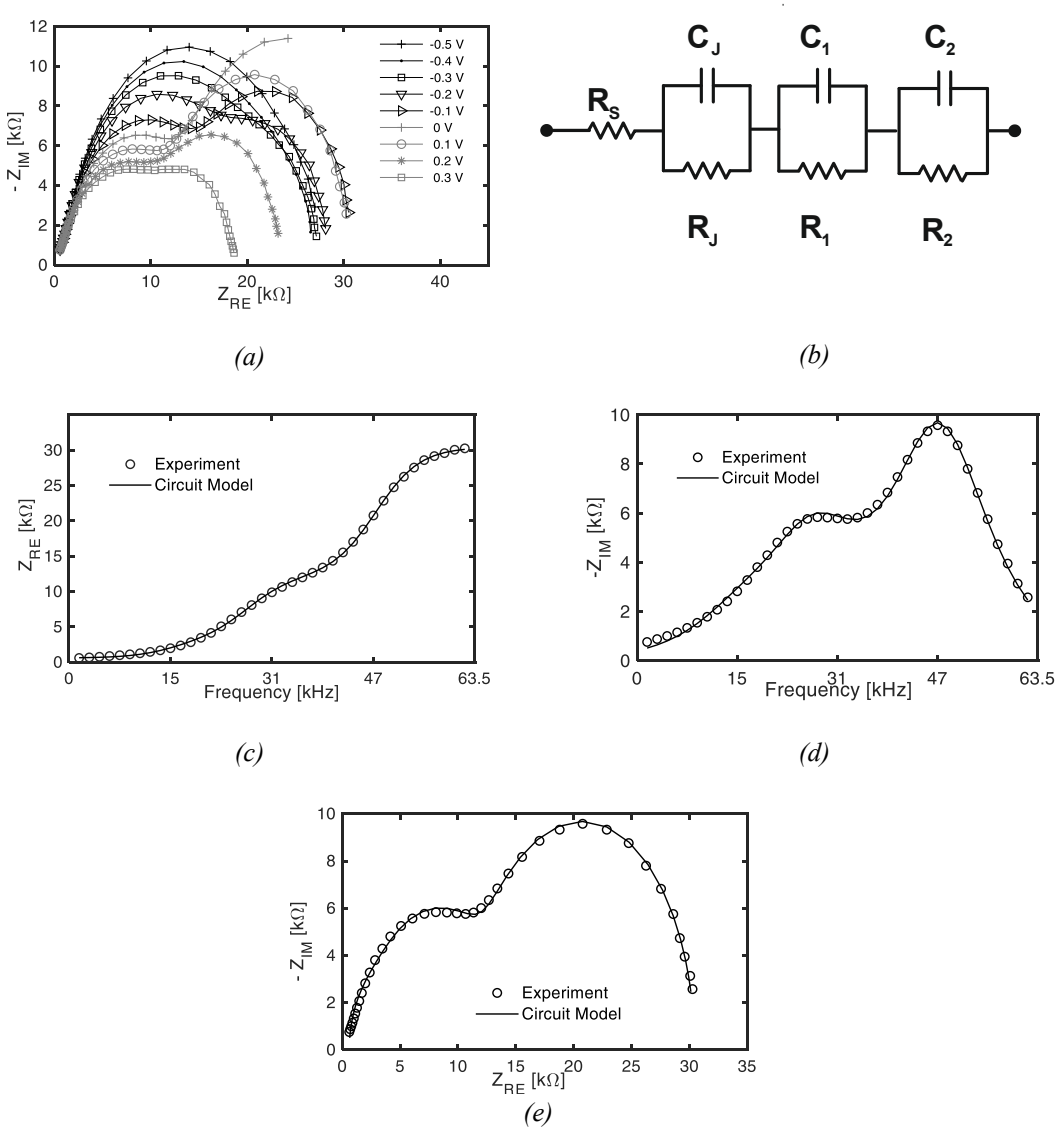
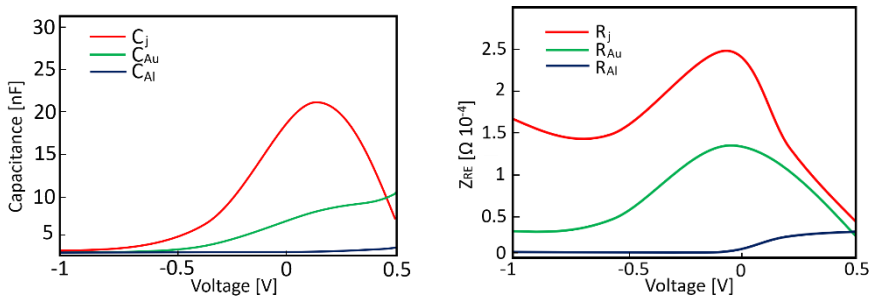


Figure 5.4. *Au/G/Si/Al solar cell a) Nyquist plot. b) Equivalent circuit extracted from the data of Figure 5.4a. c) Comparison in frequency between the real part of the impedance obtained from the circuit model extracted and the experiment data, for a DC bias of 0.1 V. d) Comparison in frequency between the imaginary part of the impedance obtained from the circuit model extracted and the experiment data, for a DC bias of 0.1 V. e) Nyquist plot comparison between the impedance obtained from the circuit model extracted and the experiment data, for a DC bias of 0.1 V.*



(a) *(b)*

Figure 5.5. *a) Extracted lumped capacitances values. The depletion capacitance, C_j, is dominant, while the C_{Au} and C_{Al} are associated to the interface between gold and graphene in one case or aluminium and silicon in the other. b) Extracted lumped resistances values. The resistance associated to the graphene–silicon junction is R_j, while the R_{Au} and R_{Al} are associated to the interface between gold and graphene in one case or aluminium and silicon in the other.*

The same analysis was performed on the solar cell with the graphitic glue contact (Graphite/G/Si/Al). The Nyquist plots are presented in Figure 5.6a. As can be seen, the Nyquist plots are almost semi-circular. This fact is a strong indication that less active interfaces are not playing an important role in this device. This assumption is corroborated by the circuit extraction procedure: indeed, only one capacitance dominates the behaviour of the solar cell, with only a marginal contribution of the aluminium-silicon interface. Therefore, the graphite-graphene interface does not behave as a parasitic junction, as is the case of the gold–graphene interface.
In Figure 5.6b, the extracted circuit configuration for the solar cell with the proposed front contact is shown. Only two lumped capacitances and three resistances are needed to describe the behaviour of the solar cell with graphitic front contact. The comparison of the modelled real and imaginary part of the impedance with the experiments are shown in Figure 5.6c,d (DC bias equal to 0.2 V). The complete Nyquist plots are reported in Figure 5.6e.

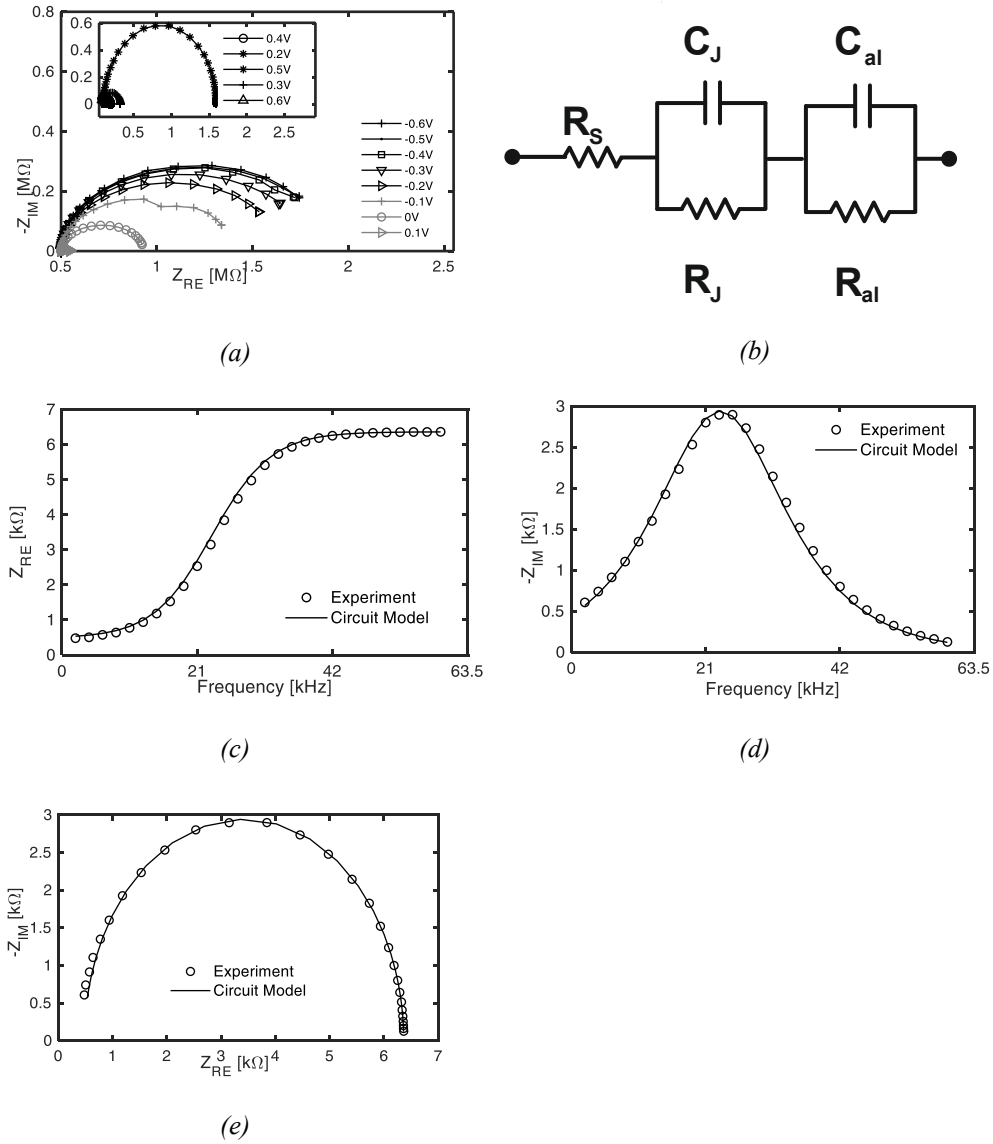


Figure 5.6. *Graphite/G/Si/Al solar cell* ***a)*** *Nyquist plot comparison between the impedance obtained from the circuit model extracted and the experiment data, for a DC bias of 0.1 V.* ***b)*** *Equivalent circuit configuration.* ***c)*** *Comparison of the real part of the impedance obtained from the experiment and from the circuit model, for DC bias equal to 0.2 V.* ***d)*** *Comparison of the imaginary part of the impedance obtained from the experiment and from the circuit model, for DC bias equal to 0.2 V.* ***e)*** *Nyquist plots comparison, for DC bias equal to 0.2 V.*

5.2.2 Extracted Parameters

Adopting the extraction procedure, the junction capacitance has been distinguished from the other contribution of the total impedance. The availability of the junction capacitance (different from the overall capacitance measurable at the terminals) made it possible to build the capacitance vs voltage (C–V) plot for each given frequency, as reported in Figure 5.7. Junction capacitance is varying with applied voltage but also with frequency, as in the mentioned Figure. The variation of the junction capacitance with frequency is due to the different behaviour of existing traps/defects/impurity with frequency. Traps can follow slow frequency signals while it is not the case for high frequency.

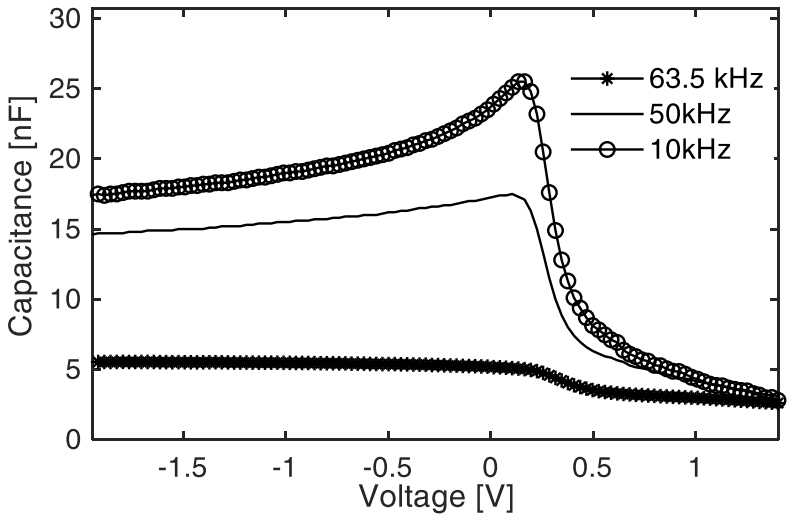


Figure 5.7 *C–V plots of the Schottky junction capacitance for the solar cell with graphitic contact.*

As it is already explained in Chapter 2 , curves like these allow for the evaluation of the built-in voltage, V_{bi}, by exploiting the following formula [139]:

$$\frac{1}{C^2} = \frac{2}{(q\varepsilon_s N_D)}(V_{bi} - V). \tag{5.2}$$

The plot of $1/C^2$ versus the voltage is reported in Figure 5.8, for the C–V curve taken at a frequency f = 10 kHz. It is easy to recognize that the intercept with the x axis is V_{bi}. From the built-in voltage, the barrier height can be evaluated as well [139]:

$$\phi_B = V_{bi} + \frac{kT}{q}\ln\left(\frac{N_C}{N_D}\right) \tag{5.3}$$

Where in the considered case the silicon doping concentration is N_D= $5\cdot10^{15}$ cm^{-3}, and N_C is the equivalent density of states. By summing the barrier height derived from measurements, ϕ_{Bmeas}, and the electron affinity of the silicon (4.1 eV), the work function, W_F, of the graphene has been obtained. Numerical values are reported in Figure 5.8.

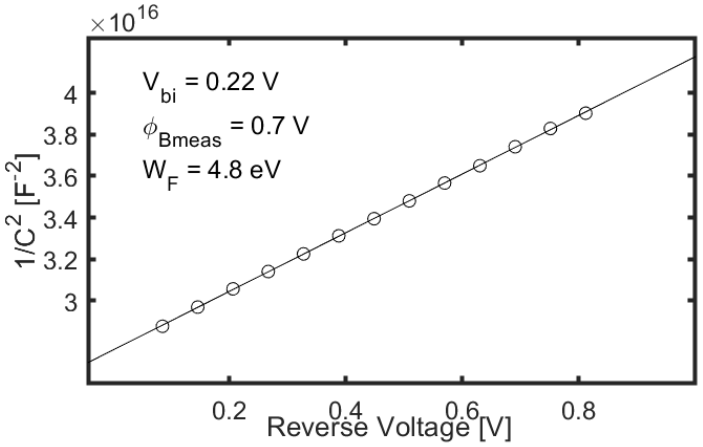


Figure 5.8. *$1/C^2$ versus V plot. Dots represents experimental values, while the straight line is the interpolating line.*

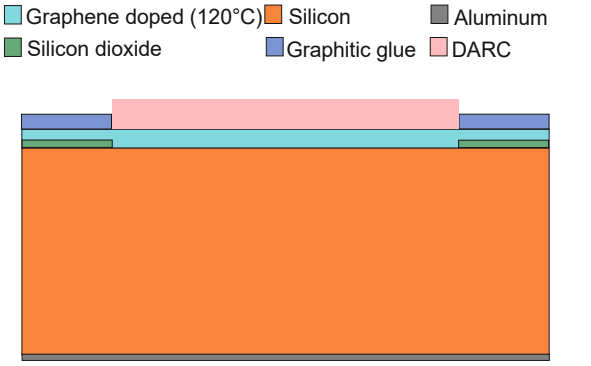
5.3 C-V curves: experimental curves and results

In this Section experimental C-V curves are presented for G/Si solar cells. A TCAD model developed in Sentaurus to analyze the considered structures is also shown. The specific case of an experimental G/Si solar cell capacitance with an additional peak is studied and the calibration of the TCAD model on such curve is performed.

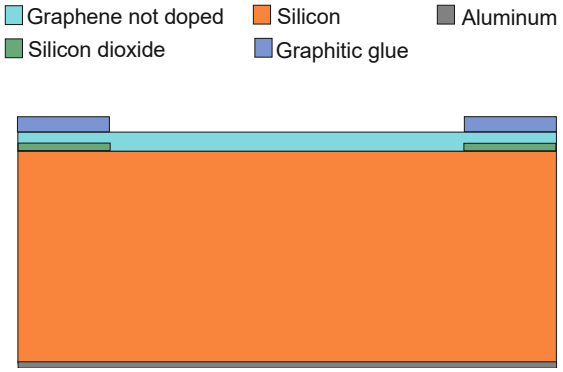
5.3.1 Experimental Capacitance curves

In this Subsection the C-V curves of three different G/Si solar cells are shown. The structures under test are presented in Figure 5.9. These solar cells have been realized through CVD deposition of few graphene layers on n type Si substrate. The front contacts are realized with colloidal graphitic glue, while the back contacts are in Al. In the first solar cell, Figure 5.9a, the graphene has been doped at 120 °C and there is a DARC (double antireflection layer coating) on the solar cell active area. In the second solar cell, Figure 5.9b, the graphene is not doped at all, while in the third solar cell, Figure 5.9c, the graphene has been doped at 100°C.

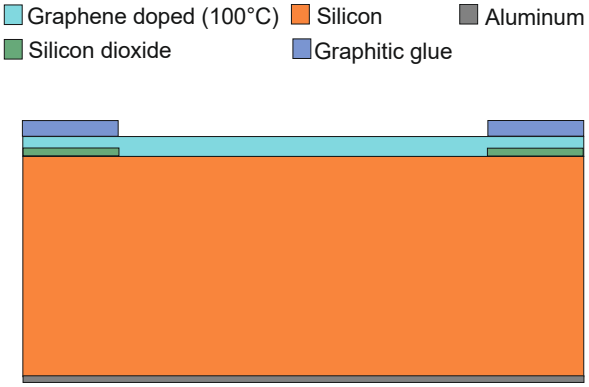
The C-V curves obtained in dark condition for such structure are presented in Figure 5.11. The C-V curves have been obtained using Solartron 1260 Impedance Analyzer. The imposed DC has been swept in the range [-1V,1V]. The frequency has been changed from 1kHz to 9kHz in steps of 1 kHz. The results for cell1 is shown in Figure 5.11a. As it is possible to notice from Figure 5.11, the capacitance profiling of the solar cells of Figure 5.10 b, c, shows the typical trend of a Schottky solar cell. This is not the case of the solar cell which has graphene doped at 120°C. The resulting capacitance of this solar cell shows an additional peak at high forward bias and, moreover, this second peak is higher as frequency is lower. In order to understand this behaviour, the development of a TCAD model has been necessary. Such model is explained in following Subsection.



(a)

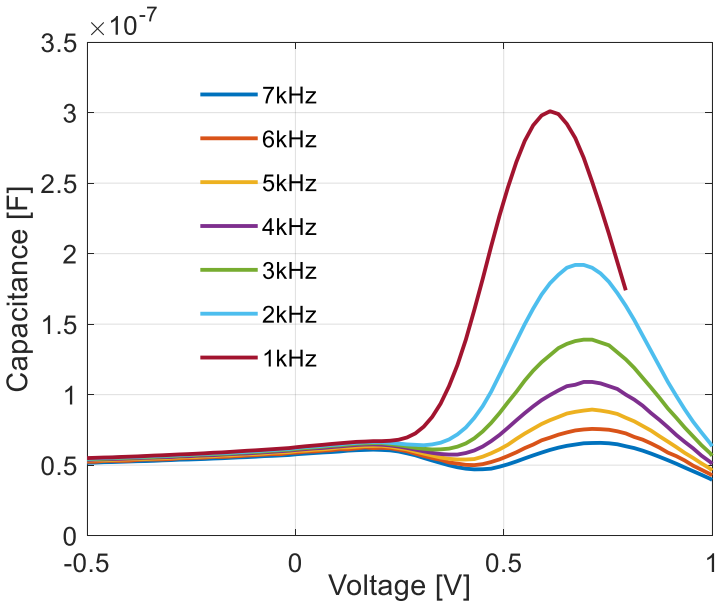


(b)

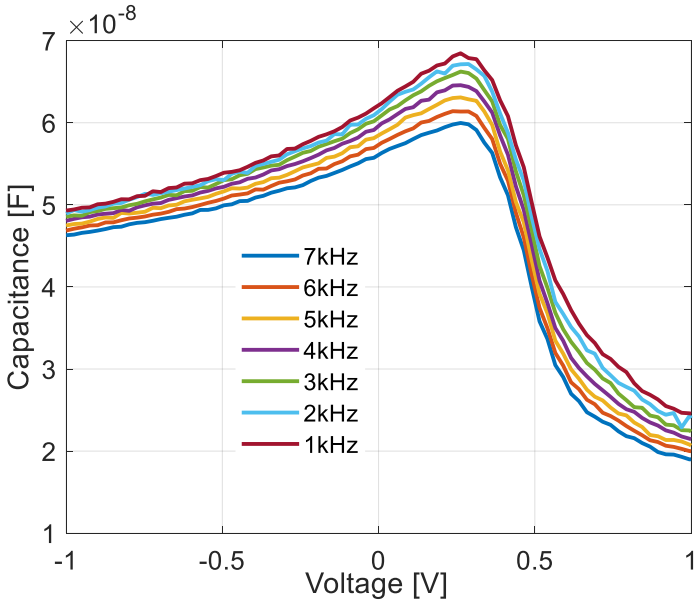


(c)

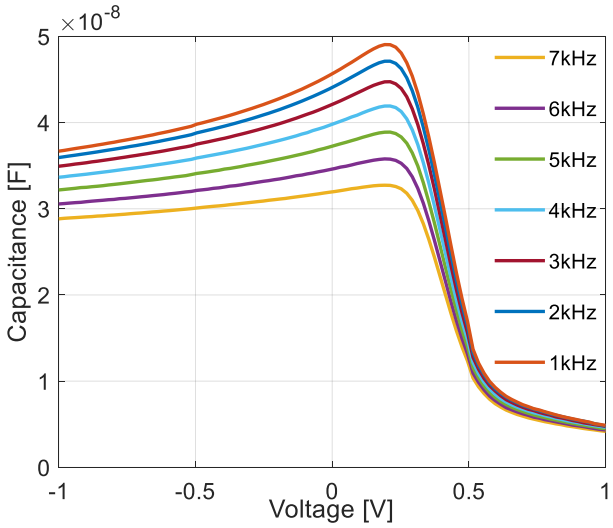
Figure.5.*10. G/Si solar cells investigated in this Section.*


×10^-7
3.5
3
2.5
2
1.5
1
0.5
0
-0.5
0
0.5
1
Capacitance [F]
Voltage [V]
7kHz
6kHz
5kHz
4kHz
3kHz
2kHz
1kHz

(a)


×10^-8
7
6
5
4
3
2
1
-1
-0.5
0
0.5
1
Capacitance [F]
Voltage [V]
7kHz
6kHz
5kHz
4kHz
3kHz
2kHz
1kHz

(b)



(c)

***Figure 5.11**. Capacitance behavior with applied DC bias for a) solar cell of Figure5.10a, b) solar cell of Figure5.10b, c) solar cell of Figure5.10c.*

5.3.2 Modelling of the solar cell

The TCAD model of the G/Si solar cell of Figure 5.10a has been developed using Sentaurus Workbench[150]. The structure has been built as much possible similar to experimental. The n-type substrate has been Arsenic doped with $N_D=5\cdot10^{15}cm^{-3}$. Since the graphene material is not available in the material list, a custom material has been developed starting from standard semiconductor material and varying the physical properties listed in Table IV. The main characteristic to change is the energy bandgap, which is very lower for graphene compared to semiconductor due to its behaviour similar to metal. Energy bandgap is usually defined as [151]:

$$E_g(T) = E_g(0) - \frac{\alpha T^2}{T+\beta} \tag{5.4}$$

where α and β are material coefficients and $E_g(0)$ is the energy bandgap at the temperature T = 0 K. In this model the α and β coefficients of previous formula are not varied, since a first order approximation is

made and only E_g(300 K) value is directly specified. The effective density of states in the conduction and in valence band at ambiance temperature, T_a, are also modified in the model. They are expressed as[152]:

$$N_c(T) = N_c(T_a)\left(\frac{T}{T_a}\right)^{\frac{3}{2}} \tag{5.5}$$

$$N_v(T) = N_v(T_a)\left(\frac{T}{T_a}\right)^{\frac{3}{2}} \tag{5.6}$$

Table IV. *Physical parameter adopted for graphene.*

Parameter	Value
E_g (300 K) [eV]	$1 \cdot 10^{-1}$
N_c (300 K) [cm^{-3}]	$1.79 \cdot 10^{19}$
N_v (300 K) [cm^{-3}]	$3.65 \cdot 10^{19}$

The physical models enabled in the simulation are the classical current flowing mechanisms cited in Section 5.1.2. The developed simulation framework replicates the Solartron 1260 measurement setup. A small signal AC analysis is carried out to compute the frequency dependent admittance. The TCAD performs such analysis only in mixed mode and it calculates the complex impedance matrix as follows:

$$i = Yv = Av + j\omega Cv \tag{5.7}$$

In this formula i and v represent respectively the small signal current and voltage vectors. A represents the conductance matrix while C is the capacitance matrix.
More in general, for a given frequency, the simulator computes the equivalent small signal model described by:

$$\delta I = Y\,\delta V \tag{5.8}$$

where δI and δV are the complex value vector of current and voltage excitations. The start and end frequencies are set to the same value, which is the one used in the experimental measurement. The simulated device dimensions are smaller than reality, but the ratio between

experimental and numerical geometry is taken into account by imposing an area factor different from one in the physics of the simulation. This factor is a multiplier for the currents and the charge of the numerical structure [150].

The numerical structure has been aligned to the experimental device, following the results explained in Chapter 2. The cell studied is that of Figure5.10a since the double peak capacitance profile emerged from this structure. According to the discussion in Chapter 2, this is due to a non-spatially uniform interface. In particular, the capacitance achieved at the frequency f = 1 kHz by means of a Solartron 1260 Impedance Analyzer, is reported in Figure 5.12. The DC voltage was swept from -0.5 V to 1.5V. The capacitance curve showed the presence of a prominent peak for V_{P2} = 0.68 V and a lower one for V_{P1}= 0.18 V.

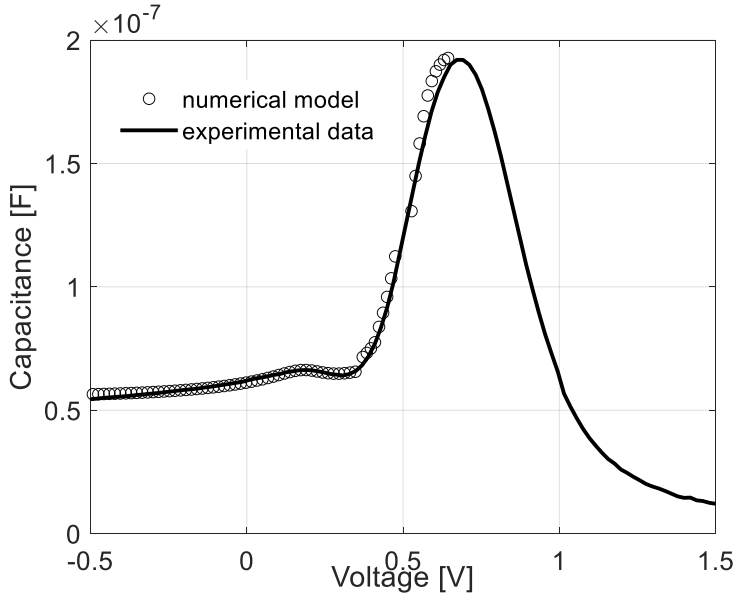


Figure 5.12. *Experimental and numerical structure capacitance profiling obtained for a frequency f=1kHz.*

According to the analysis reported in the Chapter 2, this behaviour suggests the presence of localized defects at the interface. In order to quantify defect distribution, the numerical structure whose behaviour is identical to the experiments, was developed. The procedure to find the

mentioned numerical structure performed a two-zone partition of the structure shown in Figure5.13 and assigned a fixed charge to each zone. By simultaneously varying both the ratio between the areas of the two zones and defects concentration in each of them, the best match with the experiments was found (markers in Figure 5.12).

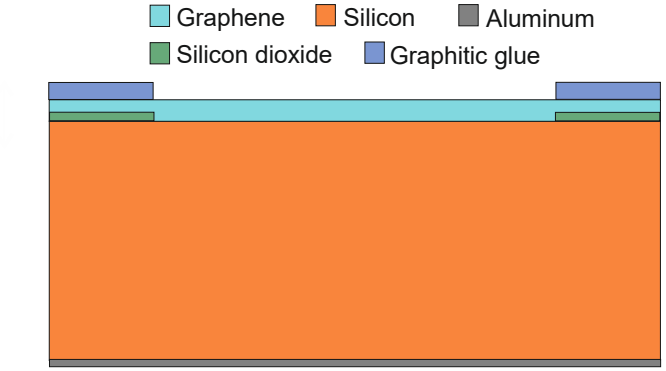


Figure 5.13. *Numerical structure developed in Sentaurus TCAD environment.*

More in detail, the analysis identified the presence of a negative fixed charge of $2.3 \cdot 10^{15} cm^{-3}$ concentrated in an area of about 0.3 cm. The hypothesis that the distortion of the capacitance curve originated by a fixed charge distribution was further confirmed by performing an annealing treatment. The solar cell has been heated for 6 minutes at 180 °C and subsequentially exposed to HNO_3 vapor for 6 minutes. The advantages of the exposition of the solar cell to HNO_3 vapor was previously proved to be effective [132] in literature. The effect on the capacitance profile of this process is shown in Figure 5.14. The main effect is the second and higher peak vanishing in the capacitance behavior. This effect stands for all the frequency mentioned in previous Section. These experimental data asses both the HNO_3 doping as a procedure to reduce trapped charge concentration and forward capacitance as a quick analysis to detect localized traps distribution at the Schottky interface.

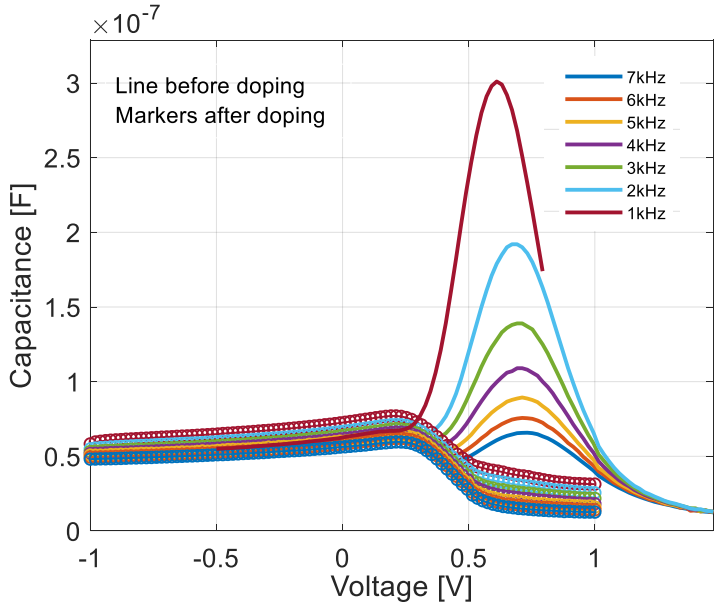


Figure 5.14. *Experimental capacitance curves obtained before doping (full line) and after HNO_3 doping (markers).*

Conclusions

In this thesis, it has been shown the importance of impedance spectroscopy and its application to different types of devices, from solar cells to power devices. This technique has been deeply studied and results are reported for some application cases. The main findings obtained are:

- An automatic procedure developed to extract equivalent electrical configuration from impedance data has been developed. This procedure is very suited for multilayer structure and has the great advantage to embed physical constraints to find resulting parameters. This technique does not require any visual inspection. The equivalent circuit configuration contemplates a RC pair for each interface embedded in the device. Only knowing the number of interfaces, it is possible to run the procedure and get the circuit configuration exhibiting the minimum relative error with respect to the experimental impedance data.

- Emergent perovskite solar cells have been studied using this technique. Moreover, the impedance data acquired have been analyzed using the proposed automatic procedure. Impedance spectra have been acquired both in dark and under illumination. Two different types of perovskite solar cells have been considered, one with doped ETL and the other with ETL not doped. Results have been shown and, in detail, it has been possible to have information on perovskite active layer and recombination process taking place in such material. Using impedance data, it has been possible to understand that ETL doping process may cause some issues to perovskite layer.

- The specific case of Schottky solar cells have also been analyzed. On these G/Si solar cells IS measurements have been performed. More in detail, it has been possible to decouple the different contribution from the overall impedance. Using the automatic procedure, two different contact technologies have been compared. It has been possible to state that conventional contact technology, made by gold, forms a parasitic junction with graphene material, lowering the total solar cell performance. From impedance spectra it has been deducted that new analyzed contact technology, made of colloidal graphitic glue, behaves in different way with respect to conventional one since no junction is formed between contact material and graphene and therefore this new contact technology ameliorates solar cells performance.

Among impedance spectroscopy data, great importance has been given to capacitance profile when the applied DC bias is swept. These curves can be used to gain a deep insight into the device physics. Capacitance versus voltage curves have widely been studied in this thesis and the obtained results are listed in the following.

- Capacitance behavior with applied bias have been analyzed in the forward bias region. The study of capacitance profile has been performed with and without traps. In the case without defects/traps, the analytical equations for forward bias capacitance peak have been found. Those equations are related to the peak height and the peak position in voltage. It has been done a sensitivity analysis of this peak with some physical parameters, such as saturation current and series resistance. It has been found that series resistance affects peak height while saturation current effect is more visible on peak position. This analysis has been carried out together with TCAD analysis.
  Also in case traps exist in the device, the capacitance behavior has been investigated. More in detail, the influence of different defects on the capacitance curve

has been explored. The acceptor and donor traps have been found to modify peak height, depending on their concentration. On the other hand, it has been figured out that fixed charge defects move peak in voltage. As fixed charge concentration increases, peak starts to shift toward lower values.

- Capacitance - voltage curves of some power devices have also been considered. The analyzed structures are power SiC MOSFETs commercially available. These devices have been studied using this measurements technique in order to analyze the traps distribution. In these devices, SiC/SiO_2 interface has a high magnitude of traps distribution and attention must be pay to such interface. Thanks to capacitance curves it has been possible to observe some non-ideality effects, such as hysteresis behavior. Capacitance versus voltage curves have been performed using different sweep direction and hysteresis arising in the different region of the curves have been pointed out. These measurement results have been clarified using a TCAD developed model. Such model has been compared to experimental data in order to understand traps distribution at SiC/SiO_2 interface. An accurate TCAD model has been proposed, considering SiC/SiO_2 interface not uniform in terms of traps properties. This model has been calibrated using experimental C-V data of commercially available MOSFETs. Traps distribution and properties have been extracted.

- Graphene solar cells have been explored using capacitance measurements. The capacitance measured exhibited an additional peak in high forward bias region. This behavior has been explained in the theoretical Section as non-spatially uniform interface properties. An accurate TCAD model has been built according to experimental structure. Numerical capacitance has been aligned to experimental data. This calibration procedure

allowed the interface characterization and more in detail the concentration of fixed charge at the G/Si interface has been quantified. This concentration has revealed to be not uniform since in a small portion a different concentration value has been detected.

- Capacitance versus voltage measurement has been proved to be a quick measurement technique to suggest if some problems happened during fabrication process by simply accessing external terminals of the considered device under test. The observation of multiple peaks arising in the high forward bias region suggests that interface properties are not uniform in the entire structure.

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