Holistic Design in
High-Speed Silicon Photonics and
Low-Power Electronics Platforms

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To my lovely parents, Nasrin, and Behnam;
and to all my teachers, mentors, and advisors
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ABSTRACT

High-speed interconnects are of vital importance to the operation of high-performance computing and communication systems, determining the ultimate bandwidth or data rates at which the information can be exchanged. Optical interconnects and the employment of high order modulation formats are considered as the solutions to fulfilling the envisioned speed and power efficiency of future interconnects. One area of growing importance in optical interconnects is the design and optimization of energy-efficient transmitters with superior power efficiency. Enhancing the electro-optical bandwidth density while keeping the power efficiency optimized, requires improvement in the optical power penalty of photonic integrated circuits. Moreover, co-optimization of electronics and photonics enables a path towards sub-pJ/b transmission efficiency. In this dissertation, architectural and circuit-level energy-efficient techniques serving these goals are presented.

First, an integrated DAC-less PAM-4 transmitter in a multi-micron silicon photonics platform using 2 binary-driven uneven-length SiGe EAMs in an unbalanced MZI is presented. The optical transmitter exhibits 5.5dB ER at 100 Gb/s with 2.1dB SNR improvement compared to single EAMs driven by PAM-4 signals. Also, A DAC-less 200Gb/s QAM-16 transmitter in a multi-micron silicon-photonics platform using 4 binary-driven SiGe EAMs in an unbalanced MZI is presented. The transmitter exhibits bit-error rates of 3×10-4 and 2.8×10-4 for square and hexagonal constellations.

Second, a 100Gb/s PAM4 optical transmitter system implemented in a 3D-integrated Silicon Photonics-CMOS platform is presented. The photonics chip includes a push-pull segmented Mach-Zehnder Modulator (MZM) structure using highly capacitive (415fF to 1.1pF), yet optically efficient (VπL= 0.8 V.cm) metal-oxide-silicon capacitor (MOSCAP) phase modulators. Two pairs of U-shaped modulator segments with effective lengths of 170µm and 450µm are driven at 50 Gbaud by a dual-channel 28nm CMOS driver, which is flip-chip bonded to the photonics chip. The driver cores utilize digitally controllable pre-distortion and inductive peaking to achieve sufficient electro-optical bandwidth. The drivers deliver 1.2Vppd swing to modulators using a 0.9V supply and on-chip serializers that generate

50Gb/s data streams. The electronics chip consumes 240mW achieving 2.4pJ/bit energy efficiency. The overall electro-optical bandwidth (EOBW), without any pre-distortion, is increased by approximately 56% and 48% for the 170µm and 450µm segments, respectively, when compared to their EOBW measured by 65GHz 50-Ohm terminated probes. The optical input power to the photonics chip is +10dBm and an erbium-doped fiber amplifier amplifies output signals by 11dB. The 50Gb/s NRZ optical raw eye diagram exhibits 4.3dB extinction ratio (ER) and 1.2dBm of optical modulation amplitude (OMA). The 100Gb/s PAM4 optical raw eye diagram shows 4.3dB ER and 1.4dBm OMA with a transmitter dispersion eye closure quaternary (TDECQ) of 1.53dB after a 5-tap feed-forward-equalization (FFE) filter. The PAM4 TDECQ changes by 53% when the temperature is increased from 30ºC to 90 ºC at the optimum forward bias voltage of 1V.

Third, an efficient cold-starting energy harvester system, fabricated in 65nm CMOS is presented. The proposed harvester uses no external electrical components and is compatible with biofuel-cell voltage and power ranges. A power-efficient system architecture is proposed to keep the internal circuitry operating at 0.4V while regulating the output voltage at 1V using switched-capacitor DC-DC converters and a hysteretic controller. A startup enhancement block is presented to facilitate cold startup with any arbitrary input voltage. A real-time on-chip 2D maximum power point tracking with source degradation tracing is also implemented to maintain power efficiency maximized over time. The system performs cold startup with a minimum input voltage of 0.39V and continues its operation if the input voltage degrades to as low as 0.25V. Peak power efficiency of 86% is achieved at 0.39V of input voltage and 1.34µW of output power with 220nW of average power consumption of the chip. The end-to-end power efficiency is kept above 70% for a wide range of loading powers from 1µW to 12µW. The chip is integrated with a pair of lactate biofuel-cell electrodes with 2mm of diameter on a prototype printed circuit board (PCB). Integrated operation of the chip with the electrodes and a lactate solution is demonstrated.

PUBLISHED CONTENT AND CONTRIBUTIONS

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A. H. T. participated in conceiving the ideas, designed the photonics chip, performed the experiments, and co-wrote the manuscript.

A. Hashemi Talkhooncheh, W. Zhang, M. Wang, D. J. Thomson, M. Ebert, K. Li, G. T. Reed, A. Emami, **"A 100Gb/s PAM4 Optical Transmitter in A 3D-Integrated SiPh-CMOS Platform Using Segmented MOSCAP Modulators"**, *IEEE Journal of Solid-State Circuits*, vol. 58, no. 1, pp. 30-44, Jan. 2023, doi: 10.1109/JSSC.2022.3210906.
A. H. T. participated in conceiving the ideas, designed the CMOS chip, performed the experiments, and co-wrote the manuscript.

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A. H. T. participated in conceiving the ideas, designed the CMOS chip, performed the experiments, and co-wrote the manuscript.

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Chapter 1

INTRODUCTION

The notion of high-speed evolves with time, reflecting the ever-growing data traffic that connects and benefits our daily lives. With the continually emerging internet applications which unceasingly incite the growth of the numbers of users and connected devices, it is observed that the volume of the data traffic has been increasing exponentially. As the momentum for fast-growing internet connections continues to thrive, it is forecasted the speed performance of various networks will advance more than two-fold from 2018 to 2023 [1]. In addition, the advent and progressive developments of both artificial intelligence (AI) and the fifth generation (5G) communication technologies also necessitate high-speed interconnects serving as the backbone to support fast data communication within the computers and infrastructures. The evolution of high-speed interconnects, in light of these technological pursuits, enables exchanging data with higher data rates and lower power, thereby shaping the future of high-performance computing and communication systems.

In response to the demand for interconnects of higher speed, efforts have been made to improve the per-pin data rate of the interconnects. In every three to four years, the speed has approximately doubled for almost all I/O standards [2]. However, on the way towards higher data rates, electrical interconnects suffer from high channel losses that increase with the modulation frequency and/or transmission distance. In consequence, improvement or even preservation of the energy efficiency with electrical interconnects becomes prohibitively difficult to achieve at high data rates. More specifically, a channel with 30-dB more loss corresponds to about 10 times more power consumption per bit [3]. By contrast, optical interconnects have shown the favorable superiority in that little modulation-frequency dependent loss is introduced by the fibers. Accordingly, optical interconnects possess promising potentials to fulfill the envisioned power, data rate, and reach requirements [4]. Meanwhile, for a given bandwidth limitation, it is feasible to increase the data rate with the utilization of high-order modulation formats thanks to the augmented spectral efficiency. In

particular, N-level pulse amplitude modulation (PAM-N) and N-point quadrature amplitude modulation (QAM-N) are appealing options, multiplying the data rates by occupying similar electro-optical bandwidths compared to on-off-keying (OOK) modulation format.

Optical interconnects and higher-order modulation formats, which promise lower channel losses and higher spectral efficiencies, have fueled the evolution of high-speed interconnects. The pivotal design considerations enabling energy-efficient high-speed interconnects leveraging optics and higher-order modulation formats are presented in the following.

1.1   Optical Interconnects

The trends show that over the past 10 years the per-pin data rates have approximately doubled every 4 years for most I/O standards. This has resulted in a rapid increase in the power consumption of data centers. As shown in Fig. 1.1, depicting data centers' electrical energy consumption per year, which is simulated and projected for up to the year of 2030 shows that there is around 24.7% of annual growth of data centers communication traffic [5].
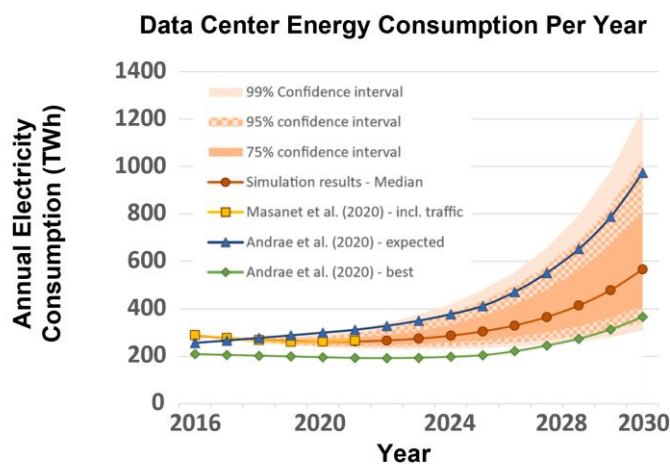
Fig. 1.1. Data Center Energy Consumption Per Year [5].

Moreover, the wireline trends for transceivers' power efficiency which is shown in Fig. 1.2 reveal that there is approximately 10 times more pJ/bit needed for 30dB more channel losses [6]. Considering these trends and challenges, optical interconnects and more specifically, silicon photonics, provide us with low cost and power efficient solutions for 100+ Gb/s/lambda data transmission, to tackle the challenges for both power and bandwidth

efficiency as well as the demands for speed. Electrical power efficiency of data centers account for approximately 30%~40% of the total power consumption. This portion, however, directly affects the temperature stabilization power consumption of data centers, which could account for ~50% of the total power consumption [5]. This motivates us towards designing more power efficient optical circuitry architectures and optical modulators.
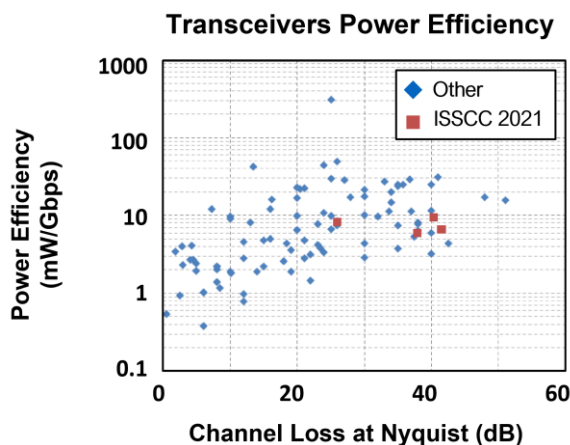
Fig. 1.2. Transceiver power efficiency [6].

1.2   Organization

This dissertation presents architectural as well as circuit-level designs and techniques enabling energy-efficient high-speed interconnects and energy harvesting for low-power sensing applications. The rest of this dissertation is organized as follows.

In Chapter 2, the fundamentals, features, and implementations of various high-speed optical transmitters are summarized. Both passive and active building blocks used in integrated silicon photonics platforms are discussed first, and their performances are compared. Since there exists various choices for platforms, types of waveguides, power couplers, and optical modulators, the important parameters to be examined and chosen for the right application are elaborated. Furthermore, at the architectural level, a link budget analysis for a typical optical transceiver link is studied to highlight the importance of the parameters chosen for the transmitter design to comply with a targeted receiver sensitivity. Chapter 2 also studies various PIC architectures achieving same higher-order modulation schemes and their advantages. It is shown that how travelling-wave phase modulators,

segmented lumped modulators, electro-absorption modulators, or ring modulators could be used in MZI structures to construct PAM-4 or QAM-16 modulation. While comparing the PIC characteristics of these architectures show interesting insights into a proper optical transmitter design, the true comparison achieved when electronics complexities and power consumption are also included in the analysis.

In Chapter 3, design, optimization, and implementation of a 100Gb/s PAM-4 Si-Ph transmitter, and a 200Gb/s QAM-16 transmitter are presented. Various ways of achieving PAM-4 and QAM-16 modulation are further discussed in chapter 3. EAMs are among the great candidates for higher-order modulation scheme transmitters. They have compact footprints and can directly modulate the light amplitude. Placing EAMs in parallel in a multi-arm MZI structure tackles the issue of their relatively high insertion losses, however, their non-linear extinction curve, as well as modulation curve should be examined closely for such arrangements. Chapter 3 discusses design flows to address these challenges, and to optimize the overall optical power penalty. Furthermore, architecture-level optimizations are discussed that reduces the overall power consumption, using custom designed optical power splitters and power couplers. Variable power splitters and combiners are designed for a parallel PAM-4 architecture with 2 binary-driven EAMs with uneven lengths. Also, an unbalanced 1×5 power splitter/combiner is proposed for a QAM-16 transmitter to optimize the overall optical power penalty and constellation centralization.

In Chapter 4, a 100Gb/s PAM4 optical transmitter in a 3D-integrated SiPh-CMOS platform using segmented MOSCAP modulators is presented. The electronics drivers should be closely optimized with the optical modulators' parameters and the PIC architecture. MOSCAP modulators exhibit excellent optical efficiencies ($V_\pi L < 1$ V.cm) and compact footprints (< 1mm). These modulators, however, could suffer from excessive insertion losses and large capacitive parasitics (~ 3 fF/µm), which could limit the electro-optical bandwidth, when combined with the drivers. The transmitter includes a push-pull segmented PIC architecture and differential drivers, which are individually designed for each segment.

Chapter 4 shows how high-speed circuit technics such as data pre-distortion and bandwidth extension through inductive peaking, combined with close EIC and PIC integration and proper layout could enable the power of MOSCAP modulators. U-shaped MOSCAP modulators show significant improvement in EOBW as the electrode's lengths are halved. The transmitter generates optical PAM-4 eye diagrams with 4.3dB extinction ratio (ER) and 1.4dBm of optical modulation amplitude (OMA) with 2.4 pJ/bit efficiency of the 28-nm CMOS chip.

Chapter 5 presents an energy-efficient CMOS design for biofuel-cell energy harvesting for low-power bio-sensing applications. It is crucial for wearable and implantable biosensors to have miniaturized footprints for minimal invasiveness. One challenge brought by mm-scaled form factors is energy source. In chapter 5, a cold-starting energy harvester system fabricated in 65-nm CMOS is presented, which could extract energy from biofuel power sources with open circuit voltages as low as 0.39V and deliver power to loads demanding 1µW to 12µW of power with 86% peak efficiency. This chapter shows how a combination of up-converting and down-converting the available voltage of the biofuel source, could keep the internal power consumption minimized, while delivering power to the load with maximum power-point tracking. The cold startup capability of this harvester and using no external storage capacitor, enables a form factor of smaller than 1 cm^2 when combined with 2 biofuel-cell electrodes, each having 2 mm of diameter. Integrated operation of this harvester in a lactate solution is demonstrated at the end of Chapter 5.

Finally, in Chapter 6, the design considerations, and highlights of the energy harvesting and transmitter circuits in both electronics and photonics domains, which are presented in this dissertation, are summarized, and conclusions are drawn.

C h a p t e r   2

BACKGROUND

2.1 Optical Interconnect Basics

The transceiver channel shown in Fig. 2.1 depicts a simple configuration of an optical channel.
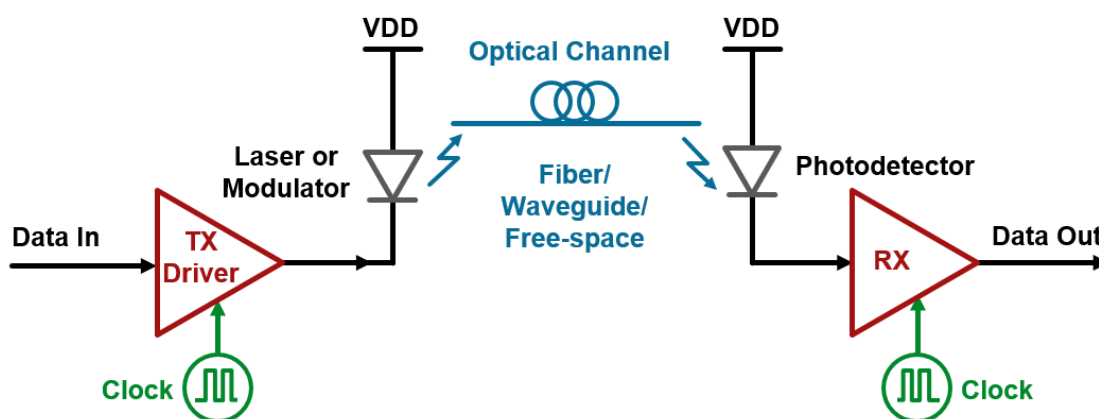
Fig. 2.1. Basic configuration of an optical transceiver link.

On the transmitter side, a stream of electrical data in the form of digital bits are converted to an optical bit stream. This is done either by directly modulating a continuous-wave (CW) laser, or through modulating an optical modulator, which receives light from a CW source. The TX driver is responsible for receiving the bit stream and modulating either the laser or the modulator. The optical bit stream is the coupled to an optical channel, in a form of optical fiber, an on-chip waveguide, or into free space. The optical data travels through the channel and is then coupled to the receiver. At the receiver front-end, a photodetector converts the optical data to an electrical bit stream. Since usually the detected stream is noisy and have small amplitudes, a receiver amplifier is put right after the photodetector to improve the quality of the received data. Clocking signals on both the TX and RX sides are synchronized to sample the received data with correct timing and to avoid detection errors. The represented optical link could of course include more sophisticated architecture to support higher-order

modulation schemes such as N-level pulse-amplitude-modulation (PAM-N), and N-point Quadrature-Amplitude-Modulation (QAM-N). These promising modulation schemes increase the overall bandwidth density efficiency. The optical channel could also be designed to guide multiple wavelengths and/or polarization states to further increase the overall electro-optical bandwidth (EOBW) of the system, by incorporating Wavelength-Division-Multiplexing (WDM) or Orthogonal-Frequency-Division-Multiplexing (OFDM). Depending on the type of the modulation and transmission scheme, the receiver architecture is modified accordingly to perform direct detection or coherent detection.

2.2 Basic Definitions

The optical eye diagram shown in Fig. 2.2, is formed by slicing the received optical data stream at 50 Gb/s by 1 unit interval (UI) and superimposing all on top of one another.
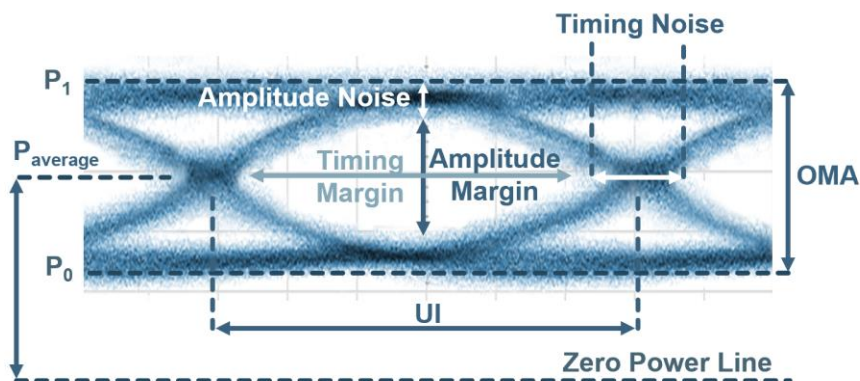
Fig. 2.2. Basic configuration of an optical transceiver link.

The transmitted 0's and 1's through the optical channel correspond to the ON and OFF states of the modulated laser or the optical modulator, transmitting optical power levels of P_0 and P_1. The difference between these two values is called the optical modulated amplitude (OMA), while the average power is defined as the mean of P_0 and P_1. Another important metric in the eye diagrams is the extinction ratio (ER), which is defined as the ratio of P_1 to P_0 in decibels. It is desirable to maximize the OMA to improve the amplitude margin (and potentially the time margin), by minimizing noise and maximizing the EOBW, which translates to smaller inter-symbol-interference (ISI) and timing noise. It is worthwhile to

know that OMA reaches $2\times P_{avg}$ as ER reaches infinity, therefore, it is also desirable to maximize ER to improve the power efficiency of the system. One useful metric to evaluate the optical power efficiency of optical links is the optical link penalty (LP), which could be defined by either the OMA or P_{avg}:

$$LP_{OMA}=10.Log\left(\frac{P_{in}}{OMA}\right)=10.Log\left(\frac{P_{in}}{P_1\text{-}P_0}\right) \tag{2.1}$$

$$LP_{avg}=10.Log\left(\frac{P_{in}}{P_{avg}}\right)=10.Log\left(\frac{2P_{in}}{P_1+P_0}\right) \tag{2.2}$$

where P_{in} is the input optical power to the system (alternatively, P_{in} can be replaced by the laser optical power P_{laser}). In an optical link, the received signal is the sum of the transmitted values and noise which appears as an added signal with random value. At the sampling point, there is a small but finite probability for the noise amplitude to be greater than the signal amplitude. This probability determines the probability of a wrong decision or the bit-error rate (BER). The BER indicates how many errors are likely to occur for a certain number of resolved bits. For example, the probability of error due to additive white Gaussian noise (AWGN) can be expressed as a function of the signal-to-noise ratio (SNR) in case of an equiprobable one or zero:

$$BER = P_{error} = \int_A^\infty \frac{1}{2\pi\sigma_n^2}\exp(-\frac{x^2}{2\sigma_n^2})dx = 1 - Q(\frac{A}{\sigma_n}) = 1 - Q(SNR), \tag{2.3}$$

where A is the signal amplitude, σ_n is the standard deviation of the noise, and $Q(x)$ represents the tail probability of the standard normal distribution. Other than the white noise there are other sources of noise that can degrade the overall SNR, such as device shot noise, supply, and substrate noise. These noise sources, unlike the white noise, are bounded in amplitude and usually scale with the signal amplitude as well as signal activity. As a result, the absolute BER cannot be solely related to the total noise power, as shown in Equation 2.3.

2.3   Integrated Photonics Building Blocks

The integrated photonics building blocks have been greatly developed over time to include more modules and functions on the PIC to further reduce the manufacturing costs. With the

wide availability of these modules described in this section, photonic circuits with complex functionalities could be designed on chip, similar to integrated electronics.

2.3.1 Passive Components

The most basic component on an integrated photonics chip is an optical waveguide. A waveguide is fundamentally formed by a transparent medium in a target wavelength and is cladded by another material with significantly different optical refractive index, to form a cavity. When a light wavefront, with the specific wavelength enters this structure, it experiences confinement in form of a single or multiple optical modes inside the cavity and gets dissipated outside this region. Different geometrical arrangements could be formed based on this phenomenon to further improve the optical confinement or support a broader wavelength range as well as polarization states. Fig. 2.3 shows some variations of fundamental waveguides:
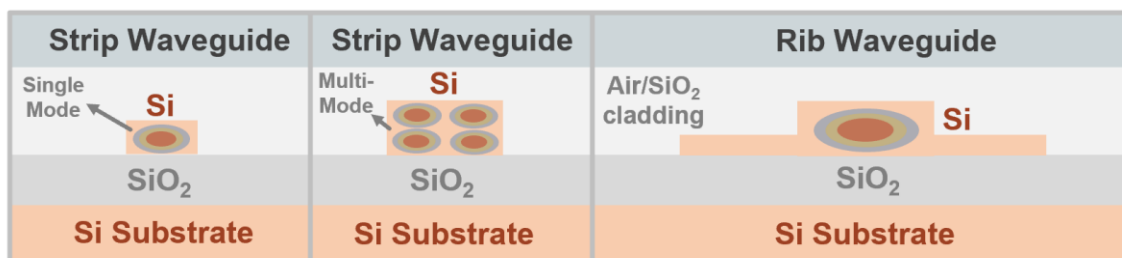
Fig. 2.3. Optical waveguide structures.

Routing optical signals on a PIC is realized by combining waveguides, bends, couplers and crosses. Optical bends are designed to redirect the light into arbitrary directions. While circular bends are common in PIC design, they are not the most efficient type of a bend. The confined light inside the waveguide experiences no losses only if there is no abrupt change in the curvature of the waveguide. Since the curvature of a straight waveguide is infinite, while the curvature of a circular bend is $1/R^2$, where R is the radius of the circle, a small proportion of light propagates away from the waveguide, whenever light enters or exits a circular bend. Alternatively, bends like a Euler bend, alleviate this challenge by decreasing the curvature of the bend gradually from zero to a specific value and back to infinity, when

attached to another straight waveguide. A few examples of waveguide bends are provided in Fig. 2.4:
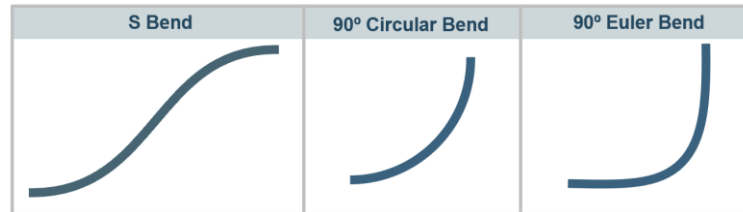
Fig. 2.4. Optical waveguide bends.

Optical power splitting and combining is realized using power couplers. Y-junctions are a typical type of splitter/couplers, with relatively compact dimensions and reasonable insertion losses (< 0.1dB), when properly designed. Alternatively, directional couplers are great candidates when a splitting ratio other than 0.5 is desired. Directional couplers operate based on capturing the evanescent optical field around a waveguide, which could be partially, or completely captured by another adjacent waveguide. Distance between the 2 waveguides, as well as the coupling length would determine the coupling ratio, which is defined as the ratio of the optical power coupled into the 2nd waveguide to the input optical power.

Y-junctions and directional couplers, however, are relatively narrow-band and do not operate well outside their designed wavelength range. They are also prone to performance degradation due to process variations or at extreme temperatures. Consistent performance of the PICs over large temperature ranges are one of the major challenges, when the PIC is scaled for high-power computing. Multi-mode interference devices (MMIs) are great alternatives for Y-junctions when a more robust performance is desired. MMIs consist of a multi-mode region attached directly to the straight waveguide. When a single-mode-confined light enters this region and travels through, the optical power is periodically transferred from the fundamental mode to the higher order modes of the region. The region could be terminated and attached to the output straight waveguide(s) when the whole power is transferred into one of the higher-order modes. Examples of Y-junctions, directional couplers and MMI couplers are shown in Fig. 2.5:
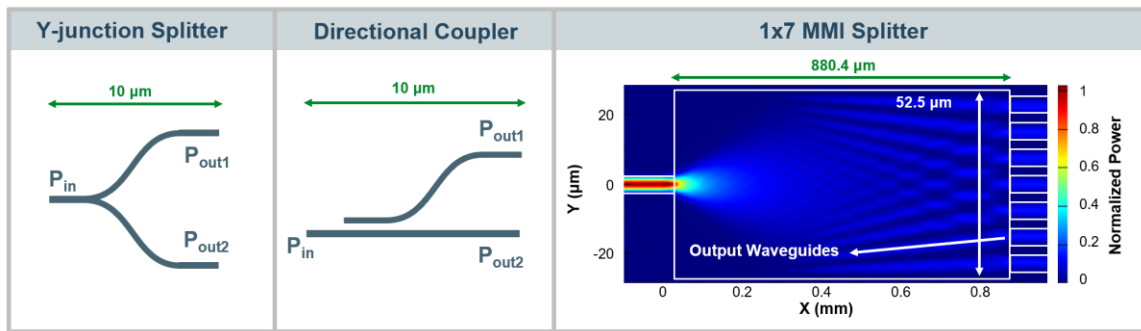
Fig. 2.5. Optical splitters/couplers.

2.3.2 Active Components

Active components in silicon photonics either modulate the phase and/or the amplitude of the light (modulators) or convert the optical power to electrical current (photodetectors). Optical modulators are structures along the waveguide that could modify the real and imaginary parts of the waveguide refractive index, in the presence of an electrical field. Various optical modulators have been developed that operate based on the plasma dispersion effect, Franz Keldysh (FK) effect, and quantum-confined Stark effect (QCSE). All modulators receive an electrical signal to modulate properties of the light, hence, they act as the bridge between the electronics and photonics on a transmitter system. In general, one should keep in mind that each modulator component, aside from the circuit architecture being used in, has a number of advantages and disadvantages. The most important factors of several optical modulators are listed in the following sections.

2.3.2.1 Phase Modulators

Phase modulators operate based on the plasma dispersion effect, which is the one mechanism that is most widely used in integrated photonic modulators [1, 2]. This effect involves changing the free carrier density of a guiding medium to induce changes in the refractive index, hence, modulating the phase. Several different mechanisms of manipulating free carrier density have been investigated. Among those, carrier-depletion-mode and carrier-injection-mode and carrier-accumulation-mode mechanisms are the most promising candidates for high-speed data communication applications.
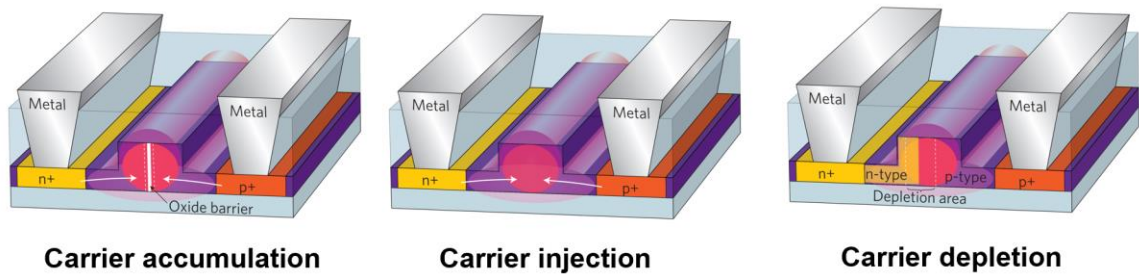
Fig. 2.6. Optical phase modulation mechanisms.

Carrier-injection devices are based on a forward-biased p-i-n diode, and carrier-depletion devices are based on a reverse-biased p-n junction. Carrier-depletion devices are widely used for high-speed operations [3-6], while carrier-injection devices are used for low-voltage applications [7, 8]. Carrier-accumulation devices include a thin oxide junction between p-doped and n-doped regions, which changes the refractive index of the structure by accumulating charges across the junction when an electric field is present [9-16].

Phase modulators could also be categorized by their footprints and electrodes geometry: 1) Travelling-wave (TW) phase modulators are relatively long phase modulators with electrodes that are significantly longer than the wavelength of the propagated modulating electrical signal. These modulators require electrical termination, which usually translates to power-hungry drivers. TW modulators require relatively large voltages (large $V_\pi L$), however, are relatively robust across temperature variations [17-26].

2) Lumped phase modulators, as opposed to TW modulators have smaller footprints with shorter electrodes, which are comparable or shorter than the propagated electrical wavelength of the modulating signal. Carrier-accumulation devices could be designed with relatively higher optical efficiency ($V_\pi L$) to afford shorter lengths. These modulators require no termination, however, they have highly-capacitive parasitics that affects the electro-optical bandwidth [9-16].

Phase modulators are excellent candidates for coherent applications, while they could also be used in non-resonant structures, such as Mach-Zehnder Modulators (MZMs), or resonant structures, such as micro-ring modulators (MRMs) to modulate the light amplitude.

2.3.2.2   Micro-ring Modulators

Resonant structures can be used to dramatically reduce area and power consumptions, which comes at the cost of a dramatically narrower line-width and susceptibility to temperature fluctuations. These modulators have their phase and amplitude tangled; hence, more consideration is required when used in parallel structures [27-38].
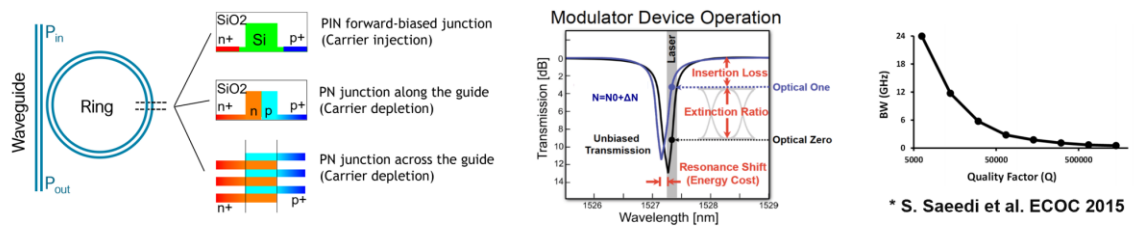
Fig. 2.7. Micro-ring modulator structure.

2.3.2.3   Amplitude Modulators (Electro-absorption Modulators)

Both FK and QCSE effects involve a change in the absorption coefficient of the medium in presence of an electrical field. Electro-absorption modulators (EAMs), which operate based on these effects, include periodic quantum well structures, either along the waveguide or perpendicular to the waveguide, to amplify the absorption effect. EAMs are excellent candidates for PAM-N modulation schemes since the electrical signal is directly translated to the amplitude of the light in these modulators [29-32]. EAMs require relatively small voltages to operate and also have compact footprints with small capacitive parasitics, which makes them attractive for low-power and high-speed applications. Major challenges with EAMs involve their non-linear extinction curve versus the applied voltage, and their input power limit [33-47]. If the optical input power crosses this limit, the EAM goes into the saturation region and the extinction coefficient degrades dramatically. This might limit the performance of the EAMs for high-power applications. Another challenge for the EAMs is their amplitude and phase entanglement, known as modulation chirp, which should be

considered when used in interferometric structure, such as Mach-Zehnder Interferometers (MZIs) [48, 49].

2.3.2.4   Photodetectors

Two commonly used types of devices for optical/electrical conversion are p-i-n diodes and metal-semiconductor-metal (MSM) diodes. In both devices the carriers generated by the incident photons are to the electrodes in presence of an electric field. The resulting current, i.e., photocurrent, is proportional to the number of photons absorbed per unit time. In a p-i-n diode, a reverse-bias across the diode ensures a strong electric field in the intrinsic region and negligible reverse bias current (dark current) in absence of light. Germanium and or SiGe are mostly suitable for integrated systems that use silicon as the guiding medium. Photodetectors could be integrated directly on the waveguide or be placed adjacent to a waveguide and absorb a portion of the light evanescently. There is a direct trade-off between the photodetector's responsivity and speed, as reducing the size of a photodetector, decreases its parasitic capacitance and its responsivity. Avalanche photodiodes (APDs) are another detecting devices that are used to improve the responsivity of photodiodes. APD is a photodetector that provides a built-in gain stage through avalanche multiplication [50]. APDs used in high-speed optical links need to achieve high gain-bandwidth products without sacrificing noise or responsivity [51].

2.4   Integration of EIC and PIC

Including more components on the chip, either the electronics, or photonics, would significantly reduce the fabrication costs when the transceiver system is scaled. However, as the demand for the data rates grow rapidly, travelling distances of the electrical signals shrink as a result, to support higher bandwidths. While this is a manageable challenge when designing electrical circuits in a single chip, it becomes more challenging when the electrical signals have to travel from the EIC to the PIC. At data rates above 25Gb/s, wire-bonding the electrical drivers from the EIC to their corresponding modulators on the PIC would not provide the optimal results, since the inductance of the wire-bonds could distort the EOBW, even at lengths as short at 100µm. Although, the inductance of the wire-bonds could be

included in the design to benefit from its inductive peaking, however, this effect is only beneficial in certain circumstances when the capacitance of the electrical pads on the EIC are comparable to the capacitive parasitics of the optical modulator. Alternatively, flip-chip bonding is an attractive form of integration since the distance between the driver and the modulator could be reduced to a copper/gold bump with a diameter smaller than 50µm. Monolithic integration is another attractive solution, which involves having both electronic and photonic components on the same die. While there will be compromises with the performance of the electronics in these platforms, the high cost of this solution has prevented it scalability to this date.
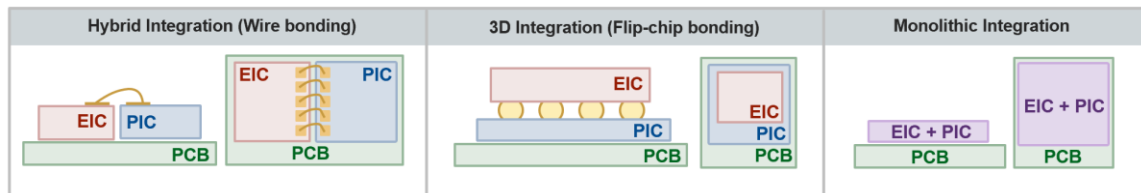
Fig. 2.8. EIC and PIC integration solutions.

2.5 PIC Architectures for PAM-4 Transmission

In this section the different PIC architectures of PAM-4 modulators are studied. For an optical PAM-4 transmitter, it is worthwhile to be reminded that it is desirable to generate 4 optical power levels that are equally spaced since direct detection is the most convenient and power efficient method to design PAM-4 receivers. Generating equally-distanced power levels would be achieved in various ways depending on the architecture of the circuit. The first method would be using a 4-level electrical driver (PAM-4 driver) to modulate a single optical modulator to map the 4 voltage levels (which could potentially be unequally-spaced) to 4 equally-spaced optical levels (Fig. 2.9 (a, b, c, d)). This involves compensating for the inherent nonlinearities of the optical modulators in the electrical domain. As an example, one could refer to the non-linear absorption coefficient of an EAM versus voltage, the non-linear cosine extinction curve of a push-pull MZI structure with phase modulators, or the inherent non-linear absorption curve of a ring modulator near its notch wavelength. These inherent nonlinearities of the modulators or the PIC architecture makes the driver design more complex and, in some cases, requires a data-dependent equalization, which inevitably

translates to more jitter compared to a binary NRZ or an evenly-spaced PAM-4 scheme. An alternative is using two NRZ OOK driving signals and two optical modulators to achieve optical PAM-4. The two modulators can be combined in series or parallel depending on the architecture. Common series architectures include segmented phase modulators in a push-pull MZI structure (Fig. 2.9 (e)), segmented ring modulators (Fig. 2.9 (f)) or two EAMs or ring modulators in series (Fig. 2.9 (g, h)). Common parallel structures include the dual-parallel MZMs (DP-MZM) (Fig. 2.9 (i)), two ring modulators in a push-pull MZI (Fig. 2.9 (j)), and two EAMs placed in parallel in an MZI structure (Fig. 2.9 (k)).
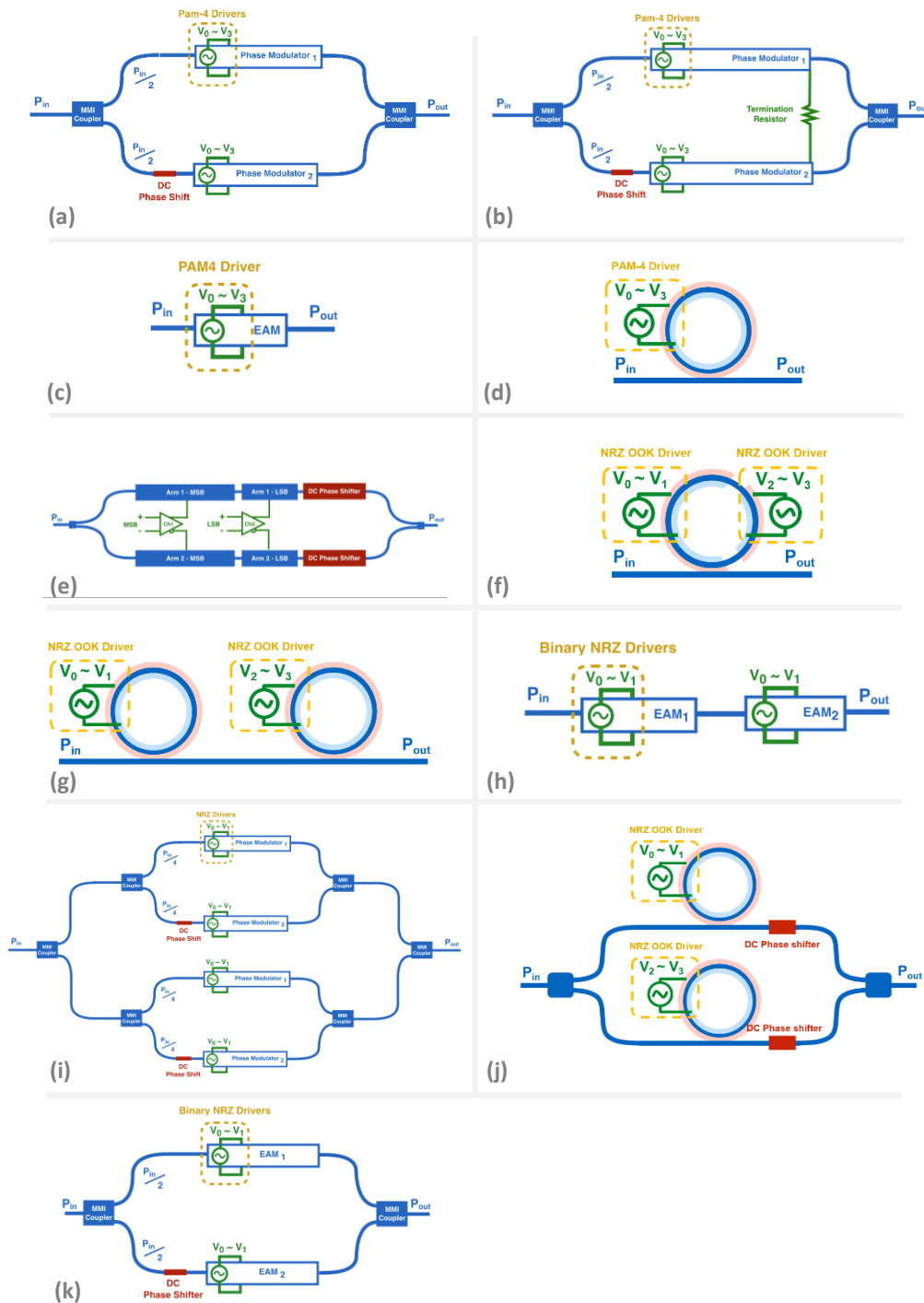
Fig. 2.9. PAM-4 optical circuit variations with PAM-4 drivers for (a) lumped phase modulators, (b) travelling-wave phase modulators, (c) an EAM, (d) a ring modulator and with NRZ OOK drivers for (e) segmented phase modulators, (f) segmented ring modulators, (g) two ring modulators in series, (h) two EAMs in series, (i) dual-parallel MZI with phase modulators, (j) two ring modulators in parallel and (k) two EAMs in parallel.

2.6   PIC Architectures for QAM-16 Transmission

In this section, similar to section 2.5, a general analysis of optical QAM-16 generation using pure phase modulators, pure amplitude modulators as well as phase and amplitude modulators are provided. In this analysis, we consider a unity-sized QAM-16 constellation and compare how much power is needed to achieve that by each architecture.

Traditionally, optical 16-QAM and in general, QAM scheme is achieved by using the nested MZM IQ modulators. In such configuration, a cascade of Y-junctions/3-db couplers have been used to split/combine the light. The drawback of such configuration is the inherent 3-db loss each time two branches get combined. In addition, increasing the number of couplers will result in an increase in a significant total optical loss, since each 3-db coupler has a certain insertion loss (typical compact structures have around 0.1 dB of insertion loss). Other structures include segmented phase modulators driven by binary NRZ drivers, or single-segment phase modulators driven by PAM-4 drivers, in an IQ-MZM configuration to achieve PAM-4 modulation in each axis (I and Q) and QAM-16 when they are combined. The major drawback of these architectures is the need of power consuming drivers to be able to drive such large and high-parasitic modulators. Moreover, electrical PAM-4 modulators typically need digital-to-analog converters (DACs) which would again add to the power consumption compared to NRZ drivers at the same baud-rate. Recently, ring resonator modulators have also been used to achieve QAM-16 modulation, however, their high sensitivity to environmental conditions and fabrication tolerances could become problematic.

We now analyze all possible variations to design optical QAM-16 transmitters. First, in Fig. 2.10 (a), two EAMs (or any other amplitude and phase modulator) are used in parallel, each being driven by an independent PAM-4 modulator. In order to generate a symmetric constellation, the input power to each arm as well as the length of the EAMs have to be the same. The generated constellation diagram on the I-Q plane is provided in Fig. 2.10(b), where the red and blue vectors represent the optical field vectors of each arm at the output of the EAMs being driven with 4-level drivers. As we can see the finite ER and the chirp of the EAMs degrades the achieved constellation size significantly. In Fig. 2.10(c), we have the

same structure EAMs being replaced by phase modulators. In this architecture the input power to one arm should be twice as the other. As it can be seen in Fig. 2.10(d), the achieved constellation size is relatively larger, however, the voltage range of each driver has to cover a 2π phase shift. Moreover, any non-ideality in the driving voltage levels would directly distort the symmetry of the constellation, rather than making its size smaller. In Fig. 2.10(e), 4 phase modulators are placed in parallel, which are driven by NRZ OOK signals. In this case, the power splitter should generate a 1:2:1:2 ratio to the arms and ideally each modulator should be rotated by π radians to achieve the largest constellation. However, having a lower phase difference between the ON and OFF states of the modulators would rotate the whole constellation and make its size smaller (as long as all the phase differences are the same). Fig. 2.10(f, g) demonstrate the constellation points under the ideal and non-ideal conditions. Lastly, in Fig. 2.10(h), we have 4 EAMs in parallel with the same architecture as in Fig. 2.10(e). As it is observable from Fig. 2.10(i), the achieved constellation would be smaller and away from the origin. In order to avoid sending excessive average optical power through the channel, a 5th arm could be predicted in the design to bring the center point of the constellation back to the origin. However, the amplitude and phase of this 5th arm should be precisely tuned according to the ER and chirp of the EAMs.
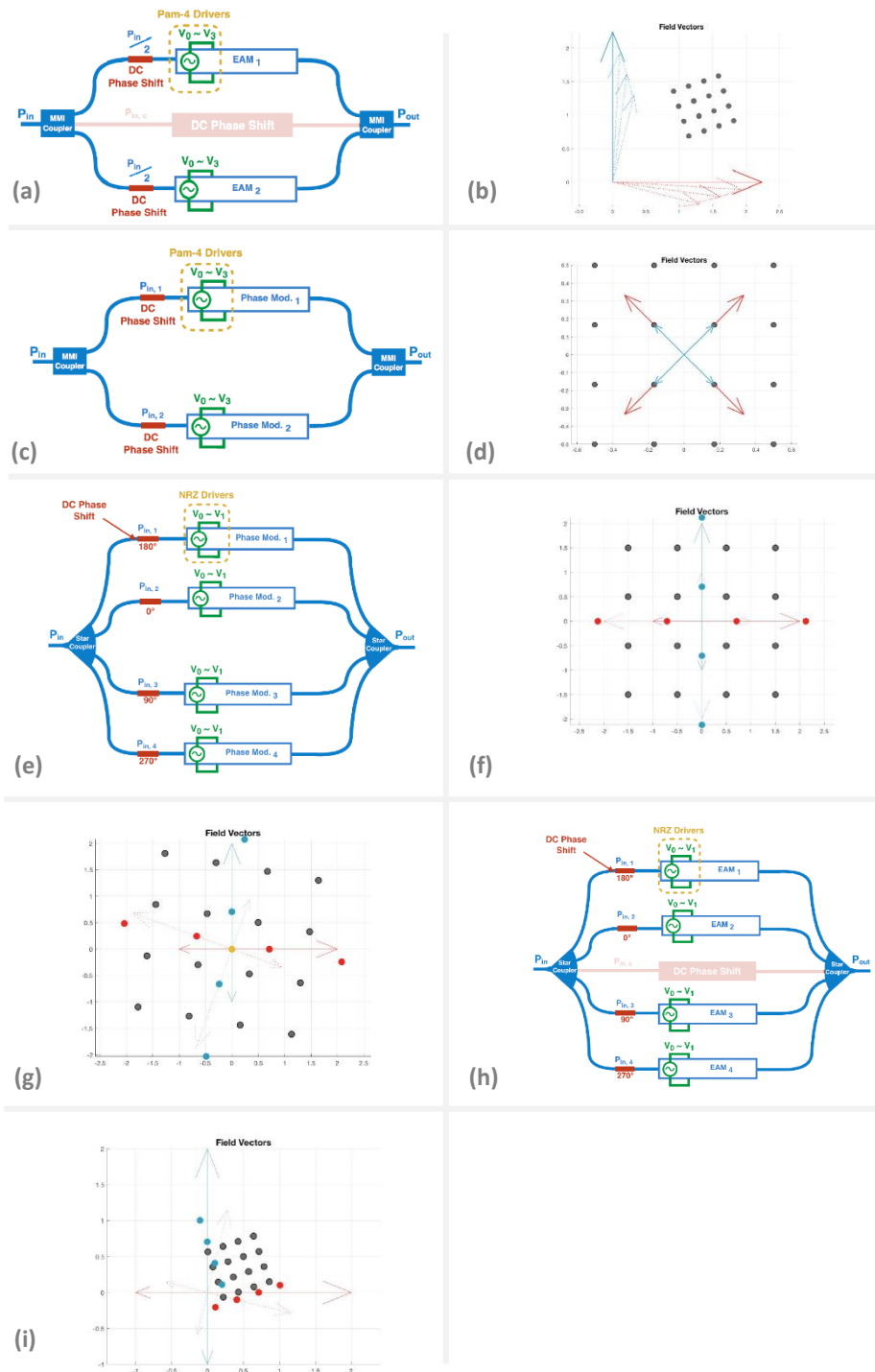
Fig. 2.10. QAM-16 optical circuit variations with (a, b, c, d) two modulators in parallel and (e, f, g, h, i) 4 modulators in parallel

2.7 System Power Penalty Analysis for PIC Architectures

In this section, we first provide a link budget analysis for a complete transceiver based on optical signal requirements according to IEEE standards for PAM-4 modulation formats. We then extend our analysis by comparing the link penalties of different PIC architectures for optical QPSK modulation. Finally, we compare the estimated total power efficiencies of the studied structures in a coherent optical link model. Considering the scalability of the QPSK PIC architectures, these analyses could be further extended to QAM-N modulation formats.

2.7.1 PAM-4 Link Budget Analysis

The generation of 400Gb Ethernet standard has been widely discussed in IEEE802.3bs 400GbE task force and is currently being adopted by network operators. Here we provide a link budget analysis based on the requirements of a typical transceiver. Fig. 2.11 shows a block diagram of a complete transceiver model in a wavelength-division-multiplexing (WDM) system, using PAM-4 modulation format in each channel and assuming that the acceptable signal that satisfies the receiver sensitivity has an optical power level of -13.8 dBm. Considering the PAM-4 SNR penalty and other optical losses, there is a +3.9 dBm of OMA is required at the output of the transmitter. This requirement puts a lower limit to the required vertical eye opening in an optical eye diagram of the transmitter module.
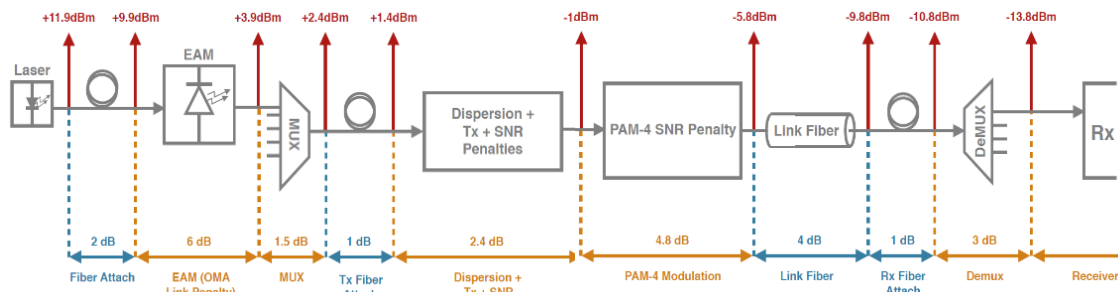
Fig. 2.11. Transceiver link budget analysis.

In this particular example, a single EAM is assumed as the modulator with an OMA link penalty of 6dB. This would require an input power of +11.9 dBm. This requirement might limit some flexibilities in designing the modulator circuits (An example would be the saturation power of an EAM that puts an upper limit to the input power). Such analysis could

be performed for any other types of modulators operating as a single transmitter or in a combination of multiple modulators.

2.7.2 Optical Power Penalty Analysis for Optical QPSK Modulators

In this sub-section, 3 QPSK PIC architectures are studied and compared. The first architecture, as shown in Fig. 2.12, involves 2 OOK-driven EAMs with same lengths placed in parallel in an MZI structure. The relative DC phase difference between the 2 arms is set to 90° and laser power is equally split into the arms. The generated constellation diagrams are shown in Fig. 2.12, when EAMs are ideal, or have finite ERs. On the constellation diagrams of Fig. 2.12, the blue vectors E_a and E'_a represent the field vectors of EAM$_1$ in its ON and OFF states, respectively. Red vectors E_b and E'_b represent similar vectors for EAM$_2$, while E_c represents the vector pointing to the center of the constellation. The black dots in the I-Q diagrams of Fig. 2.12 represent the 4 constellation points of the PIC. As shown in Fig. 2.12, even in the ideal EAM scenario, E_c is non-zero, which results in sending extra optical power into the link.
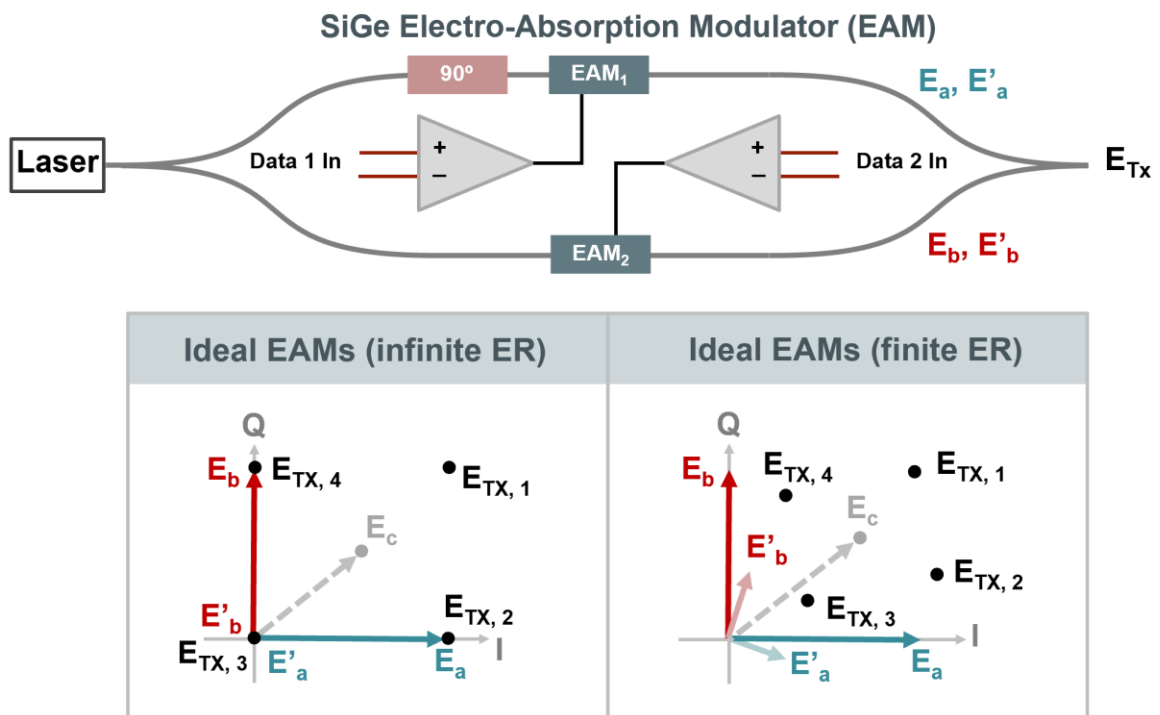
Fig. 2.12. QPSK Modulator and I-Q Diagrams using parallel EAMs in an MZI.

The EAMs' representative vectors could be defined as the following set of equations:

$$|E_a|^2 = \frac{P_{in}}{k \times 2L}, \qquad |E'_a|^2 = \frac{P_{in}}{k \times 2L \times R}, \qquad L \equiv 10^{\frac{IL_{EAM}}{10}}, R \equiv 10^{\frac{ER_{EAM}}{10}}, k=constant \qquad (2.4)$$

$$|E_b|^2 = |E_a|^2, \quad |E'_b|^2 = |E'_a|^2, \quad \theta: EAM\ chirp \qquad (2.5)$$

Starting from equations 2.4 and 2.5, the average optical power and the OMA of the QPSK constellation could be calculated as:

$$P_{Tx,\,avg} = \frac{k}{4}\left(\left|E_{Tx,1}\right|^2 + \left|E_{Tx,2}\right|^2 + \left|E_{Tx,1}\right|^2 + \left|E_{Tx,2}\right|^2\right) = \frac{P_{in}}{4L}\left(1 + \frac{1}{R} + \frac{Sin(\theta)}{\sqrt{R}}\right) \qquad (2.6)$$

$$P_{OMA} \equiv k\left|E_{Tx,i} - E_c\right|^2 = \frac{P_{in}}{8L}\left(1 + \frac{1}{R} - \frac{2\,Cos(\theta)}{\sqrt{R}}\right) \qquad (2.7)$$

Therefore, link penalties could be derived from equations 2.6 and 2.7 as:

$$LP_{OMA} = -10Log\left(\frac{P_{OMA}}{P_{in}}\right) = -10Log\left(\frac{1}{8L}\left[1 + \frac{1}{R} - \frac{2\,Cos(\theta)}{\sqrt{R}}\right]\right) \qquad (2.8)$$

$$LP_{avg} = -10Log\left(\frac{P_{avg}}{P_{in}}\right) = -10Log\left(\frac{1}{4L}\left[1 + \frac{1}{R} + \frac{Sin(\theta)}{\sqrt{R}}\right]\right) \qquad (2.9)$$

Furthermore, if the ER of the EAMs reach infinity, then the LPs would reduce to:

$$\Rightarrow if = R \rightarrow \infty:\ LP_{OMA} = 9dB + IL_{EAM} \qquad (2.10)$$

$$\Rightarrow if = R \rightarrow \infty:\ LP_{avg} = 6dB + IL_{EAM} \qquad (2.11)$$

The second and the third circuits of study involve a nested MZM with TW and segmented phase modulators, respectively. As shown in Fig. 2.13, output vectors E_A, E_B, E_c, and E_D are 90° apart from one another. E_A and E_B generate 2 possible outputs of $E_{1,1}$ and $E_{1,2}$, while E_C and E_D, produce $E_{2,1}$ and $E_{2,2}$ field vectors. The combination of the 4 possibilities would generate the 4 black constellation points named as $E_{Tx,\,I}$ in Fig. 2.13. As can be seen, the size of the constellation is directly affected by the voltage sing of the drivers, which translate to the vector phase shifts of θ in Fig. 2.13. The constellation would have its maximum size when θ is 90°. One observation here is that if the drivers do not achieve θ=90°, the

constellation would still be centered at the origin of the I-Q diagram, adding no extra average power to the constellation (E_c=0).
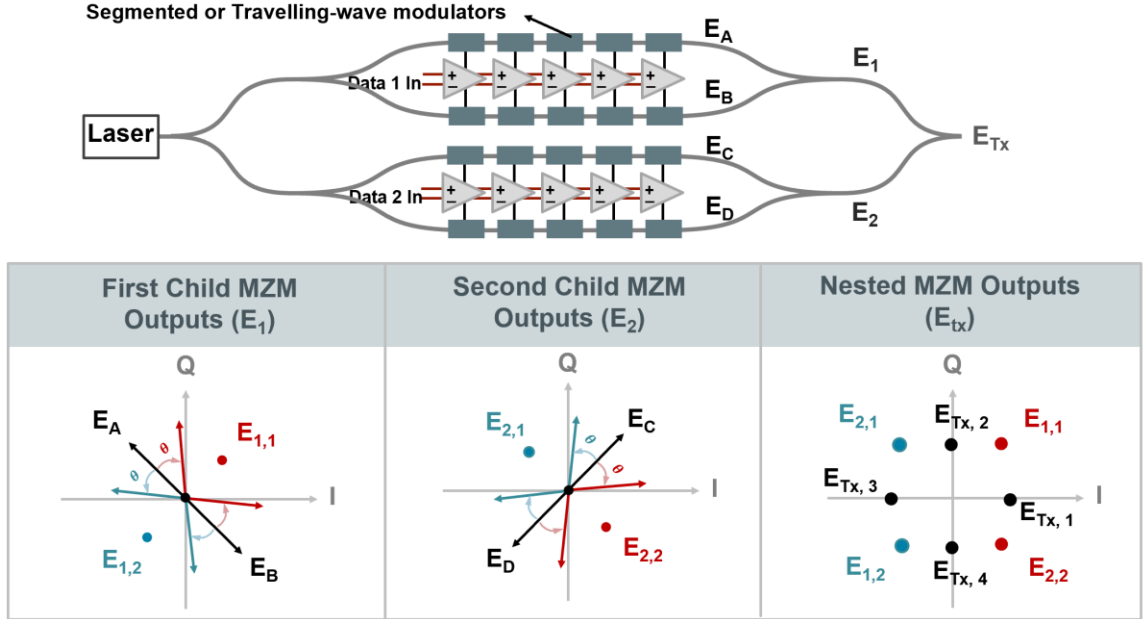
Fig. 2.13. QPSK Modulator and I-Q Diagrams using segmented or TW phase modulators in a nested MZM.

The same analysis could be repeated for this architecture to calculate the link penalties as:

$$P_{OMA} \equiv k\left|E_{Tx,i}\right|^2 = \frac{P_{in}}{4L}(1 + cos(\Delta\theta)) = P_{Tx,avg}, \quad L = 10^{\frac{IL_{PM}}{10}}, \quad \Delta\theta = \pi\left(1 - \frac{V_{sig}}{2V_\pi}\right) \tag{2.12}$$

$$LP_{OMA} = LP_{avg} = -10Log\left(\frac{P_{OMA}}{P_{in}}\right) = -10Log\left(\frac{1 + cos(\Delta\theta)}{4L}\right) \tag{2.13}$$

Furthermore, if V_{sig}=$2V_\pi$, then the LPs would reduce to:

$$\Rightarrow if\ V_{sig} = 2V_\pi: \quad LP_{OMA} = LP_{avg} = 3dB + IL_{PM} \tag{2.10}$$

To better understand the difference between the 2 architectures, both output constellations are superimposed in on I-Q diagram in Fig. 2.14. In the diagrams of Fig. 2.14, it is assumed that EAMs are ideal with infinite ER and phase modulators generate the largest possible constellation (θ=90º).
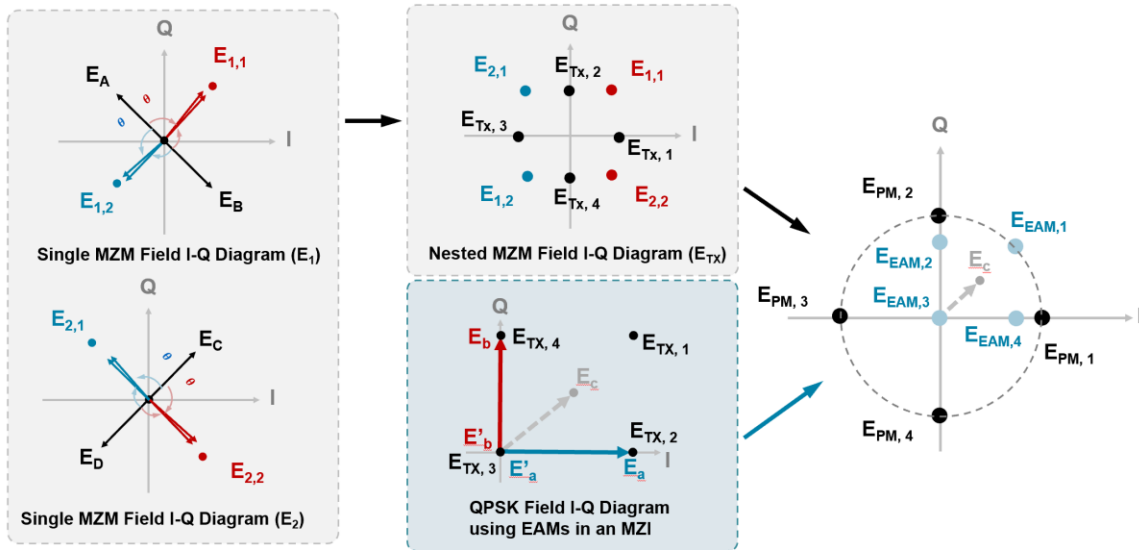
Fig. 2.14. QPSK I-Q diagrams comparison for 2 PIC architectures.

As shown in Fig. 2.14, the constellation size generated by the PIC architecture with EAMs is significantly smaller than the PICs with phase modulators. To numerically compare this difference, we calculate the link penalties for both architectures.

This might seem that phase modulators should always be better candidates for QPSK and higher-order coherent modulation schemes, however, a more comprehensive power analysis should be performed to fairly compare all architectures.

2.7.3   Total Power Efficiency Analysis for Optical QPSK Modulators

In order to properly compare the total power efficiency of the 3 PIC architectures, we study them in a coherent link model with the link budget analysis, shown in Fig. 2.15:
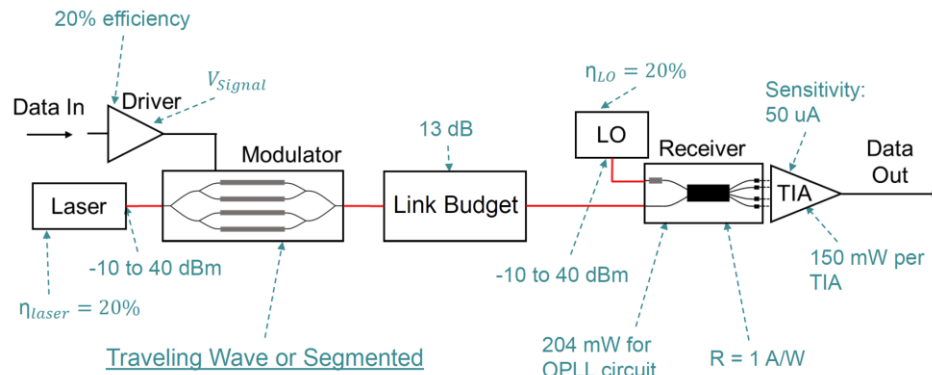
Fig. 2.15. Transceiver Link budget analysis (C. Schow, SPHPC 2019, May 30, 2019).

In this model, the total power efficiency would be similar for the 3 studied PIC architectures, except for the optical link penalties and driver power consumptions associated with each modulator type. While the architecture with EAMs has a relatively higher optical link penalty, due to their compact sized, the power consumptions of the drivers will potentially be smaller than the architectures with segmented and TW phase modulators. Tables 2.1 and 2.2 summarizes the study with the comparisons between the modulators and the power efficiencies of the 3 PIC architectures.

Modulator Type	Insertion Loss	Modulation Efficiency	Segment Length	Number of Segments	Total Capacitance	Driving Voltage	Operating Wavelength
Phase Modulators	2dB/mm	$V_\pi L_\pi = 1.5$ V.mm	200um	5	1.5 pF	1.3V	1330nm
SiGe EAMs	4dB	ER = 4.7 dB	46um	1	< 50 fF	2V	1540nm
InP EAMs	3dB	ER = 4.5 dB	46um	1	< 50 fF	2V	1540nm

Table 2.1. Modulators performance comparison.

Modulator Type	Architecture	Driving Type	Total No. of Drivers	Total Driver Power @ 50Gbd	Tx OMA Link Penalty	Tx Average Power Link Penalty	Total Power Efficiency
Phase Modulators	Seg-MZM	Push-Pull (Differential)	10	566 mW	9.03 dB	9.03 dB	8.5 pJ/b
	TW-MZM		2	70 mW			6 pJ/bit
SiGe EAMs	Single MZI structure	Single-ended / Differential	2	80 mW	19.79 dB	8.28 dB	10.05 pJ/bit
InP EAMs	Single MZI structure	Single-ended / Differential	2	80 mW	19 dB	7.25 dB	8.68 pJ/bit

Table 2.2. Power efficiency summary of the studied PIC architectures for QPSK modulation.

Chapter 3

PIC DESIGN FOR OPTICAL TRANSMITTERS

3.1 Optical PAM-4 Transmitter Using Parallel EAMs in an MZI Structure

In this section we show an SNR-optimized design of a DAC-less 100 Gb/s PAM-4 transmitter using two binary-driven uneven-length SiGe EAMs placed in an unbalanced MZI structure, and experimentally demonstrate that this design improves the power penalty and SNR of the transmitter.

3.1.1 Overview

Highly-integrated optical interconnects in silicon photonics are growing as preeminent platforms for the next generation optical transceivers for inter- and intra-datacenter applications. Multi-level Pulse-Amplitude Modulation (PAM-N) is a promising modulation scheme that increases the overall bandwidth density efficiency. However, the inherent optical power penalty imposes demanding linearity requirements on analog link components, which results in power hungry electronics. The modulator type should be carefully chosen to satisfy transmitter specifications such as optical modulation amplitude (OMA), extinction ratio (ER), signal-to-noise ratio (SNR) and electro-optical power penalties. Travelling-wave and lumped phase modulators require relatively large voltages (large $V_\pi L$) and power-hungry electrical drivers while having lower bandwidth due to excessive microwave losses and large capacitive parasitics [1]. Despite their compact dimensions, silicon photonic ring modulators require careful temperature stabilization [2]. Electro-absorption modulators (EAMs) do not suffer from the mentioned limits due to their smaller footprints and lower voltage requirements, which make them attractive for high-speed modulation and dense integration with low pJ/bit energy efficiencies [3, 4, 5, 6]. However, their performance for PAM-4 is limited by transfer function linearity, input optical power and modulation chirp. In [7] a DSP-free 128 Gb/s PAM-4 silicon photonic transmitter using two binary-driven SiGe EAMs with even 120um length has been reported to eliminate above limits. The architecture, however,

is not optimized for SNR and power penalty, and has device performance that is more sensitive to fabrication process variations due to the fixed input split ratio.

3.1.2   Transmitter Design

A strong optical modulator candidate for PAM-4 transmission is the EAM due to its small form factor, which represents relatively small parasitics (a few fF rather and a few hundreds of fF in lumped phase shifters), hence, larger electro-optical bandwidths (EOBW). EAMs also require small driving voltages ($< 2V$) to achieve the ER of more than 4.5dB. EAMs' compatibility with CMOS drivers is also attractive for integrated solutions for the 400GbE generation. Two major challenges of the EAMs are, however, their excessive insertion losses and their input optical power limit. Once the optical power crosses this limit, the EAM would go into the saturation region and there drops significantly. In this section we demonstrate how these challenges could be treated for an optimal PAM-4 transmission.

Generating equidistant PAM-4 power levels is achieved in various ways depending on the transmitter architecture. As elaborated in chapter 2, one method involves a non-equidistant PAM-4 electrical driver to modulate a single EAM. Alternatively, an optical PAM-4 is realized using 2 binary-driven EAMs. While placing 2 EAMs in series (segmented EAMs) would suffer from excessive insertion loss and limited optical input power, having them placed in parallel would break both limits, although, careful considerations for interferometric effects should be considered. In order to keep the electronics power at minimum, we choose to utilize two NRZ OOK drivers with the minimum possible voltage (2V) swing to still satisfy the ER requirements and avoid burning excessive power (since the overall electronics power consumption scales with the 2nd power of its output swing voltage).

The design and optimization problem could now be studied by generalizing the variables of the system. The design variables of the MZI structure shown in Fig. 3.1, include the input optical power ($P_{in, a}$ and $P_{in, b}$), length of EAMs (L_1 and L_2), driver voltages (V_0 and V_1) and the coupling coefficient of the combiner (k_{out}).
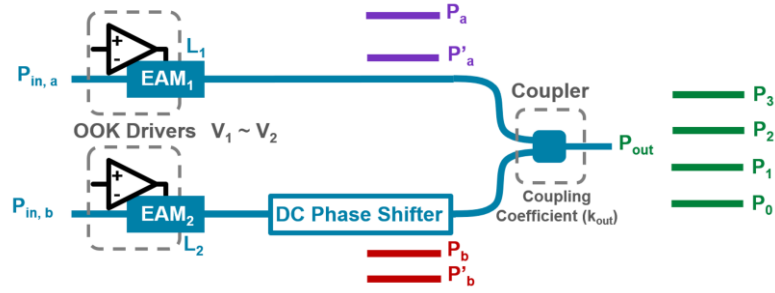
Fig. 3.1. (a) PAM-4 circuit optimization problem using EAMs in parallel

As shown in Fig. 3.2, the optical power coming from the two arms will not be added linearly. In fact, the field vectors (rather than the optical powers) from each arm are added linearly.
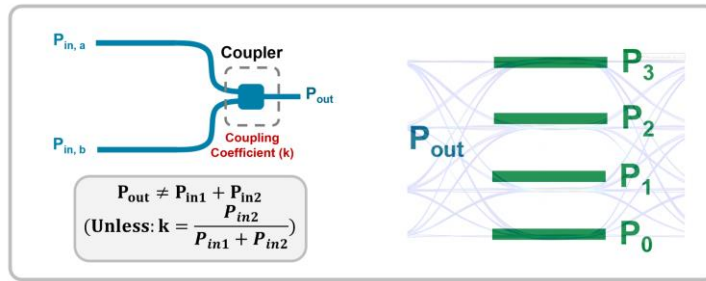
Fig. 3.2. Non-linear power addition at the optical coupler

By setting target values for the outer OMA and the ER of the transmitter, one could calculate the necessary power levels P_0 through P_3 in Fig. 3.1. Starting from the output port and going backwards, one can calculate the required power levels at the output of each EAM by determining the coupling factor of the combiner (we show that the coupling factor should not necessarily be 0.5).

$$P_{out} = \left| \sqrt{(1-k)P_{in1}} + \sqrt{(k)P_{in2}} \right|^2 \tag{1-1}$$

$$P_{out} = \left| \sqrt{(1-k)P_{in1}}\, e^{j\theta_1} + \sqrt{(k)P_{in2}}\, e^{j\theta_2} \right|^2 \tag{1-2}$$

The relationships for the power combination of a power coupler with 2 arms are provided in equation (1-1) and (1-2), when there is zero or a θ-degree phase shift between the 2 arms, respectively.

Considering equation (1-1) for the PAM-4 transmitter, a set of 4 non-linear equations (2-1) through (2-4) with 5 unknowns of P_a, P'_a, P_b, P'_b and k are generated, where P and P' are the ON and OFF states of each EAM and k is the power coupling factor of the combiner.

$$\sqrt{(1-k)P_a'} + \sqrt{k P_b'} = \sqrt{P_0} \qquad (2\text{-}1)$$

$$\sqrt{(1-k)P_a} + \sqrt{k P_b'} = \sqrt{P_2} \qquad (2\text{-}2)$$

$$\sqrt{(1-k)P_a} + \sqrt{k P_b'} = \sqrt{P_2} \qquad (2\text{-}3)$$

$$\sqrt{(1-k)P_a} + \sqrt{k P_b} = \sqrt{P_3} \qquad (2\text{-}4)$$

The problem could be simplified and reduced to a system of 4 linear equations and 4 unknowns as shown in Fig. 3.3. We now have a set of 4 linear equations with 4 unknowns. Since the left-hand sides of the equations are dependent (i.e. a linear combination of 3 chosen equations can build the 4th one), the associated matrix "A" to this system is singular (i.e. if we write the system above in the form Ax=b which "x" is the vector of the unknowns, the 4-by-4 matrix "A" would have a rank of 3 rather than 4). Hence, according to the right-hand sides of the set, the system will either have infinite answers or no exact solution. By applying the same linear combination of the 3 chosen left-hand side equations to the right-hand side, we realize that for the system to have infinite solutions (rather than having no solutions) it should be required that $\sqrt{P1} + \sqrt{P3} = \sqrt{P2} + \sqrt{P4}$. And since we know that the output power levels should be equally spaced, we should also have $P1 + P3 = P2 + P4$. These two conditions are non-consistent and in fact, the former does not hold for any set of 4 target output powers satisfying the latter. Therefore, the equation set shown in Fig. 3.3 is always a non-consistent system with no real solutions. In fact, this system has no real answers due to the resulting equidistant vector fields requirement, which are inconsistent with equidistant output power requirements.

Fig. 3.3. Original parallel PAM-4 problem.

One way to address this problem is to introduce a relative phase shift between the two arms such that the added field vectors generate equally spaced output power levels [6]. This method, however, reduces power efficiency since a significant portion of power is lost as the relative phase shift between two arms increases (one would expect a null point when this phase difference is π). Another way is to use two intensity modulators (EAMs) with even-length and uneven input power split, such as 0.33:0.66 [7]. The output OMA and the SNR could, however, be further optimized by using uneven lengths and unbalanced couplers.

To still go forward, the set of values for the unknowns *a, b, a'* and *b'* should be calculated such that the "error" of the system (Ax = b) is minimized. The proposed approach here is to solve for the 4 unknowns in presence of a mathematical noise vector, such that the overall SNR of the unequally-spaced PAM-4 levels (Fig. 3.4) is maximized.

This will turn into a convex optimization problem. There are several factors to optimize the estimated solution of the system. We first consider the symbol-error-rate equation for an unequally spaced PAM-4 transmission, assuming that symbols are equally-likely transmitted, noise statistical distribution is Gaussian and noise power is independent from the optical signal power, as given in Fig. 3.4:
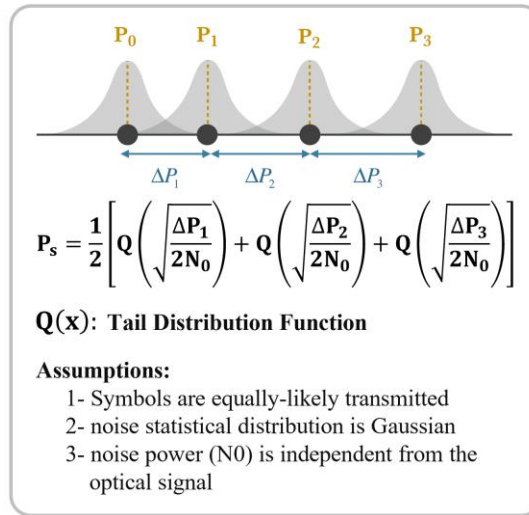
Fig. 3.4. Symbol error rate for the unequally spaced PAM-4 transmitter

Where N_0 is the Gaussian noise power and ΔP_i is shown in Fig. 3.4. It is observed from equation of Fig. 3.4 that the dominant factor affecting the BER will be the smallest eye, as the changes in the Q function are steep as the argument goes beyond 7 to achieve a BER of the order -12. Therefore, the problem turns into a convex optimization problem shown in Fig. 3.5.

Fig. 3.5. Proposed convex optimization problem for solving the unequally spaced PAM-4 transmitter

For a numerical solution to this problem, we assume that we require an ER of 5dB and an outer OMA of 2.45mW. Then, the solution to the problem, using the "cxv" optimization toolbox in MATLAB, is shown in Fig. 3.6. In the resulting simulated eye diagram of Fig. 3.6, the optimized levels (in blue) are unequally spaced, however, the smallest eye (bottom) is still larger than the minimum eye closure requirement.
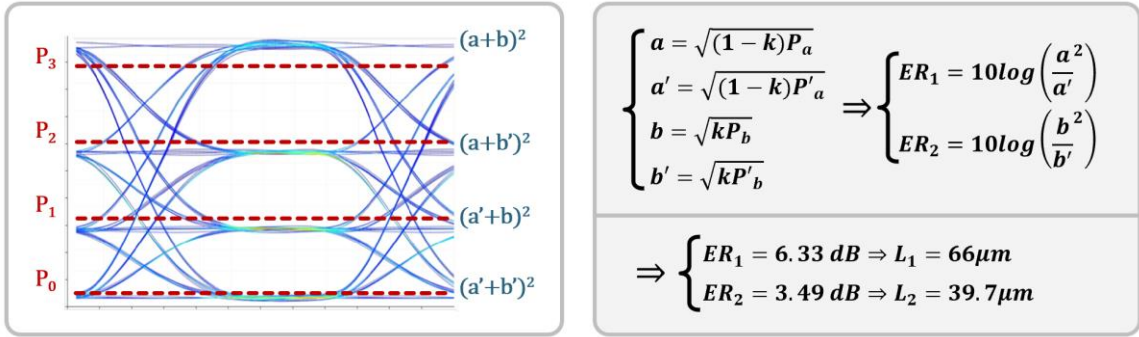
Fig. 3.6. Convex Optimization problem results for the unequally-spaced PAM-4 transmitter

Since simulation results are independent from k_{out}, it could be set independently to minimize the required input power. The required ERs for each arm would also be calculated as $ER_1 = 10 \times \log ((a/a')^2) = 6.33$dB and $ER_2 = 10 \times \log ((b/b')^2) = 3.49$dB. We should now determine the optimum coupling coefficient "k" to use the minimum input power to the modulator. The plots in Fig. 3.7 show that by sweeping over "k", one can achieve different combinations of the EAM output powers necessary for operation. From these data, and considering the insertion loss for each arm, the necessary input power to the EAMs and their sum (which would be our measure for the total input power) are provided in Fig. 3.7. The sweep for k_{out} in Fig. 3.7 shows that the required input power is minimized at 0.39 (rather than 0.5). Such design optimization for SiGe FK-EAMs operating at 1550 nm wavelengths leads to the optimum EAM lengths of 66 μm and 40 μm. While considering the input power to each EAM should not pass +6.2dBm (the gray line in Fig. 3.7), one can also consider the point at which k=0.3 in case better ER (at the cost of more input power) is desired.
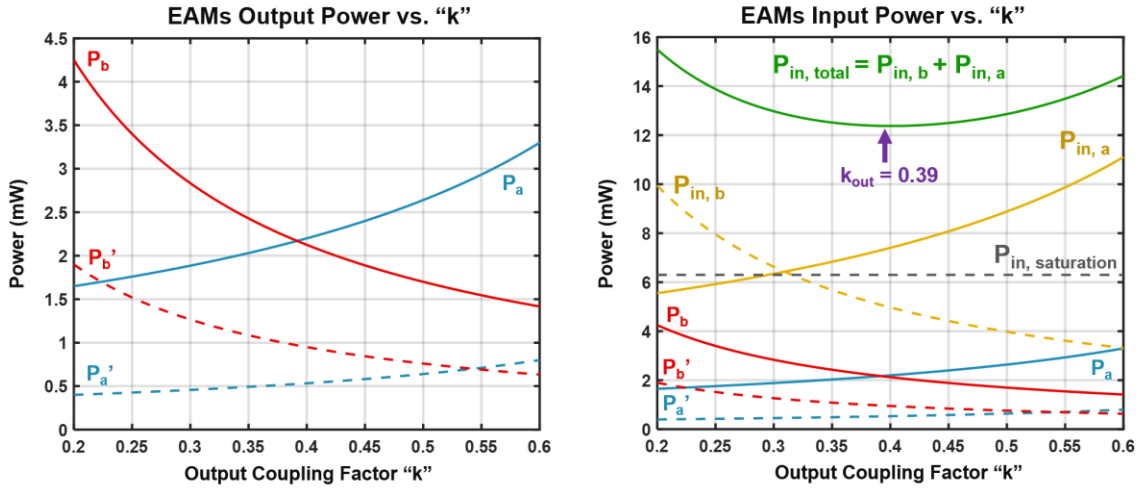
Figure 3.7. EAMs' input power vs. combiner coupling coefficient

3.1.3   Experimental Results

The photonic integrated circuit described in section II is fabricated in Rockley Photonics multi-micron Si-photonics platform, which is an EAM-based high-speed platform optimized for high density integration, low power consumption, and co-packaged optics [3, 4]. The proposed PAM-4 transmitter circuit is shown in Fig. 3.8 along with the required specifications in table (1). The unbalanced output combiner and the input power splitter are realized by MZI variable couplers using thermal phase shifters and multi-mode interference (MMI) devices (Fig. 3.8). The targeted splitting and combining ratios are set by generating a relative DC phase shift for each variable coupler. All 1×2 and 2×2 MMIs are balanced for the best performance. MMI couplers are chosen over Y-junctions and directional couplers due to their excellent insertion loss and robustness against process variations.
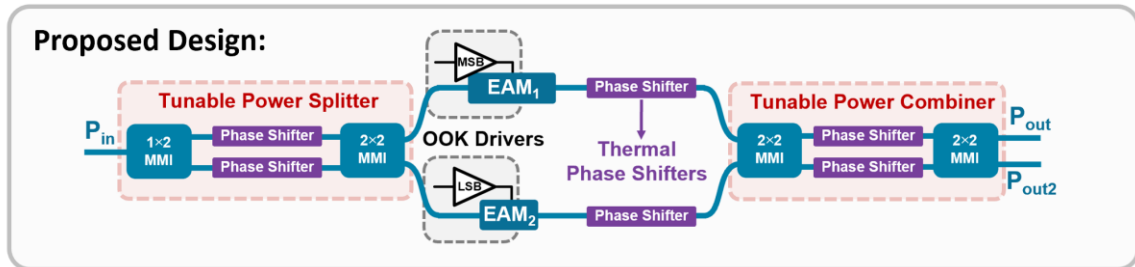
Figure 3.8. Proposed PAM-4 transmitter chip layout

Table 3.1. Proposed PAM-4 Transmitter Specifications at 1545 nm Center Wavelength

Sections	EAM Lengths	ER	P_{off}	P_{on}	P_{in}	IL	LP
	(um)	(dB)	(mW)	(mW)	(mW)	(dB)	(dB)
Arm 1							
k = 0.39	66	6.33	2.18	0.51	7.45	5.34	6.49
k = 0.3			1.9	0.44	6.49	5.34	
Arm 2							
k = 0.39	39.7	3.49	2.12	0.95	5	3.72	6.3
k = 0.3			2.74	1.23	6.44	3.73	
Total							
k = 0.39	--	4.95	4.26	1.36	12.46	4.66	6.49
k = 0.3					12.94	4.82	6.49

Measurement setup is shown in Fig. 3.9. The optical signal is amplified prior to the chip to improve the SNR. Input power increase was only possible thanks to the parallel architecture, capable of receiving approximately double the amount of laser power without saturating the EAMs.
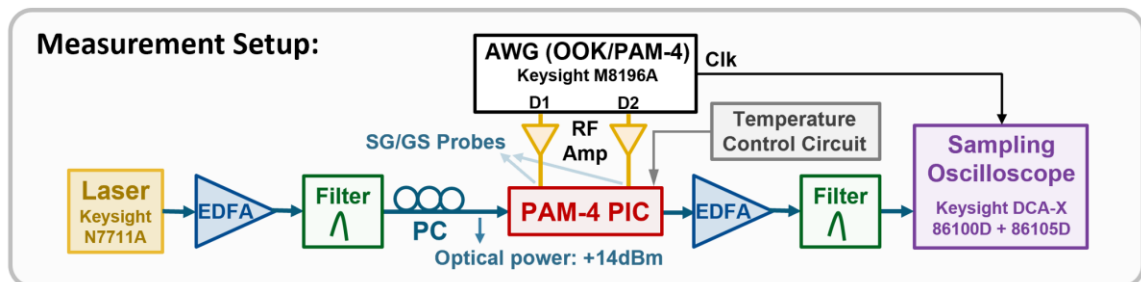
Figure 3.9. PAM-4 Transmitter Measurement setup

Fig. 3.10 shows the 66µm EAM measured ER, IL and ER/IL spectra. Fig. 3.10 also shows the same measurements for the 39.7µm EAM. It can be inferred that at room temperature, the optimal operating points of the EAMs are approximately at the wavelength of 1515nm. In order to shift the operating points back to the original target of 1550nm, a temperature sweep was performed and the spectra for both EAMs were measures. The temperature of the chip was controlled by a Peltier heater/cooler and read via an off-chip thermometer, which was placed adjacent to the PIC. As shown in Fig. 3.11 the optimal operating points of the 66µm EAM were shifted close to the target wavelength (1454nm) at 45ºC.
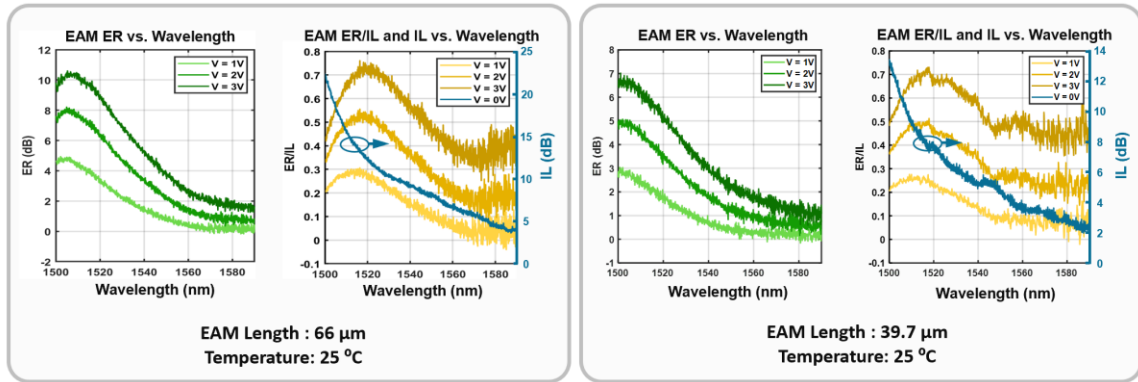
Figure 3.10. Measured ER, IL and ER/IL spectra of a 66µm EAM (left) and 39.7µm EAM (right) under different bias voltages.
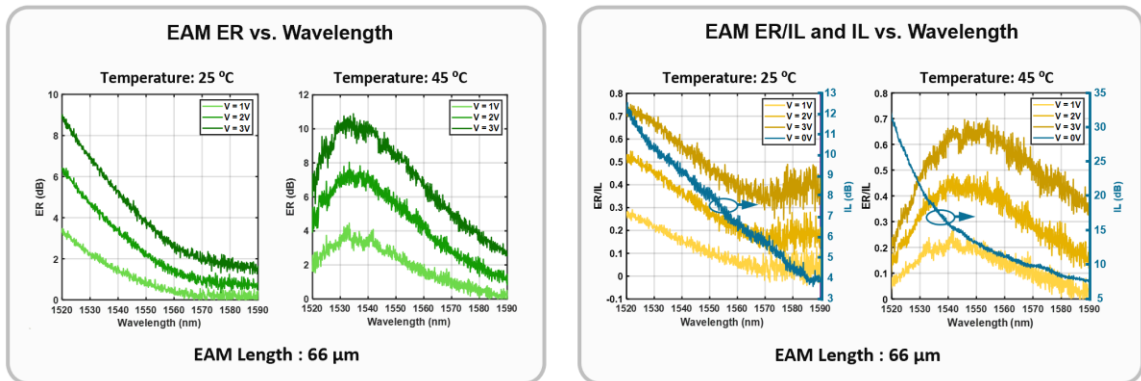
Figure 3.11. (a) Measured ER, IL and ER/IL spectra of a 66µm EAM under different bias voltages, (b) Measured ER/IL spectra of the 66µm EAM over different temperatures

This means that, ideally speaking, the temperature of the EAMs should be kept at 45ºC, while the rest of the PIC components, operate at room temperature, for the optimal performance. One problem with heating up the whole PIC would be shifting the thermal operating point of all other components, such as the MMI couplers. Although this temperature shift did not degrade the performance of the MMIs significantly, more considerations were made into the layout of the PIC to alleviate this challenge. The thermal phase shifters placed in the middle MZI structure, which were originally considered to generate DC phase shift between the 2 arms to align the optical field vectors, were placed close to the EAMs. Proximity of these phase shifters to the EAMs resulted in heat leakage from the thermal phase shifters to the

EAMs. This effect was utilized to increase the temperatures of the EAMs locally and keep the rest of the components at the ambient temperature, set by the Peltier heater. Since there was predicted 2 thermal phase shifters, one on each arm of the middle MZI, it would provide enough degree of freedom to both align the field vectors and locally heat up the EAMs simultaneously. Two voltages of 3.3V and 3.35V were applied to the middle phase shifter, at which the average voltage of 3.4V kept the EAMs at 45ºC, while the 0.05V difference kept the field vectors aligned.

Fig. 3.12 shows the electrical and optical eye diagrams measured for single EAMs at 50Gb/s with 50Ω probes. The single EAMs were fabricated on a separate PIC for verification measurements.
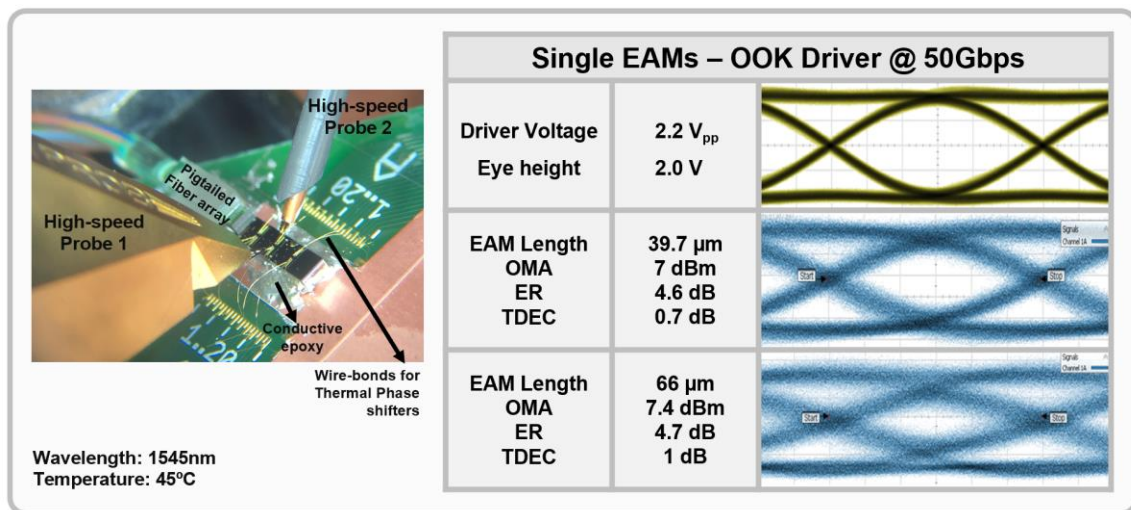
Figure 3.12. Electrical and optical NRZ eye diagrams at 50 Gb/s for individual EAMs

Fig. 3.13 displays the eye diagrams for a single EAM, as well as the proposed PAM-4 design, all driven at 50 Gbaud with 50Ω probes. The unbalanced MZI design exhibits 1.2dB better ER and 0.7dB better TDECQ at 50 Gb/s compared to a single EAM driven by an unequally-spaced and pre-emphasized PAM-4 driver. Moreover, at 100 Gb/s, the unbalanced MZI PAM-4 has 0.9dB better ER and 2.1dB better SNR. This scheme opens a pathway for sub-pJ/bit power consumption of EAM-based 100 Gb/s PAM-4 modulators, and a path to 200 Gb/s/λ by relaxing the combined requirements on EAM bandwidth, ER, and linearity for

higher PAM-4 data rates. A DAC-based Bi-CMOS driver with a significant bias is required to drive a single EAM into its linear regime, but with this scheme two 2V CMOS NRZ 50 Gbaud drivers can be used [3], resulting in < 1 pJ/b of power consumption at 100 Gb/s.

Single 66μm EAM – OOK/PAM-4 Driver			Proposed Parallel PAM-4 Design		
Rate	50 Gb/s		Rate	100 Gb/s	
OMA	7.4 dBm		OMA	7 dBm	
ER	4.7 dB		ER	5.5 dB	
Driver Voltage	$2V_{pp}$		Driver Voltage	$2 / 2.1\ V_{pp}$	
TDEC	1dB		TDECQ	2.4dB	
Rate	50 Gb/s		Rate	50 Gb/s	
OMA	7.2 dBm		OMA	8.1 dBm	
ER	4.6 dB		ER	5.8 dB	
Driver Voltage	0/ 0.4/ 0.9/ $2\ V_{pp}$		Driver Voltage	$2 / 2\ V_{pp}$	
TDECQ	2.5dB		TDECQ	1.8dB	

Wavelength: 1545nm, Temperature: 45ºC
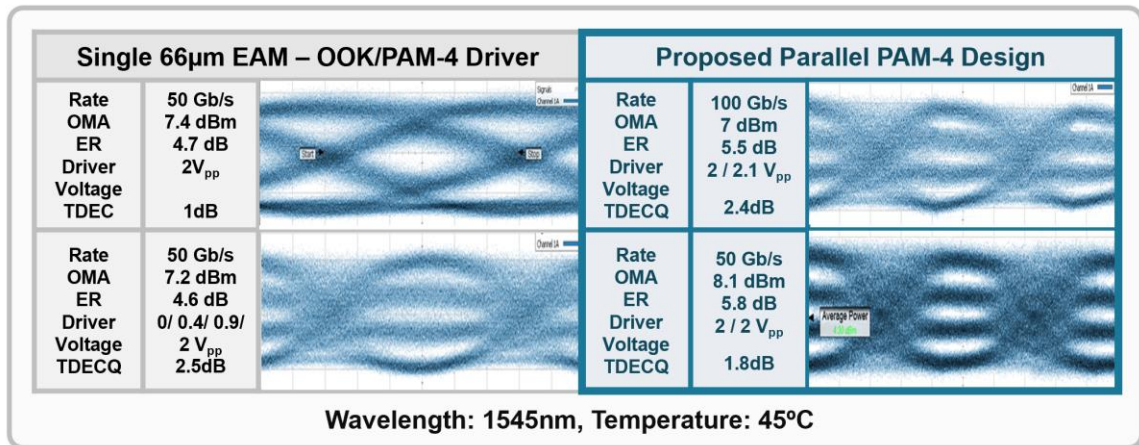
Figure 3.13. Optical PAM-4 eye diagrams for several configurations including the proposed PAM-4 chip

3.2 Optical QAM-16 Transmitter Using Parallel EAMs in a multi-arm MZI Structure

In this section, we study the design and optimization of a DAC-less 200Gb/s QAM-16 transmitter in a multi-micron silicon-photonics platform using 4 binary-driven SiGe EAMs in an unbalanced MZI structure. We experimentally demonstrate the transmitter exhibits bit-error rates of 3×10^{-4} and 2.8×10^{-4} for square and hexagonal constellations.

3.2.1 Overview

Multi-point Quadrature-Amplitude Modulation (QAM-N) is a promising modulation scheme that increases the overall bandwidth density efficiency in coherent applications. However, the inherent optical power penalty imposes demanding linearity requirements on analog link components, which results in power hungry electronics. Generating QAM-16 constellations can be achieved using several optical and electrical circuit architectures. One common way of generating a square QAM-16 constellation is through two 4-level amplitude modulators nested in an in-phase/quadrature (I/Q) modulator. Each 4-level amplitude modulator could

be implemented by either a single optical modulator and a 4-level driving signal, or 2 phase/amplitude modulators, placed in parallel, and driven by on-off-keying (OOK) signals [8, 9, 10]. Hexagonal QAM-16 constellations benefit from triangular latices, which result in 10% reduction in required power to generate a square QAM-16 constellation of the same lattice size. Hexagonal QAM-16 constellations, unlike square QAM-16, are only realizable via 4 parallel amplitude modulators.

The choice of the optical modulator for the design of a QAM-16 transmitter directly affects the overall transmitter performance metrics, such as the overall constellation size, bit-error-rate (BER), and electro-optical power penalties. Travelling-wave and lumped phase modulators require relatively large voltages (large $V_\pi L$) and power-hungry electrical drivers while having lower bandwidth due to excessive microwave losses and large capacitive parasitics [11]. Moreover, these phase modulators should exhibit π phase shift at high speeds to maximize the size of the QAM-16 constellation, since lower phase shift angles will result in a shrunk and rotated constellation. Despite their compact dimensions, silicon photonic ring modulators require careful temperature stabilization, while their undesired phase modulation (modulation chirp) should be compensated when placed in parallel [12]. Electro-absorption modulators (EAMs) do not suffer from the mentioned limits due to their smaller footprints and lower voltage requirements, which make them attractive for high-speed modulation and dense integration with low pJ/bit energy efficiencies [13, 14, 15, 16]. However, their performance for QAM-N is limited by non-linearities in the optical transfer function, maximum input optical power, and modulation chirp. In this work we show an optical signal-to-noise ratio (OSNR)-optimized design of a DAC-less 200 Gb/s QAM-16 transmitter using 4 binary-driven SiGe EAMs placed in an unbalanced 5-arm MZI structure, and experimentally demonstrate square and hexagonal QAM-16 generation with optimal power penalties and BER performance.

3.2.2   Transmitter Design

The proposed photonics circuit architecture of the QAM-16 transmitter is shown in Fig. 3.14. The circuit includes 4 identical EAMs in an unbalanced 5-arm interferometer. All EAMs

have same lengths, so that they exhibit equal modulation chirp, when driven with same driving voltage levels. This will ensure constellation symmetry for both square and hexagonal formats. The optional 5th interferometric arm is incorporated in the design to move the generated off-centered constellation back to the origin and avoid sending extra optical power into the link. This arm could alternatively be used to adjust the optical power of the carrier signal sent into the link.
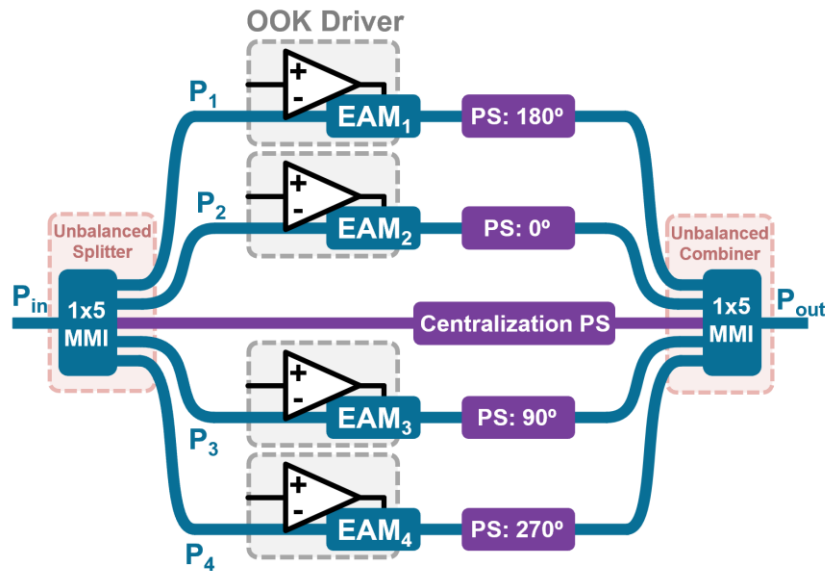
Figure 3.14: System block diagram of the optical QAM-16 transmitter.

All design parameters such as EAM lengths, optical power levels entering each arm, driving voltage amplitude, and the relative static optical phase difference between arms are included in the optimization problem, shown in Fig. 3.15.
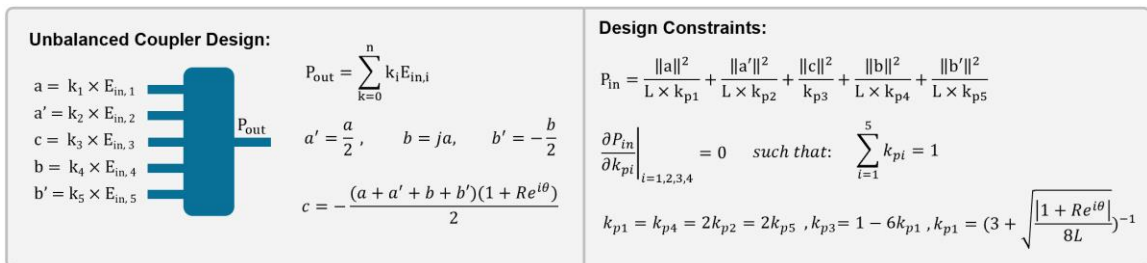
Figure 3.15: Proposed optimization problem to solve for unbalanced 1×5 splitting/coupling ratios.

The 5×1 coupler is considered to have power combining ratios k_1 through k_5 that need to be optimized based on EAM characteristics and to minimize the required total optical input power. The EAM placed on the i-th arm receives the optical power Pin, i (with an optical vector field Ein, i). The output optical field of each EAM is denoted by $E_{EAM, i}$, which is equal to $E_{in, i} \times L$ for the ON state, or $E_{in, i} \times L \times R \times e^{j\varphi(V)}$ for the OFF state, in which L stands for the EAM insertion loss (IL), R stands for the EAM extinction ratio (ER), and $\varphi(V)$ denotes the EAM modulation chirp in radians, when driven by a signal of amplitude *V*. As shown at the bottom of Fig. 3.15, the required coupling coefficients of the 5×1 combiner is calculated for both QAM-16 formats. The EAM lengths should still be optimized separately. Increasing the EAM lengths would provide more ER, however, the IL and the modulation chirp also increase.

The plot shown in Fig. 3.16 shows the required optical input power, with/without the centralization arm power included. This plot is generated for the Si-Ge FK-EAMs used in this design, resulting in optimized EAM lengths of 78 μm. The plots in Fig. 3.17 depict the resulting square and hexagonal QAM-16 constellations, along with the 4 pairs of field vectors representing the ON/OFF states of each modulating arm.
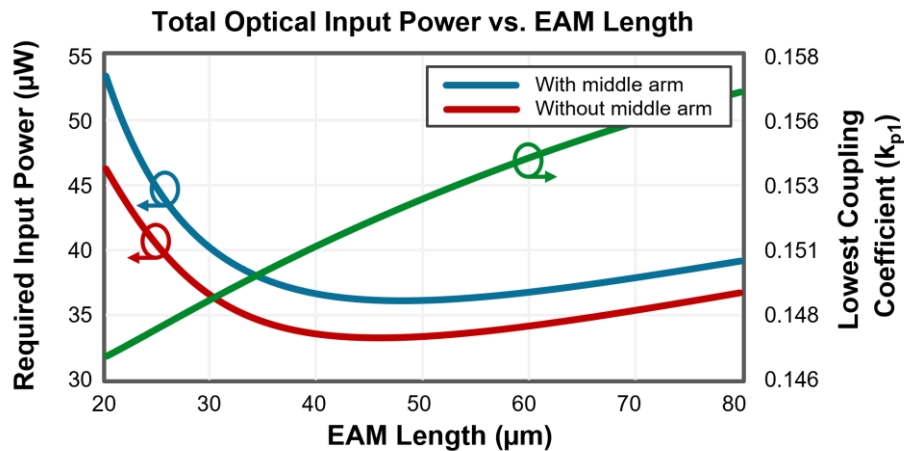
Figure 3.16: EAM length optimization.
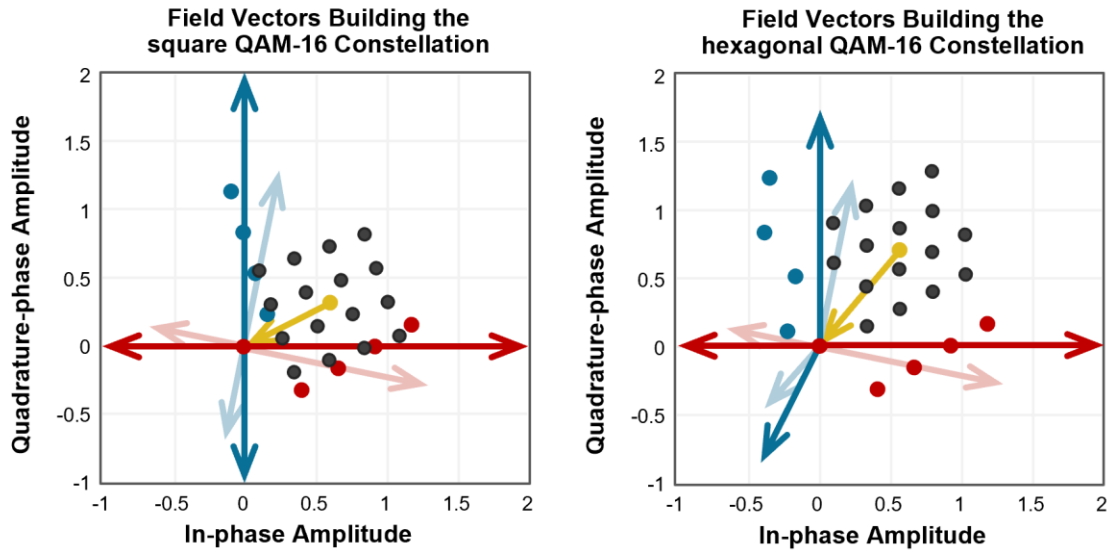
Figure 3.17: Optimized field vectors constructing the QAM-16 constellation.

The power splitting/combining ratios of the 1×5 couplers are derived as 1:2:0.78:2:1. The structure shown in Fig. 3.18 is proposed to generate the uneven splitting/combining ratios. The benefits of this structure compared to cascaded 1×2 couplers and star couplers are superior robustness across temperature, wavelength, and process variations, in addition to lower overall insertion loss. As shown in Fig. 3.18(a), A balanced 1×7 MMI is put at the input to split the incoming power into 7 equally-split outputs. Outputs 2, 3, 5 and 6 are phase matched via waveguide tapering, and are fed to balanced 2×1 MMIs to constructively combine their optical power. In order to achieve the desired splitting factor for the middle arm, an unbalanced 1×2 MMI is designed to keep 78% of the optical power and dissipate the rest. This is achieved by introducing an asymmetricity to a balanced 1×2 MMI, as shown in Fig. 3.18(b). Starting from a balanced MMI, a rectangular piece with a length lower than the total length of the MMI region is removed. This cut piece directs the power concentration of the MMI optical modes into one output. While the photonics circuit can be redesigned for the hexagonal format, we experimentally show that the design optimized for the square format can also be used for the hexagonal version, since the only difference in the hexagonal setting is the power splitting ratios and the relative static phase differences between the arms.
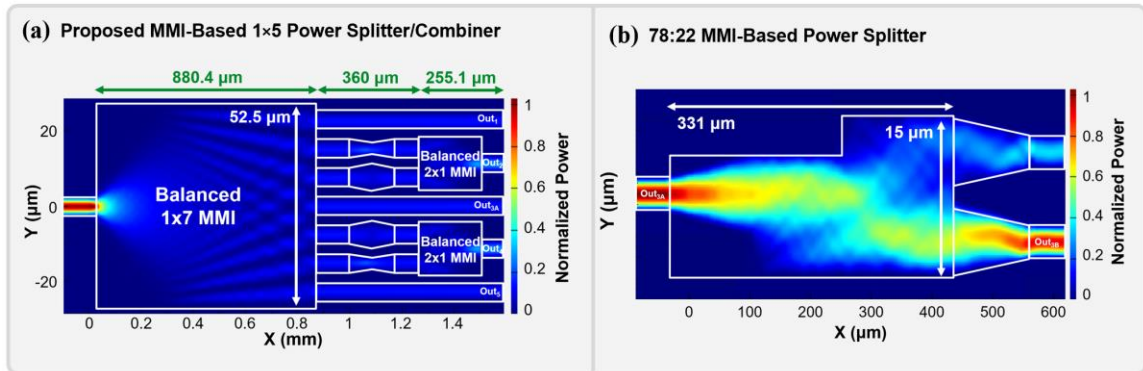
Figure 3.18: (a, b) Proposed MMI-base unbalance 1×5 power splitter/combiner.

3.2.3 Experimental Results

The photonic integrated circuit proposed in section II was fabricated in Rockley Photonics multi-micron Si-photonics platform, which is an EAM-based high-speed platform optimized for high density integration, low power consumption, and co-packaged optics [6, 7]. Fig. 3.19 shows the optical measurements of the custom-designed 1×5 splitter/coupler. The laser input power was set at 0-dBm, and the 5 optical output levels were measured across wavelengths from 1500nm to 1630nm and temperatures from 30ºC to 60ºC. Maximum output power imbalance at each wavelength was measured at 0.21dB. The overall IL of the structure at the operating point of 55ºC and 1550nm was measured at 0.44dB, with fiber-to-chip edge coupling losses of approximately 6.4dB.
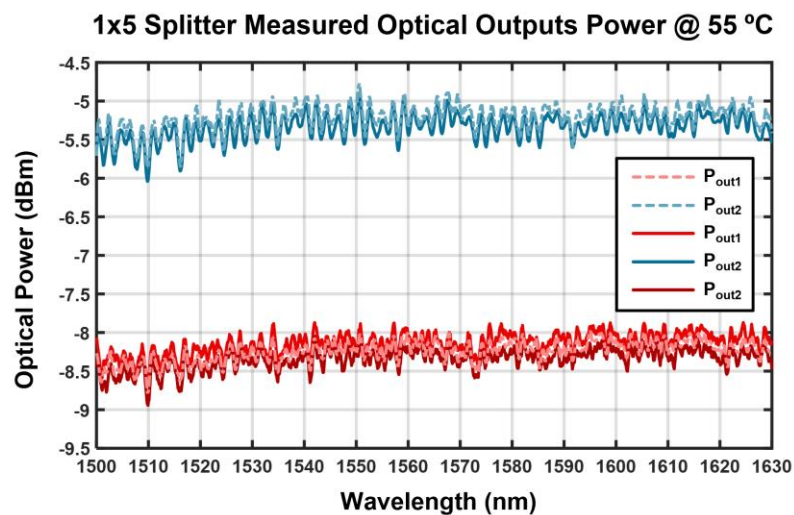
Figure 3.19: Measured optical output levels of the proposed coupler.
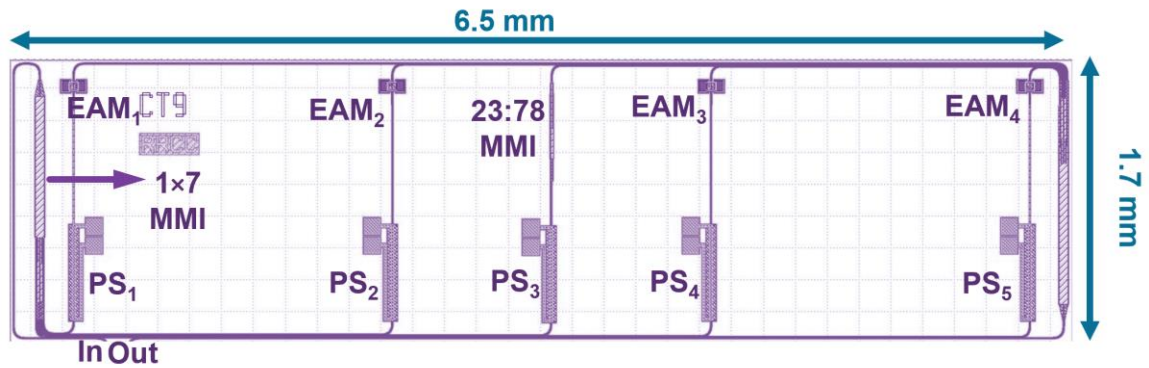
Figure 3.20: Fabricated photonics chip layout.
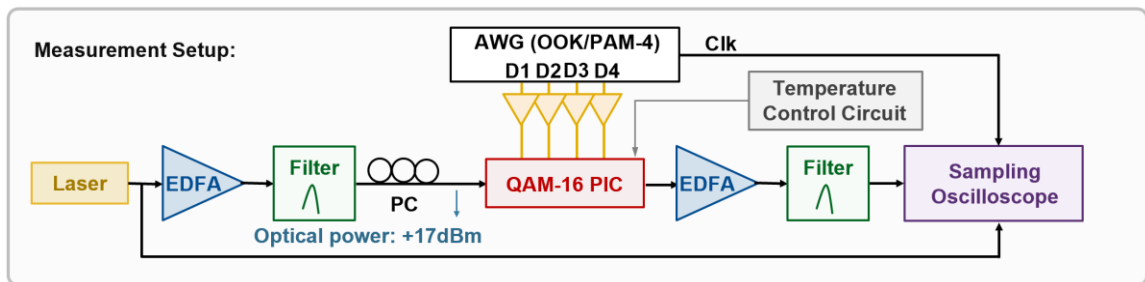
Figure 3.21: QAM-16 Transmitter measurement setup.

The complete layout of the proposed QAM-16 optical transmitter is shown in Fig. 3.20. The static optical phase shifts between arms are generated by applying DC voltages to thermal phase shifters on each arm. The measurement setup is shown in Fig. 3.21. The optical signal is amplified prior to the chip to improve the OSNR. An arbitrary waveform generator provides 40 to 50 Gb/s PRBS-31 data streams for 4 high-speed probes, which drive all EAMs with 2VPP amplitudes. The transmitter output is monitored using a high-speed coherent sampling oscilloscope, with an internal 90-degree hybrid and a self-homodyne detection architecture. Fig. 3.22 show measured square QAM-16 constellations at 40 Gbaud (160 Gb/s) and 50 Gbaud (200 Gb/s), respectively. Each figure shows measurements under two settings, when the middle arm is used to centralize the constellation, or to shift it away from the origin. As shown in both figures, the middle arm can successfully centralize the constellation. Depending on the receiver and the detection architecture, the off-centered versions with extra average power can be fed into the link.
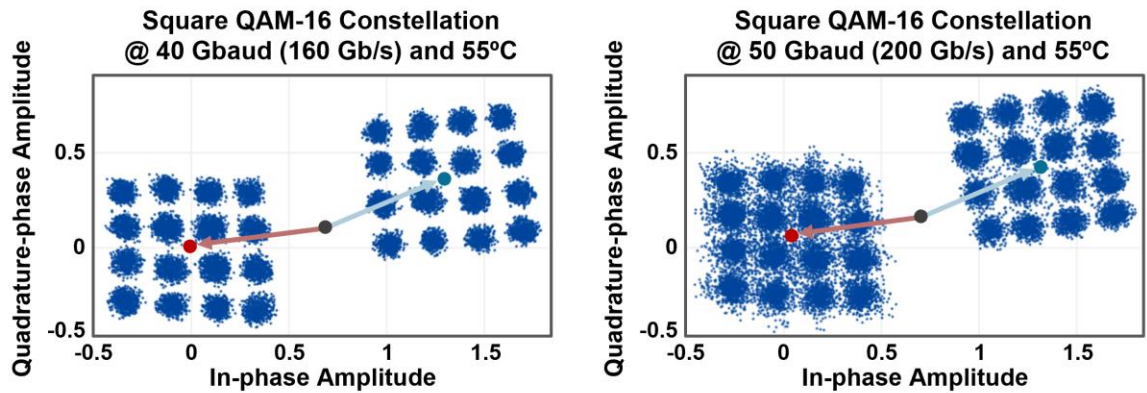
Figure 3.22: Measured square QAM-16 constellations at (a) 160 Gb/s and (b) 200 Gb/s.
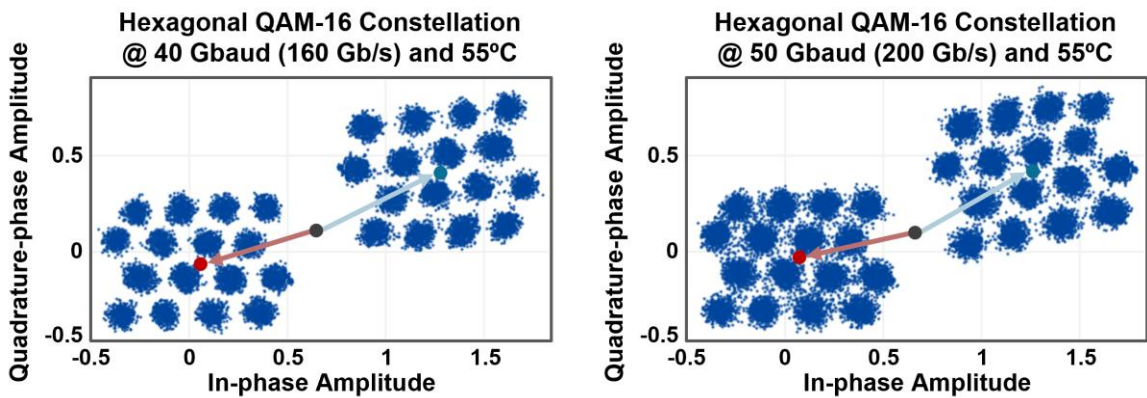
Figure 3.23: Measured hexagonal QAM-16 constellations at (a) 160 Gb/s and (b) 200 Gb/s.

For the hexagonal format, the optical power ratio into the 4th arm should be reduced to 1.73, and the relative phase shift of the 5th arm should be changed to 240º. These changes were implemented on the existing chip, which was optimized for the square format, using the thermal phase shifters and the driving voltage levels for arms 4 and 5. Fig. 3.23 show the measurements results for the hexagonal format at 40 Gbaud and 50 Gbaud, respectively. For all measurements shown in Fig. 3.22 and Fig. 3.23, the BER were measured at an OSNR of 35dB. As shown in the figures, the hexagonal settings show superior BER performance compared to their corresponding square versions.

3.3 Summary

In this chapter, a silicon photonic PAM-4 transmitter with two uneven-length SiGe EAMs in parallel within an unbalanced MZI structure is demonstrated. The fabricated chip performs PAM-4 transmission at 100 Gb/s with 5.5dB ER and 2.4dB of TDECQ. This scheme can similarly be applied to design 100 Gb/s PAM-4 Si-photonic transmitters in the O-band using hybrid-integrated InP-based EAMs with < 1pJ/bit power consumption as well to provide a path to 200 Gb/s/λ transmitters.

We also demonstrated a silicon photonic QAM-16 transmitter with 4 SiGe EAMs in parallel within an unbalanced MZI structure. The fabricated chip performs QAM-16 transmission at 200 Gb/s with 3×10^{-4} and 2.8×10^{4} of BER at an OSNR level of 35 dB for square and hexagonal constellations. This scheme can similarly be applied to design 200 Gb/s QAM-16 Si-photonic transmitters in the O-band using hybrid-integrated InP-based EAMs with < 1pJ/bit power consumption [13, 14] to provide a path to 400 Gb/s/λ transmitters.

Chapter 4

EIC DESIGN AND CO-OPTIMIZATION FOR OPTICAL TRANSMITTERS

4.1 Overview

Highly integrated Silicon Photonics (SiPh)-based solutions are growing as preeminent platforms for implementing low-cost and power-efficient 100+Gb/s/λ optical transceivers. Datacenters continue to require interconnects with more stringent bandwidth densities and energy efficiencies for inter- and intra-datacenter applications. Moreover, applications such as chip-to-chip interconnects in datacenter switches, high-performance field programmable gate arrays (FPGAs) and graphics processing units (GPUs) require small form-factors and substantial high volumes. SiPh transceivers co-packaged with CMOS electronics have the potential to meet these requirements. They can also support multi-level Pulse Amplitude Modulation (PAM-N) schemes with improved bandwidth densities. However, the inherent optical power penalty of PAM-N signaling imposes demanding linearity requirements on critical link components, which can lead to power hungry electronics. The modulator type should be carefully chosen and be co-optimized with the electrical driver to satisfy optical transmitter specifications such as optical modulation amplitude (OMA), extinction ratio (ER), signal-to-noise ratio (SNR) and electro-optical power penalties. The key characteristics of the respective SiP modulators are summarized in Table I and discussed as follows. Micro-ring modulators (MRMs) have small footprints and high electro-optical bandwidth (EOBW). However, they require relatively large voltage swings (usually > 1V) [1-8]. They also suffer from an inherent tradeoff between bandwidth and optical phase efficiency, high sensitivity to process and temperature variations, and non-linear electro-optic characteristics [9-11]. Depletion-based p-n junction phase modulators exhibit high intrinsic BWs. However, due to limited optical modulation efficiency ($V_\pi L$), they are used in Travelling-Wave Mach-Zehnder Modulators (TW-MZMs) topology, which require terminations and power-hungry drivers to compensate for microwave losses while occupying large areas on chip [12-21]. Electro-absorption modulators (EAMs) provide a balance between their intrinsic BW and

Table 4.1: Characteristics of optical modulation devices in SiPh circuits.

Ref.	[1] JLT'20	[9] PTL'18	[12] ISSCC'20	[54] JLT'18	[26] JLT'20	[70] IPC'2021	[67] Optica'20	[37] Nat.Photon'17	This Work
Mechanism	Carrier depletion	Carrier depletion	Carrier depletion	Carrier injection	Electro-absorption	Electro-absorption	Carrier Accumulation	Carrier Depletion	Carrier Accumulation
Modulator Type	p-n	p-n	p-n	p-i-n	SiGe EAM	SiGe EAM	Si MOSCAP	III-V/Si MOSCAP	Si MOSCAP
Structure	MRM	MRM	TW-MZM	SE-MZM	MZI	MZI	TW-MZM	Lumped-MZM	Lumped-MZM
Band	O	C	O	C	C	C	C	C	C
Speed of Operation	112 Gb/s PAM4	56 Gb/s OOK	53 Gb/s PAM4	56 Gb/s PAM4	106 Gb/s PAM4	100 Gb/s PAM4	100 Gb/s OOK	32 Gb/s OOK	100 Gb/s PAM4
Modulator Length	~ 628 µm	N/A	6 mm	750 µm	~ 200 µm	40µm / 66 µm	2.47 mm	750 µm	170 µm / 450 µm
ER	2.5 dB	4 dB	6 dB	4.7 dB	4.5 dB	5.5 dB	~ 3 dB	3.1 dB	4.3 dB
IL	6.5 dB	~ 6dB	3 dB/mm	~ 1.8 dB	6 dB	~ 9 dB	6.9 dB	1 dB	2.8 dB
Modulation Efficiency	30 pm/V	40 pm/V	N/A (3.6 V_{ppd})	$V_\pi L$ = 0.19 V.cm	-	-	$V_\pi L$ = 1.5 V.cm	$V_\pi L$ = 0.09 V.cm	$V_\pi L$ = 0.8 V.cm

optical efficiency (absorption coefficient). They, however, suffer from higher insertion losses, chirp, and limited maximum input power because of saturation, which should be addressed when used for higher-order modulation schemes [22-32]. Metal-oxide-silicon-capacitor (MOSCAP)-based (or the semiconductor-insulator-semiconductor capacitor (SISCAP), as reported in [33-36]) phase modulators operate based on carrier accumulation. These modulators can significantly scale the area and power of optical transmitter (OTX) due to their superior optical modulation efficiency ($V_\pi L$ < 1 V.cm) and compact footprint (< 1mm) [37-41]. MOSCAP modulators, however, could potentially suffer from excessive insertion losses due to high absorption, scattering from surface, sidewall roughness, and crystalline grains of commonly used polysilicon [42]. Moreover, these modulators impose large capacitive parasitics (~3 fF/µm), which could limit the EOBW significantly. Existing wireline drivers cannot meet the requirements of the MOSCAP modulators due to their limited output voltage swings, and their 50Ω termination design [43]. As it will be explained in Section II, a 50Ω terminated design would significantly limit the driver's BW when driving highly-capacitive MOSCAP modulators. Therefore, it is crucial to take a co-design approach and to compensate for the BW limitations imposed by these large capacitors.

In this paper, a 3D-integrated 100Gb/s 4-level pulse-amplitude modulation (PAM-4) OTX with electronic pre-distortion (PD) and BW extension techniques for driving highly-capacitive MOSCAP modulators is presented. In particular, trade-offs between MOSCAP modulator parameters are carefully studied and used for the co-design of electronics and photonics for optimal EOBW, power consumption and optical efficiency.

This paper is organized as follows: In section II the proposed system-level architecture and its advantages are presented. Section III discusses the silicon-photonics IC (PIC) design, choice of the segmented MZM and its layout, as well as the MOSCAP modulator parasitics and BW analyses. The CMOS TX architecture with all its major building blocks and their interconnections are provided in detail in section IV. The experimental results of the dual-channel CMOS driver and its integration with the PIC are included in section V. Finally, section VI summarizes this paper with performance comparisons and conclusions.

4.2 System-Level Analysis

4.2.1 OTX EOBW and Power Optimization Overview

The proposed optical transmitter system is aimed to operate at the highest possible baud rates using the standard 28nm CMOS process, while the overall power consumption is minimized. A careful electro-optical co-optimization study should be conducted to optimize modulator lengths, hence, the overall EOBW and the electro-optical power consumption. The optimal EOBW is achieved when modulator parasitics are accurately modeled and the driver is designed with proper load matching. This optimization process and driver design also depends on the modulation scheme, hence, the number of modulators.

The OTX is intended to be scalable, to provide a compatible solution for higher-order modulation schemes. In this work, we focus on PAM4 scheme to demonstrate the performance and the potential of our approach. The choice of keeping the modulation complexity in the electrical domain [44, 45] or transferring it to the optical domain [46-48], is highly dependent on the type of modulators and the electronics power budget (Fig. 4.1). Design trade-offs of the proposed U-shaped MOSCAP modulators, and the segmented push-pull MZM will be discussed in detail in section III.
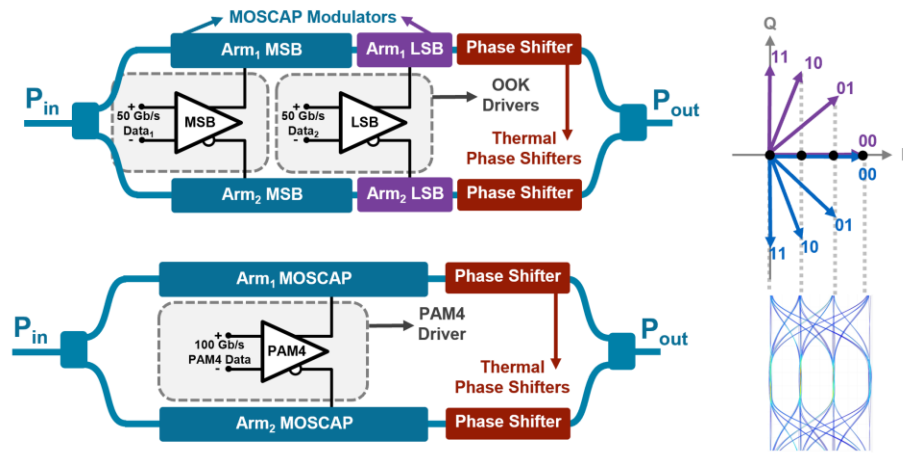
Fig. 4.1: Variations of an optical PAM4 transmitters
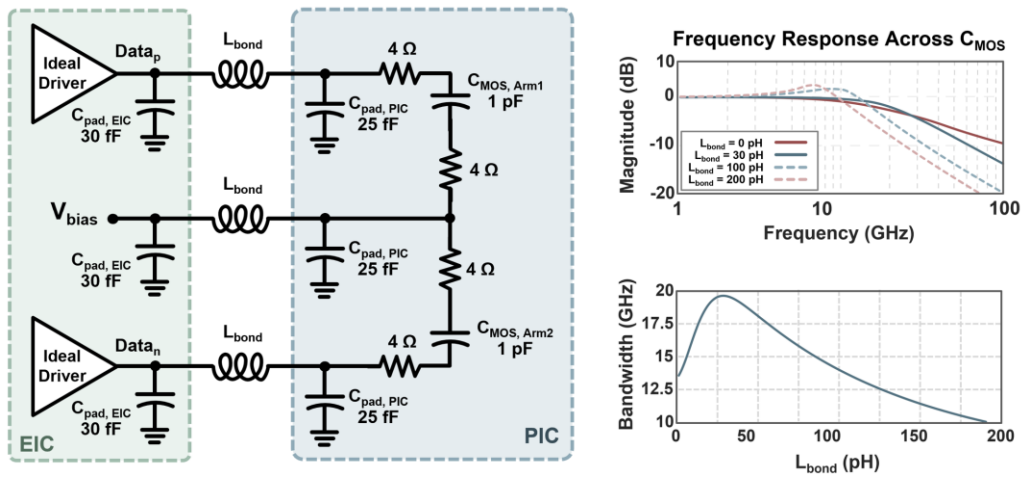
Fig. 4.2: Inductive parasitic effects of wire-bonds.
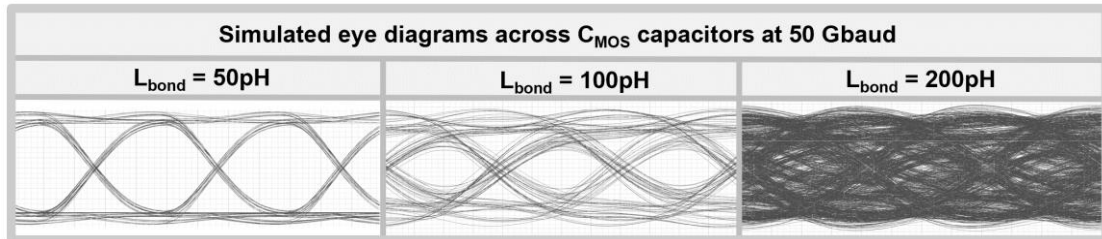
Fig. 4.3: NRZ eye diagrams across C_{MOS} with the presence of wire-bonds at 50 Gbaud.

The two on-off-keying (OOK) drivers shown in Fig. 4.1 need to drive 4 highly capacitive MOSCAP modulators (pairs of 415fF and 1.1pF capacitors). To achieve an EOBW of

35GHz, required for an error-free 50Gbaud transmission [49], the output impedances of the drivers need to be less than 5Ω and 11Ω, for the most-significant-bit (MSB) and the least-significant-bit (LSB) segments, respectively. However, even the ohmic resistance of the contacts from the PIC pads to MOSCAP junctions could be greater than these values (contact resistances are controlled by dopant densities optimized for modulators' optical efficiencies). To tackle this challenge, a combination of pre-distortion and inductive peaking are used for the core drivers to effectively extend the EOBW of all segments to 35GHz, when flip-chip bonded to the PIC.

Fig. 4.2 shows time-domain and frequency-domain simulations for a simplified network of the interface between MOSCAPs and the CMOS electronics IC (EIC) through wire-bonding. The equivalent inductance of shortest wire-bonds from EIC to PIC are approximated to be 300pH to 400pH for wire-bond lengths of 300μm to 400μm, which exceed the optimal value ($L_{bond} \approx 30$pH) for MOSCAP modulators. The closed eye diagram in Fig. 4.2 across CMOS, for a wire-bond length of 200μm, shows why the inductance of the practical wire-bond lengths would completely close the eye. These inductors perform series peaking for the driver, which could extend the BW by a factor of 1.41, only when the load capacitance (MOSCAP modulator) is more than 10 times the output capacitance of the driver (which is dominated by EIC output pad and driver output capacitances), and the inductor is approximately 10 times smaller than wire-bonding inductance values [50]. To solve this challenge, integration through flip-chip bonding was chosen to reduce L_{bond} to 50pH.

4.2.2 Transmitter System Architecture

A system-level block diagram of the OTX is shown in Fig. 4.4. It consists of PIC and a CMOS EIC flip-chip-bonded together using gold micro-pillars. The PIC consists of a segmented push-pull MZM with U-shaped MOSCAP phase modulators. Two thermal phase shifters are placed on each arm for relative optical phase adjustment to bias the MZM. Two grating couplers are used for optical I/O. The EIC includes two channels of 50Gb/s NRZ drivers with differential outputs, each receiving 2 sets of differential 25Gb/s independent data streams from an external arbitrary waveform-generator (AWG). A clock buffer path amplifies the external 25GHz clock signal to drive on-chip 2:1 serializers in each data path. A look-up-table (LUT)-based control unit receives digital signals from an external FPGA to configure drivers peaking strength, pre-distortion settings and the timing between the two drivers' data paths. As shown in Fig. 4.5, all electrical signals, including high-speed data and clocks, digital control signals, supplies and current references are fed to a printed circuit board (PCB), wire-bonded to the PIC, and routed to photonics components or the EIC pads. Analyses of these electrical paths at high-speed are provided in section IV. A Peltier heater is placed underneath the PCB that controls the temperature of the system and is controlled via and external supply.
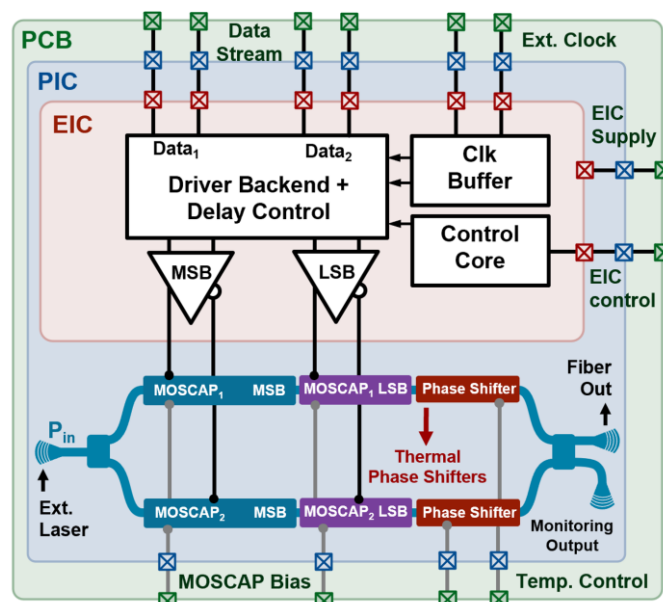
Fig. 4.4: Top-level PAM-4 OTX block diagram.
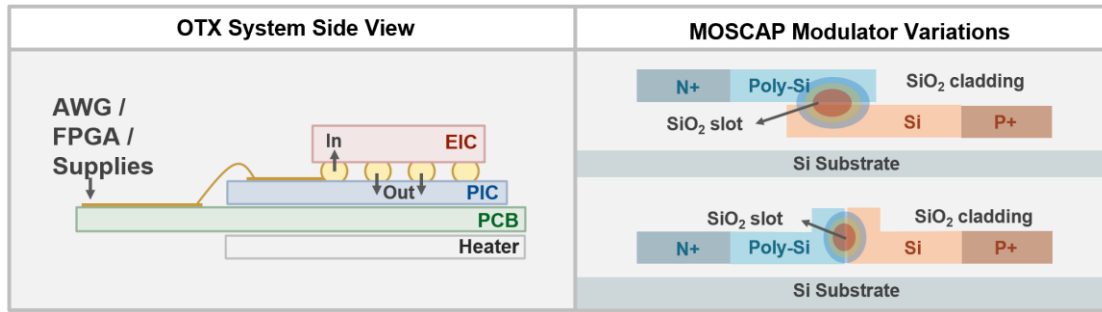
Fig. 4.5: Cross-section of the OTX system, and MOSCAP Modulator cross-sections, operating based on carrier accumulation.
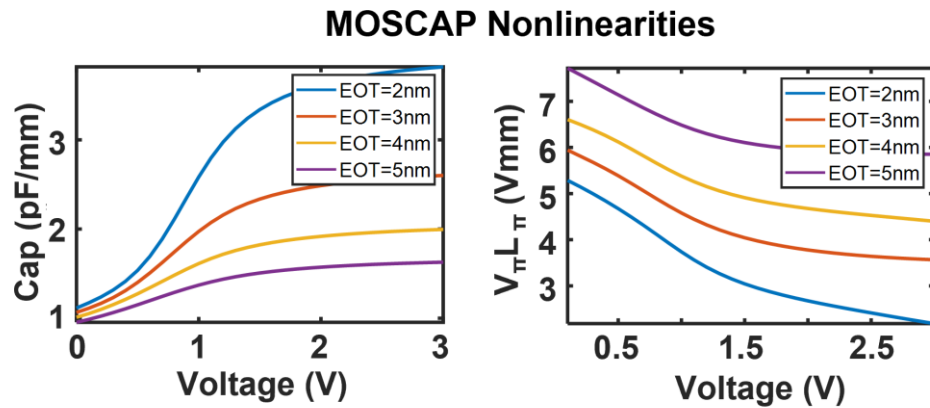
Fig. 4.6: Capacitance and $V_\pi L_\pi$ nonlinearities for MOSCAPs versus bias voltage for different oxide slot thicknesses (t_{ox}).

4.3 PIC Design

In this section we first study the structure of MOSCAP modulators and the trade-offs between all design parameters that impact the overall performance of the transmitter. The benefits of the segmented MZM over other architectures, as well as photonics layout considerations are reviewed next. A complete electrical parasitics network of the MOSCAP modulator is also provided, which was used as the actual load model to design the CMOS drivers.

4.3.1 MOSCAP Modulator Structure:

The MOSCAP phase modulators consist of an n-doped polysilicon, a thin layer of oxide (SiO_2 slot/gap), and a p-doped silicon region to form the metal-oxide-semiconductor

junction. This structure could be fabricated vertically (V-SISCAP) [33-37] or laterally (H-SISCAP) [38-41] to confine the light, as shown in Fig. 4.5. With proper doping of the poly-crystalline Silicon, this electrically active device can accumulate electrons and holes across the junction, when an electric field is present. The effective refractive index of the waveguide is therefore changed due to charge accumulation when the junction has proper overlap with the optical mode. This effect, known as the Plasma Dispersion, is mathematically described by the Drude-Lorentz model [51, 52] as:

$$\Delta n = -\frac{e^2 \lambda^2}{8\pi^2 c^2 \epsilon_0 n}\left(\frac{\Delta N_e}{m_e} + \frac{\Delta N_h}{m_h}\right) \tag{1}$$

where e is the charge of the electron, c is the speed of light, λ is the operating wavelength, n is the unperturbed refractive index, ε_0 is the vacuum permittivity, ΔN_e and ΔN_h are the free carrier concentrations of the electrons and holes, m_e and m_h are the electron and hole respective effective masses. MOSCAP modulators are compared with their 2 other phase modulator counterparts, which also benefit from the Plasma Dispersion effect. The carrier-injection-type modulators are commonly based on p-i-n junctions. These modulators suffer from limited bandwidth due to the slow diffusion of free electron in the doped region, despite having excellent modulation efficiency. In [53], a 50Gb/s p-i-n modulator using pre-emphasis signaling is reported. R-C equalization techniques can increase p-i-n modulator BW while reducing optical modulation efficiency [54-56]. Carrier depletion-based modulators are formed from reversed-bias p-n junctions and are commonly adopted in silicon photonics platforms due to their higher bandwidths. However, since the refractive index is changed due to the width of the depleted region, the $V_\pi L$ of such modulators are limited and longer segments are required (more than 1mm) to achieve reasonable ER [57]. Longer modulator segments need drivers with power-hungry terminations.

4.3.2 Modulator Design Parameters and Trade-offs:

MOSCAP modulators can be designed with excellent modulation efficiencies ($V_\pi L$ as low as 0.09 V.cm [37]). There is, however, an oxide slot thickness (t_{ox})-related trade-off between modulation efficiency $V_\pi L$, and the junction capacitance, which translates to the EOBW [38-41]. As t_{ox} is increased, the EOBW also increases, however, $V_\pi L$ degrades. Degradation of $V_\pi L$ can, however, be compensated by increasing the length or the modulation voltage levels.

An increase in the modulator length, or the voltage amplitude would directly affect the overall power consumption for a targeted optical transmitting signal (OMA and ER). Moreover, the doping of the contacts would reduce the access resistance to the junction, while degrading the optical insertion loss (IL), due to the presence of excessive free carrier charges overlapping the waveguide mode.

In addition to the above trade-offs, nonlinear effects of MOSCAP modulators under different bias voltages should be considered for optimization. The main nonlinear parameters are defined below [39, 58]:

$$L_\pi(V_b) = \frac{\lambda}{2\left[n_{eff}\left(V_b + \frac{V_s}{2}\right) - n_{eff}\left(V_b - \frac{V_s}{2}\right)\right]} \tag{2-a}$$

$$Q_\pi(V_b) = L_\pi(V_b) \int_{V_b - \frac{V_s}{2}}^{V_b + \frac{V_s}{2}} C(V)\,dV \tag{2-b}$$

$$C_\pi = Q_\pi/V_s \tag{2-c}$$

where $L_\pi(V_b)$ is the phase shifter's length for obtaining a π-shift at a given bias voltage V_b and voltage swing of V_s. The denominator of (2-a) inside the parentheses is the effective refraction index change of phase shifter's optical mode. $C(V)$ with units of (fF/μm) characterizes the capacitance of the phase shifter per unit length. $Q_\pi(V_b)$ evaluates the required charge variations in the MOS phase shifter structures at a length of $L_\pi(V_b)$ for a π phase change under a bias voltage V_b and voltage swing V_s. Fig. 4.6 shows simulation results for $C(V)$ and $V_\pi L_\pi(V)$ of the modulators with different oxide thicknesses. Increasing the forward-bias voltage of MOSCAPs decreases their $V_\pi L$, hence, improving the optical efficiency. However, this increase in the bias also increases the effective junction capacitance, C_{MOS}, hence, reducing the EOBW. This trade-off shows that an optimal bias point should be found, in which a proper EOBW and optical efficiency would result in the best optical eye quality, when driven by the CMOS drivers. Moreover, process variations could lead to changes in t_{ox}, which would result in changes in both $V_\pi L$ and EOBW. A high-speed measurement analysis is provided in section V to address these trade-offs and to guarantee a robust performance.

In addition to the above trade-offs, the optical time-of-flight along the MOSCAP modulator could potentially affect the overall EOBW [71]. The optical time-of-flight is defined as:

$$t_f = \frac{n_g L}{c} \tag{3}$$

Where n_g is the group index of the waveguide, L is the length of the lumped segment, and c is the speed of light. We first consider a sinusoid modulation with frequency of $f = 25$GHz, and its half period time of $t_h = 20$ ps, which is the one-bit time width of the 50 Gb/s data rate. In such a scenario, the time-of-flight t_f should be less than 20 ps to avoid the accumulated phase cancellation due to the interactions between the positive and negative parts of the sinusoid. This means that if $t_f = 2 \times t_h$, the phase will be completely cancelled and lead to a minimum EOBW at frequency f. A simulation model, shown in Fig. 4.7, which includes the optical phase response along the modulator segment, shows that this limitation will be minimal when $t_f < t_h/2$ (which is 10 ps for 50Gb/s baud rate).

Considering all these design trade-offs and targeted OTX specifications, a systematic approach was developed to optimize the modulator lengths, as shown in Fig. 4.8. In this design flow, a fixed total capacitance for the modulator and an initial t_{ox} is targeted. The total C_{MOS} capacitance is chosen based on the electronics driver BW capabilities to target a certain baud rate. The slot thickness t_{ox} is then chosen based on the modulator non-linear characteristics that would lead to reasonable $V_\pi L$ and a voltage bias window that the electronics can support. Based on the chosen C_{MOS} and t_{ox}, the corresponding modulator length, the $V_\pi L$, and the insertion loss of the modulator are calculated. If the resulting optical time of flight meets the operation speed target, the optimization is completed, and the drivers
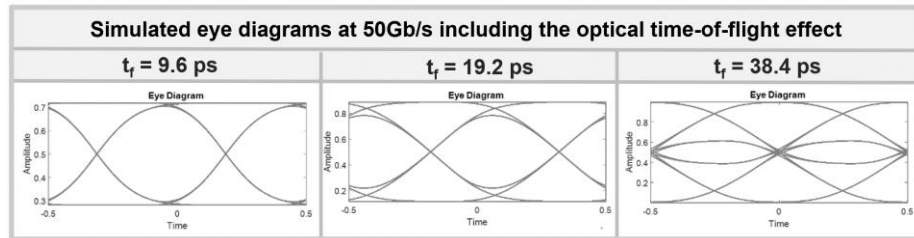
Fig. 4.7: Simulated eye diagrams at 50Gb/s including the optical time-of-flight effect ($t_f = 9.6$ ps, 19.2 ps, 38.4 ps) along MOSCAP waveguides.

could be designed accordingly. Otherwise, the modulator length should be decreased, and the calculations should be repeated until the optical time of flight target is met. To keep C_{MOS} constant, t_{ox} is also decreased in each iteration loop accordingly. When the optimal total length of the modulators is derived, then the MZM architecture and the electronics driver could be designed accordingly.

4.3.3   Modulator Length Optimization and MZM Design:

For the length optimization process of the fabricated MOSCAP modulator, nominal supply voltages of the 28nm CMOS process (0.9V) were used as the maximum allowable driving voltage to minimize the EIC power consumption. The optimization flow resulted in a total MOSCAP length of 620µm with total capacitance of 1.5pF, a t_{ox} of 4nm, and a $V_{\pi}L$ of 0.5 V.cm. This length, however, requires a TW electrode, since the maximum lumped electrode length could be estimated by $1/10^{th}$ of the wavelength corresponding to a microwave index of 2.1 for a 50GHz signal frequency, to approximately 300µm [14]. Moreover, to achieve an optical PAM4 signal, either an electrical PAM4 driver should be designed to drive this load,
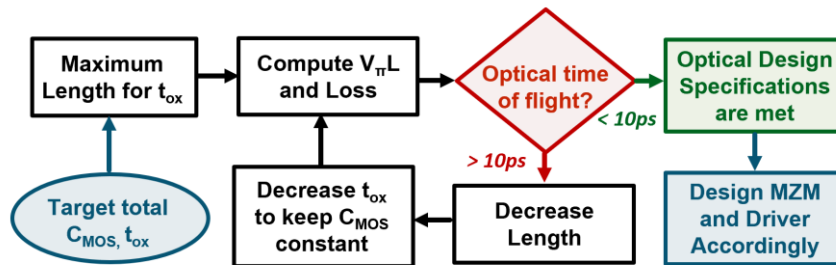
Fig. 4.8: Proposed MOSCAP modulator length optimization flow.

or the MZM can be segmented and be driven by OOK drivers (Fig. 4.1). The drawback of the former choice is that the electronics power consumption could potentially be increased, since a PAM4 driver with larger voltage swings should be designed to drive this huge capacitor. Moreover, the electrode lengths of a single segment would be approximately equal to, if not more than, 300µm, even after folding the modulator segment. Therefore, breaking the modulator into two binary-weighted segments provides a viable solution in this case.
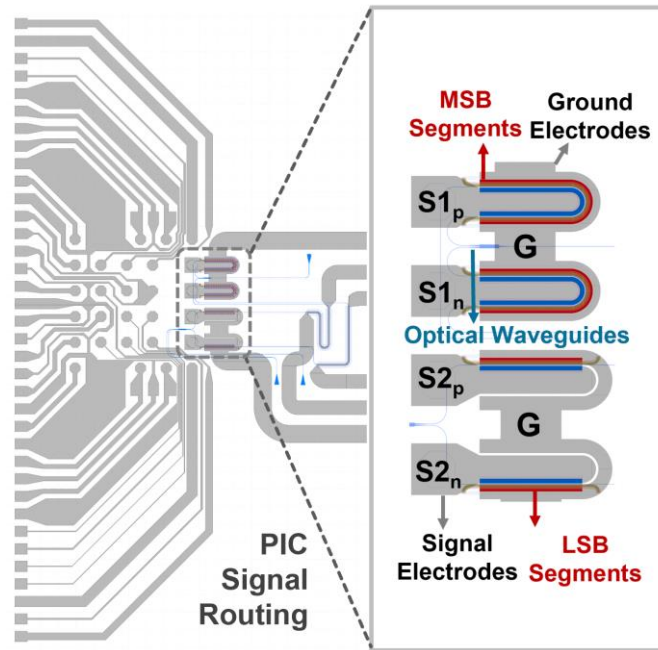
Fig. 4.9: PIC signal routing layout.

Parameter	Value
C_{air}	0.023 fF/µm
C_{metal}	0.002 fF/µm
C_{via}	0.004 fF/µm
C_{MOS}	1.5 fF/µm
C_{BOX}	0.19 fF/µm
C_{pad}	0.66 fF/µm
R_{vias}	<1 kΩµm
R_p	2 kΩµm
R_n	2 kΩµm
$R_{bonding}$	<1 kΩµm
R_{sub}	<1 kΩµm
L_{boding}	~ 1 pH/µm
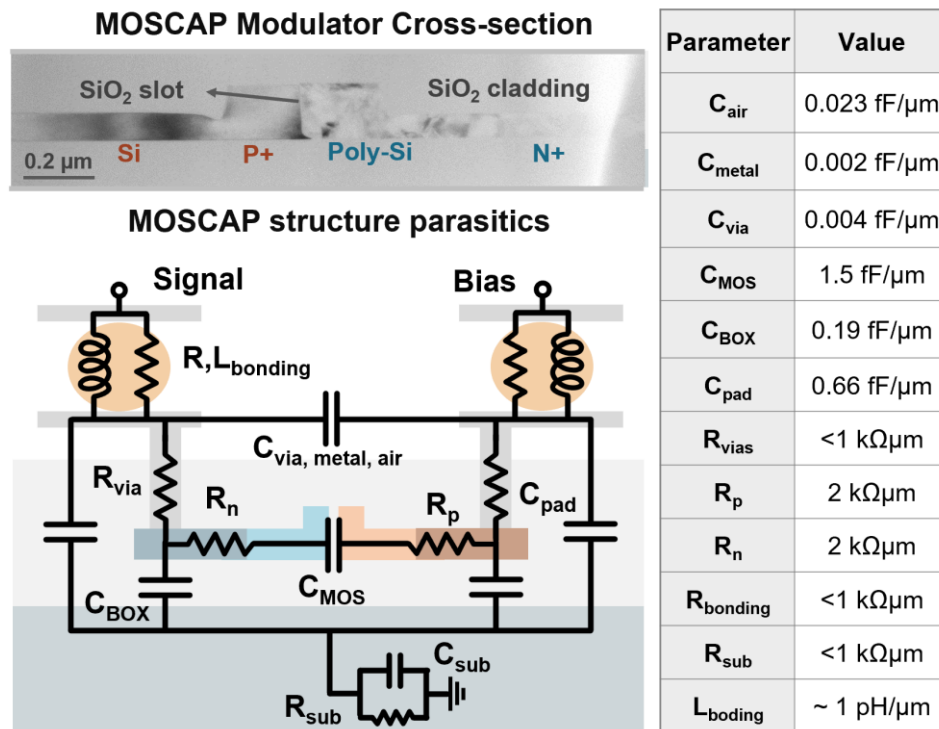
Fig. 4.10: MOSCAP modulator cross-section and electrical parasitics.

Considering the nonlinear MZM curve, the segments lengths were calculated to be 170µm

and 450µm with estimated parasitic capacitances of 415fF (LSB) and 1.1pF (MSB) to
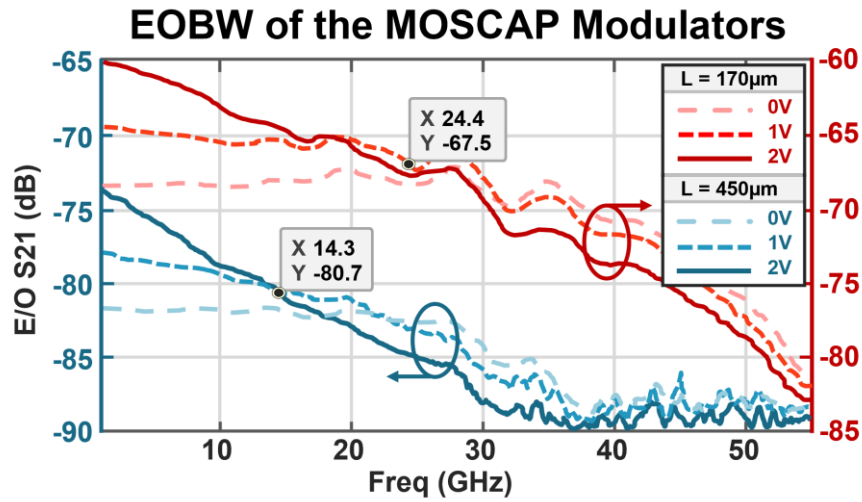
Fig. 4.11: Measured EOBW of 170µm and 450µm MOSCAP segments with 65GHz 50Ω-terminated probes.

generate equally spaced optical PAM4 levels. The layout of the modulators and signal routings on the PIC is shown in Fig. 4.9. MSB modulator segments are folded to form a U-shaped layout to effectively double the modulation efficiency with a fixed electrode length of 150µm and to avoid travelling-wave reflection effects.

4.3.4 MOSCAP Parasitics and nonlinearities:

 The actual cross-section image and the details of the parasitic structure of the vertical MOSCAP modulators are depicted in Fig. 410. These parasitics, in addition to the main junction capacitance (C_{MOS}) heavily affect the overall EOBW. As can be seen in Fig. 4.11, an EOBW measurement for 170µm and 450µm MOSCAP modulators, using a 65GHz 50-Ω terminated probe, shows 24.4GHz and 14.3GHz BW at 1V forward bias. This measurement was repeated for 5 more die samples and a f_{-3dB} variation of 5.5% centered at 23.7 GHz and 9% centered at 13.7 GHz were observed for the LSB and MSB segments, respectively. These measured BWs are significantly below the required BW for 50Gbaud modulation, which further highlights the necessity of a custom-designed CMOS driver to extend the EOBW to approximately 35GHz.
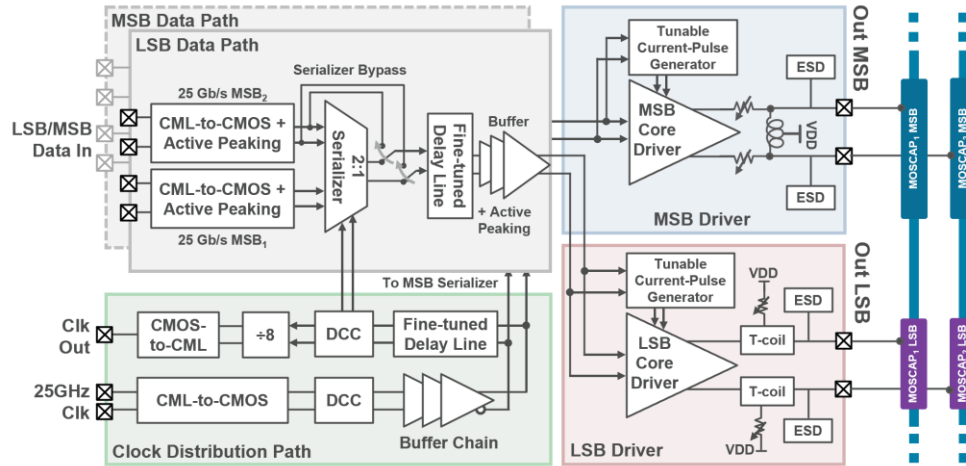
Fig. 4.12: Top-level block diagram of the 2-channel CMOS driver.
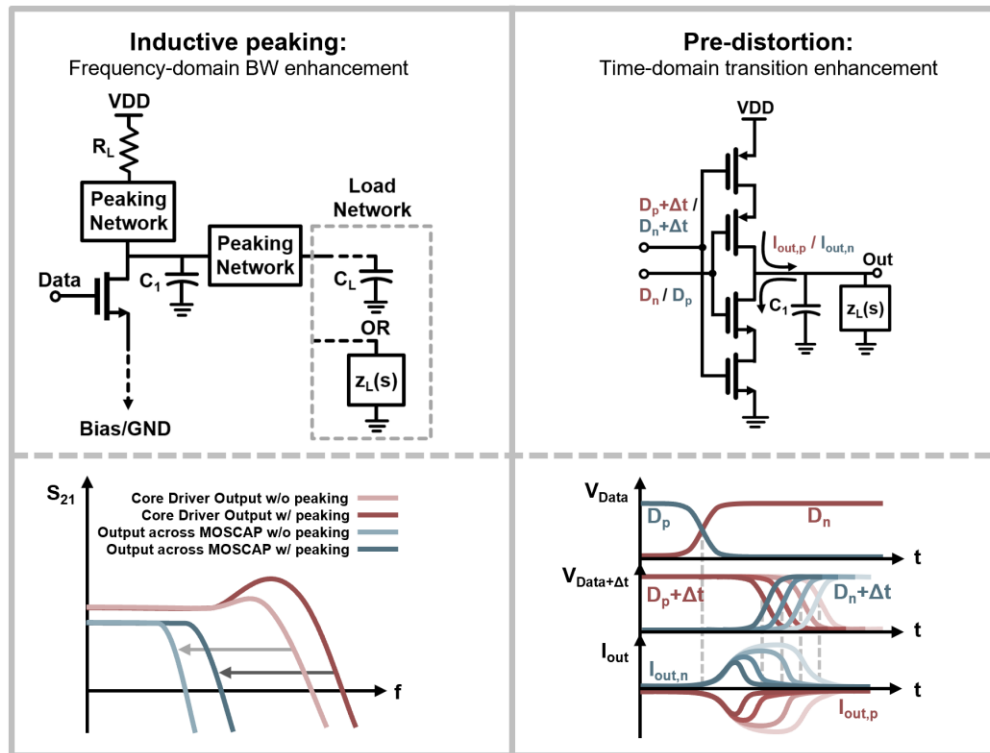
Fig. 4.13: Frequency-domain and time-domain enhancement technics used for core drivers.

4.4 EIC Design:

In this section, the top-level architecture of the dual-channel CMOS driver, followed by the details, analyses and simulation results of each block is presented.

4.4.1 EIC System Architecture:

The top-level block diagram of the EIC is provided in Fig. 4.12. Each driver channel receives two pairs of independent 25Gb/s differential data inputs, which are amplified and buffered through current-mode logic (CML)-to-CMOS stages. In the clock distribution path, a 25GHz differential input clock signal travelling from the AWG to the chip is buffered and adjusted for its duty cycle internally, before driving two 2:1 serializers. These serializers are used for each driver channel to combine the 25Gb/s data streams using the buffered 25GHz clock signal. An LUT-based delay control unit fine-tunes the relative clock delays between the serializers. Another delay adjustment unit is placed after the serializers to calibrate the 50Gb/s data delay between the driver slices. Differential active peaking is used along the data path buffers both at the back-end and the 50Gb/s buffering stage. The two 50Gb/s data streams are delivered to the last stage (core drivers). Each current-mode differential driver is BW-optimized for the corresponding MOSCAP segments with similar lengths on each MZM arm. A reconfigurable pre-distortion block generates current pulses with tunable widths at each data transition to further improve the drivers' effective BW. Details of the BW extension techniques and the driver core design are discussed next.

4.4.2 BW Extension Technics and Core Driver Design

Several circuit methods, using active/passive components have proven to effectively extend the BW of amplifiers [59-62]. The goal of BW extension in wireline applications, however, is to minimize the inter-symbol interference (ISI), hence, the data-dependent jitter (DDJ). Our approach to design the core amplifiers with sufficient BW, when connected to MOSCAP modulators, is to deploy both time and frequency domain approaches that reduce the DDJ and to combine these methods to minimize the overall power consumption.

Considering DDJ enhancement in the frequency domain, inductive peaking is an excellent method to extend the BW of wideband amplifiers, with minimal power penalty, when driving purely capacitive loads. However, the achieved BW extension ratios (BWERs) depend heavily on the ratio of the capacitance seen at the drain of the amplifying transistor, to the total capacitance that is to be driven (namely $k_c = C_1/(C_1+C_L)$ in Fig. 4.13) [50]. Series,

shunt, shunt-series, and bridged-shunt-series peaking technics can achieve BWERs in the range of 2.5 to 4, but only when $k_c > 0.3$. With asymmetric T-coil peaking, however, BWERs more than 4 is achievable for $k_c < 0.3$. It should be noted that the BWER is calculated assuming the circuit is operating in its linear region. However, this assumption does not hold true when amplifiers are driven with limiting input voltages. Therefore, the effective BWER will be smaller and might not be enough to achieve the targeted BW. Moreover, in the case of driving MOSCAPs using flip-chip bonding, the load is not purely capacitive as was shown in Fig. 4.10 (although, C_{MOS} is the dominant loading component). Additionally, the inductive peaking technics affect the group delay, which could hurt the DDJ, even when the BW is extended [50, 68, 69]. DDJ and ISI can be calculated directly from the frequency response and the group delay of the amplifier, assuming driver's linearity [68]. These calculations could be estimated criteria to choose a proper BW extension network.

DDJ can also be treated in the time domain by improving the step response of the driver [63]. DDJ occurs when the tails of prior bits perturb the data transition time, when it crosses the threshold level. If the data transition time of signal $s(t)$ with data period of T_b occurs at t_0 with the absence of prior bits, the total peak-to-peak jitter can be estimated from the slope of $s(t)$ at t_0 as [63]:

$$\Delta t_{pp} \cong \frac{1}{\left. \frac{ds(t)}{dt} \right|_{t=t_0}} \cdot \sum_{k=-\infty}^{-2} \left| p_o(t_0 - kT_b) \right| \tag{4}$$
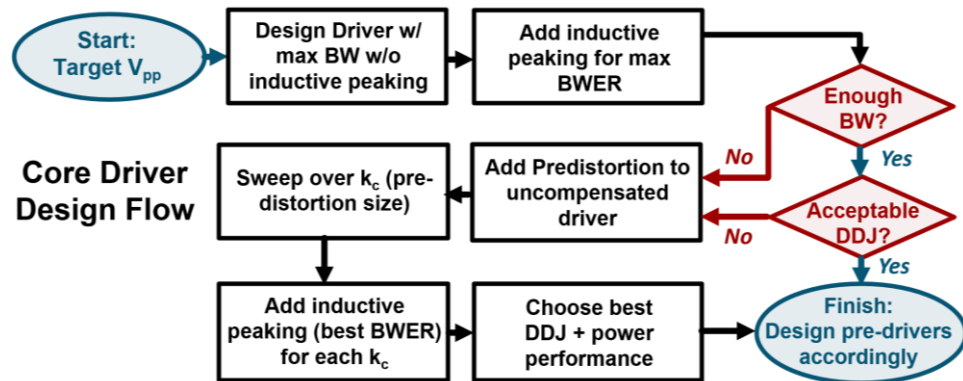
Fig. 4.14: Proposed core driver design flow for optimal BWER and minimized DDJ and power performance

Where $p_o(t)$ is the pulse response of the driver. It could be observed from equation (3) that one way of reducing the total DDJ is decreasing the contributions of prior bits perturbations (decreasing $p_o(t_0-kT_b)$). Improving the transition times by injecting a current pulse into the load, whenever a data transition occurs is one way to decrease the perturbations. This current pulse injection would shape the incoming pulse, hence, called pre-distortion. A controlled voltage-mode driver, shown in Fig. 4.15 can be used for this purpose. By applying the main data stream to the gates of the middle transistors and a delayed and inverted version of the same stream to the outer transistors, this branch can inject a current pulse into the output node. The amplitude of the current pulse can be tuned by sizing the transistors, while the width of the pulse can be tuned by the data delay. Although this method could effectively improve the overall DDJ, it comes with certain disadvantages. Using this circuit requires 2 extra buffering paths (4 in total for each driver slice) to deliver the 50Gb/s streams into the gates of the 4 transistors, and to generate an adjustable delay between the 2 paths. Having these extra buffers would burn more power. Additionally, when current pulses are injected to (or drawn from) the output, extra power from VDD is drawn. Moreover, since the output of this circuit is connected to the output of the main driver, the total capacitance seen at this node is increased, which should be considered for inductive peaking.

Considering the above trade-offs, we propose the following steps (also shown in the flowchart in Fig. 4.14) to determine the optimal BWER and overall minimized DDJ, while minimizing the power consumption:

a) Design a core driver with no peaking, but maximum BW for a targeted output voltage swing.

b) Determine C_1 and k_c: Add inductive peaking with maximum possible BWER and determine if the new BW and DDJ satisfy the performance.

c) If maximum available BWER meets the target BW but DDJ is large, reduce BWER (by tuning the BW extension network parameters, or by changing the network topology) to achieve the optimum DDJ.

d) If maximum available BWER was not enough, or if minimum achievable DDJ was large, then we start over with adding the pre-distortion block to the uncompensated
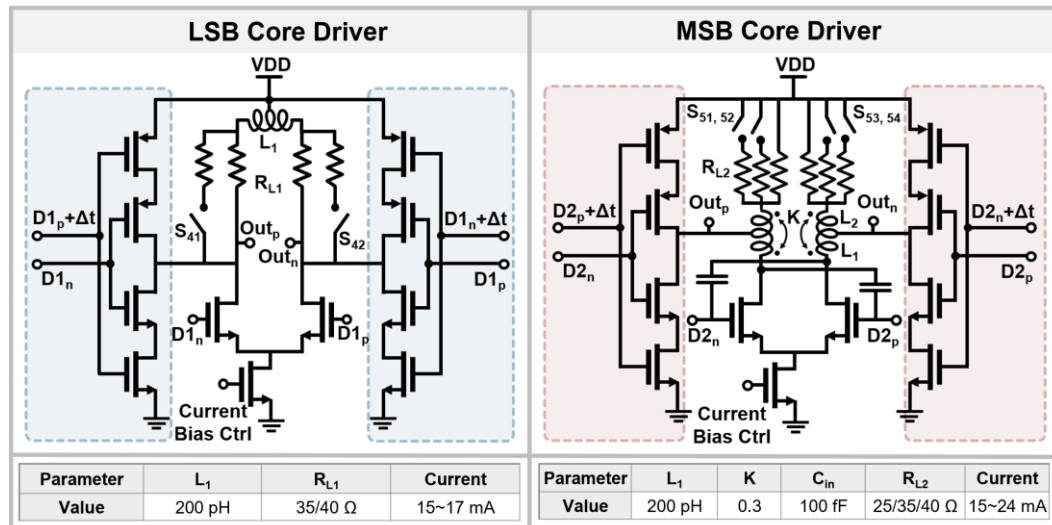
Fig. 4.15: Schematic of the MSB and LSB core drivers.

Parameter	L_1	R_{L1}	Current
Value	200 pH	35/40 Ω	15~17 mA

Parameter	L_1	K	C_{in}	R_{L2}	Current
Value	200 pH	0.3	100 fF	25/35/40 Ω	15~24 mA
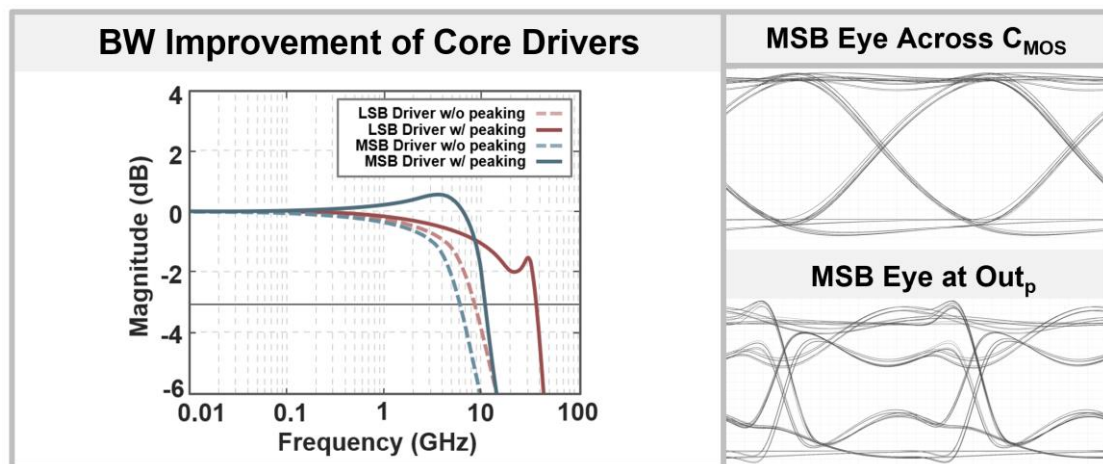
Fig. 4.16: Frequency response of the core drivers with and without inductive peaking.

driver (no peaking). The current pulse width should be kept approximately below half of the UI, to avoid ISI due to pre-distortion.

e) Increase the size of the pre-distortion blocks incrementally to improve the DDJ. Re-calculate the new k_c and choose a proper inductive peaking to extend the BW to the target value. Here, depending on the achievable k_c's, a combination of a stronger pre-distortion with a weaker peaking, or a weaker pre-distortion and a stronger peaking could result in similar overall BWs. However, there will be a compromise between power consumption and overall DDJ, since stronger peaking might perturb the group delay and could be not as helpful as a stronger pre-distortion.

Using the above approach, the LSB driver core was designed using a CML differential pair with differential T-coil peaking with digitally-reconfigurable load resistors, as shown in Fig. 4.15. The tunability for load resistors was included to compensate for MOSCAP bias calibration and PIC process variations (t_{ox}), which could both result in a change in EOBW. A pre-distortion block also helps with the overall DDJ improvement (the total DDJ is a result of both limited BW and the DDJ contribution of the inductive peaking network affecting the group delay [68]). The k_c for this block, when driving two 170µm MOSCAPs was estimated at 0.14. This amplifier drives each MOSCAP segment with a $0.6V_{pp}$ single-ended swing and consumes 55mW at 50Gbps, with the pre-distortion block contributing to 23% of the overall power consumption. The strong differential T-coils used here, delay the current flowing through the load resistor, and initially charge the drain capacitances and the output load, hence improving the BW. As a result of this current delay, the drain voltages of the amplifier experience large jumps during each transition. Two 100fF cross-coupled capacitors are placed at the input of the driver to further increase the input BW of the stage, by re-directing approximately 10% of the drain currents from the opposite outputs. The T-coil inductors were implemented using available designs in standard libraries with tunable parameters. To reduce the area consumption, a coupled differential T-coil could be custom-designed, similar to [64].

Following the proposed approach resulted in the design of the MSB driver, with more than 2 times larger pre-distortion and differential bridged-shunt peaking, also shown in Fig. 4.15. k_c of this stage is estimated at 0.38. The overall DDJ using a weaker pre-distortion and a stronger T-coil peaking would result in a worse DDJ due to distorted group delay, with $0.05 < k_c < 0.3$, although with a lower power consumption. Each output drives a 450µm MOSCAP segment with $0.6V_{pp}$ single-ended swing and consumes 98mW at 50Gb/s. The pre-distortion accounts for 38% of the total power for this stage.

The simulated normalized frequency responses of both core drivers with and without peaking are depicted in Fig. 4.16. These simulations include the parasitic capacitances of drivers' corresponding pre-distortion blocks. As evident from Fig. 4.16, the BWER of the MSB and LSB drivers are 1.8 and 2.8, with achieved BWs of 21GHz and 38GHz, respectively. Compared to the measured EOBWs using 50-Ω probes, that was shown in Fig.

4.11, the designed core drivers show 56% and 48% improvements in the overall EOBW for LSB and MSB segments, respectively. The lower BWER of the MSB driver is accompanied with a stronger pre-distortion, which results in an overall better DDJ performance. As seen in Fig. 4.16, the post-layout-simulated eye diagrams at the output of the driver stages are pre-distorted, while clean eye diagrams are applied across MOSCAP junctions (C_{MOS}), thanks to the combination of BW extension networks and the pre-distortion blocks.

4.4.3 Buffers and Current Pulse Generators (for Pre-distortion)

The schematics of the data stream buffers, the delay generators and the pre-distortion pulse width control are shown in Fig. 4.17. The multiplexed 50Gb/s differential data streams (serializer outputs) are first passed through buffers and current-starved inverter stages. Digitally controllable current-starved stages are used to fine-tune the relative delay between the differential data paths in each slice, as well as the phase difference between the two slices. These delay elements, shown in Fig. 4.17, labeled as S_{11} through S_{24}, generate fine-tuned delays in a window of 4ps with a resolution of 0.5ps. A delay calibration using these elements are performed during measurements, to equalize optical PAM4 eye openings. A non-zero delay between the data paths of the MSB and LSB slices will result in optical PAM4 eye closure, as shown in Fig. 4.18. Simulations for a relative delay of 5ps or -5ps between the MSB and LSB data paths, show ~20% and ~40% horizontal eye closure, respectively. In case of -5ps relative delay (when LSB leads MSB), the middle eye also experiences ~50% vertical closure, due to 01-to-10 transitions (or vice versa). These transitions experience momentary glitches to 00 and 11, respectively, which increases the settling time, hence increasing ISI for the middle eye.

At such high data rates, static inverter stages cannot guarantee complete settling within one UI even with low fanouts, hence, ISI and DDJ is increased. To address this challenge, differential active peaking circuits, which are highlighted in blue in Fig. 4.17 are implemented [65, 66]. The half-circuit of this active peaking block is shown in Fig. 4.19. Transistors M1 and M2, with their biasing feedback resistors, provide an output impedance with a peak at higher frequencies. When attached to the buffer outputs, the inverters provide

smaller gain with a higher BW, which effectively removes the ISI substantially, as depicted in Fig. 4.19. The feedback resistors are digitally tunable and can be switched off depending on performance requirements.

As shown in Fig. 4.17, the buffered and delay-tuned 50Gb/s data streams are passed through 4 separate buffering paths. The 2 main paths consist of fixed-sized buffers that deliver the data to both the driver core and the pre-distortion block (labeled as $D1_p$ and $D1_n$ in Fig. 4.17). The other 2 paths include a digitally controllable delay generator in addition to buffers, using bypassing inverter stages. As in Fig. 4.17, switches S_1 through S_3 control the number of inverters that data streams should pass through. Each extra inverter between these switches adds approximately 2ps of delay in the data path. Switches S_1 and S_3 add 2ps and 6ps of delay, respectively. Switch S_2 adds 4ps of delay, but also changes the polarity of the data, hence, connected to the opposite data path. The outputs (labeled as $D1_p+\Delta t$ and $D1_n+\Delta t$) are also sent to the pre-distortion block. The pre-distortion blocks generate current pulses with adjustable widths of 2ps, 4ps, or 6ps based on the chosen delay. Since these current pulses are generated based on a delay mismatch between the main path buffers and the pre-distortion buffers, the pulses will always occur at the beginning of each data transition and will never be misaligned with respect to the data path. The proper delay is chosen in measurements in an open loop manner to minimize the DDJ. This tunability further helps with compensating for MOSCAP bias calibration and PIC process variations (mainly t_{ox}).
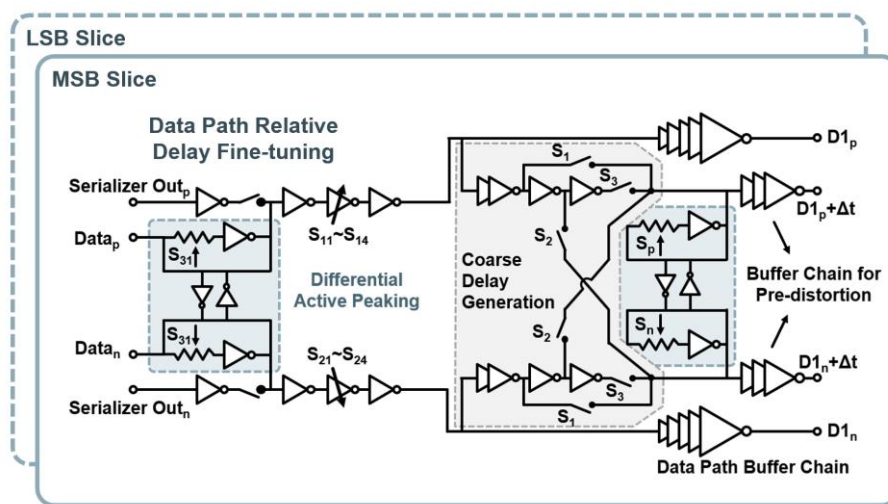
Fig. 4.17: Data-path buffers, tunable data delay generator, and current pulse width control.

Effects of MSB to LSB Delay on Optical Eye Diagrams

$$\Delta t_{total} = \Delta t_{MSB} - \Delta t_{LSB} = 0$$

$$\Delta t_{total} = 5 \text{ ps}$$

$$\Delta t_{total} = -5 \text{ ps}$$
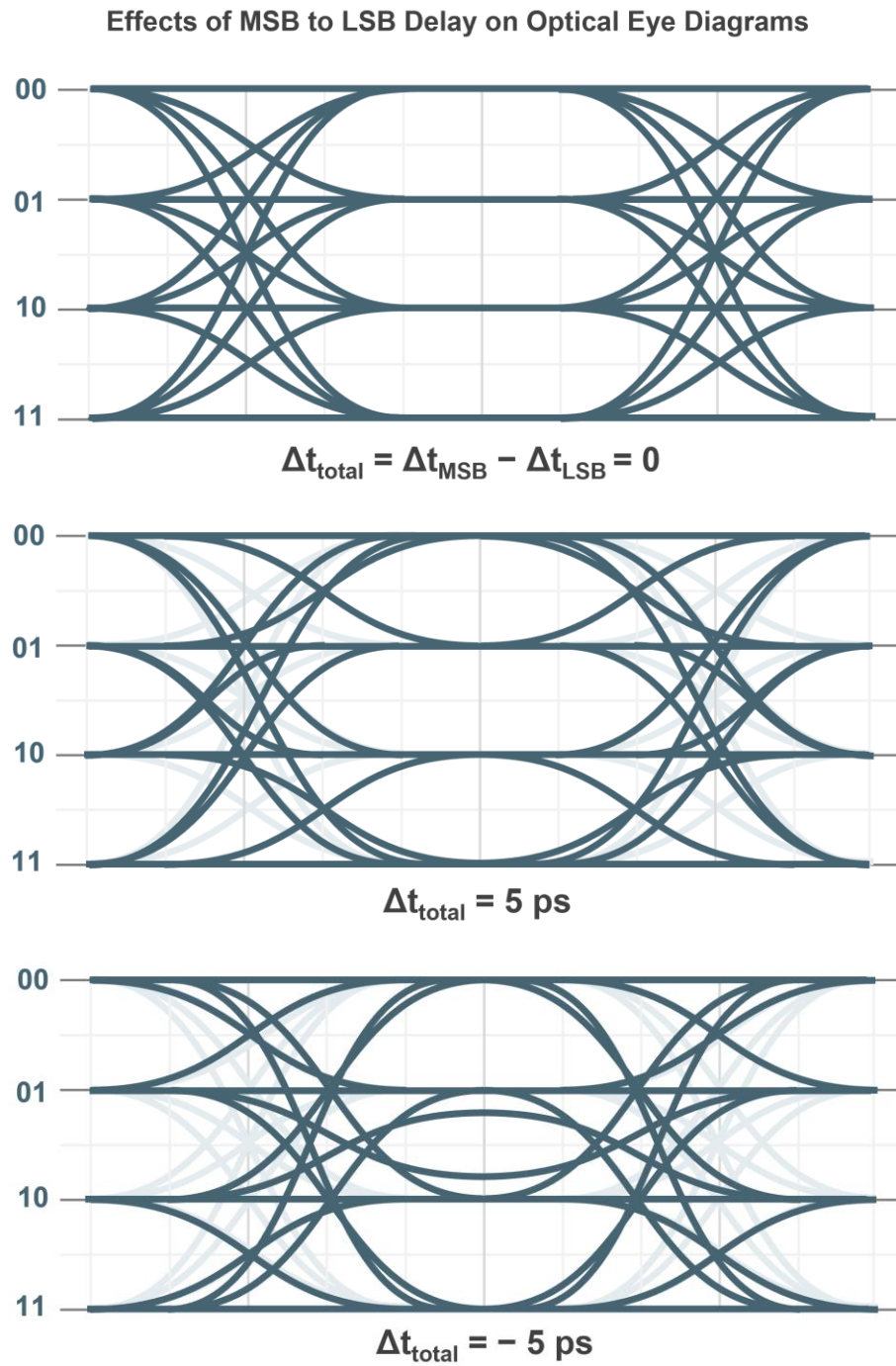
Fig. 4.18: (a) Data-path buffers, tunable data delay generator, and current pulse width control, (b) effects of MSB-to-LSB data path delay on optical eye diagrams, and (c) differential active peaking output impedance.

Differential Active Peaking
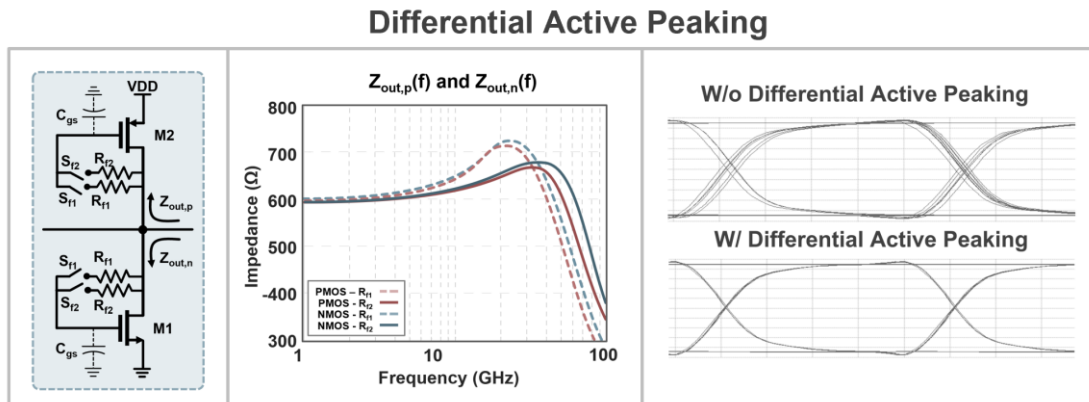
Fig. 4.19: Differential active peaking output impedance.
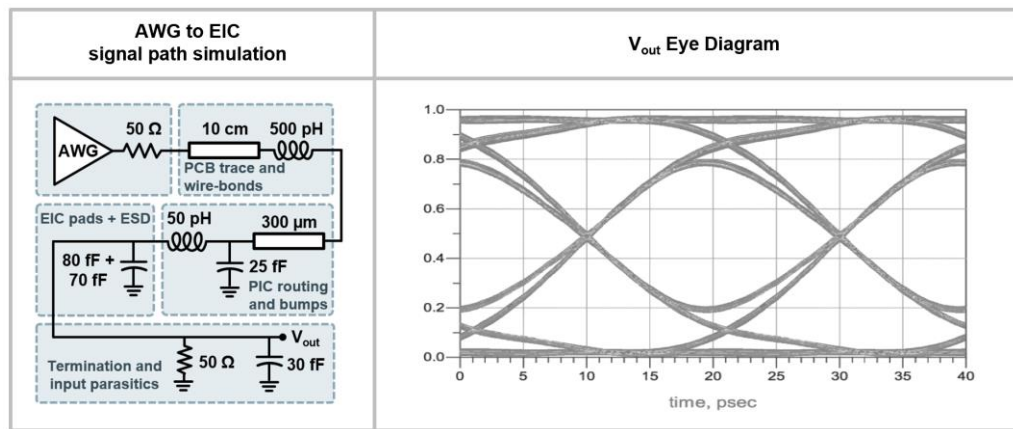
Fig. 4.20: AWG to EIC signal path simulation for data and clock signals.
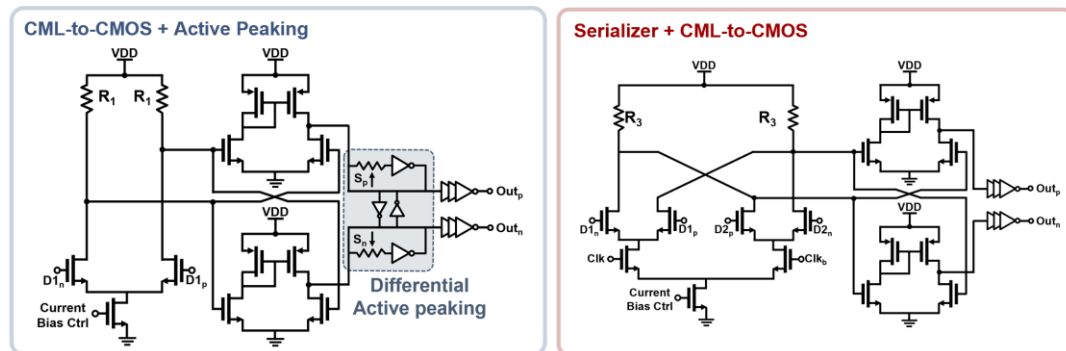
Fig. 4.21: EIC back-end, 2:1 serializer, clock buffer, DCC and bias control circuitry.

4.4.4 EIC Backend

All 25Gb/s data streams and the 25GHz clock signal are generated by an AWG and fed to the EIC through high-speed PCB traces and signal routings on the PIC. Fig. 4.20 shows the
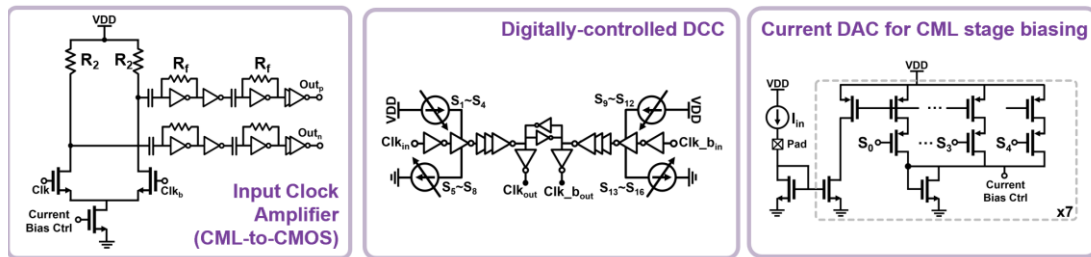
Fig. 4.22: Clock buffer, DCC and bias control circuitry.

signal path simulation results including all parasitics from AWG to the first amplifier stage inside the EIC. At the driver back-end, a CML-to-CMOS stage with differential active peaking, shown in Fig. 4.21, is used to amplify the incoming data streams at each data input. The external 25GHz clock is amplified by a CML-to-CMOS stage and then passed through AC-coupled inverter-based TIA stages and buffers, also shown in Fig. 4.21. The clock duty cycle is adjusted by a duty-cycle-correction (DCC) block, which uses controlled DC current injection to adjust the transition times. The two 25Gb/s data streams and the 25GHz clock are then delivered to the 2:1 serializer. The serializer is a differential mixer followed by a CML-to-CMOS stage to generate rail-to-rail 50Gb/s streams. Separate digital-to-analog converters (current DACs, shown in Fig. 4.22) are used to bias CML stages across all blocks in the back-end and core drivers. During the measurement process, all current DACs are initially configured at their highest bias setting (11111 for control bits S_0 through S_4, as shown in Fig. 4.22) to achieve maximum swing. The control bits are decreased gradually after achieving clean PAM4 eye diagrams, to further reduce the power consumption, while the eye quality remains unchanged. Fig. 4.23 shows post-layout simulations for process and temperature variation effects on the 25GHz duty cycle, using the highest and lowest control bit configurations (1111 and 0000, respectively, for control signals S_1 through S_4, shown in Fig. 4.22). The shaded areas in Fig. 4.23 show the duty cycle ranges covered by the DCC at each process corner. The overlap of the shaded areas show that a 50% duty cycle will be achievable across all process corners at temperatures between 30ºC and 90ºC. The timing between the 25Gb/s data paths and the 25GHz clock signal was tuned externally through the AWG, which generates these signals. This external tunability ensures the internal serializers generate 50Gb/s streams with no glitches.

4.5 Experimental Results

The TX EIC was fabricated in 28nm CMOS process with an active area of ~0.2mm², which measures 830µm by 750µm. The segmented push-pull MZM is implemented on the PIC with an overall footprint of ~1mm². The measurement setup is shown in Fig. 4.24. All control signals, voltage supplies (0.9V) and the current reference were delivered to a test PCB, on which the 3D integrated OTX was mounted. An external arbitrary waveform generator (AWG) provides 25Gb/s PRBS-31 data streams and a 25GHz clock signal to the EIC and a trigger signal for an optical sampling scope (OSS). The modulated optical output is fiber coupled to the OSS receiver for eye diagram recording and TX dispersion eye closure (quaternary) (TDEC and TDECQ) measurements. An external laser source inputs 10dBm optical power at 1550nm to the PIC via a grating coupler. An erbium-doped fiber amplifier (EDFA) is placed after OTX to amplify the optical signals by 11dB before passing them to the OSS. An optical filter was placed before the EDFA to control the optical output levels of the chip and prevent saturating the EDFA. Another optical filter was placed after the EDFA to ensure no out-of-band components generated by EDFA non-linearities enter the sampling oscilloscope.

Considering a trade-off between the optical efficiency and the EOBW of the MOSCAP
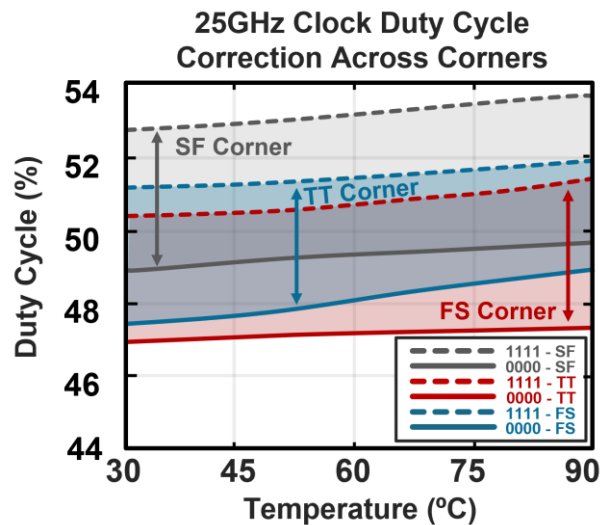
Fig. 4.23: Simulated process and temperature variations for the DCC block at bit configurations of 0000 and 1111.
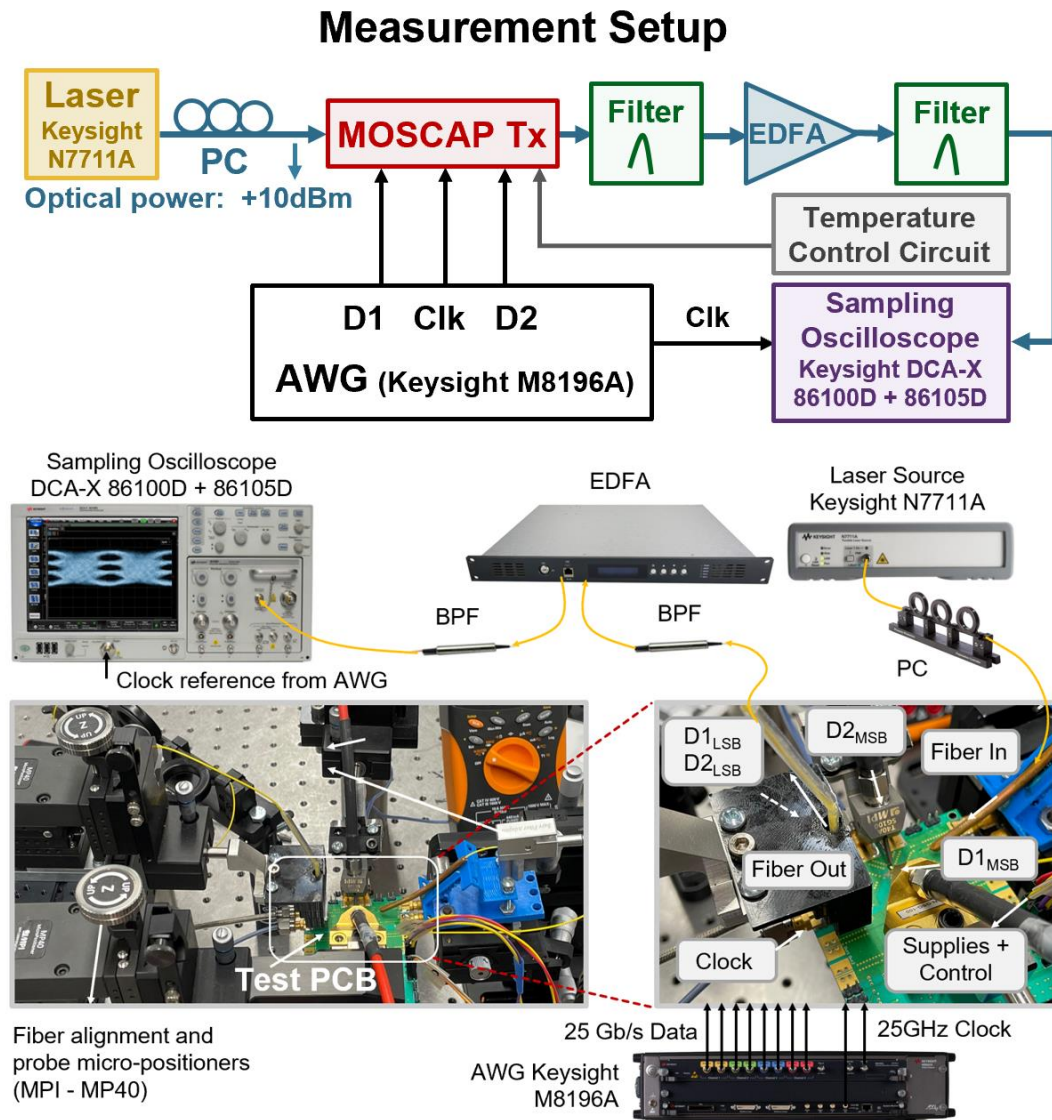
Fig. 4.24: PAM-4 OTX measurement setup.

modulators when their bias voltage is increased, all segments bias voltages were scanned and calibrated in an open loop manner, to optimize the resulting TDECQ. A forward bias at 1V exhibited an optimal performance for the sample under test. The optimum bias voltage would change due to process variations that could lead to changes in the effective t_{ox} and the overall EOBW of the modulators. However, the OTX shows steady performance with no real-time re-calibration needed. The PIC exhibits an overall 6.2dB of optical insertion loss, including the 3dB quadrature point loss. The t_{ox} of MOSCAP modulators in the fabricated PIC under

50Gbps Optical NRZ Eyes w/ and w/o Predistortion and Peaking @ 30°C	100Gbps Optical PAM4 Eyes w/ and w/o Predistortion and Peaking @ 30°C	100Gbps PAM4 Eyes (Post-TDECQ) @ Extreme Temperature and MOSCAP Bias Ranges	100Gbps PAM4 Eyes (Post-TDECQ) w/ MSB-to-LSB Relative Delays
(a)	(d)	(g)	(j)
Raw eye w/o PD: OMA: 1.3 dBm, ER: 4 dB	Raw eye w/o PD: OMA: 1.3 dBm, ER: 4.1 dB	Bias: 1V (Optimum), Temperature: 90°C OMA: -0.2 dBm, ER: 3.9 dB, TDECQ: 2. 31 dB	Bias: 1V, Temperature: 30°C, +4ps delay OMA: -0.2 dBm, ER: 4 dB, TDECQ: 2.42 dB
(b)	(e)	(h)	(k)
Raw eye w/ PD: OMA: 1.2 dBm, ER: 4.3 dB	Raw eye w/ PD: OMA: 1.4 dBm, ER: 4.3 dB	Bias: 2V , Temperature: 30°C OMA: -0.3 dBm, ER: 3.7 dB, TDECQ: 2.97 dB	Bias: 1V, Temperature: 30°C, -4ps delay OMA: -0.2 dBm, ER: 4 dB, TDECQ: 3.9 dB
(c)	(f)	(i)	(l)
TDEC 5-tap FFE filter with reference BER of 5e-5 w/ PD: OMA: 0.1 dBm, ER: 4.1 dB TDEC: 0.76dB	TDECQ filter: 5-tap FFE (IEEE802.3bs compliant) w/ PD: OMA: -0.2 dBm, ER: 4 dB TDECQ: 1.53 dB	Bias: 0.25V , Temperature: 30°C OMA: -0.8 dBm, ER: 4 dB, TDECQ: 4 dB	0.25V Bias, Temperature: 90°C, -4ps delay OMA: -1.2 dBm, ER: 3.2 dB, TDECQ: 4.7 dB

Fig. 4.25: Measured 50Gb/s NRZ and 100 Gb/s PAM4 eye diagrams before and after on-chip BW extension.

test were measured at 5.5nm, which showed an increase of 1.5nm from the design, due to process non-uniformity (2nm < t_{ox} < 6nm across wafer). This change in t_{ox} also resulted in an increase in the measured $V_\pi L$ to 0.8 V.cm. The EIC-PIC interface parasitics were estimated as was summarized in Fig. 4.10.

The measured 50Gb/s NRZ and 100Gb/s PAM-4 optical eye diagrams are shown in Fig. 4.25. Fig. 4.25(a, d) show the eye diagrams when minimum peaking and minimum pre-distortion settings are applied. Fig. 4.25(b, e) show the measured raw eye diagrams using the optimal BW extension settings for the drivers. The measured OMA (including coupling and on-chip insertion losses as well as the EDFA gain) was 1.4dBm. Both eye diagrams were filtered by IEEE 802.3bs compliant 5-tap equalizers, shown Fig. 4.25 (c, f), exhibiting a TDEC of 0.76dB and TDECQ of 1.53dB.

Further eye measurements for extreme temperatures and MOSCAP bias voltages are shown in Fig. 4.25 (g-i). At 90°C, TDECQ is degraded to 2.31dB. Increasing the bias from the optimal value of 1V to 2V has resulted in more optical efficiency, but lower EOBW. As a result, the OMA has remained unchanged, while TDECQ is degraded to 2.97dB. Also, when the bias is decreased to 0.25, eyes are widened thanks to higher EOBW, while vertical closure has resulted in a degraded TDECQ of 4dB.

The last column of Fig. 4.25 shows eye measurements when there is a relative delay between MSB and LSB data paths. Fig. 4.25 (j) shows outer eyes horizontal closure due to a
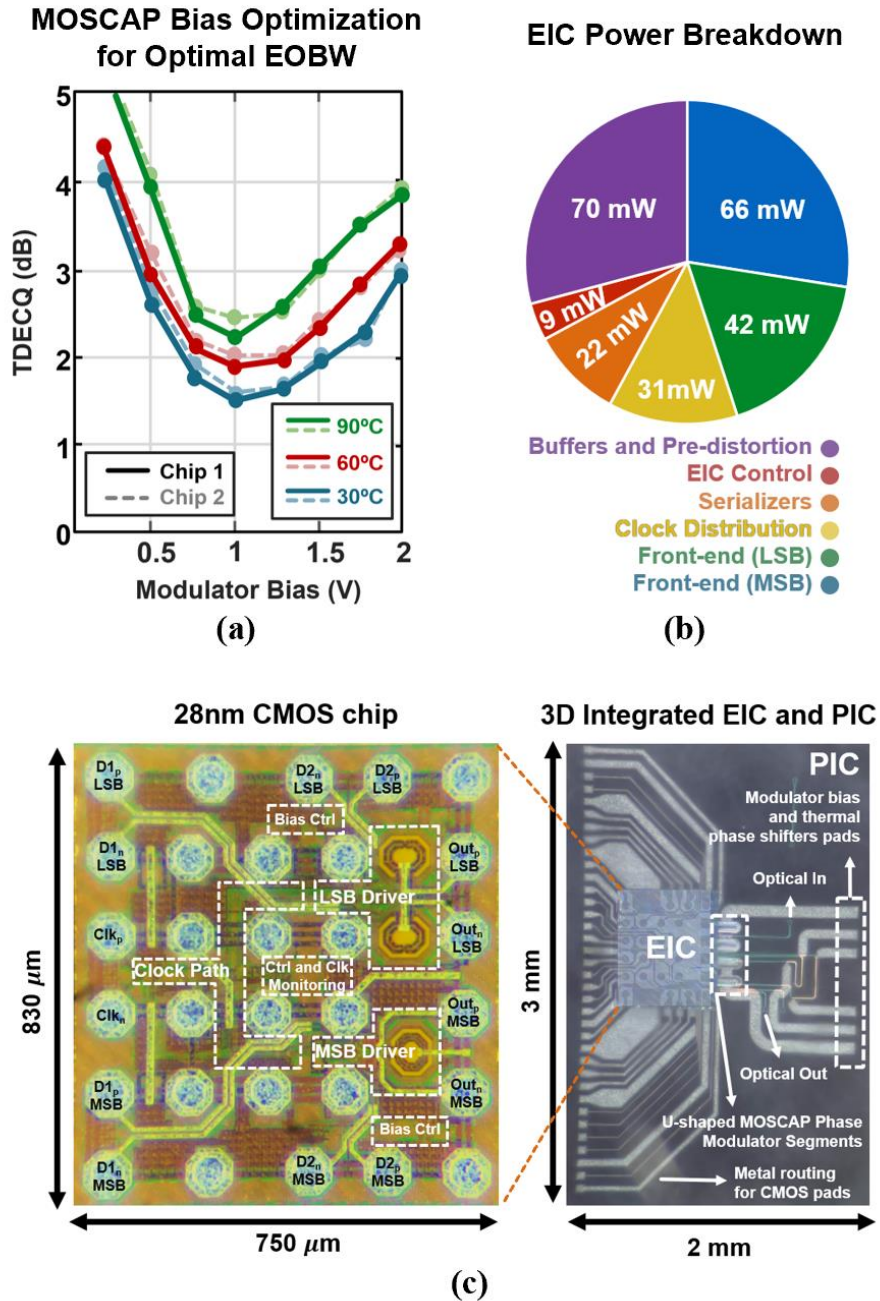
Fig. 4.26: (a) TDECQ values for 100Gbps PAM4 eye diagrams for different MOSCAP bias voltages and temperatures, (b) EIC power breakdown, and (c) die photos of the 28nm CMOS chip and 3D integration with PIC

4ps delay, which has affected the TDECQ negatively. Generating -4ps of delay degrades the TDECQ even more, since being dominated by the middle eye horizontal and vertical closure,

as shown in Fig. 4.25 (k). Finally, Fig. 4.25 (l) shows the measured eye when all extremes occur at the same time, operating at 90 ℃, -4ps of relative delay, and 0.25V of bias.

The plot in Fig. 4.26 (a) shows TDECQ values versus MOSCAP forward bias voltage for different temperatures, measured for 2 samples. The Peltier heater consumed 260mW to increase the temperature from 30 ℃ to 90 ℃. As described in section III-b, increasing the bias improves the optical efficiency while degrading the inherent BW of the MOSCAP due to the enlarged C_{MOS}. An optimal bias point is found at 1V for both chips, that minimizes the TDECQ. The OTX exhibits 53% degradation in TDECQ performance (and 56% degradation for the second sample) when biased at 1V for temperature ranges from 30 ℃ to 90 ℃. The timing settings for each new temperature were re-adjusted for optimal performance. The clock duty cycle and the relative delay between the 50Gb/s data paths were changed by approximately 5% and 0.5ps, respectively with every 30℃ increase in temperature. A closed-loop controller with an integrated temperature sensor can be used to perform this calibration in real-time.

The power breakdown of the EIC is provided in Fig. 4.26(b). The CMOS chip dissipates 240mW at 100Gb/s PAM4 (including the clock distribution, serializers and core drivers) to deliver 4dB total ER at 1.53dB TDECQ. Die images of the EIC and its 3D integration with PIC, are shown in Fig. 4.26 (c).

4.6 Summary

In this chapter, a 3D-integrated 100Gb/s PAM-4 OTX was presented. Electronic pre-distortion and BW extension techniques were implemented to compensate for MOSCAP modulator BW limitations. Trade-offs of MOSCAP modulator parameters were studied and used for co-designing the electro-optical interface for optimal EOBW, power consumption and optical efficiency. Table II shows the overall performance of the OTX in comparison with the prior art. The proposed TX achieves 2.5× better EIC energy efficiency, compared to the state-of-the-art co-integrated optical PAM4 transmitters operating at or above 100Gb/s. This efficiency was achieved by keeping the output swing of the driver below $1.2V_{ppd}$ while delivering optimal optical performance. A figure of merit that normalizes the energy efficiency to the optical power efficiency, shown below in (5) and in Table 4.2, also depicts

Table 4.2: Performance Summary and Comparison

Comparison Table	[1] JLT'20	[2] JSSC'21	[12] ISSCC'20	[26] JLT'20	[54] JLT'18	[46] BCICTS'18	[57] JSSC'22	[9] PTL'18	[18] JLT'18	[67] Optica'20	This Work	
Technology	28nm CMOS	28nm CMOS	55nm BiCMOS	55nm BiCMOS	28nm CMOS	16 nm FinFET	40nm CMOS	28nm FD-SOI	28nm FD-SOI	28nm CMOS	28nm CMOS	
Integration	Wire-bond	3D	3D	Wire-bond	3D	3D	Wire-bond	Wire-bond	3D	3D	3D	
Modulation Device	MRM	MRM	TW-MZM (6mm)	Dual SiGe EAM	SE-MZM (PIN)	SSE-MZM	SE-MZM	MRM	TW-MZM	TW-MZM	Lumped-MZM (620μm)	
Operating Wavelength	1310 nm	1310 nm	1310 nm	1565 nm	1550 nm	1490 nm	1550 nm	1550 nm	1550 nm	1550 nm	1550 nm	
Output Voltage Swing	3 V_{ppd}	3 V_{pp}	3.6 V_{ppd}	2 V_{pp}	1 V_{pp}	1.8 V_{pp}	4 V_{pp}	1 V_{pp}	5 V_{pp}	2.8 V_{pp}	1.2 V_{ppd}	
FFE / Pre-distortion	NL FFE + PD	NL+FFE + PD	No	W-bond peaking	RC Eq. on PIC	No (14 segments)	No (6 segments)	Ind. Feedback	Ind. Feedback	Ind. Peaking	Reconfigurable PD	
Signaling	PAM4	PAM4	PAM4	PAM4	PAM4	NRZ / PAM4	NRZ / PAM4	NRZ	NRZ	NRZ	NRZ	PAM4
Data Rate (Gb/s)	112 Gb/s	112 Gb/s	53.15 Gb/s	106 Gb/s	56 Gb/s	56 Gb/s PAM4	50 Gb/s PAM4	56 Gb/s	50 Gb/s	100 Gb/s	50 Gb/s	100Gb/s
Total Optical OMA	-1.24 dBm	-5.2 dBm	0.4 dBm	ER = 4.5 dB	-3.6 dBm	-2.2 dBm [4]	ER = 9.8 dB	-6 dBm	ER = 8 dB	ER = 2.97 dB	1.2 dBm [5]	1.4 dBm [5]
TDECQ	0.5 dB	0.88	1.8 dB	BER: 3.17×10⁻⁶	BER: 2.4×10⁻⁴	ER = 9.5 dB	-	ER = 4 dB	-	SNR: 2.64	0.76 dB	1.53 dB
Input Laser Power	13 dBm	12 dBm [2]	13.5 dBm	12 dBm	0 dBm	10 dBm	-	12 dBm	8 dBm	-	10 dBm	
Chip Active area (mm²)	N/A	2.25 [3]	44	0.3	0.4	15.84	4.92	-	0.69 [4]	0.5 [4]	0.62	
EIC Power Efficiency (pJ/bit)	6 [1]	6 [1]	5.2	1.5	1.59	12.6	13.64	0.71	11	2.03	2.4 [6]	
FOM (pJ/bit × Laser power / OMA)	63.7	125.9	49	-	5.5	39.8	-	151.4	-	-	17.4	

1: Including on-chip pattern generator and serializers
2: Estimated from total laser power of 160mW
3: Active area is 0.4mm²
4: Estimated from figure
5: Including coupling losses, on-chip IL and EDFA gain
6: Including serializers, clock path and control

competitive performance of the proposed OTX compared to the state-of-the-art SiPh transmitter systems:

$$FOM = EIC\ Energy\ Efficiency \times Optical\ Power\ Penalty$$

$$= \frac{EIC\ Energy\ Efficiency \times Laser\ Power}{Total\ OMA} \tag{5}$$

Moreover, a simulated optical performance, shown in Fig. 4.27, for a MOSCAP modulator structure, with t_{ox} = 5nm and a waveguide width of 360nm, shows similar optical efficiency
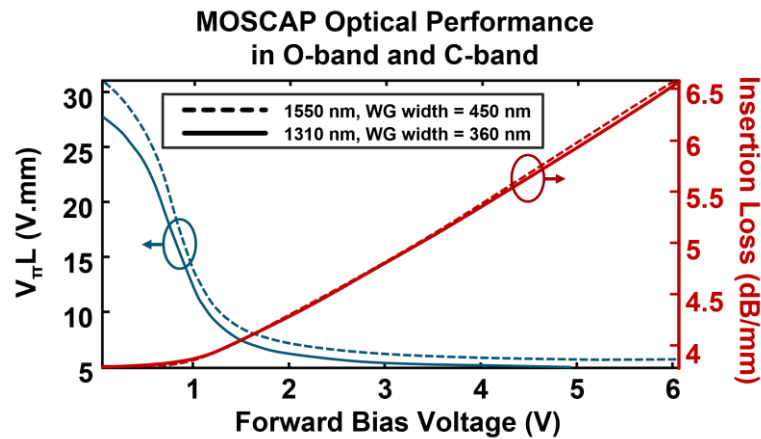
Fig. 4.27: Optical performance comparison for MOSCAP modulators in C-band and O-band, simulated for a slot thickness of 5nm.

and insertion losses in 1310nm compared to 1550nm, which shows the potentials of this structure when used in O-band.

Chapter 5

BIOFUEL-CELL-BASED ENERGY HARVESTER

5.1 Overview

Recent advances in low-power electronics have paved the way for a wide range of wearable and implantable biomedical devices for health monitoring and fitness applications. Integration of such mm-scale devices on biocompatible platforms shows great potentials for real-time biochemical sensing [1-6]. Many personalized monitoring biodevices are designed to perform multiple tasks such as on-demand wake-up, multiplexed sensing, processing, and wireless data transmission. These power-demanding operations are performed continuously or periodically over long durations, which sets challenging requirements for the energy sources and the overall power efficiency of the system [7].

Batteries have been the primary solution for many biochemical sensing systems; however, their limited capacities prevent long-term operations [8-10]. This is more pronounced when devices are miniaturized, and batteries must fit into smaller form factors. To tackle these challenges, prototypes with near-field wireless power delivery have been recently demonstrated for both implantable and wearable devices [11-14], yet their applications are limited since wireless power transmitters suffer from limited tissue depth penetration and need to be always in proximity of the sensor.

Other potential energy sources for biodevices include human body heat through thermoelectric generators (TEG), body motion via piezoelectric cells, and the sunlight with photovoltaic cells (PVC). However, they all fail to provide adequate power for local signal processing and wireless data transmission due to their low power densities [15, 16]. Off-chip storage elements could be utilized to periodically store and then deliver energy, but they increase the overall size of the system and would not allow continuous operation.

Biofuel-cells (BFCs) are promising alternatives to other forms of energy sources because of the versatile presence of biofuels and their superior energy density. Biofluids such as sweat, blood, basal tear, and saliva could serve as sustainable energy sources for the next generation of integrated biodevices [17, 18]. Glucose and lactate are fundamental energy

containing substances, which are found in abundance in biofluids. Lactate, as the main metabolic product of both muscle and brain exertion is found in sweat at tens of millimolar levels [19, 20].

Enzymatic BFCs act as biocatalysts to transform the bioenergy into electricity [21, 22]. They provide power densities at an approximately 1-40µW/mm^2 range [23]. For small surface areas, it is crucial to design energy harvesters with high efficiencies at µW input power levels. It is also important to note that the open-circuit (OC) voltage levels of the recently developed BFCs non-predictably range from 0.3-0.6V, and the energy harvester system needs to convert the voltage to higher levels as required by most sensors. The OC voltage is mainly set by the electrode design, the materials on the cathode, and even the packaging of the enzymes on the electrodes. Moreover, as power extraction continues, biofuels degrade over time and the system should track these changes to efficiently continue the operation. In fact, the available input voltage of the BFC at the maximum power point (MPP), which is always lower than the OC voltage, decreases as the BFC or the solution concentration degrades [23].

Previous integrated sensors using BFCs as their energy sources have utilized either extensive off-chip circuitry, with numerous of BFC electrodes to supply all modules [23], or bulky off-chip electrical capacitors (1µF and 1×0.5 mm^2) for energy storage because of the limited power and open-circuit (OC) voltage [24]. Other energy harvesting systems developed for IoT applications either use external electrical components [25-30], or suffer from loading condition dependencies [31], limited voltage requirements [32-34] and non-optimal power efficiencies at few-µW loading conditions [35-37].

This paper presents a cold-starting energy harvester in 65nm CMOS with source degradation tracing and automatic maximum power point tracking (MPPT) to address these BFC energy extraction challenges. A combination of two DC-DC voltage boost and buck converters with a hysteretic regulation approach is proposed to achieve 86% peak efficiency at 0.39V of input voltage and 1.34µW of output power. The chip uses no off-chip components, except for two BFC electrodes, developed using cross-dimensional nanomaterial integration, that utilizes lactate and oxygen as the fuel sources. Finally, energy extraction and power delivery from a lactate solution is demonstrated using the

proposed integrated biodevice. The fully integrated CMOS chip allows for easy integration with any compatible energy source, as well as larger health-monitoring devices, such as smart watches and skin patches. Moreover, the overall fabrication cost is reduced due to minimized component count and in the final product.

This paper is organized as follows. In section II the proposed system architecture is presented, and its advantages are described. Section III provides the system-level analysis of a generic harvester system and extends it to the proposed architecture. All major system building blocks and their interconnections are described in detail in section IV. Section V elaborates the operation of the MPPT and presents the algorithm used to perform source degradation tracing. The experimental results of the energy harvester chip and its integration with the BFCs are provided in section VI. Finally, section VII summarizes this paper with performance comparisons and conclusions.

5.2 Proposed System Architecture

State-of-the-art biofuel-cells provide power densities in a range of 1μW to 40μW per mm^2 of the electrode area. To design a compact device with a single pair of BFC electrodes with 2mm of diameter, the energy harvester should dissipate fewer than 1μW on average for a reasonable end-to-end power efficiency. It is also very important that the system wakes up immediately whenever the source power is available, and energy extraction should start immediately without any external trigger. In addition, to make the harvester system compatible with standard on-chip CMOS sensors, we intend to regulate the boosted voltage at nominal supply values (0.9V to 1.2V).

For major improvements in the overall power efficiency of the energy harvester systems, the system architecture design should be prioritized over block-level optimizations. The internal supply voltage seems to be the main bottleneck of the overall internal power consumption. In fact, the internal circuitry could be designed to operate with a lower supply to save power. It is well known that the supply voltage has a quadratic relationship with
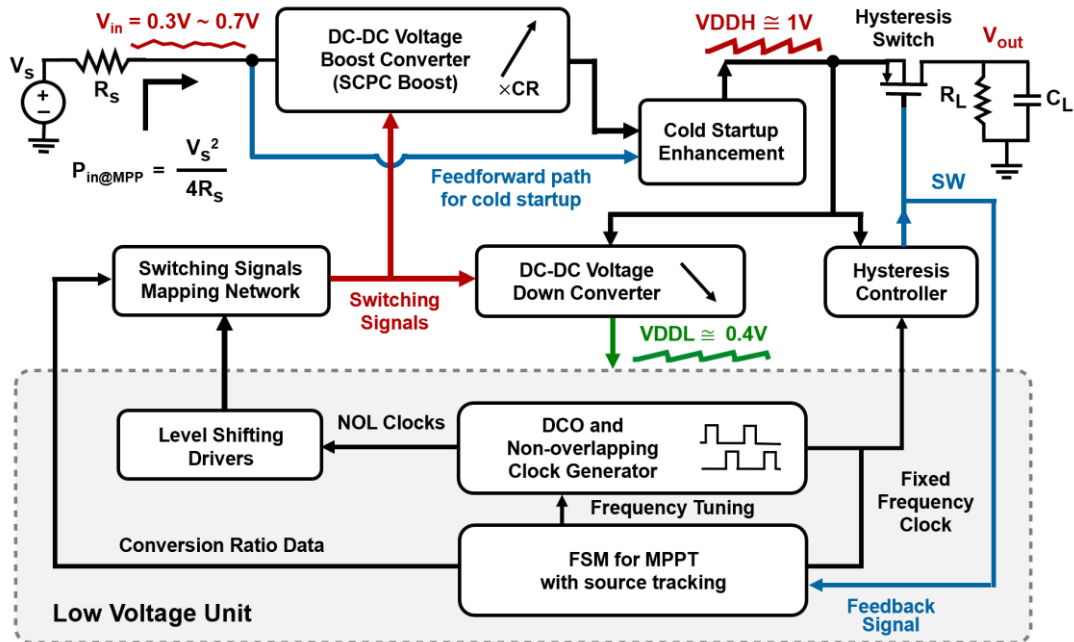
Fig. 5.1: Top level block diagram of the proposed energy harvester system.

the dynamic power and a linear relationship with the static power of the digital circuitry [38]. The proposed system architecture is designed to be supplied by the lowest reliable voltage that the 65nm CMOS technology permits. Although most designed blocks operate successfully with 0.25V, the internal supply is set to 0.4V. This voltage was chosen based on reliable operation of the logic core of the system.

A major challenge is that the internal supply voltage also needs to be regulated. Since the lower boundary value of the BFC OC voltage (0.3V) is lower than the targeted internal voltage supply (0.4V), it would not be reliable to directly down-convert and regulate the BFC voltage to supply the internals. In this paper a system-level solution is proposed to address these challenges and to achieve superior power efficiency.

The proposed top-level block diagram of the energy harvester is shown in Fig. 5.1. It consists of a reconfigurable switched-capacitor power converter (SCPC) in parallel with a feedforward path for cold startup that is initially used to bypass this block. A cold startup enhancement block receives the available voltages from these 2 paths and delivers the highest available voltage to the internal circuitry. A dual-path DC-DC voltage down converter provides voltage supply to the low-voltage unit (shaded with gray in Fig. 5.1),

which includes a digitally controlled oscillator (DCO) for the boost SCPC, a non-overlapping (NOL) clock generator, a finite-state-machine (FSM) for MPPT and 2 ring oscillators with fixed frequencies for the FSM and the buck SCPC in the voltage down converter block. Clocking signals are generated at the low voltage level (VDDL) and shifted up to the main supply voltage (VDDH) by a group of level shifters. These clock signals are fed to a mapping network, which redirects and distributes them to corresponding switches in the boost and the buck SCPCs. The switching network is designed based on a combinational logic FSM and is controlled by a conversion ratio (CR) set by the MPPT FSM dynamically. At the same time, the boosted voltage (VDDH) is regulated by a hysteretic controller between two programmable thresholds (V_{OH} and V_{OL}), which could be set according to the load requirements. The proposed architecture ensures that the system performs a cold startup with a minimum input voltage of 0.39V and continues operation when it degrades to as low as 0.25V over time. Details of the cold startup and the operation of the building blocks with low voltage supplies are provided in section IV. The reason that the voltage up converter and voltage down converter stages are not combined is their different roles in the architecture. In fact, the boost stage, provides an arbitrary gain over time for MPPT, which makes its internal stages to have arbitrary voltage levels. The buck stage, however, receives and down-converts the regulated voltage for the internals. Another benefit of cascading the down converter stage is the reduction of the ripples at VDDH by the gain of the down-conversion at the VDDL node. Utilizing the proposed two-stage topology is more power efficient only if the cascading losses are minimized and the overall power efficiency is better than having the internals supplied by the boosted voltage (0.9V to 1.2V). A power analysis based on measurements is provided in section VI to further demonstrate the benefits of the proposed system architecture.

The regulating switch on the right side of Fig. 5.1 is designed to remain ON if the loading demand is less than the deliverable power. In this case, the SW signal remains at the ground level (the switch is operated with an inverted logic and turns ON when the SW signal is low). VDDH, hence V_{out} would rise and saturate above the targeted values for regulation at the MPP and the load will be continuously powered. Then depending on the application, the gain (CR) or the switching frequency (f_{S1}) of the boost SCPC could be changed to move
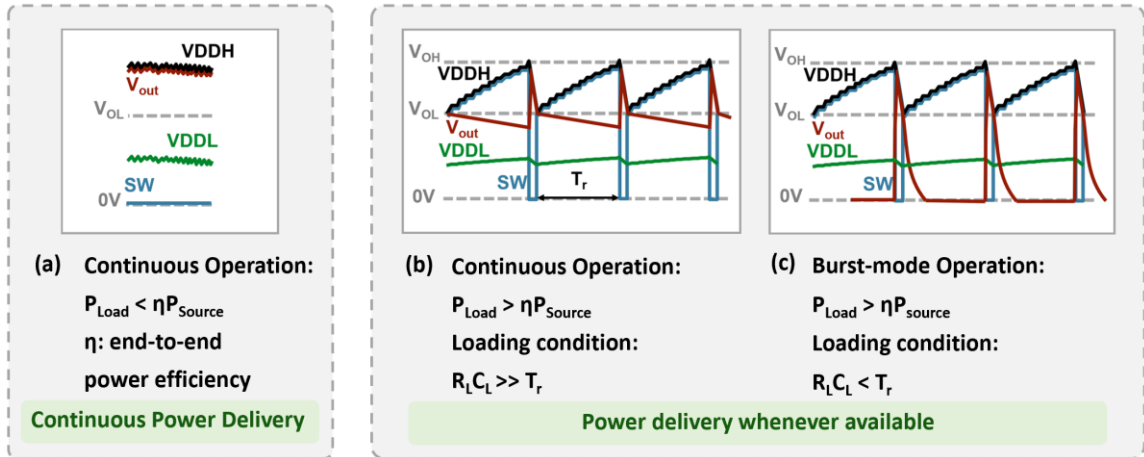
Fig. 5.2: Various loading conditions depending on the application: (a) continuous power delivery (high-power sources or low-power sensors) and (b, c) periodic power delivery (for energy-storing/wakeup-enabled sensors with high power requirements).

away from the MPP for de-stressing the BFC and improving its lifetime. This scenario is shown in Fig. 5.2(a). In the opposite case, in Fig. 5.2(b), when the loading demand is higher, the switch performs a hysteretic control to keep VDDH between 2 programmed thresholds (V_{OH} and V_{OL}). The circuit charges up an on-chip storage capacitor (C_{st}), until VDDH reaches V_{OH}. Then the switch turns ON to deliver power to the load, until VDDH drops to V_{OL}, and then turns OFF to re-charge the capacitor. In this case, the charging time (T_r) is smaller than the load RC time constant (applicable to sensors with a storage capacitor). Hence, V_{out} would remain high even when the switch is OFF, and we would again have a continuous sensing operation. In the 3rd case, in Fig. 5.2(c), the situation is similar, except that the RC time constant of the load is lower than T_r. Therefore, V_{out} drops to zero whenever the switch is OFF. This is applicable to sensors with a burst-mode (wakeup-enabled) operation, where sensing continues whenever power becomes available.

In order to show the advantages of the proposed architecture compared to the previous designs, a system-level analysis of a generic energy harvester and its extension to the proposed system are discussed next.

5.3 Harvester System Modeling and Analysis

In this section, a simplified circuit model is provided to analyze the nonlinear characteristics of a generic harvester system. By the pseudo-static assumption, a general-purpose energy harvester could be modeled as a voltage boost converter in series with a switch that connects the output of the harvester to the load, as shown in Fig. 5.3. Depending on the application and the chosen architecture, this switch could always be kept closed, or designed to operate periodically to regulate the output voltage (load regulation). The inefficiencies of the system are modeled by a series resistance R_{CP}, causing a voltage drop after boosting, and a parallel resistance R_{int}, accounting for internal power consumption. Furthermore, a storage capacitor C_{st} is in parallel with R_{int} to support power delivery to both internal circuits and the load. R_{CP} and R_{int} would consist of both constant and dynamic portions depending on the architecture. A few examples of dynamic variables are the conversion ratio, switching frequencies, switching transistors widths and the supply voltage. We have provided generic circuit models for the energy source (a voltage source V_S in series with resistance R_S) and the load (R_L in parallel with C_L) to extend our analysis for various sources and loading conditions. All these 4 variables could change over time (for example, to mimic source degradation in a BFC or a stand-by mode in a sensor). We define $P_{in, MPP}$ as the maximum transferable power from the source of energy to the system. According to the theorem of maximum power transfer, $P_{in, MPP}$ is calculated as:

$$P_{in, MPP} = \frac{V_S^2}{4R_S} \tag{1}$$

We also define P_{out} as the average of delivered power to the load, which could be written as:

$$P_{out} = \frac{V_{out}^2}{R_L} \tag{2}$$
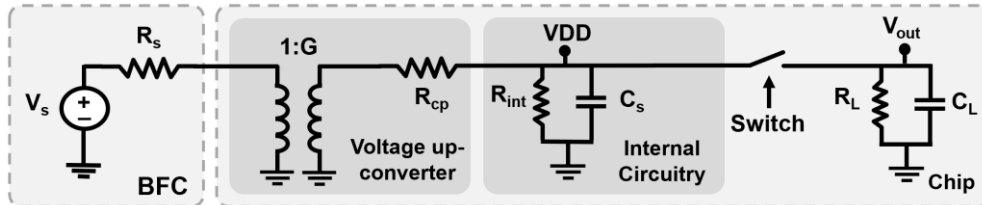
Fig. 5.3: Simplified circuit model of a generic energy harvester system.

We now consider the following conditions of operation for further analysis:

5.3.1 Continuous Power Delivery (Switch always ON)

In this case, no output voltage (or load) regulation is performed, and the power is constantly delivered to the load. This would be applicable to cases with powerful sources or less demanding loads. Depending on the loading conditions and the available power, the output voltage ($V_{out} = VDD$) would settle to an arbitrary value. With a given V_S, R_S, R_{CP}, and R_{int}, V_{out} is derived by the following equation:

$$V_{out} = V_S \left(\frac{R_L^{'} \times G}{R_L^{'} + R_{CP} + R_S \times G^2} \right) \tag{3}$$

where $R_L^{'} = (R_{int} \, || \, R_L)$. The end-to-end power efficiency would also be calculated as:

$$\eta_{out} = \frac{4R_S G^2}{R_L} \left(\frac{R_L^{'}}{R_L^{'} + R_{CP} + R_S \times G^2} \right)^2 \tag{4}$$
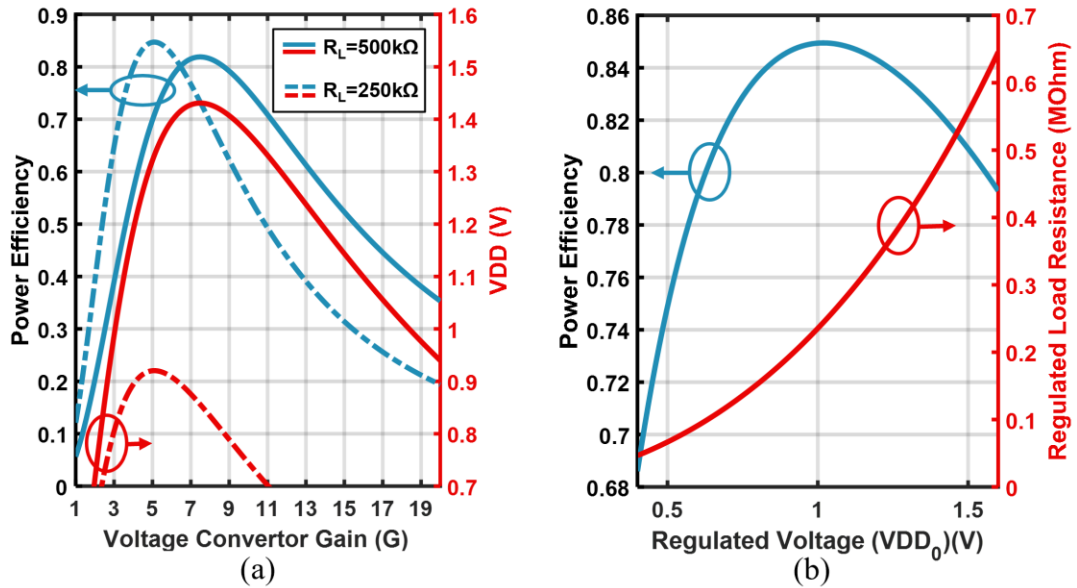
Fig. 5.4: Generic nonlinear system characteristics for (a) continuous power delivery (switch always ON) and (b) load regulation (VDD regulation).

This shows that the boost converter gain G and the load resistance R_L could be tuned to satisfy the load voltage requirements. However, if the maximum power efficiency is intended, R_L will be the only factor that sets V_{out}. A simulated plot is provided in Fig. 5.4(a) to show the generic nonlinearities of (3) and (4). By maximizing the power efficiency with respect to G, we would have:

$$\eta_{out,\ MPP} = \left(\frac{R_L^{'}}{R_L^{'} + R_{CP}} \right) \left(\frac{R_{int}}{R_{int} + R_L} \right) \tag{5}$$

This maximum happens at,

$$G_{MPP} = \sqrt{\frac{R_L^{'} + R_{CP}}{R_S}} \tag{6}$$

and the output voltage is then set to:

$$V_{out,\ MPP} = \frac{G_{MPP} \times V_S}{2} \left(\frac{R_L^{'}}{R_L^{'} + R_{CP}} \right) \tag{7}$$

Equation (7) shows that R_L sets $V_{out,\ MPP}$, which is not desired. Although, if the source is powerful enough to remove the need of MPPT, the gain G could be tuned away from the MPP to set V_{out} independent of R_L.

5.3.2 Load Regulation (VDD Regulation)

In this case, the switch is used to regulate VDD at a target value required by the load. This scenario is considered when the output power delivery is lower than loading demand, even at the MPP. The switch turns ON only when power is available, while keeping VDD above V_{OL} and below V_{OH} (hysteretic control). With the pseudo-static assumption, we can assume VDD is set to an average (VDD_0) by replacing the load and the switch with a new averaged load resistor R_{Lav}. This resistance depends on the switch toggling rate, which keeps VDD at VDD_0. By rewriting the equations, the power efficiency at MPP is derived as:

$$\eta_{out,\,MPP} = \frac{2}{1+\sqrt{1+\left(\frac{R_{CP}}{R_S}\right)\left(\frac{V_S}{VDD_0}\right)^2}} - \frac{4R_S \times VDD_0{}^2}{R_{int} \times V_S{}^2} \tag{8}$$

The first term in (8) is the overall efficiency of the transferred power to the right side of the voltage booster and the second term is the power penalty of the internal circuits. At this maximum, the voltage gain (G_{MPP}) is:

$$G_{MPP} = \sqrt{\frac{R'_{Lav}+R_{CP}}{R_S}} = \frac{VDD_0}{V_S} + \sqrt{\left(\frac{VDD_0}{V_S}\right)^2 + \frac{R_{CP}}{R_S}} \tag{9}$$

Where $R'_{Lav} = (R_{int} \,//\, R_{Lav})$ and R_{Lav} can be calculated by:

$$R_{Lav} = \frac{R_{int}}{\sqrt{1+\left(\frac{R_{int}}{R_{CP}}\right)}} \tag{10}$$

Fig. 5.4(b) shows simulated trends of R_{Lav} and power efficiency $\eta_{out,\,MPP}$ versus VDD_0. It is worth noting that in this scenario, the power efficiency at MPP depends on VDD_0. If the supply requirement for a sensor is different than the maximum point of this curve, then extra power is burnt internally. This inefficiency is due to a resistance mismatch between R_{Lav} and the rest of the circuit (even at the MPP). Another noticeable observation is that R_{Lav} is independent of R_L, which is desired in designing an energy harvester without taking loading conditions into account.

The simplified circuit model of the proposed energy harvester system is shown in Fig. 5.5. By using a secondary voltage converter, the boosted and regulated voltage (VDDH) is converted down (VDDL) to supply the internal circuits. A switched capacitor structure is used for both voltage converters to achieve superior voltage conversion efficiency. Capacitors can be designed precisely in CMOS processes, which helps with accurate system-level modeling. While inductor-based voltage converters also provide a similar performance, it is desirable to avoid using bulky off-chip or area consuming on-chip inductors. The reconfigurable boost SCPC allows for having independent control over the gain (G_1) and the switching frequency (f_{S1}). Another SCPC with a fixed gain (G_2) and a
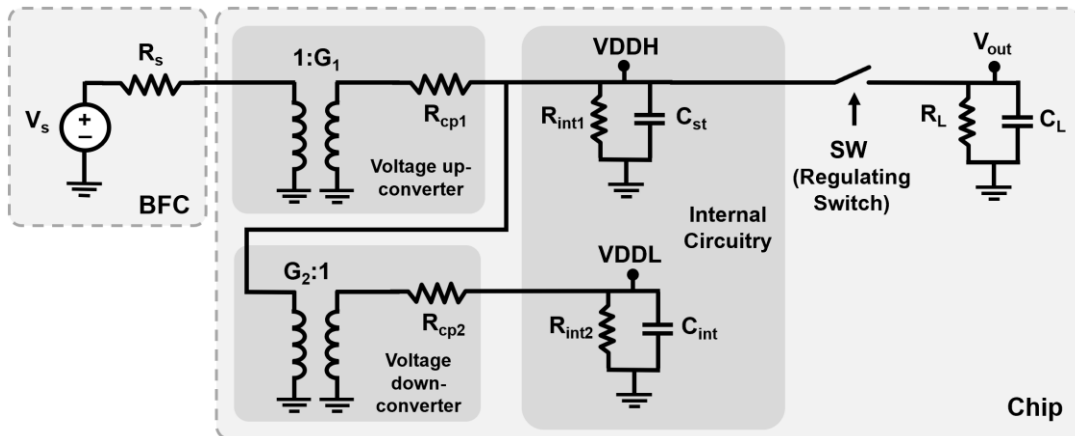
Fig. 5.5: Simplified circuit model of the proposed energy harvester system.

fixed switching frequency (f_{S2}) is used to down-convert the voltage at steady state. VDDL is chosen to be 0.4V to ensure reliable internal operations, therefore, G_2 is set to 2.5. The resistors R_{CP1} and R_{CP2} in Fig. 5.5 are inversely proportional to their corresponding flying capacitors and switching frequencies (f_{S1} and f_{S2}). Finally, R_{int1} and R_{int2} are resistors that account for both dynamic and leakage power.

The model provided in Fig. 5.5 would be more power efficient at steady state compared to traditional architectures that do not down-convert the internal voltage supply. However, this would hold true only when all circuit blocks are operating at the steady state, which will not be the case during the startup. At startup, neither of the SCPCs are functioning since the clock is not generated yet. Hence, there will be numerous challenges to be addressed to perform cold startup. These challenges will be studied and addressed in the following sections.

5.4 Design and Analysis of Main Building Blocks

In this section, critical building blocks of the proposed energy harvester system are discussed in more details.

5.4.1 Cold Startup Enhancement Block

The cold startup sequence is first explained in this sub-section, and circuit details are presented next. Initially, when the BFC is connected to the chip, the feedforward path

bypasses the boost SCPC (since no clock signal is available). This voltage path is then shorted through the cold startup enhancement block and the buck SCPC. Hence, the available voltage is delivered to the internal circuitry with minimized drop to maximize the chances of starting the low voltage unit. The DCO and the FSM start operating, and the clock signals are sent to the level shifters. Through the mapping network, the clocking signals are delivered to both SCPCs. When voltage boosting starts, the FSM choses the boost SCPC over the feedforward path to use the increased supply for VDDH. At the same time, the buck SCPC keeps VDDL at 0.4V. When VDDH reaches the voltage thresholds, the regulating switch starts delivering power to the load and the chip operates according to one of the 3 loading conditions mentioned in the previous section in Fig. 5.2. The feedforward path is not directly connected to the low-voltage unit since the open-circuit voltage of the BFC (V_S) is non-predictable. If V_S is larger than 0.4V, then the internal circuitry would burn excessive power, which would either shorten the lifetime of the BFC [17, 21, 23] or prevent the system to transit from cold startup to the steady state (because of excessive voltage drop across R_S). In fact, the DC-DC voltage down converter block ensures that VDDL never exceeds 0.4V even if the source voltage is higher.

The cold startup enhancement block, shown in Fig. 5.6, consists of 4 low-V_{th} (LVT) PMOS switches to initially isolate VDDH from the output of the boost SCPC (V_{cp}) and the V_{cap} node with a 1.3nF storage capacitor (C_{st}). These switches are controlled by two latch-based comparators that dynamically compare VDDH to V_{cap} and V_{cap} to V_{cp}, respectively. At startup, signals S1 and S2, as shown in Fig. 5.6, are both zero so that the VDDH node is first pulled up to V_{in} by M3 and isolated from V_{cap} by M4 (V_{in} is the node after the source resistance R_S). Therefore, the SCPC is bypassed, and the internal blocks start operating. At the same time, the storage capacitor C_{st} is being charged by V_{in} through M1 while V_{cp} is boosted by the SCPC. Once V_{cap} reaches V_{in} and V_{cp} reaches V_{cap}, S1 and S2 are toggled to ensure a smooth supply transition from V_{in} to V_{cp} for the VDDH node as soon as the boost SCPC and C_s are ready.
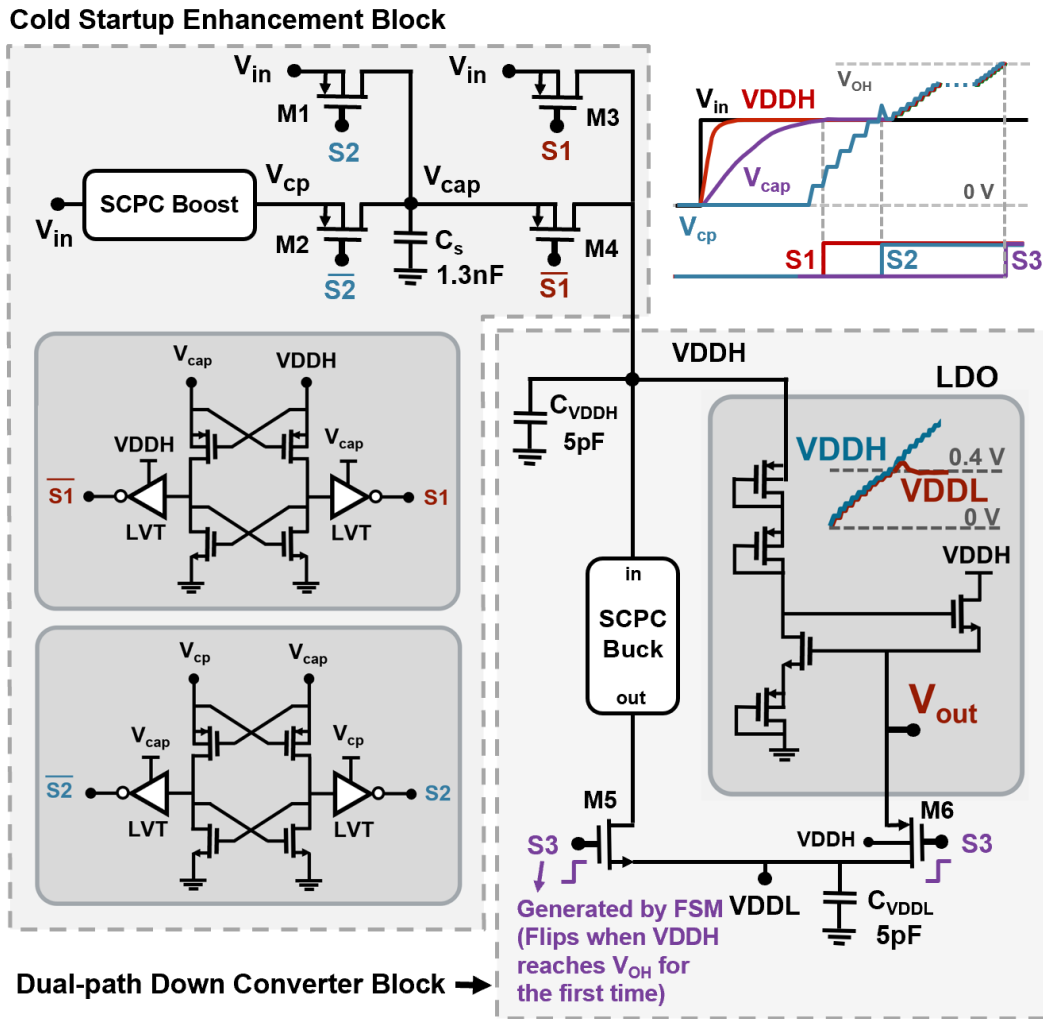
Fig. 5.6: Cold startup enhancement and the dual path down converter blocks.

5.4.2 Dual-Path Down Converter Block

The dual-path down converter block works closely with the cold startup enhancement block. The first sub-block in the dual-path down converter is a low-dropout voltage regulator (LDO). As shown in Fig. 5.6, the LDO can be modeled as a controlled high-pass filter, in which the output (VDDL) initially follows the input voltage (VDDH) and then gets regulated at 0.4V. This block is used at startup, as soon as VDDH is pulled up to V_{in}, to deliver the initially available voltage to the internal circuitry in the low-voltage unit. The LDO is mainly designed to not rely on clocking signals at startup. Hence, the output of the LDO is shorted to VDDL through M6 with signal S3 which is initially zero.

The first critical sub-blocks that should start functioning with VDDL are the oscillators that start both SCPCs. As soon as these oscillators start, the level shifters convert the clocking signals levels to VDDH (which is equal to V_{in} at that moment). The clocking signals are then sent to both SCPCs through the switch mapping network. The settings of the mapping network are pre-programmed to set the boost SCPC to a conversion ratio of 6, even before the FSM starts the MPPT. This CR_0 was chosen based on simulations in section II as the closest initial guess to the correct CR for MPPT. Furthermore, this CR_0 ensures that VDDH reaches V_{OH} even though it might not be the optimum CR at steady state.

When the boost SCPC is clocked, VDDH starts rising above V_S. Since a similar architecture is used for all oscillators, they would start oscillating simultaneously. Therefore, while VDDH is being boosted, the FSM starts tracking it and the buck SCPC down-converts VDDH. The output of the buck SCPC is however isolated from the VDDL node initially through M5 and with signal S3, which is generated by the FSM. When VDDH reaches V_{OH} for the first time, the FSM toggles S3 to switch the down-conversion path from the LDO to the more power-efficient buck SCPC. The buck SCPC continuously multiples VDDH by 2/5 through cascading a standard $\times 1/5$ voltage divider with a voltage doubler.

The metal-insulator-metal (MIM) storage capacitor C_{st} is chosen to be larger than 1nF, based on the requirements of a previously designed on-chip sensor in [11]. The size of C_{st} was limited by the chip area and was set to 1.3nF. This relatively large on-chip capacitance also helps reducing the switching clock ripples at the VDDH node to lower than 5mV. The ripple at VDDL due to the ripple at VDDH is also decreased by a factor of 0.4, which reduces the clocking ripples to lower than 2mV. The additional ripples due to the DCO, the non-overlapping clock generator, the MPPT FSM and level shifters are negligible at the VDDL node. In fact, the 5pF capacitor at the VDDL node (C_{VDDL}) is mainly chosen such that the transition from the LDO to the buck converter is smooth. The 5pF capacitor at the VDDH node (C_{VDDH}) has only a role at startup when the boost SCPC is bypassed. It is chosen to be 5pF to match C_{VDDL} such that when the LDO is effectively shorted (when VDDH < 0.4V) there will be minimized charge sharing losses between C_{VDDL} and C_{VDDH}.
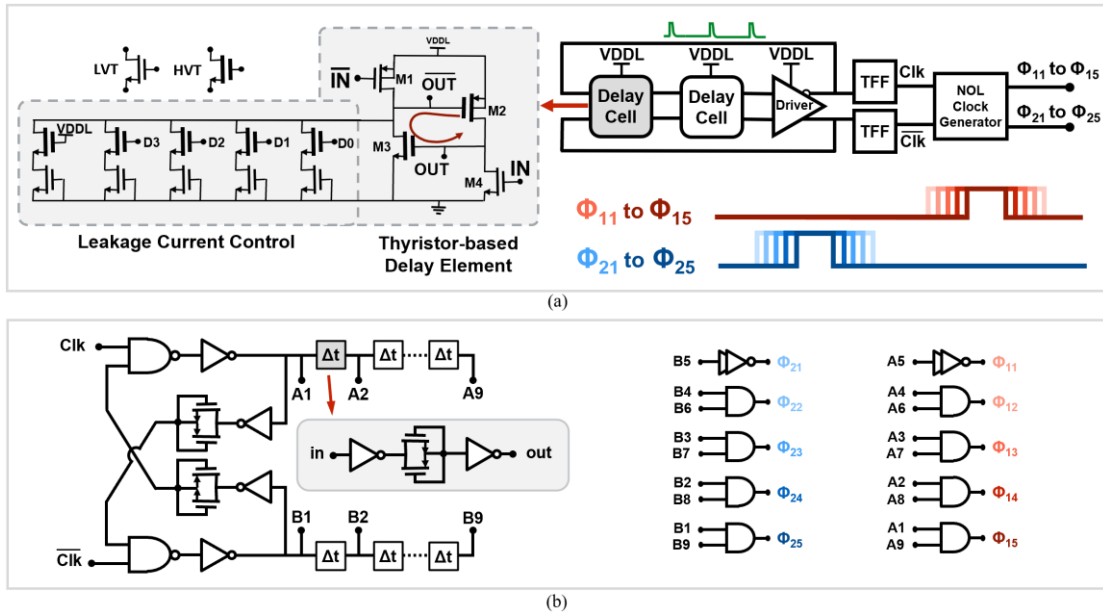
Fig. 5.7: (a) Schematics of the digitally controlled oscillator followed by the non-overlapping clock generator. (b) Schematics of the non-overlapping clock generator.

5.4.3 Low-Voltage Digitally Controlled Ring Oscillator (DCO)

The digitally controlled ring oscillator, shown in Fig. 5.7(a) operates at a minimum of 0.25V supply voltage and provides clocking signals to the boost SCPC through the NOL clock generator, level shifters and then the switch mapping network. It consists of two thyristor-based delay cells followed by an inverter buffer. In each delay cell, as depicted in Fig. 5.7(a), transistors M1 and M4 first reset the block with a pulse signal at their gates. Subsequently, the drain voltages of M2 and M3 start accumulating/dissipating charge through the sub-threshold leakage current paths that M1 and M4 provide. The outputs then switch through the positive feedback loop that is formed by M2 and M3. The duration of this transition (hence, the frequency of the oscillator) is adjusted by the binary-weighted branches of sub-threshold transistors. These branches provide leakage current paths driven by signals D0 through D3, which are controlled by the FSM. Minimum-size LVT transistors are chosen for M1 and M4 to minimizes the overall power consumption while providing enough leakage current. M2 and M3 mainly operate in sub-threshold and are HVT to be more robust across process corners. It should be noted that the frequency tuning range would be lower than the

theoretical 16x with 4 control bits. There are several non-idealities in the design that should be considered. One major contribution to this non-linearity is from the switch transistors (controlled by D0 through D3 in Fig. 5.7(a)). Even when all switches are OFF, all branches would still contribute to the overall leakage current. Moreover, the control paths impose additional capacitance to the OUT_bar node in Fig. 5.7(a). The total capacitance at this node changes as the control bits are altered, which results in a change in charging/discharging time. In addition, increasing the number of ON branches would eventually result in frequency saturation. This is primarily due to transistor M1 in Fig. 5.7(a) becoming the bottleneck of the leakage current. This could be improved by increasing the size of M1 (and M4), with a trade-off for more power consumption and oscillation failure at lower supply voltages. In this work, since the lowest possible operating supply (0.25V) is of main concern, the dimensions of M1 and M4 were minimized, which eventually resulted in a lower frequency tuning range. The outputs of this ring oscillator are two complementary impulse trains, the width of which are defined by the delays that the inverter buffers generate. In order to get clean clock signals with 50% duty-cycles, both outputs are passed through two T-flip-flops. The thyristor-based delay elements burn less power than conventional inverter-based delay cells. The main reason is that the inputs of the thyristor-based cells toggle much faster than their outputs, hence, the short-circuit current is significantly reduced. Moreover, the thyristor-based delay cells are inherently slow (in contrast with inverters), due to their operation based on leakage current, which makes them excellent candidates for low-frequency oscillators.

The schematics of the NOL clock generator are shown in Fig. 5.7(b). All transistors used in this block are LVT to make sure the transitions are as fast as possible even at very low voltage supplies. Any slow transitions in the waveforms would result in overlapping signals, which would decrease the boost/buck SCPC efficiency significantly and even preventing the harvester from performing cold startup.

5.4.4   Switched-Capacitor DC-DC Boost Converter (SCPC)

The boost SCPC consists of 4 stages of interleaved voltage doublers, each performing a ×1, +1 or ×2 operation. With this arrangement, all integer conversion ratios (CR, which is

equivalent to the gain G_1 in section III) from 1 through 16 except for 11, 13, 14 and 15 are achievable. Fig.5.8(a) shows the details of each stage. PMOS and NMOS transistors are used

(a)

(b)

(a)

(b)
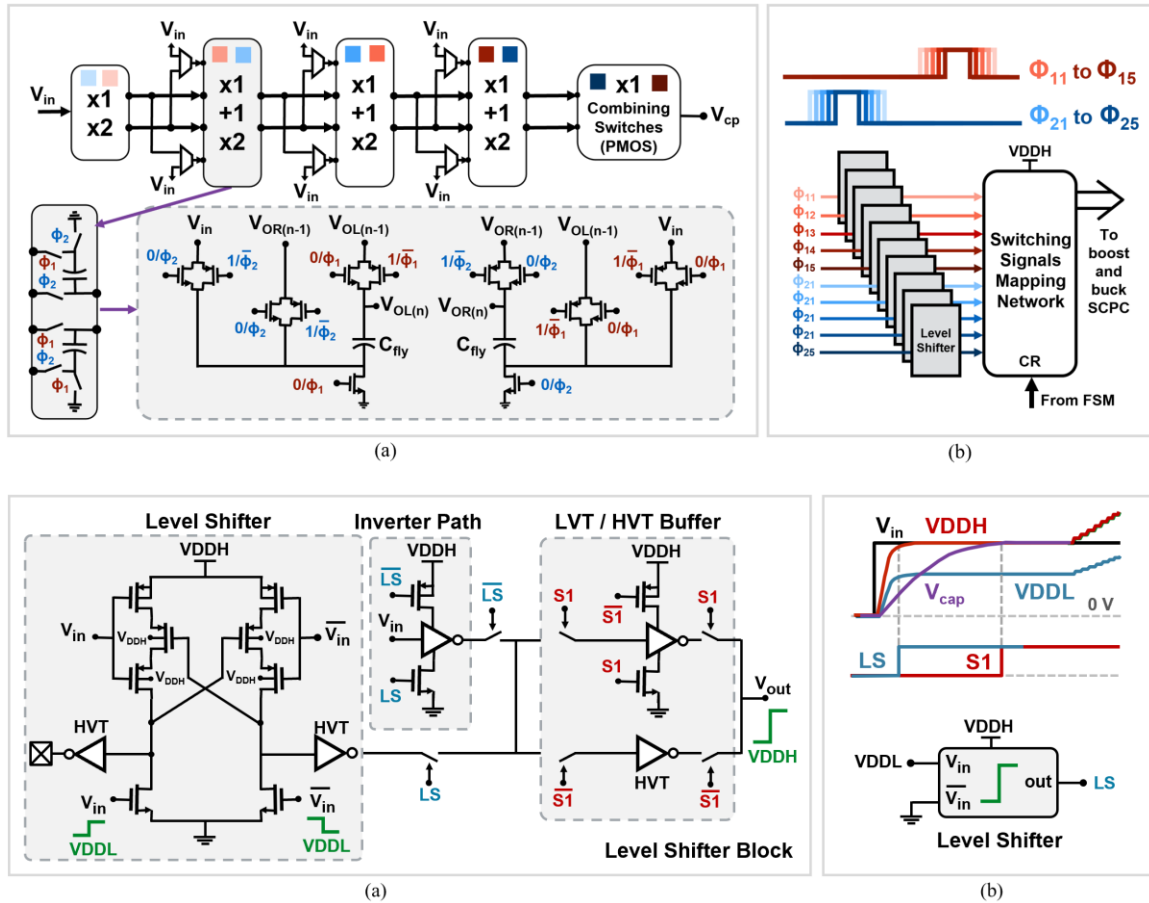
Fig. 5.8: (a) Schematics of the reconfigurable switched-capacitor power converter (boost). (b) Arrangement of the level shifters and the switch mapping network. (c) Schematics of the dual-path level shifters. (d) Generation of the LS signal through an identical level shifter with its input connected to VDDL. Signal S1 is generated by the comparison of VDDH and V_{cap} through a latched comparator.

for both the high-side and the low-side switches for a minimal ON resistance, especially when the switching signals have lower swings at startup. PMOS switches are avoided for ground connection of bottom plates of the flying capacitors since they provide a shorted path from V_{in} to the ground at startup. Each transistor is sized individually for an optimum ON resistance, gate capacitance, and isolation (when turned off).

For an efficient performance, the switches of the SCPC should always be driven with VDDH-level clock signals. This is critical especially when a switch connects the output of a stage to the input of the next. Maximized gate voltages would bring switches to deep ON/OFF states to reduce voltage drops and leakage currents. It is also important to determine the order of level-shifting and distributing the clocking signals. The switch mapping network consists of fundamental logic gates that form a combinational logic FSM. Hence, its average dynamic power consumption scales quadratically with its supply voltage. It might seem reasonable to put the mapping network first, followed by the level shifters; however, the necessary number of level shifters would increase from 10 to 54 for the boost SCPC and to 88 for the buck SCPC. A power optimization analysis is performed to choose the appropriate placement order of the level shifters and the mapping network. Considering the total number of SCPC switches and the average activity factor of all mapping network circuitry (which depends on the chosen CR), placing the level shifters first, saves power by 40% (Fig. 5.8(b)).

5.4.5   Level Shifters

The level shifters are used to convert the voltage levels of several logic and clock signals from VDDL to VDDH, while maintaining the timing margins of the non-overlapping clocks. The proposed level shifter circuit is shown in Fig. 5.8(c). At startup, when both VDDH and VDDL are below V_S, the input signal is passed through the LVT inverter path followed by the LVT buffer, since no level shifting is required, and transitions should be as sharp as possible. In fact, VDDH is initially pulled up to V_S and is then boosted towards V_{OH}, while the LDO and then the buck SCPC keep VDDL at around 0.4V. This transition separates VDDL from VDDH gradually. It is desirable to choose the level shifter path over the inverter path as soon as a significant difference is detected between VDDL and VDDH. The LS signal in Fig. 5.8(c) is toggled to choose the level shifter over the LVT inverter path when this difference is detected. The details of generating the LS signal are discussed next.

The level shifter sub-block consists of a stacked and cross-coupled structure to enhance the gain. This architecture ensures that the level-shifting operation is feasible under all combinations of VDDL and VDDH from 0.4V to 1V. For voltages below 0.4V, due to its

stacked structure, the level shifter will have a dead zone, in which the level shifting fails even if there is a difference between VDDL and VDDH. To tackle this challenge and change the path from the inverter to the level shifter at a correct moment, an identical level shifter with a fixed input of VDDL and a supply of VDDH is used to generate the LS signal for all other level shifter blocks (Fig. 5.8(d)). A high output of this block ensures that all other level shifters will be ready to convert a signal with the current VDDL amplitude to VDDH.

As VDDH increases further, an HVT buffer is selected over the LVT buffer to prevent excessive dynamic short currents during each transition. Static power would also be slightly improved since subthreshold leakage currents of HVT transistors are smaller. The transition to the HVT buffer is made by the S1 signal generated by the latched comparator, comparing VDDH and V_S. It is worth noting that the toggling order of the LS and S1 signals could be exchanged according to different BFC open-circuit voltages; however, the transition timings of the non-overlapping clock signals will be maintained.

5.4.6   Hysteretic Controller

The hysteretic controller (Fig. 5.9(a)) consists of two clocked comparators that compare VDDH to V_{OH} and V_{OL}. Since V_{OH} and V_{OL} are not physically available to be compared to VDDH, an indirect comparison is performed. VDDH is divided by two separate voltage divider ladders to VDDH/d_1 and VDDH/d_2 as shown in Fig. 5.9(a). These ladders are programmable and are initially set to 2 and 11/6, respectively. Two comparators are used to
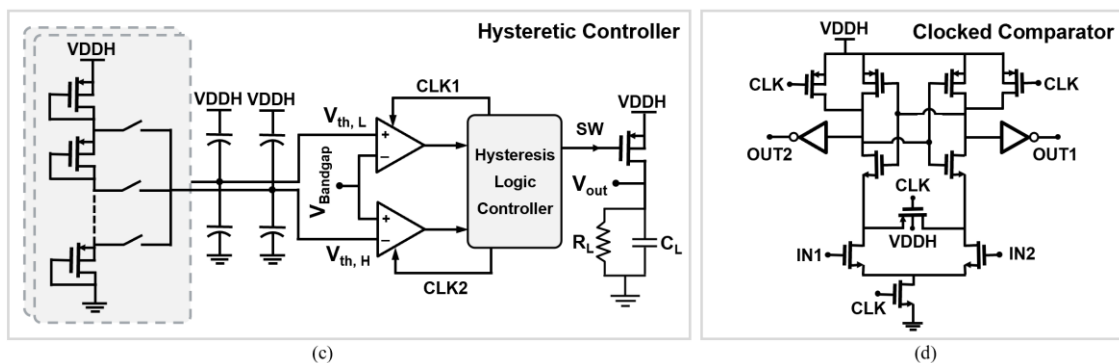
Fig. 5.9: (a) Hysteretic controller schematic. (b) Schematic of the clocked comparators used in the hysteretic controller.

compare $VDDH/d_1$ and $VDDH/d_2$ to a bandgap voltage reference ($V_{ref} = 0.55V$), which effectively makes the controller compare VDDH to $V_{OH}=d_1 \times V_{ref}$ and $V_{OL}=d_2 \times V_{ref}$. Depending on the loading conditions, VDDH is either kept between V_{OH} and V_{OL} or gets saturated (above V_{OL}). In this work, the ladders are designed to provide flexibility for choosing V_{OH} and V_{OL} with the minimum separation of 0.1V for demonstration purposes. In general, this distance could be arbitrarily reduced and entirely set by the load requirements without compromising the harvesting efficiency. In fact, the separation of V_{OL} and V_{OH} could be reduced such that after each clock cycle, the boosted voltage is instantly delivered to the load (similar to reference [35]). However, in case the load is capacitive, there will be a significant drop in VDDH whenever the power is delivered to the load, due to charge sharing between the load capacitance and the internal storage capacitor of the harvester. Increasing the ripple of the VDDH node provides the advantage of tolerating these voltage drops to prevent the harvester from failure. It should be noted that the ripple on the V_{out} node is of our main concern, and not the VDDH node. In fact, V_{out} is the actual node that supplies the loads. As we recall from Fig. 5.2, depending on the loading conditions, along with the settings for VDDH ripple, the ripple of the V_{out} node could be entirely different.

A hysteretic controller logic block, which is another sequential logic FSM that is synthesized with HVT transistors is used to receive inputs from both comparators to toggle the SW signal. The SW signal controls the hysteretic PMOS switch that connects the VDDH node to the load (V_{out}). The schematic of the clocked comparator is shown in Fig. 5.9(b). The frequency of the clock that enables the comparators should be sufficiently high such that they respond quickly when VDDH crosses V_{OH} or V_{OL}. To set the correct frequency for the comparators, two extreme cases should be taken into account; when the source is too powerful such that after each clock cycle, VDDH rises above V_{OH} from V_{OL} (at steady state), and when the load is too demanding such that when the hysteretic switch turns ON, VDDH drops instantly below V_{OL}. In this design, the same clock frequency of the main MPPT FSM is used for the comparators.

5.5 MPPT and Source Degradation Tracing

The MPPT controller is an FSM synthesized with HVT transistors supplied by VDDL to reduce the dynamic and leakage power consumption. When the BFC becomes available, the input voltage is delivered to the low-voltage unit, including the MPPT FSM and its fixed-frequency clock generator. Following the first clock signal, a power-on-reset circuitry resets the FSM and all variables in the FSM are initialized. As shown in Fig. 5.10(a), the algorithm
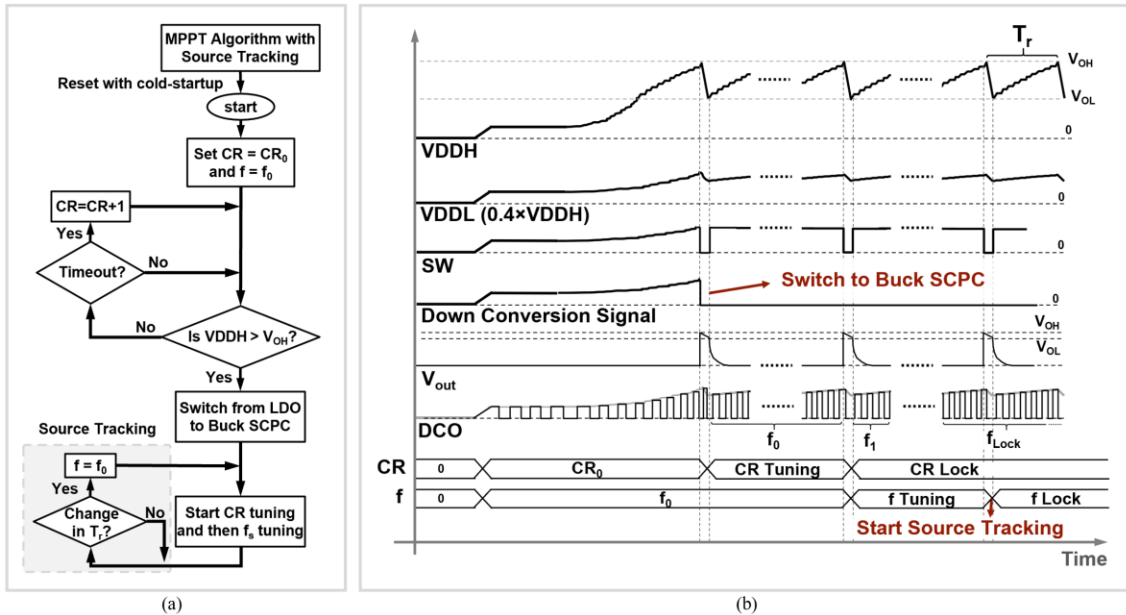
Fig 5.10: (a) Flow chart of the proposed MPPT algorithm with source degradation tracing capability. (b) Timing diagrams of the important nodes of the harvester system while MPPT is being performed.

initially assumes the pre-programmed conversion ratio of $CR_0=6$ and the lowest bit configuration (0000) for the DCO to prepare the SCPC to charge VDDH towards V_{OH}. Once VDDH approaches V_{OH} for the first time, the FSM switches the down conversion path from the LDO to the buck SCPC. If VDDH does not reach V_{OH} (if CR_0 is too high/low) a linear search for CR is performed until the first crossing occurs. The 2D MPPT then starts by minimizing the storage capacitor charging time from V_{OL} to V_{OH} (T_r) with a linear search for the optimum CR (coarse tuning) followed by the switching frequency (fine tuning). After finding the optimum CR and frequency the circuit goes into the "Source Tracing" state. In this state, CR and the frequency will remain locked and T_r is continuously monitored to detect

a noticeable change compared to the locked value ($T_{r, Lock}$). A dynamic threshold is introduced in the algorithm to always compare the latest T_r to $T_{r,Lock}/4$ (for detecting a 25% change). This threshold is set to ignore small changes in T_r which might be due to temperature fluctuations and/or other external perturbations. If a change is detected in T_r, which is presumably due to source degradation, the circuit will repeat the MPPT, starting from the latest locked CR and the minimum frequency. With this algorithm, any increase in the input power will also be detected (if more biofuel becomes available). In general, the number of clock cycles to lock to the new MPP depends on the locked conversion ratio (CR_{Lock}) and on how large the change is. In the case of BFCs, which degradation occurs gradually over a few minutes under heavy use, or several hours when occasionally used [23], the new CR would be either 1 step lower or higher than the locked CR. The new locked frequency could be different than the locked frequency by a maximum of 15 steps. This results in a worst case of 20 tuning cycles, including the change detection. The total time of the re-tuning also depends on the distance of V_{OL} and V_{OH}. For a 0.1V ripple target, it would take approximately 4ms for a worst-case scenario re-tuning, which is significantly shorter than the rate of BFC degradation.

Since VDDL is just the down-converted version of VDDH (at steady state), we would see a variation at VDDL with the amount of (V_{OH}-V_{OL})×0.4. As a result, the frequency of the DCO increases gradually as VDDL rises by approximately 60mV during each cycle. However, since T_r is compared to the locked $T_{r,Lock}$ by counting the clock cycles, rather than by measuring the actual time passed, this effect is cancelled out. In fact, the source power determines how many cycles (and not how much time) it takes for VDDH to rise from V_{OL} to V_{OH}.

5.6 Measurement Results

The energy harvester chip is fabricated in a 65nm CMOS process. The circuit performs cold startup and automatic MPPT with an input OC voltage of at least 0.39V and an average input power (P_{in}, defined as the maximum deliverable power) of 1.56μW, as shown in Fig. 5.11(a). Peak power efficiency of 86% is achieved with 220nW of internal power consumption.

   Three more experiments are shown in Fig. 5.11. In one case (Fig. 5.11(b)), the input voltage is first decreased from 0.6V to 0.5V to mimic a degradation in the BFC energy source while delivering power to an internal 60 kΩ test resistor. As shown in Fig. 5.11(b), the system first detects a change in the rise-time of VDDH. Then the CR value and the switching frequency are modified to find and lock onto the new MPP. The chip has responded and locked onto the new MPP after a total of 7 cycles, which has approximately taken 2ms to demonstrate almost instant adaptation to source degradation. The loading condition for this case is set to mimic power-demanding burst-mode-operated sensors. In another case in Fig. 5.11(c), the output power is comparable to the loading condition (1 MΩ external resistor). The input OC voltage is decreased to 0.25V after MPPT lock and the average input power is set to 2.25μW, while V_{out} settles to 1.01V. In the last case (Fig. 5.11(d)), a continuous mode operation for a capacitive load is demonstrated, in which the instantaneous P_{Load} is more than P_{out}. VDDH is still regulated while V_{out} remains above 0.9V.
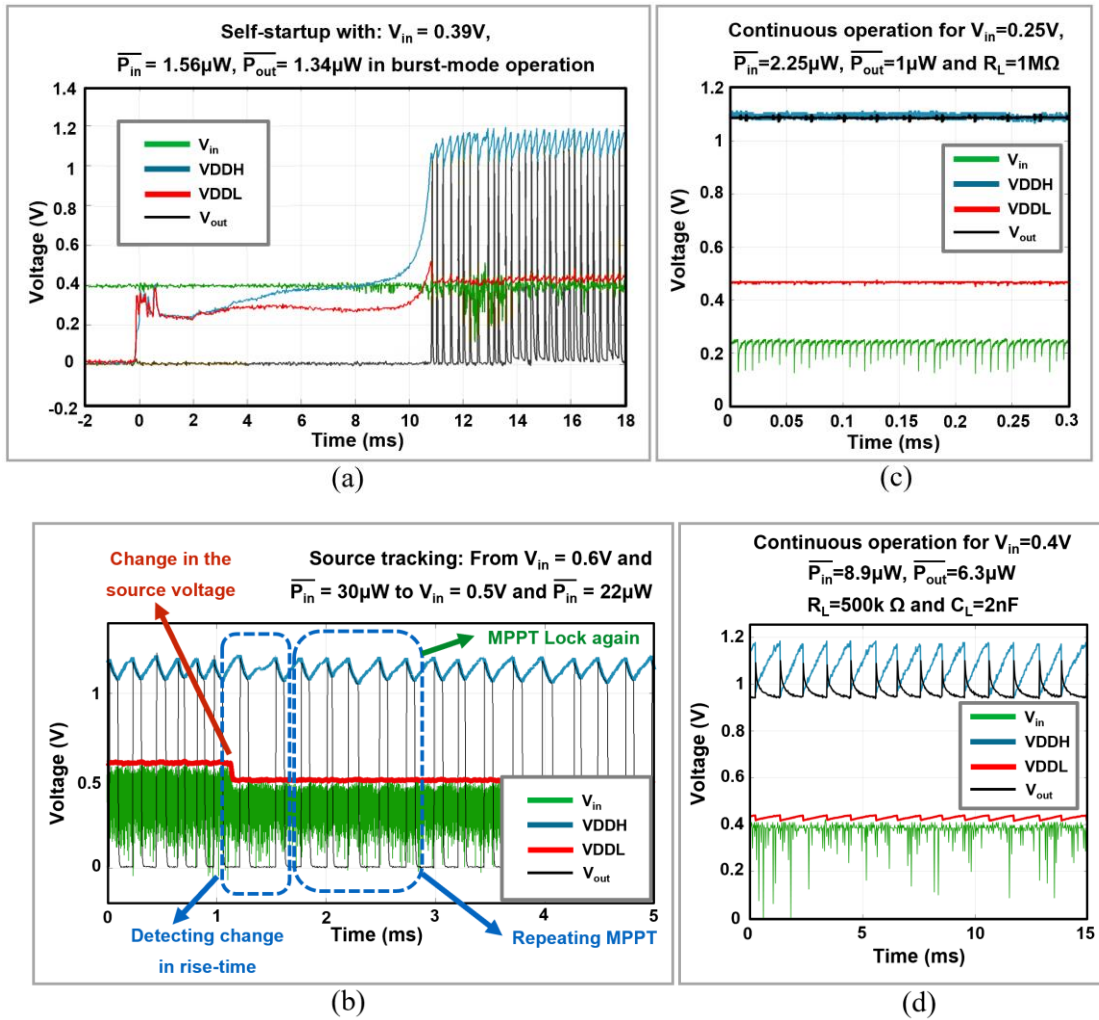
Fig 5.11: Measurement results: (a) cold startup in burst-mode sensing (b) source-adaptive MPPT; Continuous supply for V_{out} (c) when $P_{Load} > P_{out}$ and (d) when $P_{Load} < P_{out}$.

In Fig. 5.12, another test case is shown to demonstrated switching between power delivery modes. The system is initially locked at the MPP for an internal 60 kΩ test resistor with an input voltage of 0.4V and input power of 12μW. The load is then changed to an external 1 MΩ resistor. Since P_{out} becomes greater than P_{Load}, the power is continuously delivered to the load and the output voltage settles at 1.4V until the load is changed back to the internal test resistor.
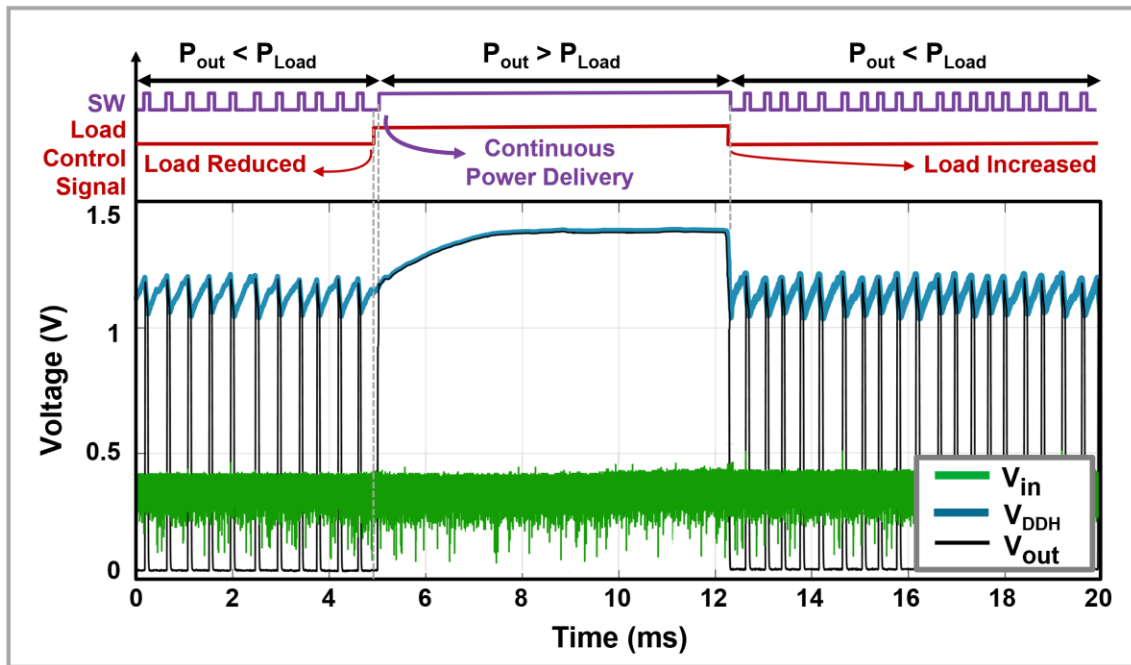
Fig 5.12: Measurement results: Transitions of different power delivery modes when load is changed over time ($P_{Load} > P_{out}$ to $P_{Load} < P_{out}$ and vice versa.

In an in-vitro experiment, a pair of biofuel-cells with a 2mm diameter, similar to [23] is used to extract energy in a 20mM lactate solution (Fig. 5.13(a)). The OC voltage is initially 0.56V with approximately 5.9µW of average input power. The circuit performs cold startup and locks at the MPP with 3.1µW of average power delivered to an internal 60 kΩ test resistor. The OC voltage degrades to 0.39V after 10 minutes and then to 0.25V after 30 minutes, while the chip continues its operation (Fig. 5.13(b-c)). After 30 minutes, the system stops operating since the input voltage decreases below 0.25V. In this case, the lifetime of the continuous operation could be improved by using a more concentrated solution or larger electrodes.
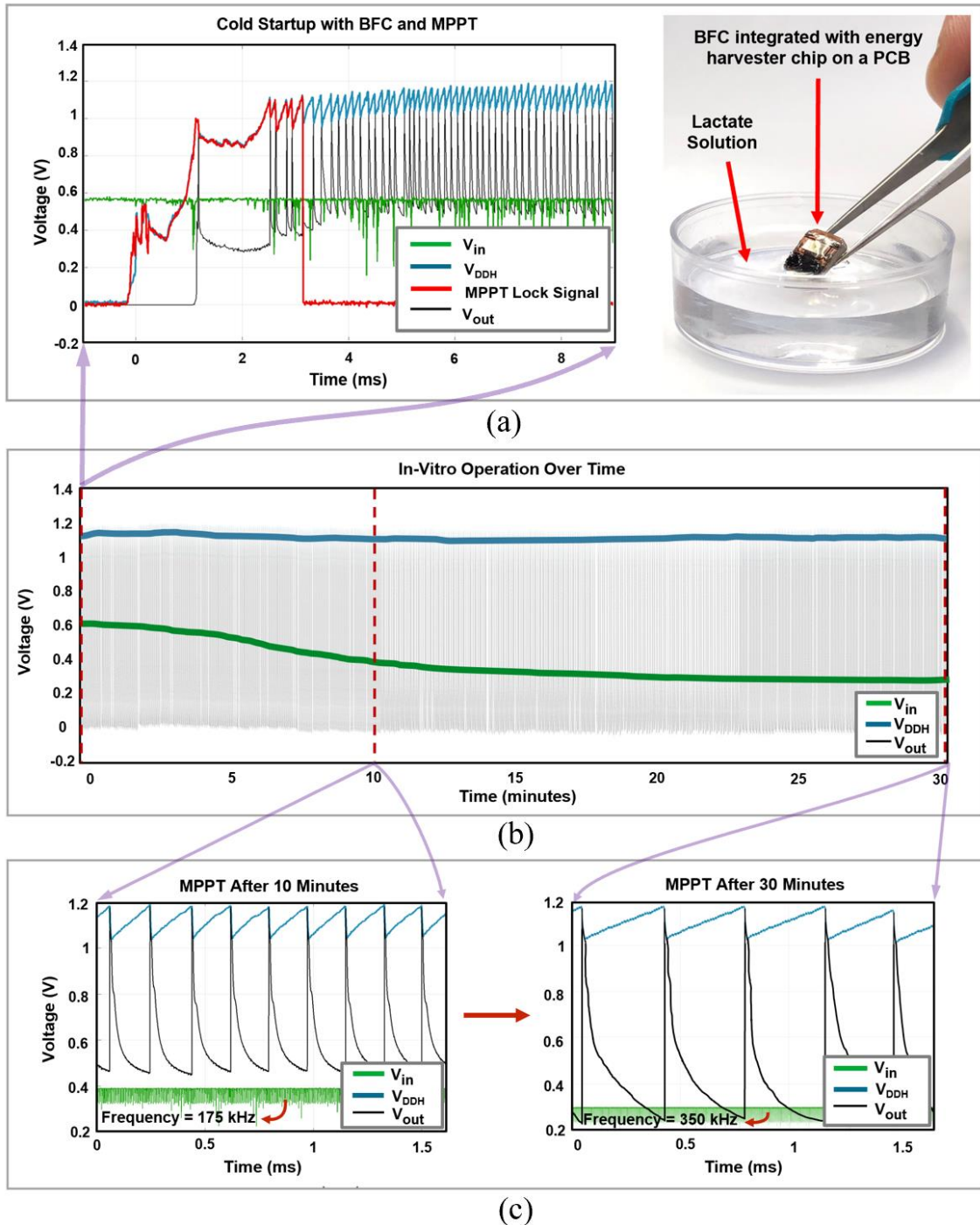
Fig 5.13: (a) In-vitro measurement test setup with lactate BFC, demonstrating cold startup and MPPT. (b) Harvesting operation with tracing the source OC voltage degradation from 0.56V to 0.25V over 30 minutes. (c) MPPT lock after 10 minutes and 30 minutes.

The die micrograph and the PCB are shown in Fig. 5.14. The chip and the wire-bonds are encapsulated with polydimethylsiloxane (PDMS) to avoid short circuit connections when dipped into the lactate solution. A power efficiency plot for a V_S of 0.3V and 0.39V at steady state is provided in Fig. 5.15(a). This plot shows a reliable operation over a wide range of output power. The end-to-end power efficiency is kept above 70% for loading powers from 1μW to 12μW, which verifies the compatibility of the energy harvester chip with BFC power levels. At higher average output power levels, a decrease in efficiency is observed, which is due to a transition to the continuous power delivery mode and an increase in VDDH (hence VDDL). This increase results in excessive internal power consumption and non-optimal overall efficiency. In Fig. 5.15(b), measured results for power efficiency versus various loading condition ratios are provided. The results show a flat efficiency response, which verifies that the performance is independent from loading conditions due to load regulation at higher loading ratios.
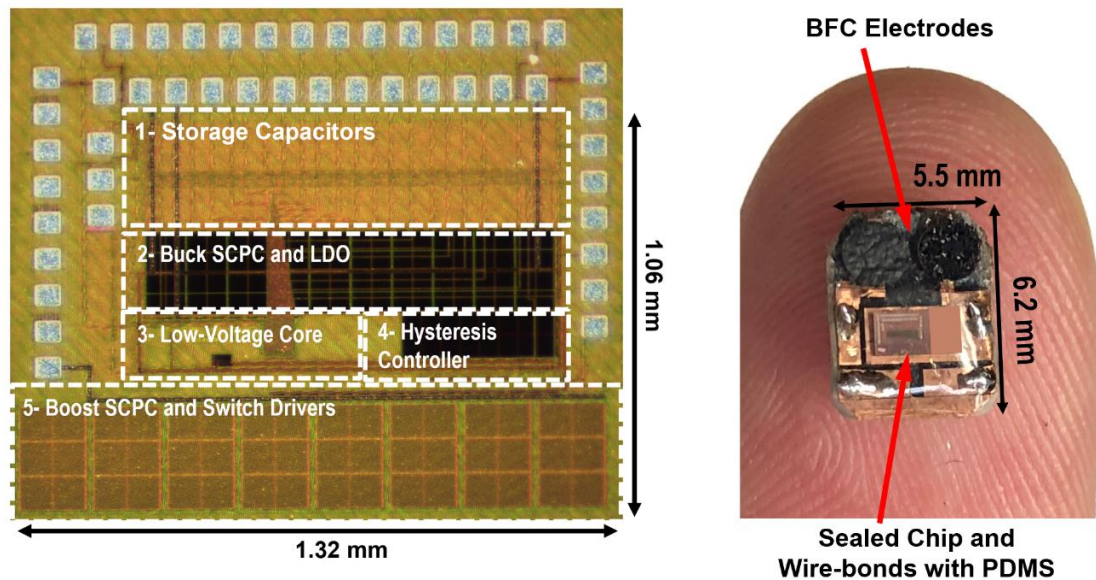
Fig 5.14: 65nm CMOS Chip Micrograph and the PCB with BFC and the chip.
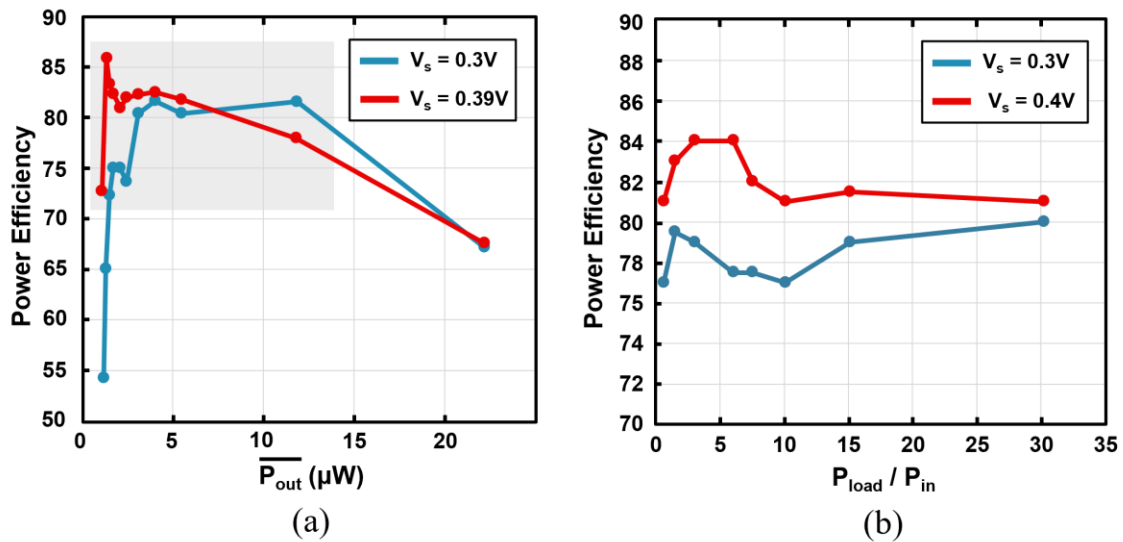
Fig 5.15: (a) Measured efficiency plots of the energy harvester. (b) Measured power efficiency versus loading condition ratio.

A power breakdown for the internal circuitry is provided in Fig. 5.16, for a 220nW total average power consumption at the peak efficiency. A major portion of the power is consumed by the level shifters, which in fact, indicates that the total power consumption would have increased significantly, if the internal voltage supply had not been down-converted. In fact, the total internal power consumption is estimated to increase by 68%, considering the power scaling of the low voltage core for both dynamic and leakage power.
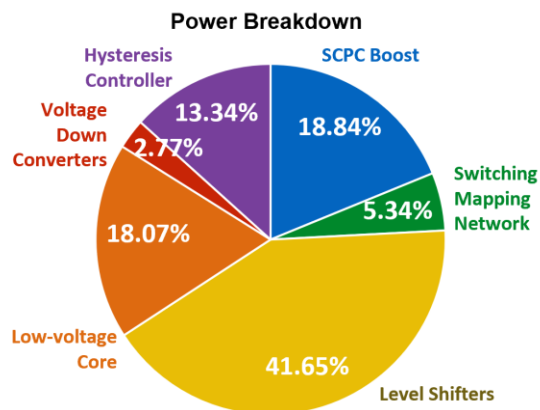
- Total internal power consumption at steady state: 220nW

- Estimated total power without voltage down-conversion: 370nW

- 68% improvement in internal power consumption

Fig 5.16: Simulated power breakdown of the internal circuitry.
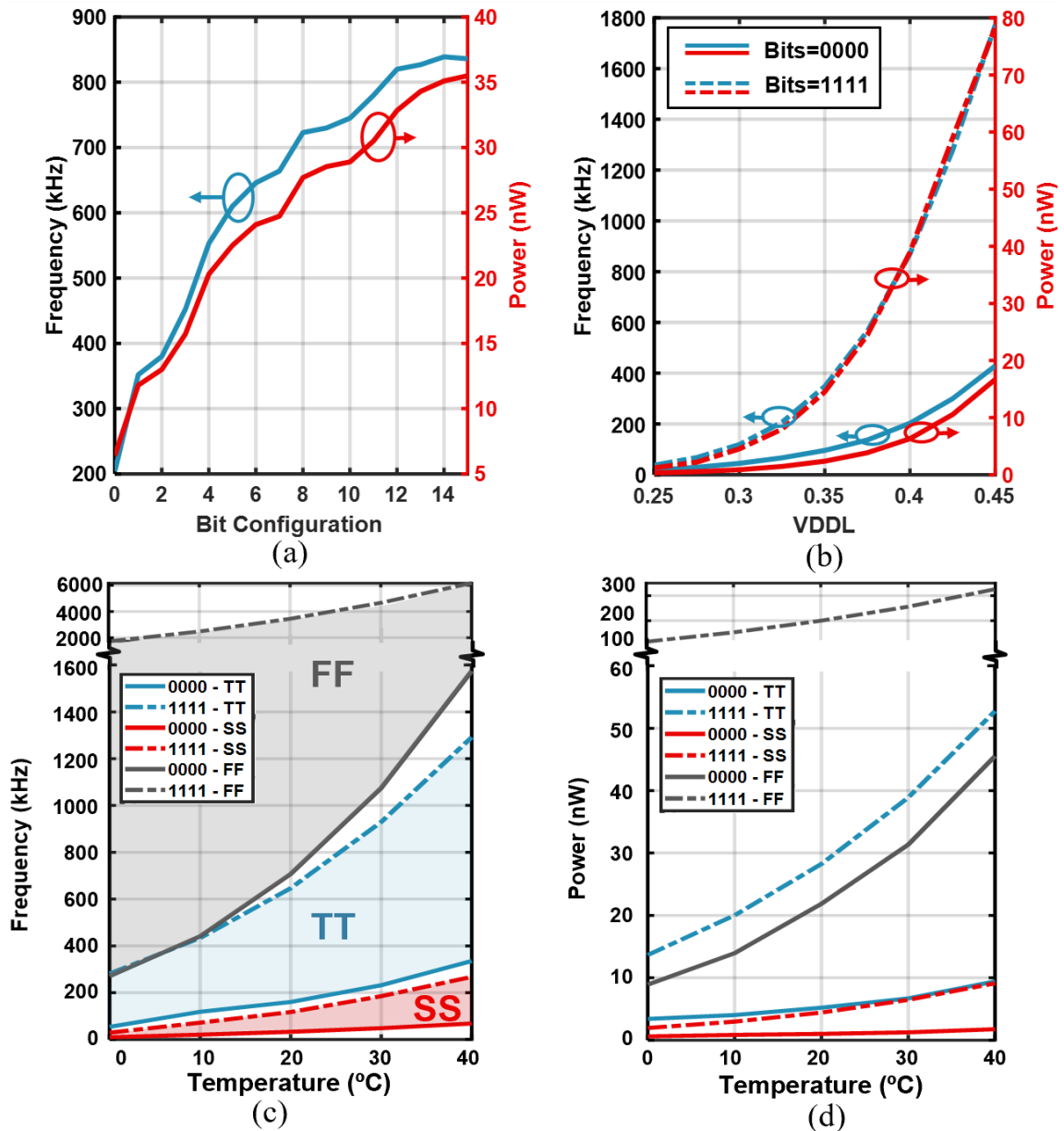
Fig 5.17: (a) Measured DCO frequency and power consumption versus configuration bits. (b) Simulated frequency and power consumption of the DCO versus supply voltage for the lowest and highest bit configurations. (c) Simulated process and temperature variations for DCO frequency at bit configurations of 0000 and 1111. (d) Simulated process and temperature variations for DCO power consumption at bit configurations of 0000 and 1111.

In Fig. 5.17(a), the measured frequencies and power consumptions of the DCO is provided at a 0.4V supply for all configuration bits. The frequency range is measured to be approximately 600kHz with highest at 836kHz while dissipating 35.5nW of power. In Fig. 5.17(b), simulated power consumption and frequency range of the DCO are provided when

the voltage supply (VDDL) is swept from 0.25V to 0.45V. The DCO stops oscillating at 0.25V with lowest configuration bits, which can be improved by making the leakage current paths stronger at the lowest bit configuration. Fig. 5.17(c) and Fig. 5.17(d) show process and temperature variation effects on the DCO frequency and power consumption at 0.4V supply. The shaded areas in Fig. 5.17(c) show the covered frequency ranges by the DCO at each process corner. For a more robust performance across process corners, the number of control bits could be extended to increase the overlap of the shaded areas. Furthermore, LVT transistors could be replaced with HVT with the trade-off of oscillation failure at lower supplies.

5.7 Conclusion

In this chapter we present an energy harvester chip that performs cold startup with a minimum input voltage of 0.39V utilizing a startup enhancement block. As the operation continues, the system can trace input voltage changes to as low as 0.25V. Table 5.1 shows the overall performance of the energy harvester system in comparison with the prior art. The energy harvester chip achieves a superior efficiency with less than 0.4V of input voltage and 5.5µW of average output power.

Table 5.1: Performance Summary and Comparison

	JSSC'18 [24]	VLSI'15 [25]	JSSC'15 [26]	JSSC'18 [27]	JSSC'16 [31]	JSSC'18 [32]	TCAS-I'18 [35]	This Work
Technology	65 nm	0.18 µm	0.18 µm	28 nm	0.18 µm	65 nm	0.18 µm	65 nm
Fully Integrated	External Cap	External Inductor	10 µH Inductor	10 µH Inductor	Yes	Yes	Yes	Yes
Source Type	BFC	Solar Cell	PV	PV / TEG / BFC / Battery	TEG / PV	TEG / PV	PV	BFC
Topology	Duty-cycled	Inductive Buck/Boost	Inductive Buck/Boost	Inductive Buck/Boost	Boost SCPC	Boost SCPC	Boost SCPC	Boost + Buck SCPC
MPPT	Matched resisor	Manual	Yes	2D	2D	3D	2D	2D
Output Voltage (V)	0.3	1	1V, 1.8V and 3V	0.4 - 1.4	3.3	1	1.2 - 1.8	0.9 – 1.5
Input Voltage Range (V)	0.3 - 0.5	0.14 – 0.62	1	0.2 – 0.5	0.45 - 3	0.35 - 1	0.5 - 1.8	0.25 - 1
Min Cold startup (V)	0.3	0.33	No cold startup	Yes	2.1	0.35	0.72	0.39
Frequency Range	100 Hz	N/A	10 kHz	< 500 kHz	27 kHz – 1 MHz	19 kHz – 16 MHz	25 kHz – 1 MHz	100 kHz – 2 MHz
Throughput Power (µW)	400 – 800	10nW - 1µW	1mW – 10mW	1µW – 60mW	< 50	0.1 – 300	5.9 – 35.1	1 – 100
Peak Efficiency	N/A	84% @ 0.62V and P_{in}=1µW	83% @ 100µW	89% @ 20mW	81% @ 1.2V and 16µW	88% @ 0.85V and 200µA	72% @ 1.2V and 35µW	86% @ 0.39V and 1.34µW
Efficiency at BFC-level source power				76% @ 1µW	42% @ 0.6V and 1µW	70% @ 0.5V and 5µA	66% @ 0.9V and 6µW	80.4% @ 0.4V and 5.5µW
Chip Active area (mm²)	0.58*	9	4.62	0.5	2.89*	0.54	0.55	1.4

* Estimated from provided figures

C h a p t e r   6

CONCLUSION

Optical interconnects continue to pave the way towards an ever-increasing connected future. The growing demand in computation power and data traffic, as well as necessity for interconnectivity among users and data centers, requires improvement in the energy efficiency of high-speed interconnects. That is, it is of great value and significance to achieve higher data bandwidths with a constant power budget. A holistic design approach is key to tackle limitations of both electrical and optical domains and to design entirely new architectures and bring the performance of current systems to unprecedented levels. In this dissertation, efforts leading to energy efficient high-speed transmitters and interconnects are presented.

In the first part, a silicon photonic PAM-4 transmitter with two uneven-length SiGe EAMs in parallel within an unbalanced MZI structure is demonstrated. The fabricated chip performs PAM-4 transmission at 100 Gb/s with 5.5dB ER and 2.4dB of TDECQ. This scheme can similarly be applied to design 100 Gb/s PAM-4 Si-photonic transmitters in the O-band using hybrid-integrated InP-based EAMs with < 1pJ/bit power consumption as well to provide a path to 200 Gb/s/λ transmitters. We also demonstrated a silicon photonic QAM-16 transmitter with 4 SiGe EAMs in parallel within an unbalanced MZI structure. The fabricated chip performs QAM-16 transmission at 200 Gb/s with $3\times10-4$ and 2.8×104 of BER at an OSNR level of 35 dB for square and hexagonal constellations. This scheme can similarly be applied to design 200 Gb/s QAM-16 Si-photonic transmitters in the O-band using hybrid-integrated InP-based EAMs with < 1pJ/bit power consumption to provide a path to 400 Gb/s/λ transmitters.

In the second part, a 3D-integrated 100Gb/s PAM-4 OTX was presented, which achieves 2.5× better EIC energy efficiency and 3.6× overall performance improvement, compared to the state-of-the-art co-integrated optical PAM4 transmitters operating at or above 100Gb/s.

This efficiency was achieved by keeping the output swing of the driver below $1.2V_{ppd}$ while delivering optimal optical performance. Electronic pre-distortion and BW extension techniques were implemented to compensate for MOSCAP modulator BW limitations. Trade-offs of MOSCAP modulator parameters were studied and used for co-designing the electro-optical interface for optimal EOBW, power consumption and optical efficiency. The proposed tightly-integrated SiPh-CMOS OTX demonstrates the potential of compact MOSCAP modulators co-optimized with CMOS drivers, to provide a path for the future $100+Gb/s/\lambda$ SiPh transmitters. While this work was focused on optical PAM4 transmission, the system can be scaled up for higher-order coherent modulation schemes, such as quadrature phase shift keying (QPSK) and N-level quadrature amplitude modulation (QAM-N). Moreover, a simulated optical performance shows the potentials of this structure when used in O-band.

In the final part of this dissertation, the holistic design approach was studied in the field of energy harvesting and biomedical sensing. We presented an energy harvester chip that performs cold startup with a minimum input voltage of 0.39V utilizing a startup enhancement block. As the operation continues, the system can trace input voltage changes to as low as 0.25V. The overall performance of the energy harvester system in comparison with the prior art shows a superior efficiency with less than 0.4V of input voltage and 5.5μW of average output power. This performance improvement was enabled by a holistic design of the energy harvesting system, considering the electrical characteristics of the bio-fuel cell electrodes. The compatibility of this harvester system with low-power integrated biomarker sensors, could potentially pave a path towards battery-less wearable/implantable sensors with continuous biomarkers monitoring capability.

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