Ultra-High Density Scanning Electrical Probe Phase-change Memory for Archival Storage

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1. Introduction

Digital archiving is becoming increasingly important and the total archival capacity required world-wide will exceed 3800 ExaBytes by 2013 [1]. The conventional forms of storage technologies like magnetic hard disks, optical storage disks, and flash storage suffer from the super paramagnetic limit, optical diffraction limit and device scaling limits respectively. A new candidate, the scanning probe-based phase change memory which has the potential of ultra-high capacity, non-volatility, low power consumption, low cost and write-once/rewritable capabilities, could be suitable for archival and back-up storage markets. Therefore, various research groups worldwide have been putting their efforts into developing scanning probe phase-change memories and have successfully demonstrated the potential of this approach experimentally and using simulations [2, 3]. In our work, we investigate the recording and readout performance of such phase-change memories and demonstrate experimental and simulation results which are based on a particular medium stack (Si/TiN/DLC/GST/DLC). The recording is achieved by injecting electrical current from a conductive tip to the storage medium to cause phase transformation through Joule heating, while readout is realised by sensing the current variation due to the significant differences in the electrical resistivity between the amorphous and crystalline phases. The experimental results clearly show that a crystalline bit with approximately 30nm diameter can be produced and readback, in good agreement with the corresponding simulations of the write/read processes.

2. Experimental setup

The medium stack used in our experiments comprises a 10nm $Ge_2Sb_2Te_5$ (GST) layer sandwiched between 4nm diamond-like-carbon (DLC) capping layer and a 10nm DLC underlayer, which was deposited on a 10nm TiN bottom electrode on the top of a Si substrate. For the conductive mode AFM (C-AFM) experiments, a nanoscale PtSi conductive tip with a diameter of around 30nm, which was fabricated by IBM [4], was used instead of the commercially available conductive tips because of the good wear characteristics of the PtSi tip. Figure 1 shows the schematic of the experimental and simulation setup.

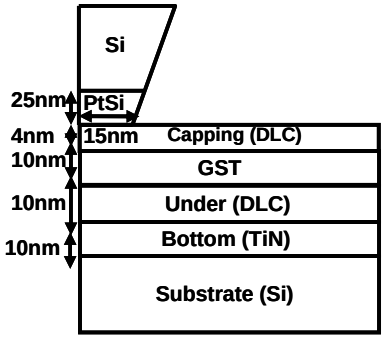

Fig. 1. Schematic of the probe storage system

The writing experiment was performed by applying a 3V pulse of 1.1μs width into an initially amorphous GST layer, through the PtSi tip, to generate a crystalline mark. The resulting crystalline mark was detected through a current scan, with a readout potential of 1V and is shown in Fig. 2.

3. Results & discussion

The current images in Figure 2(a) clearly reveal that a crystalline mark, with a diameter of approximately 30nm was written after the application of the voltage pulse, demonstrating the potential of storage density of 1Tbit/inch^2. Figure 2(b) shows a line scan through centre of marks, showing a high reading contrast (defined by I_{max}/I_{min}) value of 12. The writing power and energy consumption were around 0.036mW and 0.04nJ respectively, which are much lower than previous reported values [2].

In order to understand the physical processes involved in the use of phase change materials for electrical data storage applications, and to design and optimize future devices, we have also developed a comprehensive (pseudo-3D) theoretical model for electrical, thermal and phase-change processes involved in writing and reading data by simultaneously solving Laplace equation, the heat conduction equation and the JMAK (Johnson-Mehl-Avrami-Kolmogorov) equation [3]. It is therefore instructive to compare the experimental data presented above with the simulation results in order to verify the physical reality of our

phase-change model. Figure 3(a) and (b) shows the simulated mark shape and the readout signal under the same conditions as the experiment.

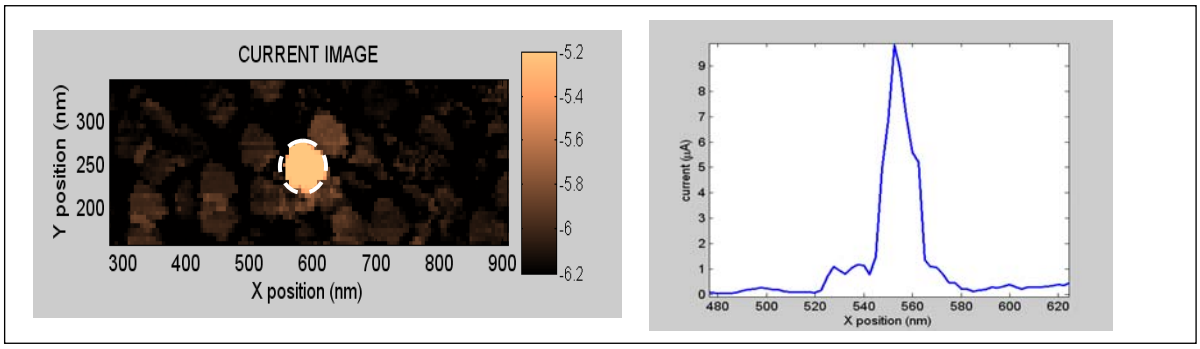

Fig. 2. (a) Experimental current image (b) Experimental readout signal

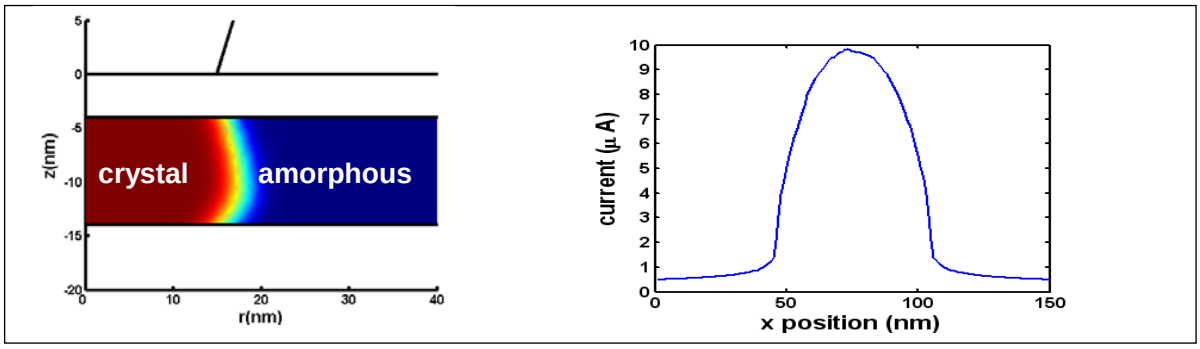

Fig. 3. (a) Simulated mark shape (b) Simulated readout signal

As shown in Figure 3(a), the diameter of the simulated mark size was around 30nm with power and energy consumption of 0.05mW and 0.06nJ, respectively, fitting the experimental data very well. Moreover, the calculated reading contrast of 20, which is also in good agreement with the observed experimental ones. The granularity and changes in electrical conductivity in the carbon capping layer, in addition to surface roughness effects and hence non-uniform tip-medium contact may contribute to the narrow pulse width of the experimental readout current compared to the simulated one. In the work presented here, we do not consider surface roughness and contact resistance in the simulations of Fig. 3.

4. Conclusions

The recording and readout performances of scanning probe phase-change memory based on a particular medium stack (Si/TiN/DLC/GST/DLC) has been investigated using both experimental and theoretical methods. Both methods reveal that a minimal crystalline mark size of 30nm can be produced after a 3V pulse of 1.1μs duration, demonstrating the capability of this technique in achieving 1Tbit/inch^2 areal density and 1Mbit/s/tip data rate.

Acknowledgement

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References

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