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REALIZATION

OF FULLY DISTRIBUTED RC NETWORKS

USING THICK FILM TECHNOLOGY

A thesis submitted by

Mahnoosh MOTAMEDI-AZARI, BSc

in partial fulfilment of the requirements

for the degree of

Master of Philosophy

of the Council for National Academic Awards

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In the Name of GOD, the Beneficent, the Merciful

Praise be to Almighty ALLAH Whose Help sufficed for me to complete this work.

I dedicate this work to the memory of the martyrs of the Path of ALLAH who have watered the tree of the Islamic Revolution with their innocent blood: what little dedication for such splendid self-sacrifice.

ABSTRACT

The problems associated with the fabrication of Fully Distributed RC (FDRC) networks using thick film techniques have been discussed. Also, a comprehensive investigation into the fabrication of fully distributed RC networks has been carried out in which a series of resistor - dielectric ink combinations were examined for compatibility. The investigations resulted in the successful fabrication of thick film FDRC devices.

It must be mentioned, however, that the conventional methods of trimming could not be used in view of the fact that the first resistor layer of the FDRC network is completely covered with a layer of dielectric and that the physical shape and size of the distributed network should not be changed by trimming. The high voltage pulse trimming technique was therefore examined in detail since it neither required accessibility to the surface of the resistor nor did it change the physical shape of the resistors. A suitable electronic circuit was designed for this purpose and was used to adjust the values of several fully distributed RC components.

The manufactured thick film FDRC devices was examined in various electronic networks such as multivibrators, phase shift oscillators and active filters with successful results.

ACKNOWLEDGEMENTS

Compiling of a list of the people who have contributed to the completion of my research would be virtually an endless task. However, I must express my great depth of gratitude to Mr. D J Daruvala from whom I received continuous help throughout my research.

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CHAPTER 1

INTRODUCTION

After more than a decade of successful application throughout the electronics industry, thick films have proven themselves to be useful general purpose devices. More recently, they have been increasingly used in precision applications which in the past often required discrete or thin film networks. These networks are now realized by utilizing high density precision thick film network modules.

Thick film technology offers many potential advantages over vacuum evaporation thin film technology. For resistor elements, a large range of sheet resistances from 10Ω/sq to 10MΩ/sq is easily attainable. A second possible advantage is resistance to thermal and environmental degradation. The high firing temperature of thick film circuitry (850°C-900°C) should result in structures resistant to degradation at ambient as well as slightly elevated temperatures. Also, the high firing temperatures should result in dense materials that are resistant to penetration and degradation by contaminants. The use of thick film networks for precision applications offers the prospects of lower cost, smaller size and higher reliability with comparable, if not superior, performance to most traditional approaches.

Interest in thin film technology for microcircuits has largely given way to 'thick film' techniques using screened glazes. Over the

past decade, thick film technology has developed rapidly from its original concept of simple resistor conductor networks. Many of the more complex circuits now being manufactured in hybrid form have generated a necessity for fabrication capability of crossovers as well as multilayer structures. Many circuits are sophisticated multilayer structures containing several conductor and dielectric layers. To obtain high yields during the production of these multilayers, careful selection of materials and attention to process techniques is required.

It is a matter of no great difficulty to form two layer circuits of some complexity using commercially available materials. Greater number of layers may be formed but at an increasing cost. The difficulties that arise in moving beyond two levels are centred on the number of screen printing processes involved. The multilayer pattern requires more steps in manufacturing and, therefore, compatibility must be maintained throughout the several firing stages involved.

Most multilayer structures do not employ resistors or, if they do, these are frequently printed onto the ceramic substrates rather than over a prefired thick film dielectric or insulating layer. In microelectronics, the tendency is to develop a component and a circuit to fulfil a task which would have earlier needed several components. The recent trend of crowding more circuitry into limited space on thick film substrates caused a number of workers to try to develop multilayer resistor - dielectric circuits. A viable method of printing resistors onto a fired layer with a minimum change in properties from those on alumina would simplify some of the design problems of such a multilayer system. One example of this multilayer structure is the distributed RC network (DRCN), which is made by

forming the conductive, dielectric and resistive layers on top of each other.

A DRCN can replace two to three resistors when used in active or passive filters. This results in a saving on space, a reduction in the number of interconnections and an increase in reliability and further means that the circuit is less sensitive to changes in the value of the active and passive elements. For this reason simpler active components can be used [1].

The concept of a "DISTRIBUTED NETWORK" has been known since early 1956, when Smith and Cooper made distributed components on printed circuits [2]. Further development using vacuum deposition of thin film conductive, resistive and dielectric materials on supporting substrates were made by Hager in 1959 [3]. Later, in 1960, Kaufman developed a semiconductor monolithic distributed notch filter [4]. The use of thick films for the fabrication of DRC networks was first suggested by Pitt in 1975 [5]. Subsequent development in this field has been due to advances in thick film materials and techniques.

The aim of this research is to construct a distributed network consisting of resistor- dielectric- resistor layers on a thick film substrate to be used as a notch filter. This structure has been called an R-C-NR network by some workers who have analysed the structure. However, it is referred to as a Fully Distributed RC (FDRC) network in this research.

In Chapter 2 of this work, the indefinite admittance matrix of an FDRC network is developed and a method for measurement of the capacitance of FDRC structures is outlined.

Chapter 3 reviews some of the important advances in thick film materials for resistors, dielectrics and their printing vehicles.

Chapter 4 presents an introduction to the Fully Distributed RC network (FDRC). It then proceeds to give a full account of the problems encountered in fabricating an FDRC structure on a thick film substrate. Finally, it provides some solutions to the problems and concludes with a discussion of the several investigations which were carried out into the fabrication of the FDRC structures using thick film techniques.

Chapter 5 of the work considers some methods of trimming the resistors in the FDRC structure, giving the advantages and shortcomings of the various techniques. It then presents the most appropriate method for trimming the FDRC structure. In section 5.5.4 the full design procedure for the trimmer is given. The trimming results and conclusions are presented at the end of the chapter.

Chapter 6 shows some of the applications of the FDRC networks fabricated in this research. It outlines the necessary design formulae for each application and provides computer plotted frequency responses of the FDRC notch filter for different values of N. A comparison is made between the measured frequency responses and the computer plotted ones of three of the networks fabricated in this research. Finally, conclusions are drawn and suggestions for further research are given.

CHAPTER 2

THE FDRC NETWORK ANALYSIS

2.1 INTRODUCTION

The fully distributed RC network was first proposed by Castro and Happ in 1960[6]. Their approach towards the FDRC network was to develop an indefinite admittance matrix (IAM) describing the FDRC network. The FDRC forms a building block for further types of distributed network. In the past most of the work has been concerned with either single resistive, or multilayer DRC.

There are many advantages to be realized in deriving the IAM of a distributed network, as the formulation of the IAM allows a systematic derivation of the network functions of all possible one-ports and two ports obtainable from this basic network. This type of derivation has been discussed by Castro and Happ[6], Castro, Nichols and Kaisel[7], and Kavanough[8]; the theoretical work in this chapter is attributed principally to the sources just mentioned. The advantages of using the IAM become apparent when undertaking computer aided analysis of networks. The physical view of an FDRC is shown in Fig.(2.1) and an incremental section of the RC line is shown in Fig.(2.2).

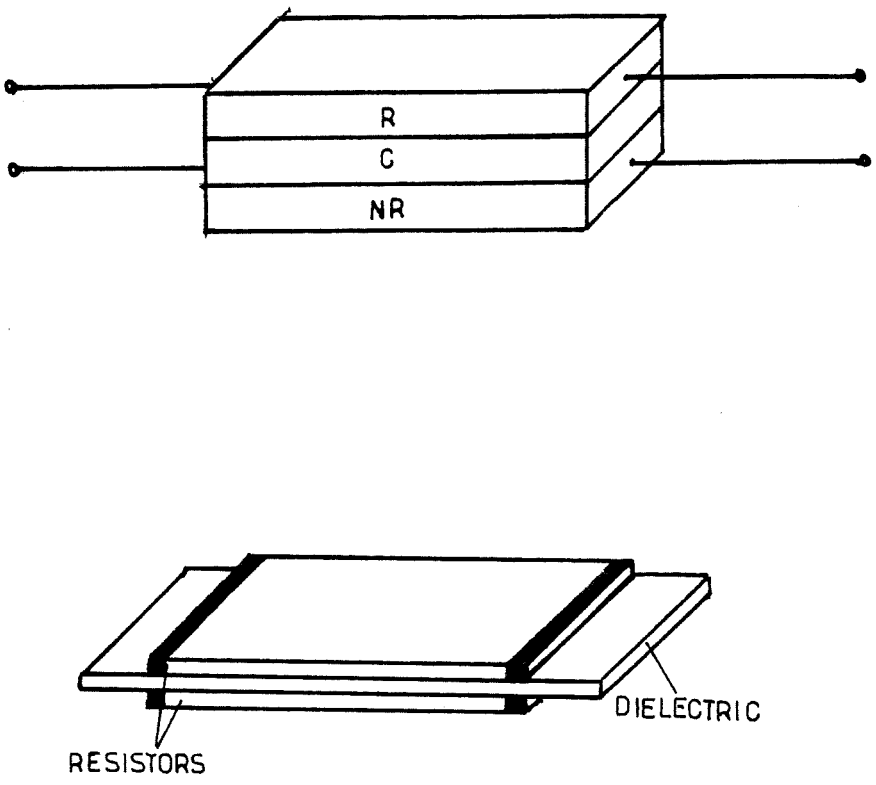


Fig.(2.1) A physical view of an FDRC structure.

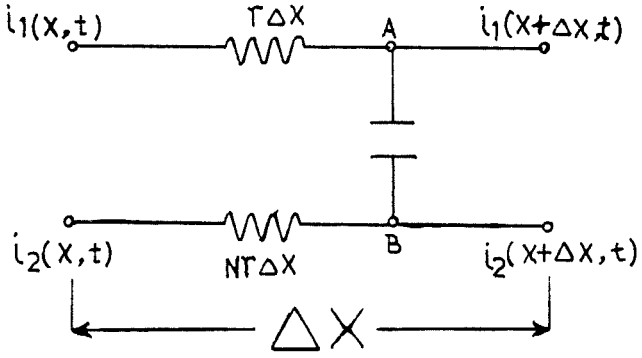


Fig.(2.2) An incremental section of the FDRC structure.

For the network shown in Fig.(2.2), the Kirchhoff's voltage law can be written as follows:

$$V(x,t) = r\Delta x\ i_1(x,t) + V(x+\Delta x,t) - Nr\ \Delta x\ i_2(x,t)$$

$$V(x,t) - V(x+\Delta x,t) = r\, i_1(x,t)\ \Delta x - Nr\, i_2(x,t)\ \Delta x \qquad 2.1$$

dividing both sides of equation 2.1 by Δx and taking the limit as $\Delta x \longrightarrow 0$,

$$\frac{V(x,t) - V(x+\Delta x,t)}{\Delta x} = r\, i_1(x,t) - Nr\, i_2(x,t) \qquad 2.2$$

$$\frac{\partial V(x,t)}{\Delta x} = Nr\ i_2(x,t) - r\, i_1(x,t) \qquad 2.3$$

Using Kirchhoff's current law at nodes A and B,

At A $$i_1(x,t) = c\ \Delta x\ \frac{dV(x+\Delta x,t)}{dt} + i_1(x+\Delta x,t) \qquad 2.4$$

At B $$i_2(x,t) = -c\ \Delta x\ \frac{dV(x+\Delta x,t)}{dt} + i_2(x+\Delta x,t) \qquad 2.5$$

From equation 2.4

$$i_1(x+\Delta x,t) - i_1(x,t) = -j\omega c\ \Delta x \cdot V(x+\Delta x,t)$$

dividing both sides by Δx and taking the limit as $\Delta x \longrightarrow 0$

$$\frac{di_1(x,t)}{dt} = -j\,\omega c\ V(x+\Delta x,t) \qquad 2.6$$

similarly equation 2.5 can be written as

$$i_2(x+\Delta x, t) - i_2(x,t) = \Delta x \, j\omega c \, V(x+\Delta x, t)$$

dividing both sides by Δx we get

$$\frac{i_2(x+\Delta x, t) - i_2(x,t)}{\Delta x} = j\omega c \, V(x+\Delta x, t)$$

and taking the limit as $\Delta x \longrightarrow 0$

$$\frac{di_2(x,t)}{dx} = j\omega c \, V(x+\Delta x, t) \qquad 2.7$$

from equation 2.6 and 2.7

$$\frac{di_1(x,t)}{dx} = -\frac{di_2(x,t)}{dx} = -j\omega c \, V(x+\Delta x, t) \qquad 2.8$$

Integrating with respect to x both sides of equation 2.8,

$$i_1(x,t) = -i_2(x,t) + f(x) \qquad 2.9$$

From equations 2.3 and 2.9

$$\frac{dV(x,t)}{dt} = Nr\, i_2(x,t) - r[-i_2(x,t) + f(x)]$$

$$\frac{dV(x,t)}{dt} = i_2(x,t)(Nr+r) - r f(x)$$

$$\frac{d^2V(x,t)}{\Delta x^2} = \frac{di_2(x,t)}{dx}(Nr+r)$$

$$\frac{d^2V(x,t)}{dx^2} = j\omega c \, V(x,t)\, r(N+1) \qquad 2.10$$

It should be noted that the above equations 2.6, 2.7 and 2.10 are diffusion equations, so that the voltage and current diffuse into the structure from the input terminals.

The solutions for equations 2.10 and 2.6 and 2.7 are subject to boundary conditions. Their solutions are respectively as follows:

$$V(x,t) = Ae^{\alpha x} + Be^{-\alpha x} \qquad 2.11$$

$$i_1(x,t) = -\frac{j\omega c}{\alpha}\left(Ae^{\alpha x} - Be^{-\alpha x}\right) + D_1 \qquad 2.12$$

$$i_2(x,t) = \frac{j\omega c}{\alpha}\left(Ae^{\alpha x} - Be^{-\alpha x}\right) + D_2 \qquad 2.13$$

Where A, B, D_1 and D_2 are arbitrary constants and

$$\alpha = \sqrt{j\omega c r(1+N)}$$

The equivalent circuit to the FDRC network (ie the FDRC network) is shown in Fig.(2.3).

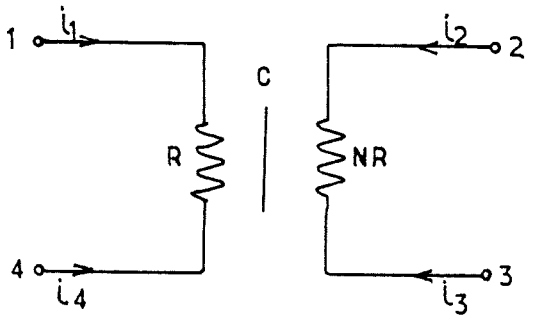


Fig.(2.3) Equivalent circuit to FDRC network.

Imposing the boundary conditions x=0 and x=L (where L is the physical length of the structure) gives the voltages at each end and the currents at each terminal. The currents are:

$$i_1 = i_1(o,t) \qquad 2.14a$$

$$i_2 = i_2(o,t) \qquad 2.14b$$

$$i_3 = i_3(L,t) \qquad 2.14c$$

$$i_4 = i_4(L,t) \qquad 2.14d$$

and the voltages are:

$$V_{(o,t)} = V_1 - V_2 = V_{12} \qquad 2.15a$$

$$V_{(L,t)} = V_4 - V_3 = V_{43} \qquad 2.15b$$

$$V_{14} = \int_o^L i_1(x,t)\, dx = V_1 - V_4 \qquad 2.15c$$

$$V_{23} = \int_o^L i_2(x,t)\, N\Gamma\, dx = V_2 - V_3 \qquad 2.15d$$

Using the relationship of the terminal currents of equations 2.14 and terminal voltages of equations 2.15 to evaluate the arbitrary constants in terms of voltages and currents applied to the basic network, shown in Fig.(2.4) leads to:

$$V_{dc} = A + B \qquad 2.16$$

$$V_{ab} = A e^{\sigma} + B e^{-\sigma} \qquad 2.17$$

$$V_{ad} = \frac{1}{1+N}\left[A(e^{\sigma} - 1) + B(e^{-\sigma} - 1)\right] + G \qquad 2.18$$

$$V_{bc} = \frac{1}{1+N}\left[A(-e^{\sigma} + 1) + B(1 - e^{-\sigma})\right] + G \qquad 2.19$$

where G is an arbitrary constant and

$$\theta = \alpha L = \sqrt{j\omega(1+N)RC}$$

and where L is the total length of the film structure, and R = rL and NR = NrL are the resistances of the two resistive films respectively, and C = cL is the total capacitance between resistive films.

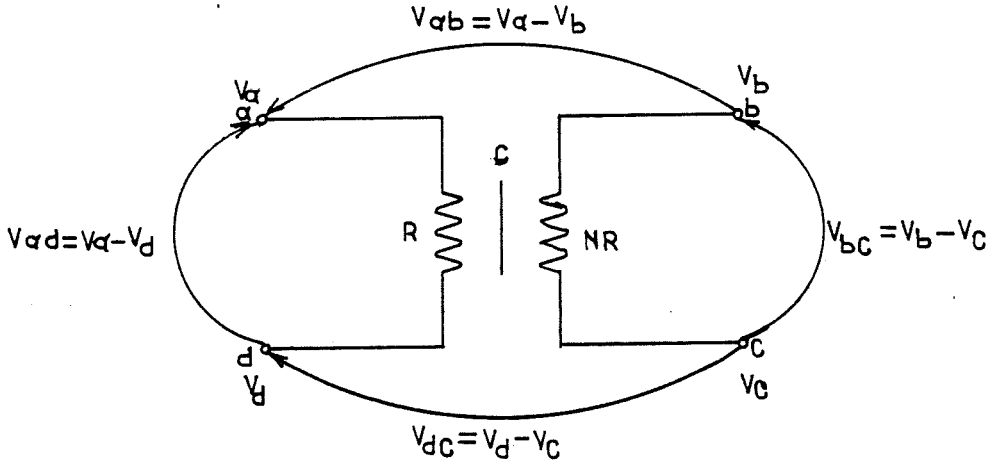


Fig.(2.4) FDRC network equivalent circuit with voltages indicated.

The terminal currents are given by

$$I_a = \frac{\theta}{(1+N)R}\left(A e^{\theta} - B e^{-\theta}\right) + \frac{G}{R} \qquad 2.20$$

$$I_b = \frac{-\theta}{(1+N)R}\left(A e^{\theta} - B e^{-\theta}\right) + \frac{G}{NR} \qquad 2.21$$

$$I_c = \frac{\theta}{(1+N)R}\left(A - B\right) - \frac{G}{NR} \qquad 2.22$$

$$I_d = -\frac{\theta}{(1+N)R}\left(A - B\right) - \frac{G}{R} \qquad 2.23$$

Equations 2.16 to 2.23 give the general solution for the basic 4-terminal network in terms of the constants A, B and G. If the network is to be specialized further, for example, by connecting a driving generator across a given pair of terminals and connecting or floating other terminals, these constants can be evaluated in terms of the driving generator for each configuration.

Alternatively, the constants A, B and G can be eliminated once and for all and the terminal currents given in terms of the terminal voltages. Let us find A and B in terms of the terminal voltages.

Assuming $Y = \exp(-\theta) - 1$

and $X = \exp(\theta) - 1$

the equations 2.17, 2.18 and 2.19 may be written as follows:

$$V_{ab} = A(X+1) + B(Y+1) \qquad 2.17a$$

$$V_{bc} = \frac{1}{1+N}(AX + BY) + G \qquad 2.18a$$

$$V_{bc} = -\frac{N}{1+N}(AX + BY) + G \qquad 2.19a$$

Substituting for A from equation 2.16 into 2.17a

$$V_{ab} - V_{dc}(X+1) = B(Y+1) - B(X+1)$$

therefore

$$B = \frac{V_{ab} - V_{dc}(X+1)}{Y - X}$$

$$B = \frac{V_{ab} - V_{dc}e^{\theta}}{e^{-\theta} - e^{\theta}} \qquad 2.24$$

substituting for B in equation 2.16

$$A = \frac{V_{dc}\, e^{-\sigma} - V_{ab}}{e^{-\sigma} - e^{\sigma}} \qquad 2.25$$

from equation 2.24

$$B e^{-\sigma} = \frac{V_{ab}\, e^{-\sigma} - V_{dc}}{e^{-\sigma} - e^{\sigma}} \qquad 2.24a$$

from equation 2.25

$$A e^{\sigma} = \frac{V_{dc} - V_{ab}\, e^{\sigma}}{e^{-\sigma} - e^{\sigma}} \qquad 2.25a$$

from equations 2.24a and 2.25a

$$A e^{\sigma} - B e^{-\sigma} = \frac{V_{dc} - V_{ab}\, e^{\sigma}}{e^{\sigma} - e^{-\sigma}} - \frac{V_{ab}\, e^{-\sigma} - V_{dc}}{e^{-\sigma} - e^{\sigma}}$$

$$= \frac{V_{dc} - V_{ab}\, e^{\sigma} - V_{ab}\, e^{-\sigma} + V_{dc}}{e^{-\sigma} - e^{\sigma}}$$

$$= \frac{2V_{dc}}{e^{-\sigma} - e^{\sigma}} - V_{ab}\, \frac{e^{\sigma} + e^{-\sigma}}{e^{-\sigma} - e^{\sigma}}$$

$$= \frac{-V_{dc}}{\sinh \sigma} + \frac{V_{ab}}{\tanh \sigma} \qquad 2.26a$$

from equations 2.24 and 2.25

$$A - B = \frac{V_{dc}\, e^{-\sigma} - V_{ab}}{e^{-\sigma} - e^{\sigma}} - \frac{V_{ab} - V_{dc}\, e^{\sigma}}{e^{-\sigma} - e^{\sigma}}$$

$$= V_{dc}\, \frac{e^{-\sigma} + e^{\sigma}}{e^{-\sigma} - e^{\sigma}} - \frac{2V_{ab}}{e^{-\sigma} - e^{\sigma}}$$

$$= \frac{V_{ab}}{\sinh \sigma} - \frac{V_{dc}}{\tanh \sigma} \qquad 2.26b$$

Now let us work out G/R, from equation 2.19a

$$G = V_{bc} + \frac{N}{1+N}(AX + BY)$$

replacing X and Y by their values from (2.23a) and (2.23b) and substituting for A and B from equations 2.24 and 2.25,

$$G = V_{bc} + \frac{N}{1+N}(V_{ab} - V_{dc})$$

$$G = \frac{1}{1+N}(V_b - V_c + NV_a - NV_d) \qquad 2.27$$

$$\frac{G}{R} = \frac{1}{(1+N)R}(V_b - V_c + NV_a - NV_d) \qquad 2.27a$$

Now the terminal currents Ia, Ib, Ic and Id can be written in terms of the terminal voltages. From equations 2.20, 2.26a and 2.27a Ia is:

$$I_a = \frac{\sigma}{(1+N)R}\left[-\frac{V_{dc}}{\sinh\sigma} + \frac{V_{ab}}{\tanh\sigma}\right] + \frac{1}{(1+N)R}(V_b - V_c + NV_a - NV_d)$$

$$I_a = \frac{1}{(1+N)R}\left[\left(\frac{\sigma}{\tanh\sigma}+N\right)V_a + \left(1-\frac{\sigma}{\tanh\sigma}\right)V_b + \left(\frac{\sigma}{\sinh\sigma}-1\right)V_c + \left(\frac{-\sigma}{\sinh\sigma}-N\right)V_d\right] \qquad 2.28$$

from equations 2.21, 2.26a and 2.27a Ib is given by:

$$I_b = \frac{-\sigma}{(1+N)R}\left[\frac{V_{ab}}{\tanh\sigma} - \frac{V_{dc}}{\sinh\sigma}\right] + \frac{1}{(1+N)R}(V_b - V_c + NV_a - NV_d) \times \frac{1}{N}$$

$$I_b = \frac{1}{(1+N)R}\left[\left(1-\frac{\sigma}{\tanh\sigma}\right)V_a + \left(\frac{\sigma}{\tanh\sigma}+\frac{1}{N}\right)V_b + \left(\frac{-\sigma}{\sinh\sigma}-\frac{1}{N}\right)V_c + \left(\frac{\sigma}{\sinh\sigma}-1\right)V_d\right] \qquad 2.29$$

from equations 3.22, 2.27a and 2.26b Ic is given by:

$$I_c = \frac{\sigma}{(1+N)R}\left(\frac{V_{ab}}{\sinh\sigma} - \frac{V_{dc}}{\tanh\sigma}\right) - \frac{1}{(1+N)R}\left(V_b - V_c + N V_a - N V_d\right) \times \frac{1}{N}$$

$$I_c = \frac{1}{(1+N)R}\left[\left(\frac{\sigma}{\sinh\sigma} - 1\right)V_a + \left(\frac{-\sigma}{\sinh\sigma} - \frac{1}{N}\right)V_b + \left(\frac{\sigma}{\tanh\sigma} + \frac{1}{N}\right)V_c + \left(1 - \frac{\sigma}{\tanh\sigma}\right)V_d\right] \qquad 2.30$$

from equations 2.23, 2.27a and 2.27b Id is given by:

$$I_d = \frac{-\sigma}{(1+N)R}\left(\frac{V_{ab}}{\sinh\sigma} - \frac{V_{dc}}{\tanh\sigma}\right) - \frac{1}{(1+N)R}\left(V_b - V_c + N V_a - N V_d\right)$$

$$I_d = \frac{1}{(1+N)R}\left[\left(\frac{-\sigma}{\sinh\sigma} - N\right)V_a + \left(\frac{\sigma}{\sinh\sigma} - 1\right)V_b + \left(\frac{-\sigma}{\tanh\sigma} + 1\right)V_c + \left(\frac{\sigma}{\tanh\sigma} + N\right)V_d\right] \qquad 2.31$$

Hence from the equations 2.28, 2.29, 2.30 and 2.31, the indefinite admittance matrix corresponding to the FDRC network of Fig.(2.4) can be obtained as shown in equation 2.32[7].

$$\begin{bmatrix} I_a \\ I_b \\ I_c \\ I_d \end{bmatrix} = \frac{1}{(1+N)R} \begin{bmatrix} \frac{\sigma}{\tanh\sigma} + N & 1 - \frac{\sigma}{\tanh\sigma} & \frac{\sigma}{\sinh\sigma} - 1 & \frac{-\sigma}{\sinh\sigma} - N \\ 1 - \frac{\sigma}{\tanh\sigma} & \frac{\sigma}{\tanh\sigma} + \frac{1}{N} & \frac{-\sigma}{\sinh\sigma} - \frac{1}{N} & \frac{\sigma}{\sinh\sigma} - 1 \\ \frac{\sigma}{\sinh\sigma} - 1 & \frac{-\sigma}{\sinh\sigma} - \frac{1}{N} & \frac{\sigma}{\tanh} + \frac{1}{N} & 1 - \frac{\sigma}{\tanh\sigma} \\ \frac{-\sigma}{\sinh\sigma} - N & \frac{\sigma}{\sinh\sigma} - 1 & 1 - \frac{\sigma}{\tanh\sigma} & \frac{\sigma}{\tanh\sigma} + N \end{bmatrix} \begin{bmatrix} V_a \\ V_b \\ V_c \\ V_d \end{bmatrix}$$

2.32

The indefinite admittance matrix makes it possible to treat all terminals on an equal basis and simplifies the derivation of the parameters for particular configurations. For certain two port configurations an impedance matrix is more convenient to use than an admittance matrix. The indefinite impedance matrix for a FDRC network is shown in equation 2.33, where the labelling corresponds to the network shown in Fig.(2.5).

$$\begin{bmatrix} V_1 \\ V_2 \\ V_3 \\ V_4 \end{bmatrix} = \frac{R}{\sigma} \begin{bmatrix} \frac{N+1}{\tanh\sigma} & -N\tanh\frac{\sigma}{2} & \frac{-N+1}{\sinh\sigma} & -\tanh\frac{\sigma}{2} \\ -N\tanh\frac{\sigma}{2} & \frac{N}{N+1}(\sigma+2N\tanh\frac{\sigma}{2}) & -N\tanh\frac{\sigma}{2} & \frac{-N}{1+N}(\sigma-2\tanh\frac{\sigma}{2}) \\ -\frac{N+1}{\sinh\sigma} & -N\tanh\frac{\sigma}{2} & \frac{N+1}{\tanh\sigma} & -\tanh\frac{\sigma}{2} \\ -\tanh\frac{\sigma}{2} & \frac{-N}{N+1}(\sigma-2\tanh\frac{\sigma}{2}) & -\tanh\frac{\sigma}{2} & \frac{1}{1+N}(N\sigma+2\tanh\frac{\sigma}{2}) \end{bmatrix} \begin{bmatrix} I_1 \\ I_2 \\ I_3 \\ I_4 \end{bmatrix}$$

2.33

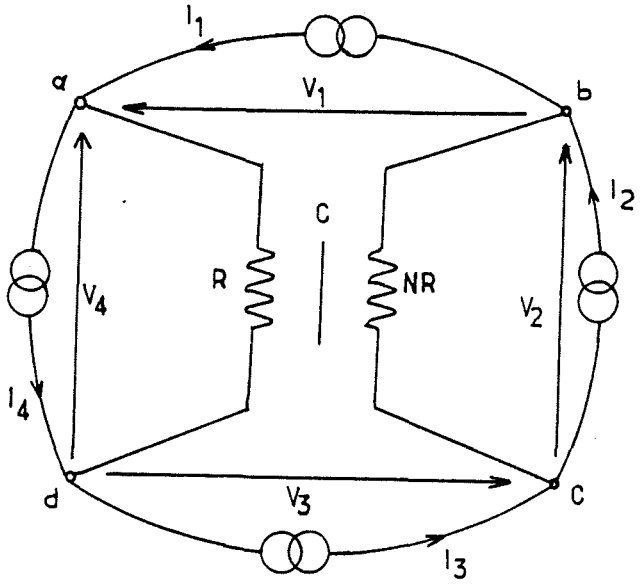


Fig.(2.5) Current and voltage indication for FDRC network.

The FDRC network can be reduced to a DRC network by appropriate terminal connections and by letting N$\longrightarrow$ 0. If N = 0 and terminals 2 and 3 are connected together a uniform DRC network results as shown in Fig.(2.6). The IAM for Fig.(2.6) is obtained from equation 2.32 and is shown in equation 2.32a.

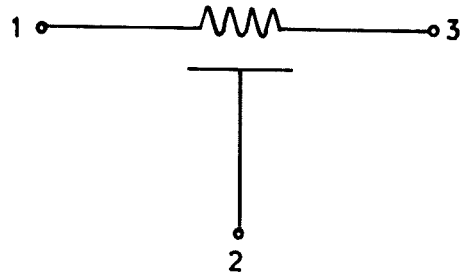


Fig.(2.6) DRC network equivalent circuit.

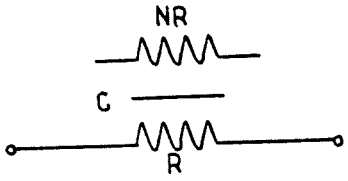
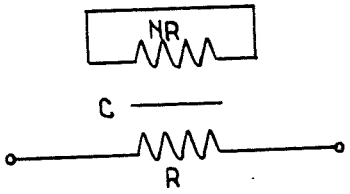
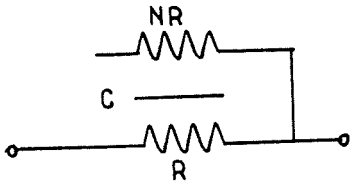
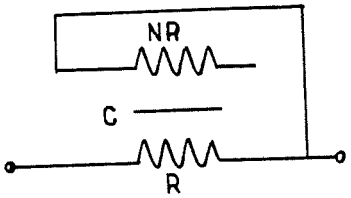
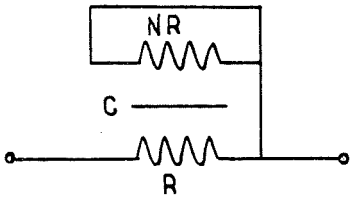
$$\frac{\Gamma}{R}\begin{bmatrix} \frac{1}{\tanh\Gamma} & \frac{1}{\sinh\Gamma}-\frac{1}{\tanh\Gamma} & -\frac{1}{\sinh\Gamma} \\ \frac{1}{\sinh\Gamma}-\frac{1}{\tanh\Gamma} & \frac{2}{\tanh\Gamma}-\frac{2}{\sinh\Gamma} & \frac{1}{\sinh\Gamma}-\frac{1}{\tanh\Gamma} \\ \frac{1}{-\sinh\Gamma} & \frac{1}{\sinh\Gamma}-\frac{1}{\tanh\Gamma} & \frac{1}{\tanh\Gamma} \end{bmatrix} \qquad 2.32\ a$$

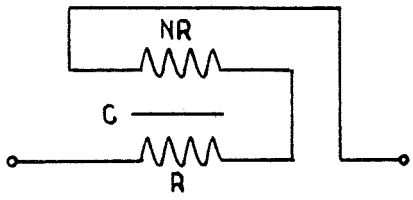
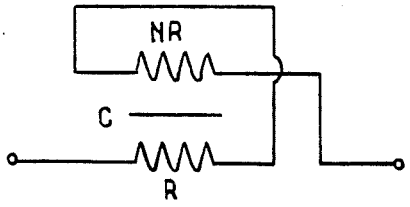
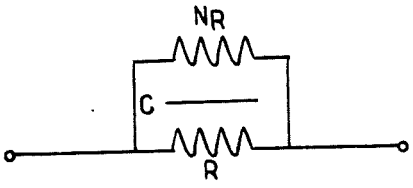
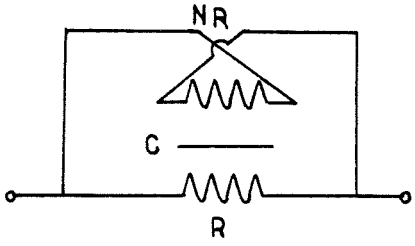
where $\Gamma = \sqrt{j\omega cR}$ and R = rL

The equations 2.32, 2.33 and 2.32a can now be used to derive possible network functions of one port and two ports.

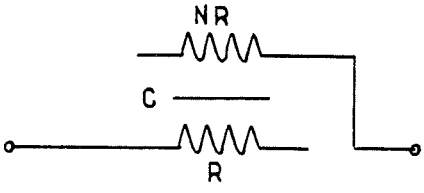
2.2 ONE PORT CHARACTERISTICS

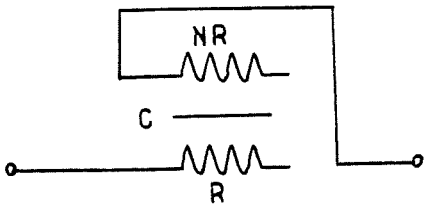
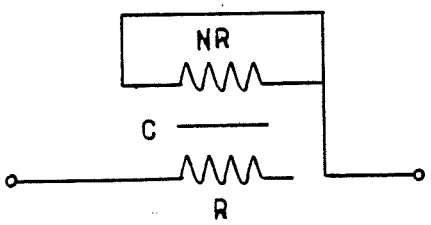
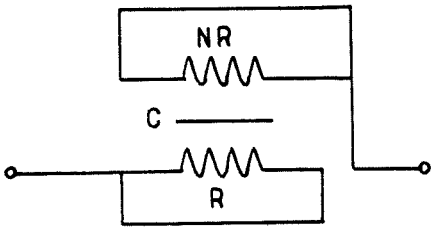
The following one port networks have a resistive path from terminal to terminal and reduce to a resistance at DC [7].

	NETWORK	DRIVING POINT IMPEDANCE (Z/R)
1-		$\frac{1}{(N+1)\Gamma}\left(N\Gamma + 2\tanh\frac{\Gamma}{2}\right)$
2-		$\frac{(N+1)\tanh\frac{\Gamma}{2}}{\frac{\Gamma}{2} + N\tanh\frac{\Gamma}{2}}$
3-		$\frac{(N+1)}{\Gamma}\left[\frac{N\Gamma\cosh\Gamma + \sinh\Gamma}{N\Gamma\sinh\Gamma + (N^2+1)\cosh\Gamma + 2N}\right]$
4-		$\frac{(N+1)\tanh\Gamma}{\Gamma + N\tanh\Gamma}$
5-		$\frac{(N+1)\tanh\Gamma}{\Gamma + N\tanh\Gamma}$

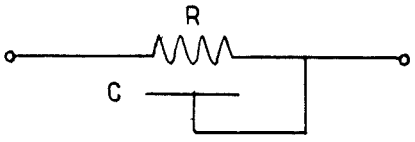
NETWORK	DRIVING POINT IMPEDANCE (Z/R)
6- 	$(N+1)\,\frac{\tanh\Gamma}{\Gamma}$
7- 	$\frac{(N+1)}{\Gamma}\left[\frac{(N+1)^2\sinh\Gamma + 2N\Gamma(\cosh\Gamma+1)}{(N^2+1)\cosh\Gamma + N(\Gamma\sinh\Gamma+2)}\right]$
8- 	$\frac{N}{N+1}$
9- 	$N(N+1)\,\frac{\tanh\frac{\Gamma}{2}}{(N+1)^2\tanh\frac{\Gamma}{2} + 2N\Gamma}$

The following networks do not have a resistive path from terminal to terminal and thus reduce to a capacitor at DC.

NETWORK	DRIVING POINT IMPEDANCE (Z/R)
10- 	$\frac{1}{(N+1)\Gamma}\left[N\Gamma + \frac{N^2+1}{\tanh\Gamma} + \frac{2N}{\sinh\Gamma}\right]$

NETWORK	DRIVING POINT IMPEDANCE (Z/R)
11- 	$\frac{N+1}{\Gamma \tanh \Gamma}$
12- 	$\frac{N+1}{\Gamma}\left[\frac{\Gamma \cosh \Gamma + N \sinh \Gamma}{\Gamma \sinh \Gamma + 2N(\cosh \Gamma - 1)}\right]$
13- 	$\frac{N+1}{2\Gamma \tanh \frac{\Gamma}{2}}$

For the special case in which the parameter N = 0, the first seven networks reduce to

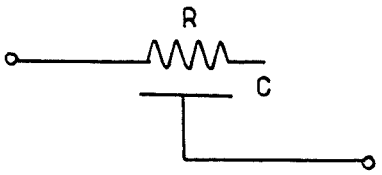


with the driving point impedance of

$$\frac{Z}{R} = \frac{\tanh \Gamma}{\Gamma} \qquad 2.34$$

where in some cases Γ becomes $\Gamma/2$.

Networks (8 and 9) are short circuits and the last four networks reduce to:



with the driving point impedance of

$$\frac{Z}{R} = \frac{1}{\Gamma \tanh \Gamma} \qquad 2.35$$

where for the last network Γ becomes $\Gamma/2$ and R becomes R/4.

For the special case where $N \rightarrow \infty$ networks (1) to (5) and networks (8 and 9) reduce to the resistance R and the rest become open circuits.

Since Γ is complex, equations 2.34 and 2.35 will have both magnitude and phase. Rewriting (2.34) as

$$\frac{Z}{R} = \frac{\tanh j\omega RC}{j\omega RC}$$

with magnitude given by:

$$\left|\frac{Z}{R}\right| = \frac{1}{\sqrt{\eta}} \left[\frac{\cosh\sqrt{2\eta} + \cos\sqrt{2\eta}}{\cosh\sqrt{2\eta} - \cos\sqrt{2\eta}}\right]^{\frac{1}{2}} \qquad 2.36$$

and phase angle of Z/R is given by:

$$\angle\left(\frac{Z}{R}\right) = ARC \tan \frac{\sin\sqrt{2\eta} - \sinh\sqrt{2\eta}}{\sin\sqrt{2\eta} + \sinh\sqrt{2\eta}} \qquad 2.37$$

where $\omega RC = \eta$. A full derivation of the magnitude and the phase angle of the Z/R is given in Appendix 1.

These equations are plotted in Fig.(2.7) together with their asymptotic approximations [1] These networks behave asymptotically similar to a parallel lumped network consisting of a resistance and a capacitance having the same RC product with the exception: that the high frequency attenuation slope and phase shift have one half the lumped circuit values. For this reason there is perhaps some justification for calling these networks "RC- half section".

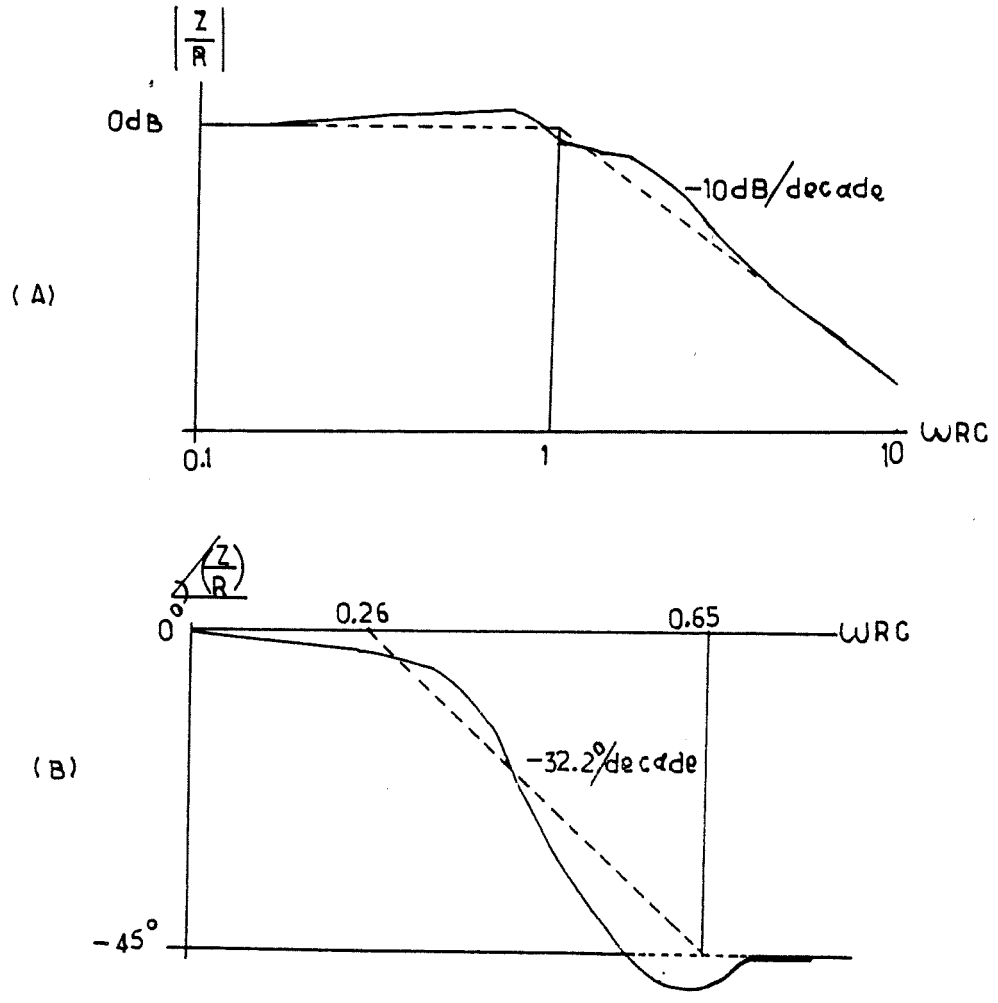


Fig.(2.7) Driving point impedance magnitude and angle for networks 1-7 when N=0.

Rewriting equation 2.35 as

$$\frac{Z}{R} = \frac{1}{\sqrt{j\omega RC}} \cdot \frac{1}{\tanh\sqrt{j\omega RC}}$$

The magnitude and the phase angle of this Z/R, in terms of γ (γ = RC) are

$$\left|\frac{Z}{R}\right| = \frac{1}{\sqrt{\gamma}}\left[\frac{\cosh\sqrt{2\gamma} + \cos\sqrt{2\gamma}}{\cosh\sqrt{2\gamma} - \cos\sqrt{2\gamma}}\right]^{\frac{1}{2}} \qquad 2.38$$

$$\angle\left(\frac{Z}{R}\right) = ARC\tan\left[\frac{\sin\sqrt{2\gamma} + \sinh\sqrt{2\gamma}}{\sin\sqrt{2\gamma} - \sinh\sqrt{2\gamma}}\right] \qquad 2.39$$

A log-log plot of equations 2.38 and 2.39 with their asymptotes, (Fig.2.8)[7] shows that the networks behave as a pure capacitance for low frequencies and an RC half-section for high frequencies.

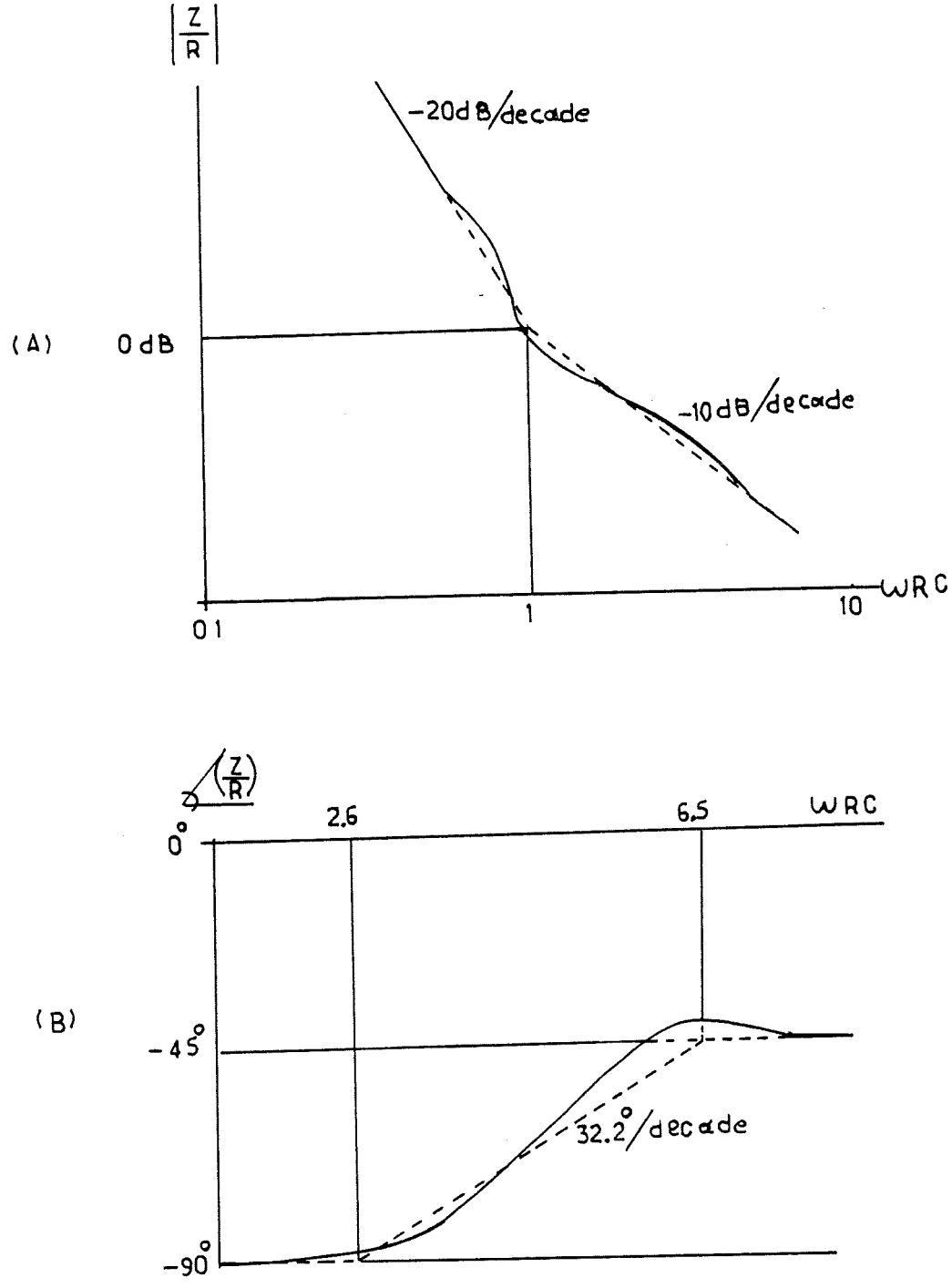


Fig.(2.8) Driving point impedance magnitude and angle for network 10-13 when N=0.

2.3 TRANSFER RATIOS FOR AN FDRC CONFIGURATION

The voltage transfer ratio V_1/V_3 and the current transfer ratio $(-I_1/I_3)$ the most needed transfer ratios in the FDRC applications, -see section (2.6). For these applications, terminal 2 of the FDRC is connected to the supply and is, therefore, at AC ground, and terminal 4 is usually connected directly to DC ground; these assumptions then give rise to the networks of Fig.(2.9) with terminals 2 and 4 grounded which are then used to develop the above two transfer ratios [8].

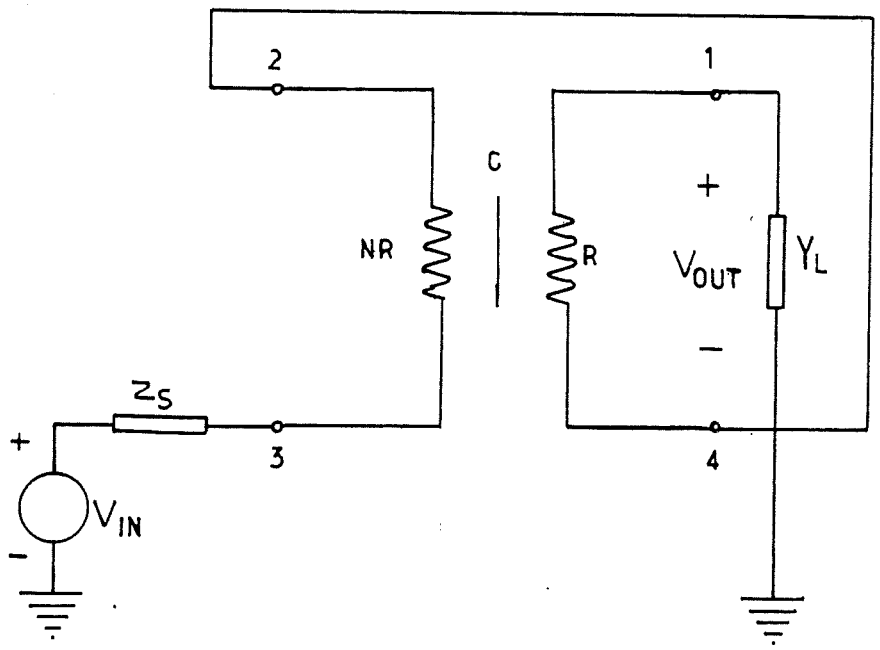


Fig.(2.9a) FDRC connections to develop voltage transfer ratio.

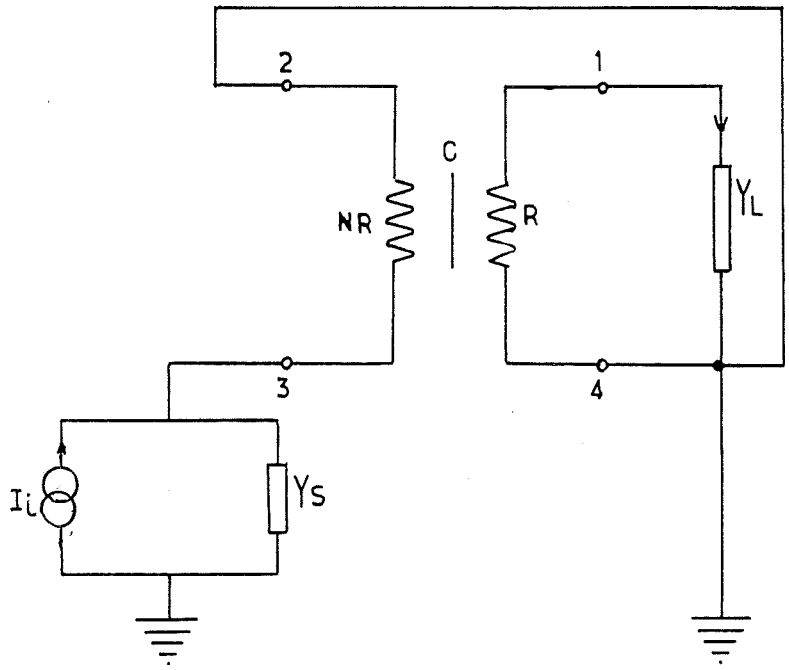


Fig.(2.9b) FDRC connections to develop current transfer ratio.

Fig.(2.9a) shows the FDRC appropriately connected to develop the voltage transfer ratio, and Fig.(2.9b) is then used for the development of the current transfer ratio. Both transfer ratios will take into account source and load immittances. For Fig.(2.9a), since both terminals 2 and 4 are grounded, the rows and columns numbered 2 and 4, respectively, will be eliminated from the matrix of (2.32). This operation yields the two equations

$$I_1 = Y_{11} V_1 + Y_{13} V_3 \qquad 2.40$$

and

$$I_3 = Y_{13} V_1 + Y_{33} V_3 \qquad 2.41$$

Writing a node equation at terminal 3 and solving for V_3,

$$V_3 = \frac{V_{in} Y_s - V_1 Y_{31}}{Y_s + Y_{33}} \qquad 2.42$$

Letting $I_1 = -Y_L V_{out}$, $V_1 = V_{out}$ and substituting these and

equation 2.42 into 2.40, after some algebraic manipulation, will give the desired voltage transfer ratio.

$$\frac{V_{out}}{V_{in}} = \frac{-Y_{13}\,Y_S}{(Y_S + Y_{33})(Y_L + Y_{11}) - Y_{13}\,Y_{31}} \qquad 2.43$$

The current transfer ratio can be calculated using Fig.(2.9b). Writing the nodal equation for terminal 3 and solving for V_3, we obtain:

$$V_3 = \frac{I_i - Y_{31}V_1}{Y_S + Y_{33}} \qquad 2.44$$

Letting $I_1 = -I_o$, $V_1 = I_o Z_L$, substituting (2.44) into (2.40) and manipulating gives

$$\frac{I_o}{I_i} = \frac{-Y_L\,Y_{13}}{(Y_L + Y_{11})(Y_S + Y_{33}) - Y_{13}\,Y_{31}} \qquad 2.45$$

Therefore equations 2.43 and 2.45 give the desired transfer functions for the FDRC. The immittance transfer functions $Z_T(Z_T = \frac{V_o}{I_i})$ and $Y_T(Y_T = \frac{I_o}{V_i})$ may be found by dividing (2.45) by Y_L and multiplying (2.15) by Y_L, respectively.

2.4 THE FDRC NETWORK AS A PASSIVE NOTCH FILTER

Let us consider the FDRC network connected with terminal 3 floating as shown in Fig.(2.10). In this mode of connection the network clearly degenerates into a 3-terminal network with terminal 3 of the network of Fig.(2.3), (ie the terminal c of the network of Fig.(2.4)) suppressed.

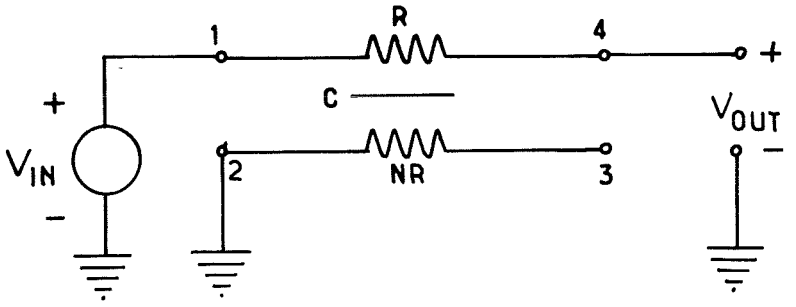


Fig.(2.10) FDRC connected as a three terminal network.

Let Yrs (r,s=1,2,3,4) denote the elements of the IAM of equation 2.32 ,then y'rs (r,s=1,2,4), the elements of the 3 by 3 IAM of the 3 terminal network of Fig.(2.10), are given by [8]:

$$\begin{bmatrix} Y_{11}-\frac{Y_{13}Y_{31}}{Y_{33}} & Y_{12}-\frac{Y_{13}Y_{32}}{Y_{33}} & Y_{14}-\frac{Y_{13}Y_{34}}{Y_{33}} \\ Y_{21}-\frac{Y_{23}Y_{31}}{Y_{33}} & Y_{22}-\frac{Y_{23}Y_{32}}{Y_{33}} & Y_{24}-\frac{Y_{23}Y_{34}}{Y_{33}} \\ Y_{41}-\frac{Y_{43}Y_{31}}{Y_{33}} & Y_{42}-\frac{Y_{43}Y_{32}}{Y_{33}} & Y_{44}-\frac{Y_{43}Y_{34}}{Y_{33}} \end{bmatrix} \qquad 2.46$$

Where from equations 2.46 and 2.32 the required values of Y's (r,s=1,2,4) are:

$$Y_{11}^{*} = \frac{1}{(1+N)R}\left[\frac{N\sigma^2\tanh\sigma + \sigma + N\sigma(2\,\mathrm{Sech}\,\sigma + N)}{N\sigma + \tanh\sigma}\right]$$

$$Y_{12}^{*} = Y_{21}^{*} = \frac{1}{(1+N)R}\left[\frac{\sigma(1-N)(\mathrm{Sech}\sigma - 1) - N\sigma^2\tanh\sigma}{N\sigma + \tanh\sigma}\right] \qquad 2.47a$$

$$Y_{14}^{*} = Y_{41}^{*} = \frac{1}{R}\left[\frac{-(N\sigma + \sigma\,\mathrm{Sech}\sigma)}{N\sigma + \tanh\sigma}\right]$$

$$Y_{22}^{*} = \frac{1}{(1+N)R}\left[\frac{N\sigma^2\tanh\sigma + 2\sigma(1-\mathrm{Sech}\,\sigma)}{N\sigma + \tanh\sigma}\right]$$

$$Y_{24}^{*} = Y_{42}^{*} = \frac{1}{R}\left[\frac{\sigma(\mathrm{Sech}\,\sigma - 1)}{N\sigma + \tanh\sigma}\right] \qquad 2.47b$$

$$Y_{44}^{*} = \frac{1}{R}\left[\frac{\sigma(1+N)}{N\sigma + \tanh\sigma}\right]$$

Since terminal 4 is open circuited (or the load impedance at terminal 4 is very much larger than R), the current at terminal 4 can be neglected. This yields

$$0 = Y_{41}^{*} V_1 + Y_{44}^{*} V_4 \qquad 2.48$$

Letting $V_1 = V_{in}$, $V_4 = V_{out}$, and solving for the voltage transfer ratio gives:

$$\frac{V_{out}}{V_{in}} = \frac{-Y_{41}^{*}}{Y_{44}^{*}} \qquad 2.49$$

Substituting the expressions for Y_{41}^{*} and Y_{44}^{*} from equations 2.47 into equation 2.49 gives the desired voltage transfer ratio for the FDRC passive notch filter as [8]:

$$\frac{V_{out}}{V_{in}} = \frac{1+N\cosh\theta}{(1+N)\cosh\theta} \qquad 2.50$$

The notch frequencies are determined by the zeros of $1+N\cosh\theta=0$. Letting $\theta = J\omega(1+N)RC = J\phi$, means that some values of ϕ gives a zero of (2.50). Letting $\phi = \omega(1+N)RC = \omega/\omega_o$ and rearranging the numerator of equation 2.50 yields:

$$\cosh\sqrt{\frac{J\omega}{\omega_o}} = -\frac{1}{N} \qquad 2.51$$

Since

$$\sqrt{\frac{J\omega}{\omega_o}} = \sqrt{\frac{\omega}{2\omega_o}}\,(1+\dot{J}) = u\,(1+\dot{J}) \qquad 2.52$$

equation 2.51 now becomes:

$$\cosh u\ \cos u - \dot{J}\sinh u\ \sin u = -\frac{1}{N} \qquad 2.53$$

Equating the real and imaginary parts from both sides of (2.53) gives:

$$\cosh u\ \cos u = -\frac{1}{N} \qquad 2.54$$

and

$$\sinh u\ \sin u = 0 \qquad 2.55$$

equation 2.55 is satisfied for

$$u = n\pi\,, \quad n = 0\,, \pm 1\,, \pm 2\,, \pm 3, \ldots$$

Choosing n=$\pm$ 1 gives u= $\sqrt{\omega/2\omega_o} = \pm\pi$. Solving for ω, and noting that

$$\omega_o = \frac{1}{(1+N)RC} \qquad 2.56$$

gives [7]:

$$\omega = \frac{19.75}{(1+N)RC} \qquad 2.57$$

Substituting u= $\pm\pi$ into equation 2.54 yields:

$$\cosh(\pm\pi).\cos(\pm\pi) = -1/N \qquad 2.58$$

or, since $\cosh(\pm\pi) = \cosh(\pi)$

and $\cos(\pm\pi) = \cos(\pi) = -1$,

equation 2.58 becomes:

$$\cosh(\pi) = 1/N \qquad 2.59$$

Solving equation 2.59 for N yields:

$$N = 0.086266 \qquad 2.60$$

This, then, indicates that for N=0.086266, a true zero of transmission exists for the FDRC passive notch filter at ϕ = 19.75. For N not equal to 0.086266 the transmission factor is no longer zero and, as seen from equation 2.57, a slight shift in frequency also occurs.

2.5 CAPACITANCE EVALUATION BY THE MEASUREMENT OF NOTCH FREQUENCY

In an FDRC device, because of the distributed nature of the capacitance, it cannot be measured directly but its value has to be deduced indirectly from other measurements.

One obvious possible method is to measure C indirectly via equation 2.57, ie by the measurement of the notch frequency with the FDRC device connected in the configuration of Fig.(2.10). (Ofcourse, the values of R and N will need to be knowm accurately and if N = 0.086266 then suitable corrections would have to be made).

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CHAPTER 3

THICK FILM MATERIALS

3.1 RESISTORS

Thick film resistor inks consist of dispersions of metal and/or metal oxides, semiconducting compounds and glasses in resinous screen printing vehicles. Thick film resistors are made by fusing together an intimate mixture of resistive and vitreous, non-conductive materials. The temperatures employed not only fuse the vitreous and resistive materials together, but also bond them to a ceramic substrate, such as alumina, to give a highly reliable resistive unit which is able to dissipate a relatively large amount of power. The resistance is controlled by varying the volume fraction of conducting oxide particles. Other additions are made to control temperature coefficient of resistance (TCR) or other properties. The complexity of the behaviour of thick film resistor systems has been the subject of extensive investigations for many years. However, it is not well understood, particularly by the users.

Electrical properties of thick film resistors depend not only on their ingredient materials but also on the various processes employed in combining these materials and in fabricating the finished resistors. Various investigators have sought to explain the factors contributing to such properties as sheet resistance, temperature coefficient of resistance, voltage coefficient (stability), ohmic and non-ohmic behaviour, thermal stability and related properties.

The growth in complexity of film circuit configurations requires resistor properties to be predicted under a wide variety of design considerations. Many models proposed as a means of predicting and correlating resistor properties to ingredient properties fall short of their expectations when applied broadly to different systems.

Over the past decade there has been a dramatic and continuing improvement in the properties of thick film pastes. Today's state of the art of resistor and conductor and dielectric pastes have much improved electrical characteristics with respect to their predecessors. These improvements are most certainly desirable but unfortunately there still exist many major problems for the average thick film circuit producer. Perhaps one of the most outstanding practical difficulties is the incompatibility of some resistors with conductors and dielectrics, necessitating the introduction of complex correction factors depending upon the particular resistor/dielectric or conductor combinations.

3.1.1 GLASS BASES FOR THICK FILM RESISTORS

Glasses most commonly used for fabricating resistors are basically selected from the lead-borate, lead-boro-silicate, boro-silicate and lead-boro bismuthate systems. These types of glasses have been selected as the base solvent for some of the same reasons water is used as a solvent, viz availability, cost, and chemical behaviour. Also, these types of glasses are used because of their physical characteristics; they can be made to possess similar coefficients of expansions as "wet" ceramic which is commonly used as carrier. They have also the ability to be reheated to die bonding temperature without degradation and are relatively insensitive to moisture.

3.1.2 CONDUCTING PHASE CONSTITUENTS OF THICK FILM RESISTORS

Many compositional variations of conducting particles for thick film resistors are reported. Such materials as indium oxide, thallium oxide, certain amphoteric narrow-band semiconductive oxides, carbides, nitrides mixtures of tungsten and palladium oxide as well as finely divided noble metals are used to produce thick film resistor inks.

3.1.3 SUBSTRATE EFFECT ON RESISTANCE

The conduction in thick film resistors depends partly on particle to particle contact, and paths sometimes are only completed by additional layers of particles. One of the factors that contributes to keeping the particles apart and hence increasing the resistance is the roughness of the substrate surface. As the thickness of the film deposited is reduced until it approaches that of the undulation on the surface of the substrate, the resistance of the resistor deposited become more and more dependent on the roughness of the substrate.

In an investigation by Huang & Stein [9], some tests of resistance versus firing time were performed using borosilicate glass, soda lime glass, forsterite and alumina(Al203 96%) substrates and their results, are shown in Fig.(3.1). All curves follow the same pattern of dropping resistance with increased firing time. The resistors on soda lime glass obtained the lowest resistances. And on the ceramic materials gave higher values. And on borosilicate glass substrates achieved values about 5 times higher than the values on window glass. They also performed some tests on the TCR's of the resistors on different substrates, and their results are shown in Fig.(3.2). The TCR's shifted towards more negative values in going

from soda lime to borosilicate glasses. The resistance and TCR results with borosilicate substrates are partially due to thermal expansion coefficient mismatches.

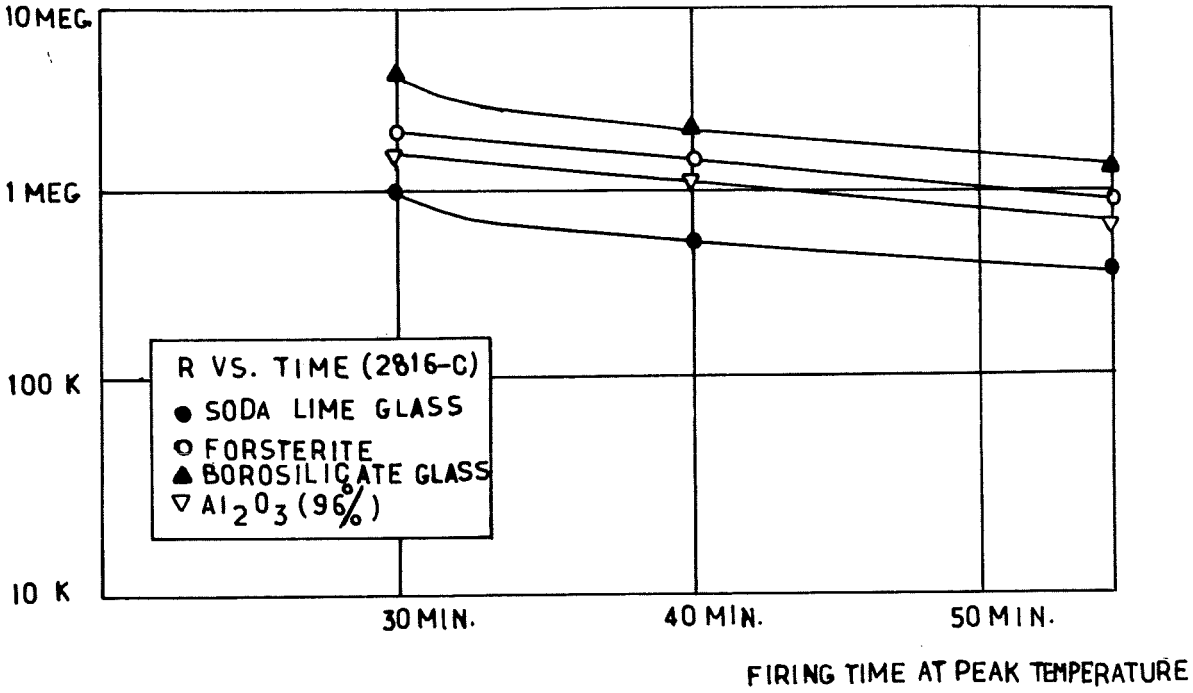


Fig.(3.1) Effect of substrates type on resistivity [9].

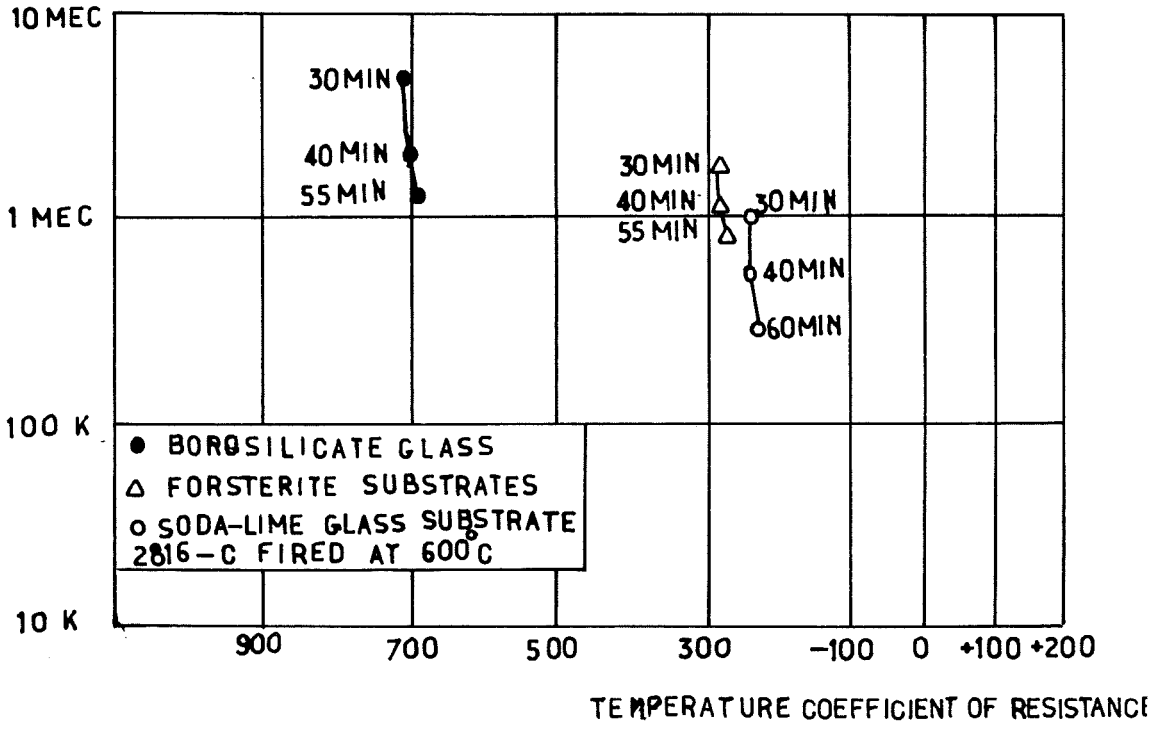


Fig.(3.2) Effect of substrates type on TCR [9].

3.1.4 CONDUCTOR TERMINATIONS

The choice of conductors in some instances also affects the behavior of the resistors. Conductor migration into the resistor film has deleterious effects on sheet resistance, temperature coefficient and stability, depending on the resistor length and aspect ratio. Permanent resistance changes due to voltage stresses, see Chapter 5, reported [10] to be partly affected by the resistor termination. Both VCR and contact resistance (resistor - termination interface) are also affected by the terminations.

3.1.5 GEOMETRY OF THE RESISTOR

The dependence of sheet resistance of a thick film resistor on aspect ratio is generally known. It is both a function of film thickness variation and interactions with the terminations. Typically, small resistors print thicker than large resistors; an effect tending to decrease resistance. Interaction between the conductor and resistor can lower the resistance values. Depending on the net effect of these contributions, small resistors can have values less than or greater than large resistors. However, with improved inks this effect can be minimized to a very small value.

Stein et al [11] have reported that the ESL 3800 series resistor inks have been little affected by a particular composition of Pt-Au termination for larger size resistors, and as the size drops below a certain value, the resistance increases in every case. His investigation on another resistor type with the same terminations and firing profile showed a drop in resistance for small sizes. He added that these effects become greater when the resistance is increased. These effects are apparently due to the interaction of the conductor and resistor compositions.

Temperature coefficient of resistance is particularly sensitive to the geometry of the resistor, where the mechanism of interaction is diffusion of conductors into the resistance film. Conductor metals, because of their high positive TCR tend to cause significant shift in the resistor TCR, even with moderate amounts of diffusion [12]. It is not unusual for the TCR values of short resistors to be substantially different from values obtained on long resistors. Often, certain restrictions of resistor size may be necessary to maintain a desired TCR range.

3.1.6 VOLTAGE COEFFICIENT OF RESISTANCE

Whilst most materials used for the construction of resistive elements are required to exhibit reasonable linearity between current and voltage it is generally recognised that perfect linearity only exists in the case of bulk metallic alloys. Other materials exhibit some degree of non-linearity which is frequently represented by a "voltage coefficient". It is rare to find that this parameter is a coefficient in the true sense as its value is very dependent on the voltage applied.

The temporary change of resistance due to high voltage can be related to the voltage coefficient of the resistor. The temporary change of resistance (VCR) is believed to be due to tunneling barriers where the electron transport is proportional to the voltage. When the voltage, is removed, recovery occurs. Stein et al [13] suggested that VCR values drop sharply, independent of termination, for long resistors since the VCR is a combined effect of the contact resistance and the characteristic of the resistor structure. As the resistor's length increases, the VCR approaches the actual resistor's characteristic. He also reported that no significant change of VCR

was observed for different peak firing temperatures. The voltage coefficient will increase when the thickness and size of the resistor is decreased. Voltage coefficient for high value resistors can be reduced by increasing the number of squares and using pastes of lower resistance. However, Herbst [10] has emphasised that the voltage coefficient for a fixed resistance is linearly dependent on resistor length. Isaak [14] has shown that as the temperature is increased to 210°C, the VCR decreases to 25% of that at room temperature. And also as the resistor is scaled up in size the VCR becomes less negative.

3.1.7 THE AGEING EFFECT

An investigation on the effect of ageing on some particular resistor inks (1400 series) both at high and low temperatures and unglazed and over-glazed resistors has been performed by Coleman [15]. The rate of change of the unglazed resistors at 200°C is approximately a square root of time. The magnitude of the change is greater in nitrogen than in air, this may be due to loss of oxygen. At lower temperatures the rate of change of unglazed resistors is less than the square root of time and may be approximated to the cubic root of time dependence. The magnitude of resistance change in unglazed resistors as fired was higher than in overglazed or refired (through the overglazed profile) resistors. Further refiring also improved the stability at higher ageing temperature. This was believed [15] to be due to the decrease in the amount of conducting oxide at or near the resistor surface, and hence a reduction in the effect of oxygen diffusion out of the resistor.

The ruthenium dioxide systems, when aged in nitrogen atmospheres with 1% hydrogen experience a large increase in resistance. In

summary the factors affecting the stability of a particular resistor system with a particular conductor termination are the size and shape of the resistors, whether they are overglazed and trimmed, the operating temperature and atmospheres and the firing schedules that the resistors have experienced.

3.1.8 CURRENT NOISE IN RESISTORS

Current noise is observed in all resistance elements except those manufactured from bulk metallic alloys and is a form of excess noise observed above the thermal or Johnson noise level, which occurs when current is passed through the resistor. The greater the number of parallel conducting paths for current flow through the resistor, the lower will be the noise, therefore the noise increases with decreasing thickness and size of the resistor. It is typical with thick film systems that noise increases with resistance.

The basic conduction mechanism in thick film resistors [16], involves the transport of electrons through a series of metal-insulator- metal sandwiches. It is expected that an extremely large amount of defects exist around the metal to insulator interfaces. Associated with these defects are electron traps which will trap and release electrons. If the number of trapped electrons fluctuates, the barrier height between two conducting particles will fluctuate. If the electron trapping time constant varies over a wide range, then 1/f noise is generated [17].

3.1.9 REFIRING EFFECT

Stein et al [11] and Huang et al [18] have reported that, refiring will cause a decrease in resistance and this decrease tends to diminish with repeated firing. They also believe that the

resistance change due to refiring is most pronounced for higher resistivities and becomes progressively less pronounced for lower resistivities. Garvin et al [12] have shown a 10 to 15% drop, for resistors fired at 980°C. The resistance of resistors made with Au terminations will drop less than that of those made with Pd/Ag terminations. Among Pd/Ag terminations, those containing more Ag will show larger resistance decreases [13]&[18]. This may be related to the higher mobility of Ag as compared to Au in diffusing into the resistor. As resistance values are decreased by multiple firing with several Au-bearing terminations, the TCR's shift towards positive values by 10 to 30 ppm/°C for each refire [13].

3.1.10 SHEET RESISTANCE

As the volume concentration of the conductive particles is decreased, the resistance increases rapidly and TCR shifts to negative values. Resistances of 0.1 MΩ to 10 MΩ/sq fall on the increasingly steep slope of the dilution curve. This causes greater sensitivity to the firing conditions, resistor geometry, metallurgy of conductor termination, voltage coefficients of resistance and to various forms of thermal, voltage and thermomechanical stresses. Stein [13] has shown a typical reduction in sheet resistance with resistor length for all conductor terminations. This may be related to a thicker print for shorter length. However, the Pd/Ag combination showed a more extensive drop for small sizes due to Ag diffusion. This effect is particularly severe for 0.5mm long resistors and becomes more extensive for higher resistances such as 10 MΩ/sq [13].

3.2 DIELECTRICS

Thick-film dielectric compositions fall into three functional classes: (I) crossovers and multilayers, (II) capacitors, (III) encapsulants. Crossover dielectrics electrically isolate two conductor lines, one of which crosses over the other. Dielectrics for multilayer circuits perform a similar function, isolating layers of printed conductor wiring. Both dielectric types were developed to increase circuit density through more efficient use of the substrate area, and both are used routinely in circuit manufacture. Dielectrics for screen-printed capacitors have not been used widely in the past, due to a lack of hermeticity and a low maximum capacitance density (15 nF/sq cm) compared to discrete chip capacitors. Recently, however, materials improvements and increased penetration of thick-film circuitry into the home entertainment market have opened new opportunities for these materials. Of particular significance are tuner-related circuits with as many as 60 screen-printed capacitors, currently being manufactured in large volumes. Glass encapsulants are used routinely to protect thick-film circuit elements from adverse environments.

3.2.1 CROSSOVER/MULTILAYER DIELECTRICS

The first really practical thick film multilayer dielectrics were introduced in 1967 [19],[20],[21]. These were devitrifying glasses, ground to a fine particle size, and dispersed in a screen printing vehicle. Within a few years, the use of this type of material to increase hybrid circuit density was widespread. Applications included LSI arrays [22], as crossovers and low value capacitors in microwave IC's [23], in opto electronic displays [24],[25], and in circuits ranging from very small to as large as 6 inches on a side [26].

The primary function of crossover and multilayer dielectrics is to electrically insulate conductive layers. Crossover dielectrics requires a low dielectric constant (K), low electrical loss, high insulation resistance and breakdown voltage, environmental stability, and co-fireability require thermal expansion match with the substrate, good via resolution, smooth surface, and high thermal conductivity. Three types of materials have been developed to meet these needs: glasses, crystallizable glasses, and crystal-filled glasses.

SINGLE-PHASE GLASS DIELECTRIC

The first crossover dielectrics were based on high melting point single-phase glasses with low temperature coefficients of viscosity. Although these performed well electrically, processing was often a problem because of the need for a hierarchy of firing temperatures. That is, all firings subsequent to the firing of the glass softening point. This was necessary to prevent conductors printed on top of the glass from moving laterally or from sinking into the glass. This movement often leads to electrical shorting and impaired solderability.

CRYSTALLIZING DIELECTRIC

To avoid the deficiencies of the single-phase glasses, crystallizable glasses with low dielectric constants were developed. Crystallizable dielectrics offer the hybrid circuit manufacturer a new and uniquely useful processing parameter. In the initial stages

of firing the dielectric behaves like a single phase glass going through the normal processes of sintering, softening and coalescence. As the initial period of firing is passed, however, crystals appear and cause a large increase in viscosity. Properly controlled in size and concentration, the formation of crystals can actually cause the dielectric layer to become solid and intractable. The dispersed crystals strengthen the matrix glass and retard its flow during subsequent firing. In a well structured glass, crystallization is complete at a relatively low temperature, 800° C. This permits conductors to be separately fired or co-fired on the dielectric at 850 °C, a common thick-film firing temperature, without conductor movement.

The crystallizable crossover offers just as much hermeticity and insulating properties as a single phase crossover with a strong advantage in the properties of the over-printed conductor and beneficial in making multilayer circuits and screen printed capacitors. The electrical properties of a conductor printed over the crystallizable crossover are markedly superior to those obtained over a single phase crossover.

The need for better multilayer dielectrics led to the development of crystal-filled glass systems which provide greater latitude for physical property design.

3.2.2 CAPACITOR DIELECTRICS

A thick film capacitor is produced by three sequentially printed layers- two electrodes separated by a dielectric material. Usually, the composition for the bottom electrode is used to simultaneously print the conductor wiring for the entire circuit. Depending on performance and cost considerations, electrode metals span the range from Au to high Ag-content alloys. The capacitor dielectric may be comprised of glasses, glass ceramics, ferroelectric crystalline oxides, or some combination of these materials.

Dielectric constants of 10 to 700 can be obtained with present technology. This yields capacitance densities of 175p F/cm^2 to about 34 nF/cm^2. Crossover dielectric compositions with K values of 10-15 are used for very low value capacitors [27]-[28]. In general, these materials are hermetic and so not require encapsulation. Capacitors fabricated with dielectric materials with K greater than 15 are porous and require encapsulation for operation in humid environments.

The composition of the binder within the conductor also influences dielectric performance. Chemical reaction with the dielectric can yeild low K phases which lower the overall capacitance. Also, conductors containing crystalline oxides that react chemically with the alumina substrate to promote adhesion may contribute to low capacitance density and poor electrical performance. For example, conductors with too high a copper oxide content can yield high dissipation factors and promote capactor shorting. Performance of a screen printed capacitor system is primarily determined by the thick film materials, but the printing procedures and firing sequence are also very important.

3.2.3 ENCAPSULANT DIELECTRICS

The primary purpose of an encapsulant is to protect the circuit elements against adverse environments; both organic and glass coatings have been used for this purpose. Glass encapsulants were initially developed to protect Pd/PdO/Ag resistors. These were based on low softening point of lead borosilicate glasses which could be fired at 500° C. The low firing temperature was essential to minimize the resistance change during the refiring process. With the development of the more stable ruthenium based resistor systems the need for encapsulation was not as great. Nevertheless, the encapsulation of resistors is still common, particularly in high reliability applications.

A glass encapsulant with a very low thermal coefficient of expansion (TCE), lower than that of the substrate, tends to crack. The problems presented by the large differences in TCE's were resolved through the use of two separate encapsulant layers. The first layer is a crystal filled glass with a TCE greater than that of alumina but lower than that of the dielectric, placing it in compression over the printed capacitor. The second layer, a glass with a TCE slightly lower than that of alumina, seals defects in the first layer and is in compression over the capacitor and alumina. The structure is like a graded seal in concept.

3.3 CONDUCTORS

In thick film hybrid circuits, conductors function as bonding sites for discrete active devices and as the interconnection between these discrete devices, printed passive elements, and leads or pins for external connection. Key performance requirements are low resistance, compatibility with other printed elements, ease of producing soldered or wire interconnection bonds with good adhesion to the substrate when subjected to peel forces. Both the functional phase and the binder contribute to performance, and conditions of substrate surface porosity and chemistry can have an important effect on adhesion.

SOLDERABLE CONDUCTORS

Most air fireable thick film microcircuit conductors in current use are based on Au,Ag, and binary or ternary alloys of Au,Ag,Pt, and Pd. Sheet resistance values range from about 3 mΩ/sq for Au and Ag - about two to four times their bulk resistances - to 150mΩ/sq, exhibited by some of the Pt/Au's. Although Au may be soldered with special Pt-In solders, it is usually thought of as non-solderable because of the rapid dissolution in common Sn-Pd solders.

The solder interconnection of lead frames, discrete passive elements such as capacitors, and packaged or passivated active devices is common. However, solderable conductors and bare active devices are interconnected by one of several wire bonding techniques: the thermocompression bonding of gold wire, the thermosonic bonding of gold wire, and the ultrasonic bonding of aluminum wire. It can be said that the thermocompression method - the combined use of heat and pressure to create a metallurgical bond between the Au wire and the

thick film conductor - is used routinely to produce strong reliable bonds. The technique of attaching Al wire to solderable conductors is used, but less frequently. The thermosonic attachment of gold wire is a relatively new bonding method in which thermal and ultrasonic energy are used simultaneously. Following the initial manual indexing of a circuit, the machines can be programmed to automatically produce bonds at all appropriate circuit locations.

GOLD CONDUCTORS

Traditionally, the use of thick film Au conductors has been used only in very high reliability applications, eg., military and telecommunications circuits. The basis for this is the nobility of the metal - that is, its resistance toward corrosion and reaction in many ambients. However, Au is not completely benign, and certain Au-containing metallurgical systems have presented problems. Also, as with the solderable conductors, the binder system is an important contributor to most aspects of performance, and the development of binders for Au conductors usually had poor optical density with large areas of glass on the surface. At high firing temperatures, uncontrolled sintering produced an excessive enlargement of both the Au grains and the glass area. Many of the modern oxide and mixed bonded Au systems have overcome these deficiencies of optical density and process latitude and exhibit much better adhesion than the early materials. Historically, Au conductors and bare active devices have been connected by chip and wire techniques: the thermocompression bonding of Au wire and the ultrasonic bonding of Al wire. Recently, an automated thermosonic technique for bonding Au wire has been developed, and its use appears to be increasing.

3.4 VEHICLES

The vehicle component of thick film compositions is the medium in which the inorganic particles are dispersed, and renders the latter screen printable. Both the vehicle and dispersed phases contribute to composition flow characteristics - but, the chemical nature and, usually, the particle size distribution and morphology of the solids are fixed by fired-film performance needs. Thus the vehicle is the key variable in arriving at suitable printing characteristics. In addition, it determines the drying rate of the composition on the screen and of the print, the change in flow properties with temperature, and it is important in forming a temporary bond to the substrate before firing. Unless it burns smoothly and cleanly during firing, it can adversely affect the properties and cosmetics of fired films.

Many of the early vehicles, such as simple mixtures of terpineol type solvents and cellulose type resins, still perform well with a many solid system in a variety of printing environments. Viscosity is the most widely used parameter for assessing a composition's flow behavior. It is the internal resistance exerted by a fluid to the relative motion of its parts and expressed in units of Pascal-seconds (Pa.s). It is defined as shear stress divided by shear rate; where shear stress is the force in Pascals applied to a viscous fluid to cause its movement, and shear rate in seconds is the rate of travel of two parallel plates separated by fluid, divided by the distance between the plates [$(cm/s/cm)=s^{-1}$].

3.5 MULTILAYER THICK FILM STRUCTURES

Printing resistors on multilayer circuits presents problems [29]. When a resistor is printed on a dielectric, its resistance and temperature coefficient of resistance vary greatly from those of the same material printed on a bare alumina substrate. If vias were left in the dielectric, so that resistors could be printed on the bare substrate, the typical problems associated with printing onto a cavity must be encountered, and distributions and average resistance are hard to control. Also, some of the advantage of high circuit density obtained by the multilayer technique are lost as valuable substrate real estate has to be set aside for resistors. It has been necessary, then, to design circuits with a minimum of printed resistors, utilizing such techniques as incorporating the resistors in monolithic chips to work around this problem. In 1975 Pitt [5] used the idea of printing resistors on top of dielectrics to fabricate distributed networks. Hain [30] has evaluated the EMCA 5300-1 resistor series on newly developed multilayer dielectrics and concluded that the resistor-over-dielectric technique is a viable process in thick film circuitry. Although in both the multilayer circuitry and distributed network, the resistor needs to be printed on top of the dielectric , the demands for each application are different.

In multilayer circuitry the object is to minimize the interference and connection between the layers. This is possible by simply reducing the dielectric constant of the insulating layer and thickening it, so as to reduce the capacitance between the layers. However, in RC distributed networks, high capacitance is required between the layers in order to realize the RC network. At lower operating frequencies the required capacitance is even higher, hence,

in these cases either high dielectric constant for the insulating layer or larger area of distribution have to be employed. Printing resistors on top of dielectrics inevitably has some associated problems, (especially in cases of high dielectric constants) which are dealt with in some detail in Chapter 4. However, in distributed networks the capacitance required is high and as the operating frequency decreases the capacitance needs to be as high as possible so as to result in a smaller distribution area.

In fully distributed RC (FDRC) networks where a dielectric layer is sandwiched between two resistor layers, the problems are even more extensive. In here, the dielectric has to be fired on top of the resistor and that in turn produces its own problems. The fabrication of FDRC networks is discussed in sections 4.7 - 4.19 .

CHAPTER 4

THE FDRC STRUCTURE FABRICATED ON THICK FILM

4.1 INTRODUCTION

A distributed RC (DRC) structure consists of successive layers of conductive- dielectric- resistor films. Attempts to make a distributed RC network (ie conductor- dielectric- resistor structure) on thick film substrates have been made since at least 1975 [5]. Other workers [31-32] have also studied thick film DRC network.

A fully distributed RC (FDRC) structure is formed by the deposition of resistor- dielectric- resistor films onto a substrate. Such a structure has been referred to as R-C-NR network. Some workers [33-36] have tried to analyse different R-C-NR networks to formulate design procedures for using them in various applications. R-C-NR networks have already been fabricated using thin film techniques [37 through 40]*. However, thin film techniques do not offer economical ways of achieving the large variety of products needed in custom design circuits.

The idea of fabricating the FDRC network using thick film was first introduced by the author in 1980 [41], since then efforts have been made to print and fire the successive layers of resistor- dielectric- resistor onto a ceramic substrate to accomplish an acceptably good FDRC network.

* After an extensive investigation, it seemed that FDRC networks had not been fabricated using monolithic techniques. Even if they were, they would suffer the same drawbacks as their thin film counter parts.

In section 4.2 of this chapter a review of the work on the fabrication of DRC (ie conductor- dielectric- resistor) networks on thick film substrates and the problems associated with this process are presented. Section 4.3 is concerned with the particular considerations for fabrication of the FDRC (R-C-NR) network using thick film techniques. Section 4.4 gives a brief account of material selection. Section 4.5 explains how the substrates are codified throughout this research. Section 4.6 proposes two patterns for the thick film FDRC network and explains some aspects of the work associated with them. Then a number of experimental examinations, each with discussions, are presented under the heading of investigation in sections 4.7 to 4.19 which constitute the main body of this chapter. Section 4.20 give a brief conclusion for the work of this chapter. Section 4.21 describes how an indication of the capacitances of the FDRC networks [fabricated as described in investigations (2), (5), (6) and (7)] can be obtained using the bridge method of measuring capacitances. At the end of this section a short comment is given for the results of this measuremen.

4.2 THICK FILM DRC NETWORK FABRICATION REVIEW

Thick film distributed RC devices require deposition of a thick film resistor onto an insulating or dielectric glaze, where the resistance and capacitance are distributed throughout the films rather than lumped within individual components. Fig.(4.1) shows the structure of a thick film uniformly distributed RC component. The resistor and the conductor layers act as the two electrodes of a capacitor and the dielectric layer is the insulating layer between the two electrodes. The electronic circuit equivalent to this structure is shown in Fig.(4.2).

In 1975, Pitt et al have encountered two main problems in deposition of thick film resistors onto dielectrics [42]:

1. The resistor values showed marked differences from those on ceramics. The nature of the change depended on the sheet resistance, the type of the resistor and dielectric and the relative permittivity of the dielectric.

2. The number of pin-holes causing electrical shorts through the insulator of the filters were considerably larger than those in the control capacitors.

It was also reported [26] that the pin-hole effect has shown itself particularly when large dielectric areas were used.

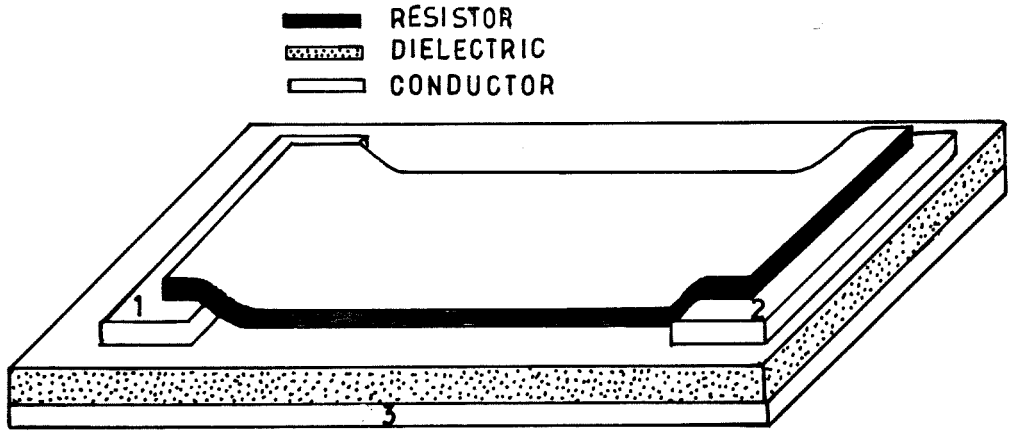


Fig.(4.1) Thick film structure of distrinuted RC network (DRCN).

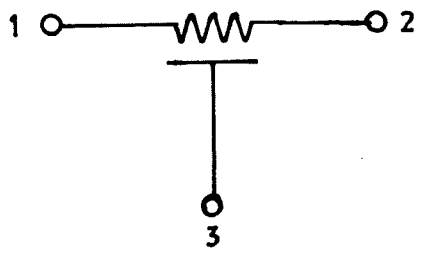


Fig.(4.2) Equivalent circuit to the DRCN of Fig.(4.1).

It was suggested [43] that the probability of the presence of pin-holes in the dielectric layer can be minimized by two layers of dielectric printed with double the squeegee pressure and a second printing pass in the same or opposite direction. Great cleanliness in processing, with clear air passing over the printer and the prevention of dust particles falling on levelling or drying prints gives useful second order improvements. Carefully tensioned stainless steel screens and viscosity control of the paste both contributed to the successful elimination of pin-holes in most of the dielectrics.

Ratios of the resistance on a dielectric to the one on the substrate vary within a few decades in some cases. As an example, during the firing of a particular resistor ink deposited on top of an insulator [42], glass migrates from the resistor into the insulator causing a catastrophic drop in resistance to about 150 Ω instead of 5 M Ω (as designed).

The high permittivity dielectric inks relay for their properties on filling a glaze with a ceramic of the titanate type and are all currently of the form which react very much with the resistors. However, the introduction of thick film multilayer networks brought about new crystallizing dielectrics [44], and hence made it possible to print resistors on top of dielectrics with a resistance drop which was in many cases very much less pronounced. Using crystallizing dielectrics, acceptable results have been obtained over the whole range of sheet resistances [5]. The main disadvantage with crystallizing dielectrics is their low permittivity which results in a limited capacitance density. For complete elimination of the short circuits between the top resistor and the bottom conductor and to increase the yield, at least three layers of dielectric are required

to be printed and fired [43] even though the large thickness (35-45 micrometers) of the dielectric layers reduces the capacitance of the whole structure even further.

To conclude this section, some problems associated with the materials for producing good quality resistors on top of a dielectric surface have been solved by the recent improvements in the materials that have become available for use in thick film technology and also by the increased accuracy in the process. It is now possible to produce good quality resistors on multilayer dielectrics with values very close to those obtained on alumina[31].

4.3 PARTICULAR CONSIDERATIONS IN FABRICATION OF THE FDRC NETWORK

The structure of a fully distributed RC (FDRC) network consists of a resistor layer followed by an insulating (dielectric) layer followed by another resistor layer. The process of building up the FDRC structure involves printing and firing a dielectric onto a resistor layer, which is a new process in thick film technology. The problems of printing a thick film resistor onto a dielectric film have been studied by several workers [5,31,32,42,43] (see section 4.2), and a considerable body of information exists on this subject. However, the printing of thick film dielectrics onto resistor films, as is required in the fabrication of an FDRC, has not been reported before and therefore the problems of material interaction and compatibility have not previously been solved and are the subject of study in this work.

Table (4.1) shows the different stages in the process for the building up of an FDRC structure. It can be seen from Table (4.1) that the bottom resistor is fired five times after the completion of the overall process. It is important that refiring has either little

effect on the electrical properties of the resistor or has a predictable effect which can be taken into consideration during the circuit design.

PRINT	CONDUCTOR 1
LEVEL 10 Minutes	
DRY at125^{O} C, 15Minutes	
FIRE	
PRINT	RESISTOR 1
LEVEL,DRY&FIRE as above	
PRINT	DIELECTRIC 1
LEVEL,DRY&FIRE	
PRINT	DIELECTRIC 2
LEVEL,DRY&FIRE	
PRINT	DIELECTRIC 3
LEVEL,DRY&FIRE	
PRINT	CONDUCTOR 2
LEVEL,DRY&FIRE	
PRINT	RESISTOR 2
LEVEL,DRY&FIRE	

Table (4.1) Printing and firing sequence

4.4 MATERIAL SELECTION

Material selection is a critical step for the thick film circuit designer and is particularly important in applications such as the fabrication of multilayer distributed RC networks where process techniques are significant factors in producing an acceptable circuit. The selected material must combine "processability" with the desired performance of the fired films and the chosen material system must often be a balance between these two factors. The dielectric, the resistors and the conductor terminations in an FDRC network should be carefully selected for compatibility, or various chemical and physical reactions, both visible and invisible, may occur.

The thick film inks commercially available so far have not been developed to fulfil the necessary requirements for printing and firing of a dielectric on top of a resistor owing to lack of demand. In order to define and solve the existing problem of producing good quality resistors both underneath and on top of a dielectric layer and to assess the compatibility of the ink combinations, investigations had to be carried out on a number of combinations of dielectric and resistor inks. As the number of all combinations considering all the commercially available materials, was potentially very large, some restrictions had to be made on the choice of the inks.

The FDRC networks fabricated in this research are to be used in electronic circuits such as filters and oscillators, etc. The main objective being to use the FDRC network as a notch filter with the notch frequency ranging from 50kHz to 10MHz. From equation 2.57:

$$f = 19.75 / [2 \pi RC (1+N)] \qquad 4.1$$

where $N = 0.086266$ 4.2

N is the ratio of the two resistor values in the FDRC and F is the notch frequency of the device. It has been shown [5] that with low permittivity dielectrics a capacitance of about 2pF/mm can be obtained in a distributed RC network. Assuming this to be also true for an FDRC network, a capacitance of about 300pF is obtainable with an area of 20mm by 8mm. Using this value and equations 4.1 and 4.2, the approximate limits for R can be obtained as follow:

$$50\ \text{KHZ} < F < 10\ \text{MHZ}$$

$$1\ \text{K}\Omega < R < 200\ \text{K}\Omega$$

Therefore, sheet resistances of 1KΩ/sq , 10KΩ/sq and 100KΩ/sq with a number of low permittivity dielectrics were considered for use in the first investigation. Investigations of the resistor - dielectric ink combinations have been carried out and the details of each investigation are given in sections 4.7 to 4.19.

4.5 SUBSTRATE CODIFICATION FOR THIS RESEARCH

The method of coding the substrates in this research is such that identification of the inks used for each FDRC device is quick and very simple. Alphabetic letters are assigned to each resistor ink and single digit numbers are assigned to each dielectric ink. Tables of the resistor and dielectric inks used in this research together with their codes are given on page 66.

The first item of the code is always an alphabetic letter and represents the first resistor (bottom resistor). The next three numbers in the code refer to the three dielectric layers and, finally, the lower case letters after the numbers represent the second resistor (top resistor).

4.6 FDRC NETWORK PATTERN CONSIDERATIONS

An ideal FDRC network has a 100% distribution between the top and bottom resistors. However, in practice, due to the inherent limitations of thick film technology, it is not possible to get 100% distribution. This departure from the ideal occurs because some area has to be reserved for the terminals of the resistors. The two possible pattern designs for an FDRC network are shown in Fig.(4.3a) and (4.4a).

Referring to patterns of Fig.(4.3a), d1 and d2 are the two undistributed areas corresponding to the top and bottom resistors respectively. Although the undistributed resistors, which are parasitics to the distributed parts, can be minimized by reducing the areas d1 and d2, they can increase in value depending on the sheet resistances of the inks . The electronic equivalent circuit of the structure of Fig.(4.3a) is shown in Fig.(4.3b).

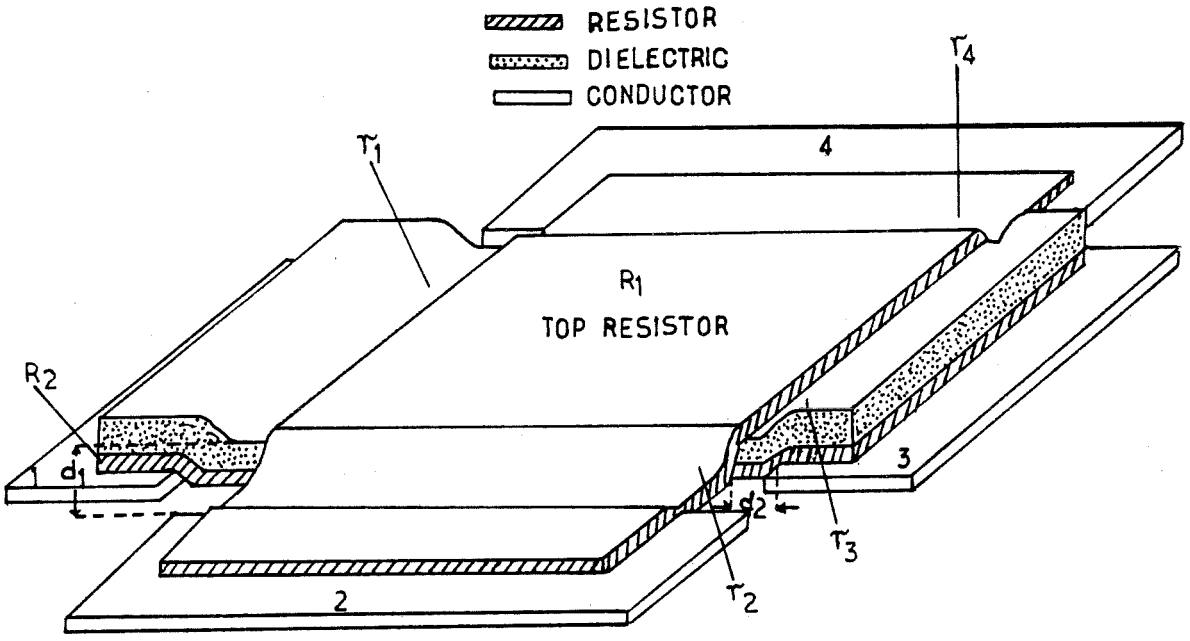


Fig.(4.3)a Structural design of a thick film FDRC network.

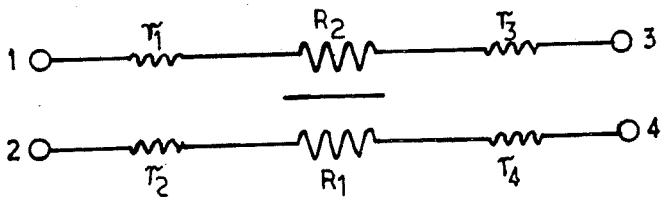


Fig.(4.3)b Equivalent circuit of Fig.(4.3)a.

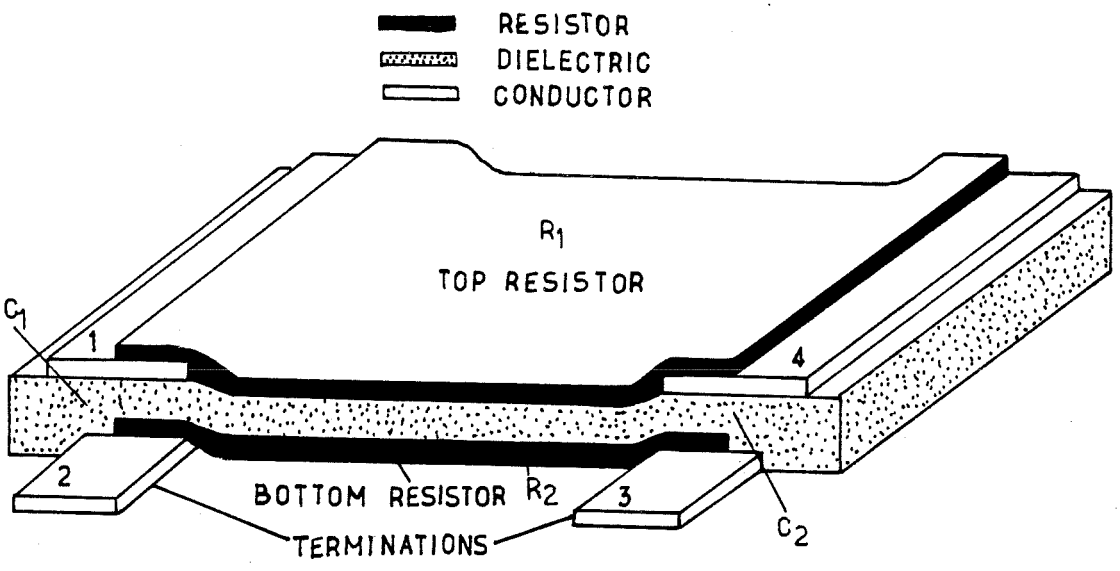


Fig.(4.4)a Structural design of a thick film FDRC network.

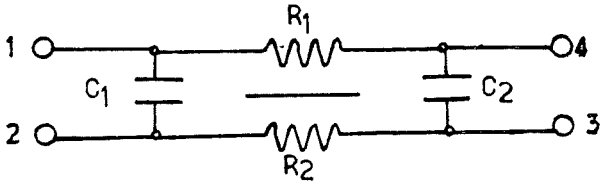


Fig.(4.4)b Equivalent circuit for Fig.(4.4)a.

Consider the pattern of Fig.(4.4a). Here, one resistor together with its terminals areplaced on top of the other resistor. Although the resistors seem to have 100% distribution (ie if the resistors are printed with the same screen and ignoring any misalignment and inaccuracy), there are some undistributed capacitances owing to the conductor terminals (required for the resistors), one lying on top the other. These undistributed capacitances can be minimized by making the resistor terminals very narrow. However, these parasitic capacitances are bound to be very small due to the low permittivity of the dielectric material. Fig.(4.4b) shows the electronic equivalent circuit of the structure of Fig.(4.4a). Since consideration of the undistributed parts in the analysis of the FDRC makes the mathematics very difficult, it is advisable to choose a technique in which the undistributed parts are very small and hence negligible .

Comparison of the above patterns suggests that the parasitic effect in the pattern of Fig.(4.4a) is very much less than that of Fig.(4.3a). In conclusion it can be said that there are always some inherent parasitic resistance and/or capacitance associated with the thick film fully distributed RC networks which cannot be eliminated. The thick film pattern of Fig.(4.4a) is used throughout the investigations in this research.

4.7 INVESTIGATION (1)

In this investigation, a quick test on the degree of resistor - dielectric compatibility was carried out by printing a number of dielectric inks onto several resistors using a very simple pattern of two resistors on substrates of 1/2" by 1/2", Fig.(4.5).

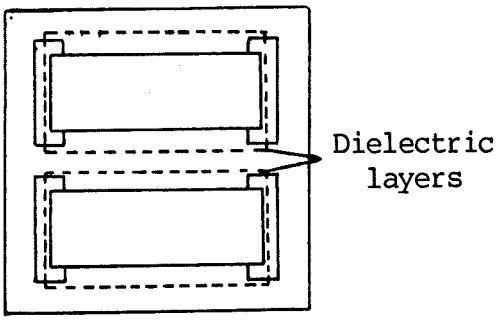


Fig.(4.5) The pattern designed for investigation (1).

A judicious selection of 1kΩ /sq., 10kΩ /sq. and 100kΩ /sq. resistor inks and some crystallizing and filled glaze dielectric inks with low permittivity of about 9-12 was made. The inks selected are listed in tables (4.2) and (4.3) where possibles the inks were selected from the college (Middelesex Polytechnic) stock. Only in a few cases were they obtained specially for this research. The letter codes (A).....(J) and the number codes (1).....(7) are assigned to resistor and dielectric inks respectively, and the substrates are marked according to the resistor and dielectric codes. The ESL 9635 B conductor ink was used to make terminations for all the resistors in this examination.

Manufacturer	1000Ω/sq	10000Ω/sq	100000Ω/sq
ESL	3113 (a) 2813 (A)	3114 (b) 2814 (B)	3115 (c) 2815 (C)
DuPont	1331 (D)	1341 (E)	1451 (F) 9477 (G)
EMCA	5033 (H)	30K5034(I)	-----
Elect-Film	-----	1040 (J)	-----

Table (4.2) Resistor inks selected for investigation (1)

Manufacturer	Type No. of the Dielectric Inks.		
Dupont	9427 (1)	9429 (2)	9950 (3)
Heraprint	IP 065 (4)	-----	-----
ESL	4608CFBM2(5)	4903 (6)	-----
Englehard	33-390 (7)	-----	-----

Table (4.3) Dielectric inks selected for investigation (1).

To monitor the change, due to refiring only, in the resistor values, substrates with control resistors were also refired the same number of times as the other substrates. Any change in the values of the resistors with dielectric, other than the change in the control resistors was considered to be due to the presence of the dielectric on top of the resistors.

The measure of compatibility of a resistor and a dielectric ink corresponds to the amount of interaction between the two layers. Some combinations of inks showed apparent interaction between the dielectric and the resistor in the form of bubbling of the dielectric surface and also a very significant change in resistance when compared with the control substrates. Fig.(4.6) shows the dielectric surface of two incompatible inks.

Graphs of the firing characteristics of the resistor inks were obtained and are shown in Fig.(4.7)a,b,c and d, and in Fig.(4.8)a,b,c and d.

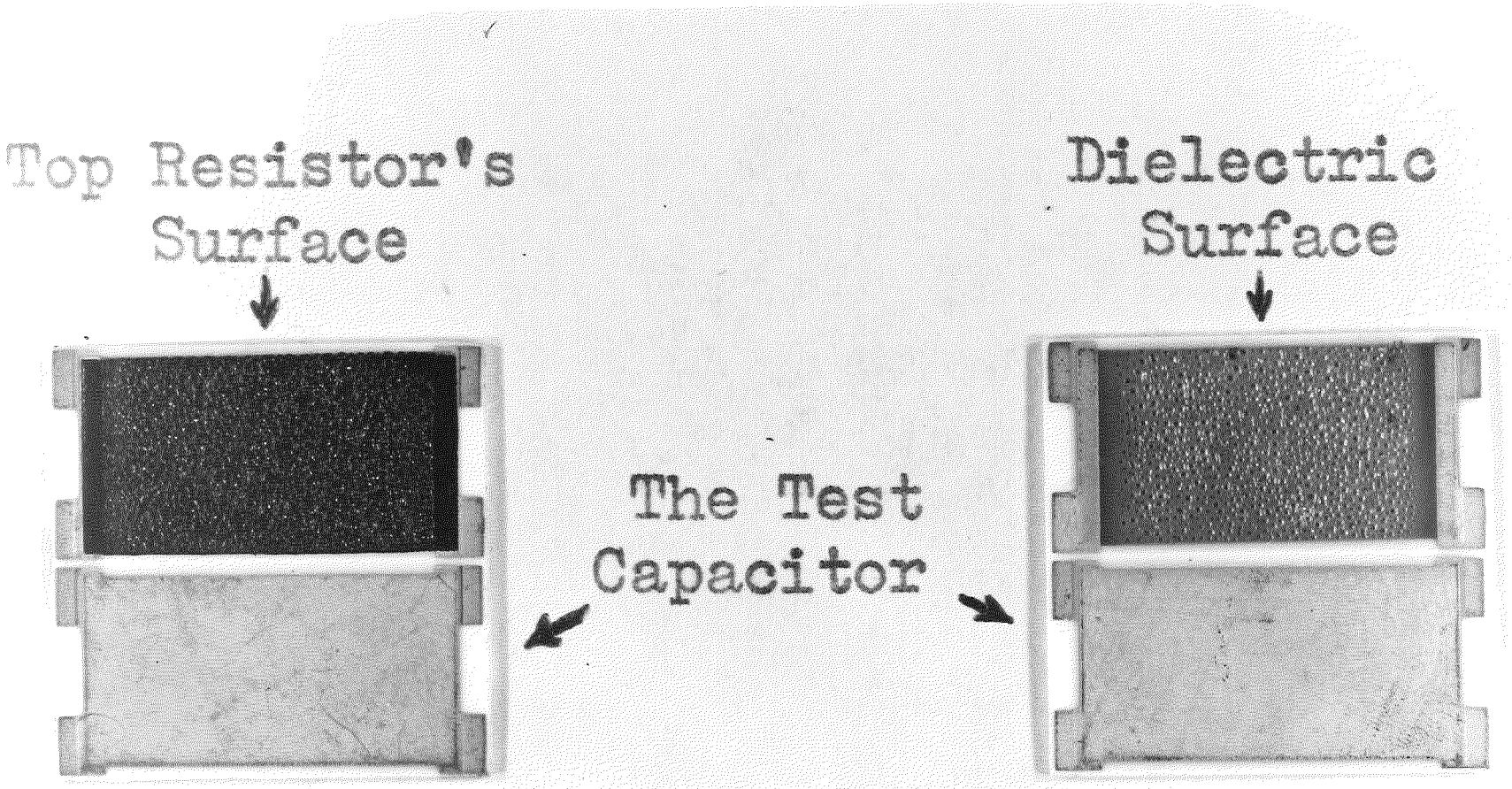


Fig.(4.6) Dielectric surface of two incompatible inks.

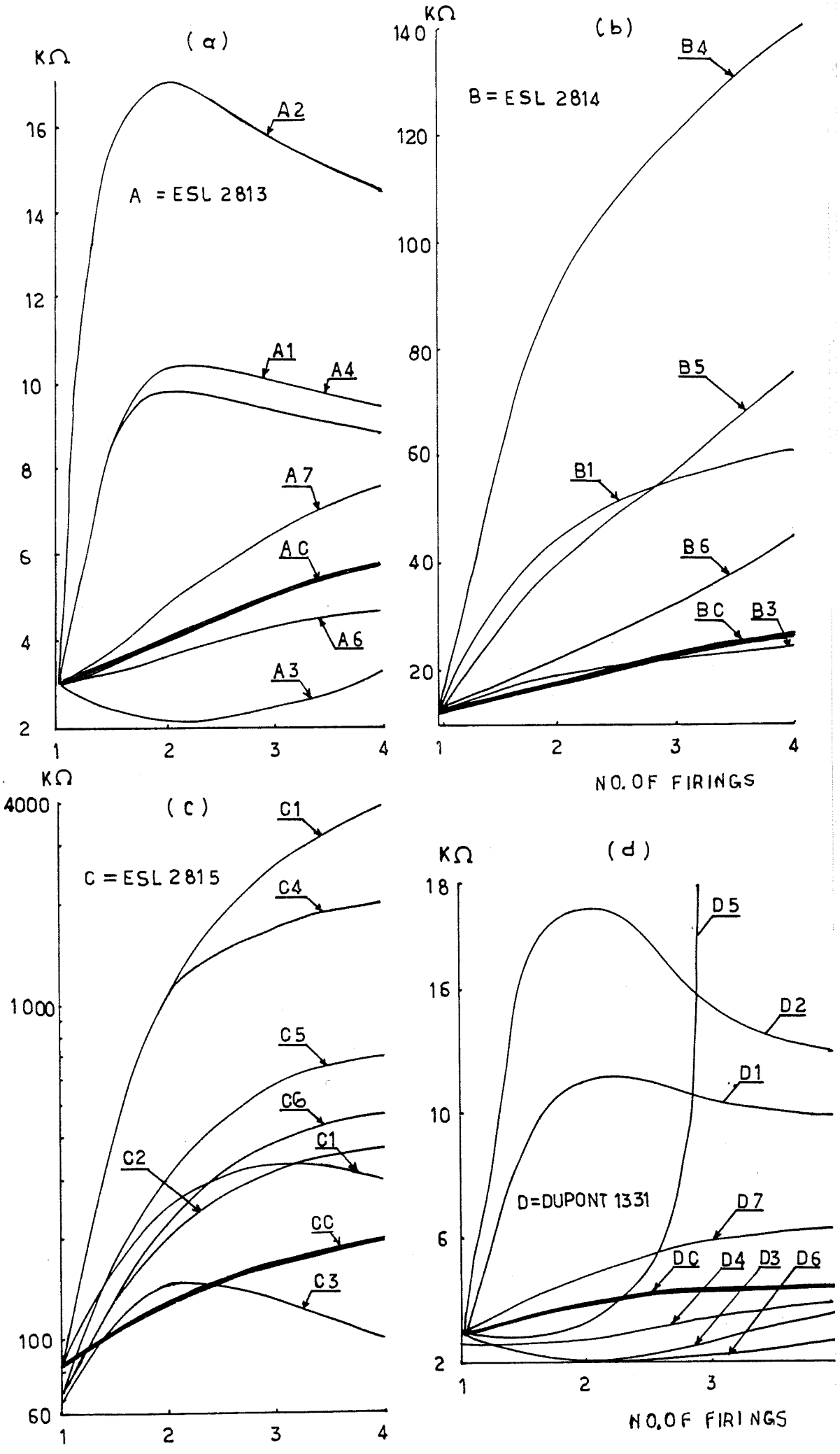


Fig.(4.7) Firing characteristics of the resistor inks used in investigation (1) with some dielectric inks.

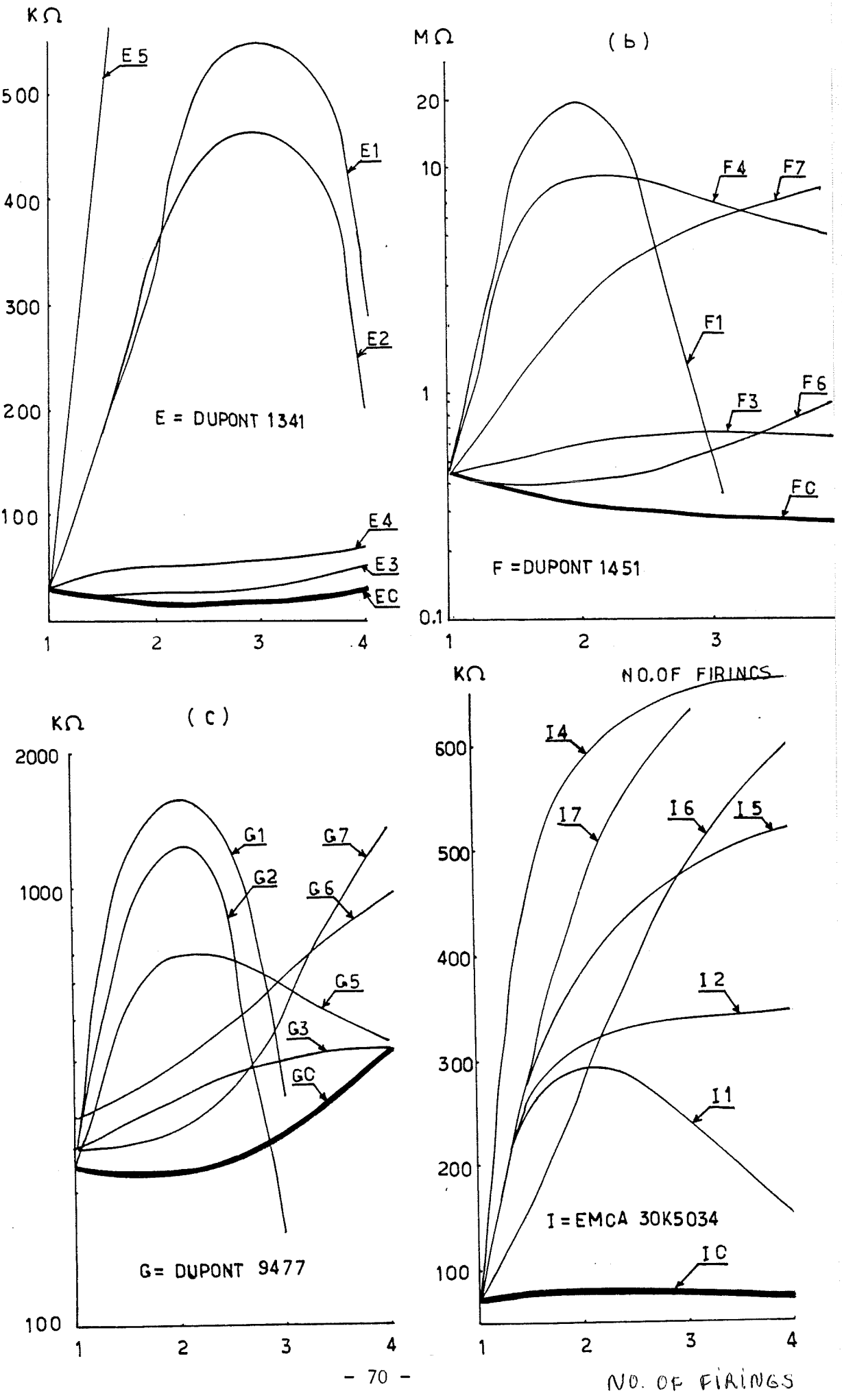


Fig.(4.8) Firing characteristics of the resistor inks used in investigation (1) with some dielectric inks.

4.8 DISCUSSION

In figures 4.7 and 4.8 the horizontal axis shows the number of refirings and the vertical axis shows the variations in resistance after each firing. The graphs of the control resistors are marked with the resistor ink code followed by a 'C' which stands for control.

In this research, the resistors with firing characteristics very close to the control resistors are considered as being 'good' and the resistors which have characteristics similar to and not very far from the control resistors are considered as being 'promising' and the ones with firing characteristics very far form the control resistors are considered as being 'unacceptable'. Graphs of figures 4.7 and 4.8 were studied and, considering the criteria just given, a summary of the results for all the resistor - dielectric ink combinations are given in tables (4.4), (4.5) and (4.6).

The Dupont 1400 resistor series is designed to be compatible with low K dielectrics such as Dupont 9950 (3) when the resistor is printed on top of the dielectric. In this programme, the low K dielectrics were printed on top of the Dupont 1400 resistor series and the results showed no compatibility between the two inks. Therefore, it can be concluded that the material requirements for both the resistor and the dielectric compositions, depending on whether the resistor is printed underneath or on top of the dielectric, are very different.

Resistor ink		Dielectric ink
ESL 2813 (A)	with	ESL 4903 (6)
ESL 2814 (B)		Dupont 9950 (3)
Dupont 1331 (D)		Heraprint IP065 (4)
Dupont 1341 (E)		Dupont 9950 (3)

Table (4.4) List of "GOOD" resistor - dielectric combinations.

Resistor ink		Dielectric ink
ESL 2813 (A)	with	Dupont 9950 (3)
ESL 2815 (C)		Dupont 9950 (3)
Dupont 1331 (D)		Dupont 9950 (3) and ESL 4903 (6)
Dupont 1331 (E)		Heraprint IP065 (4)

Table(4.5) List of "PROMISING" resistor -dielectric combinations.

all the combinations of the following resistor inks		
ESL 2813 (A) ESL 2814 (B) ESL 2815 (C) Dupont 1331 (D) Dupont 1341 (E)	with	Dielectrics other than the ones mentioned in tables(4.4) and (4.5).
Dupont 1451 (F) Dupont 9477 (G) EMCA 30K5034(I)	with	all the dielectric inks
EMCA 5033 (H)		no results could
Electrofilm 1040(J)		be obtained

Table(4.6) List of "UNACCEPTABLE" resistor - dielectric combinations.

4.9 INVESTIGATION (2)

In this section a number of new resistors and two of the resistors used in investigation (1), in conjunction with some of the dielectric inks were examined for compatibility. A list of the resistors and dielectric inks with their codes and the conductor inks for the resistor terminations used in this investigation are found in tables(4.7) a, b and c respectively.

Dupont	1331	D
ESL	3913	K
ESL	3914	L
ESL	3915	M
ESL	2813	A

(a) Resistor Inks for the first resistors layer

Englehard	33/390	(7)
Heraprint	IP065	(4)
ESL	4903	(6)
Dupont	9950	(3)

(b) Dielectric inks

ESL	3114	(b)

(c) Resistor ink for the second resistor layer

First resistor termination	ESL	9635
Second resistor termination	ESL	9695

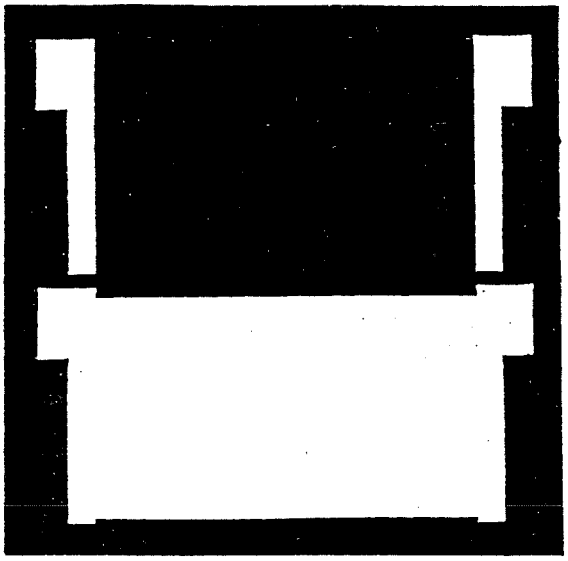
(d) The conductor inks for the resistors terminations

Table (4.7) The Inks used in Investigation (2)

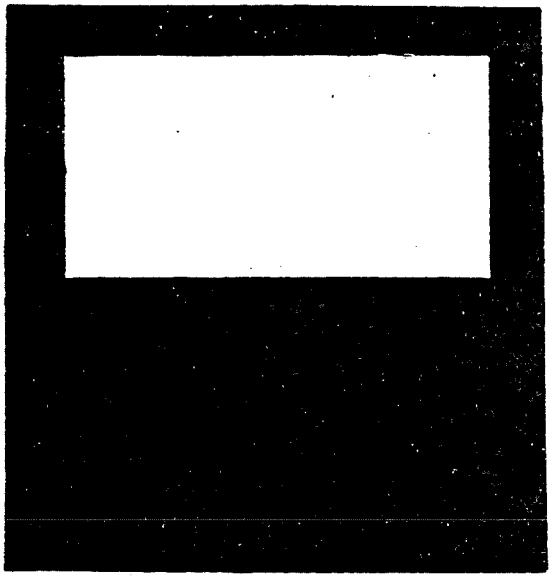
Substrates of size 1" by 1" and the patterns of Fig.(4.9) were used for this investigation. Half the area of the substrate was allocated for the distributed network and the other half was reserved for a capacitor (ie conductor- dielectric- conductor) of exactly the same size as the distributed network. The object of including this capacitor is to enable us to investigate the difference between the overall capacitance of the distributed network (ie the capacitance between the top and bottom resistors of the distributed network) and the capacitance of the discrete capacitor of the same size.

To design an FDRC notch filter R and C in equation 4.1, page 59, should be chosen to result in the required notch frequency. To estimate the capacitance obtained per unit area in an FDRC structure, let us go back to the results obtained previously by other workers on the DRCN. The capacitance of the DRCN obtained by the conductor-dielectric- resistor structure of Fig.(4.1) was measured [5] to be approximately 2pF per square millimetre. And since the conductor electrodes of the capacitor in DRCN of Fig.(4.1), is replaced by a resistor layer in FDRC network of Fig.(4.4a), the capacitance of the FDRC network is bound to be less than 2pF/sq mm This is because of the reduced conductivity in one of the capacitor's electrodes. From this argument we can estimate the capacitance corresponding to the structure of Fig.(4.4a) to be 1.5 pF/sq mm and the maximum practical area for the distribution of the two (ie the top & bottom) resistors on half of the area of a 1" by 1" substrate to be 20mm by 9mm.

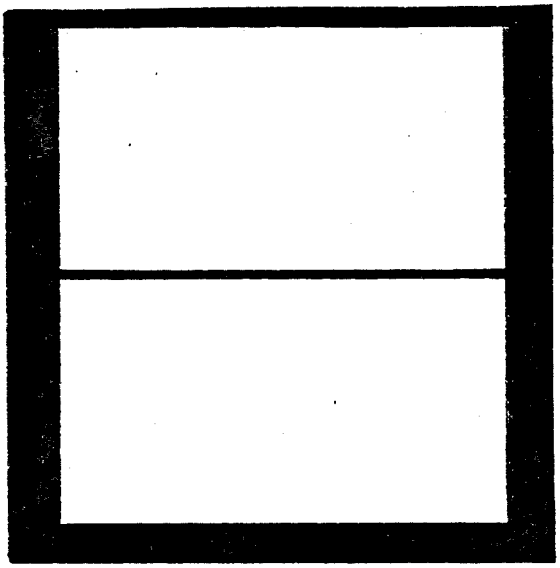
$$20 \text{ mm} \times 9 \text{ mm} \times 1.5 \text{ pF/mm} = 270 \text{ pF} \qquad 4.3$$



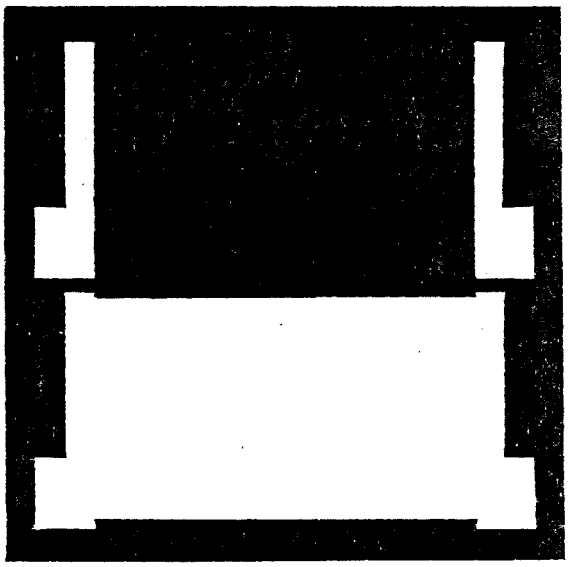
(a) Bottom Terminations



(b) Bottom and top Resistors



(c) Dielectric insulator



(d) Top Terminations

Fig.(4.9) The pattern designed for investigation (2).

Therefore, a capacitance of about 270pF should be obtained from this area. Using equations 4.1, 4.2 and 4.3 and recalling that the sheet resistances of materials to be used were in the range of 1 k Ω to 100 k_{Ω}, we have:

$$\text{if} \qquad 2\,k < R < 200\,k$$

$$53\,kHz < F < 5.3MHz$$

which is an appropriate frequency range for handling.

Using a home made tensioned 300 mesh stainless steel screen, the patterns were deposited. The inks given in Table (4.7) were printed and fired in the sequence given in Table (4.1) and in accordance with the manufacturers' recommended profiles.

Seven substrates were used for each resistor - dielectric ink combination (see table 4.7), and any change in resistance was recorded after each firing. The changes in resistance for each combination were averaged and plotted against the corresponding number of firings. These graphs are shown in Fig.(4.10) a, b and Fig.(4.11) a, b and c. It must be pointed out that these resistances all correspond to the first (bottom) resistor layer of the FDRC network.

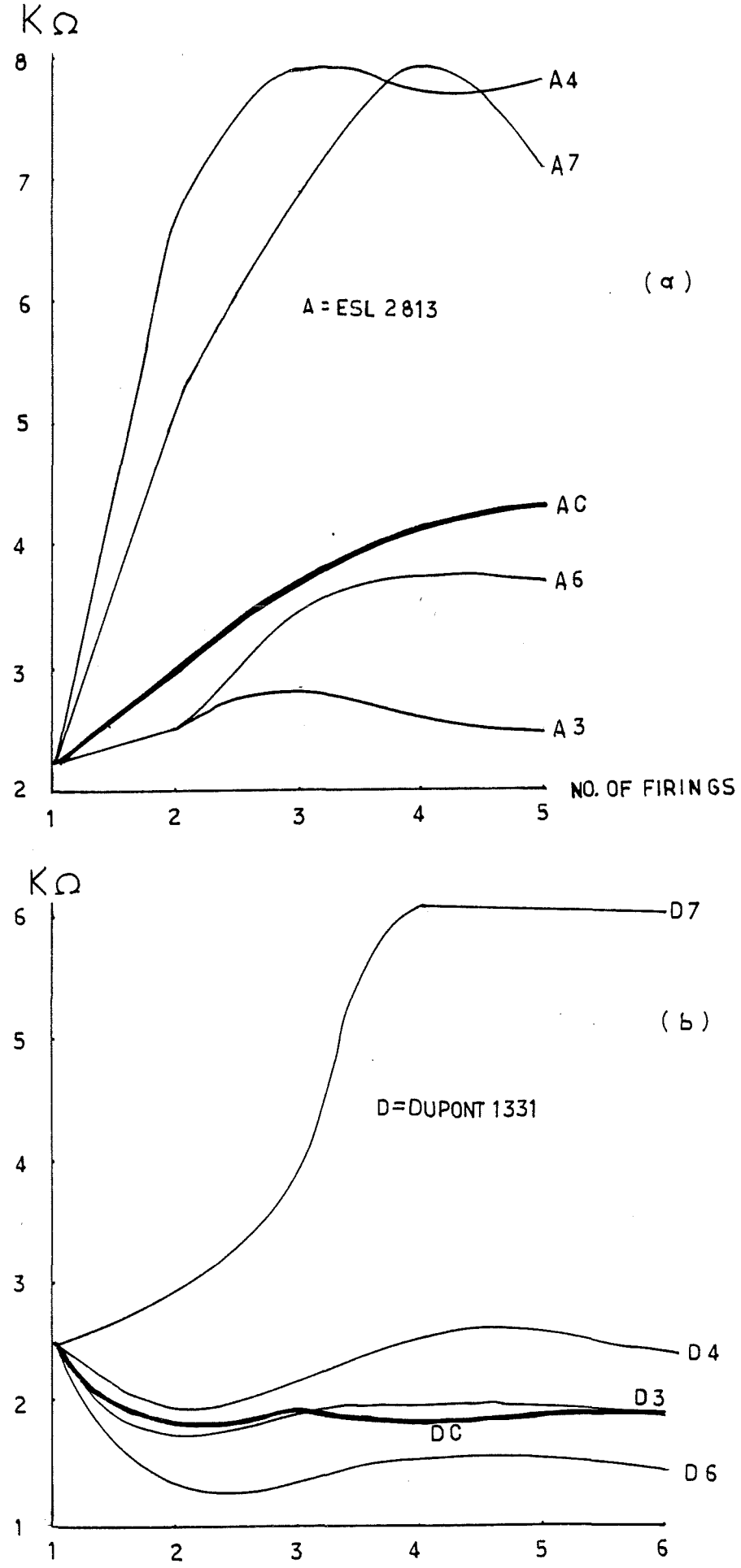
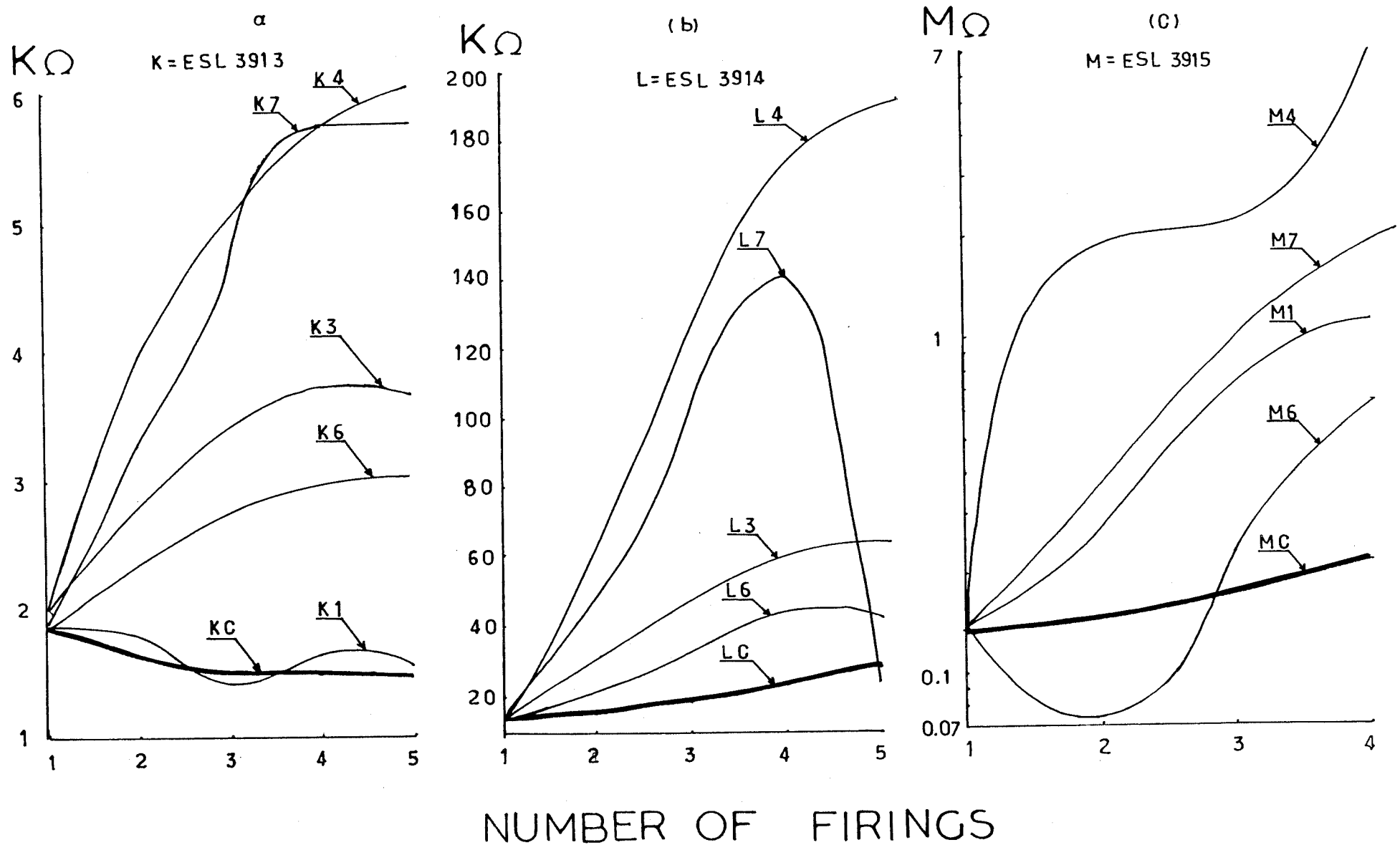


Fig.(4.10) Firing characteristics of resistors A and D with dielectric 3, 4, 6 and 7- see Table (4.3).

Fig.(4.11) The firing characteristics of resistors K, L and M with dielectrics 1, 3, 6 and 7.



4.10 DISCUSSION

From the results of the above two investigations it is apparent that the higher sheet resistance inks (10kΩ /sq and 100kΩ /sq) are less compatible with the dielectric inks than materials of lower resistance.

The recommended firing temperature of the ESL 2800 resistor series is 780°C, if the instructions given by the manufacturer are not practised, then a change in the characteristics of the resistor may be expected. In this research the ESL 2800 resistors have to be refired several times at temperatures higher than 780°C (ie. 850°C) because of the subsequent top layers. This makes it impractical to predict the value of the resistances after the completion of the process and because of a probable large departure from the design value. Trimming may not be possible in some cases.

However, referring to the graphs of resistor A in Fig.(4.10)a, the refiring characteristic of A6 substrates is quite close to the control substrates. This means that ESL 2813 (A) resistor ink and ESL 4903 (6) dielectric ink are less mutually interactive than the combinations of ESL 2813(A) and other dielectrics. However, after printing and firing the second resistor layer ESL 3114 (b) over the dielectric layer ESL 4903 (6), tests indicated electrical short circuits between the top (ESL 3114 (b)) and the bottom (ESL 2813 (A)) resistors. Despite the good firing characteristics of D444, D666 and K111 substrates (see Fig.4.10 and 4.11) these electrical short circuits were also measured between the top and the bottom resistors of these substrates. This indicated that Heraprint IP065 (4), ESL 4903 (6) and Dupont 9427 (1) dielectric inks could not provide the necessary insulation between the top and bottom resistors, in this investigation.

Up to this point, only the combination of Dupont 1331 (D) resistor and Dupont 9950 (3) dielectric inks had given good firing characteristics and sufficient insulation to avoid any short circuit. The following list gives the inks that had resulted in a successful construction of an FDRC device.

1. ESL 9635 conductor termination for the first resistor.
2. Dupont 1331 (D) resistor as the first resistor layer.
3. Three layers of Dupont 9950 (3) dielectric as the insulating layer.
4. ESL 9695 conductor termination for the second resistor.
5. ESL 3114 (b) resistor as the second resistor layer.

It was thought that the probability of interaction between the resistor and the top dielectric layers may be reduced if the peak firing temperature of the dielectric layer was lower than the peak firing temperature of the resistor. In fact, one way out of the interaction problem seemed to be reducing, in descending order, the firing temperatures of successive layers. This appeared to offer the following prospects:

1. The refiring process would have less effect on the fired resistor.
2. The layers that had already been fired, would not get to the melting temperature again. Therefore, decreasing the firing temperature would decrease the chance of the adjacent layers interacting with each other.

To examine these possibilities, a set of inks for the two resistors, the dielectric layer and the conductor terminations was selected such that firing temperatures in descending order could be used. These inks are listed in table (4.8) and considered for use in the next investigation.

	Type of ink	Firing temperature
Resistor (1)	ESL 3900 series	10-12 min. at 850°C
Dielectric	EMCA 9041 (8)	10-12 min. at 600-750 °C
Resistor (2)	ESL 3100 series	10-15 min. at 625 °C

Table (4.8) Proposed for Investigation (3)

4.11 INVESTIGATION (3)

The pattern of Fig.(4.9) was used on a 1/2" by 1" substrate. In this investigation the capacitor on the pattern was eliminated. Using table (4.8), the following ESL 3900 resistors, which were available in stock, and Dupont 3113 (D) were used as the first resistor layer:

ESL 3912 (α)

ESL 3994 (β)

ESL 3995 (γ)

Dupont 1331 (θ)

The multilayer crystallizing low K (ie ε = 12-14@ 1KHz) EMCA 9041 (8) dielectric was used as the insulating layer and the following ESL 3100 resistors were printed as top resistor layers:

ESL 3112 (d)

ESL 3113 (a)

The conductor inks ESL 9635B and ESL 9695 were used for the terminations of the bottom and top resistors respectively. All the layers were printed and fired consecutively as indicated in Table (4.1). The firing temperature for each ink was that already given in Table (4.8). The variations of the first resistor were recorded after each firing and graphs of the resistance variations against the corresponding number of firings were plotted in Fig.(4.12).

After firing the top resistor, tests indicated short circuits between the two resistor layers of all the devices. Therefore, the yield obtained for these combinations of inks was nil.

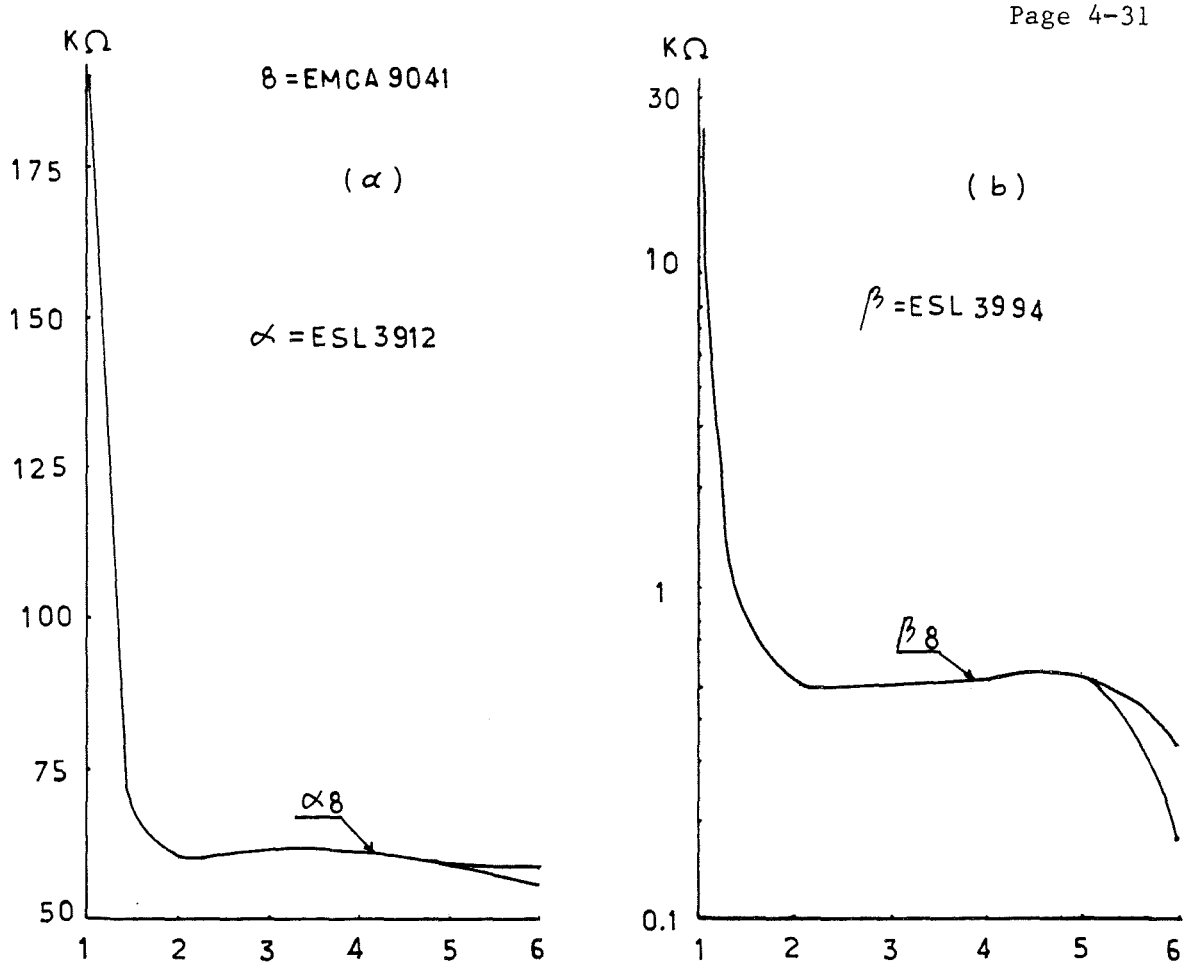
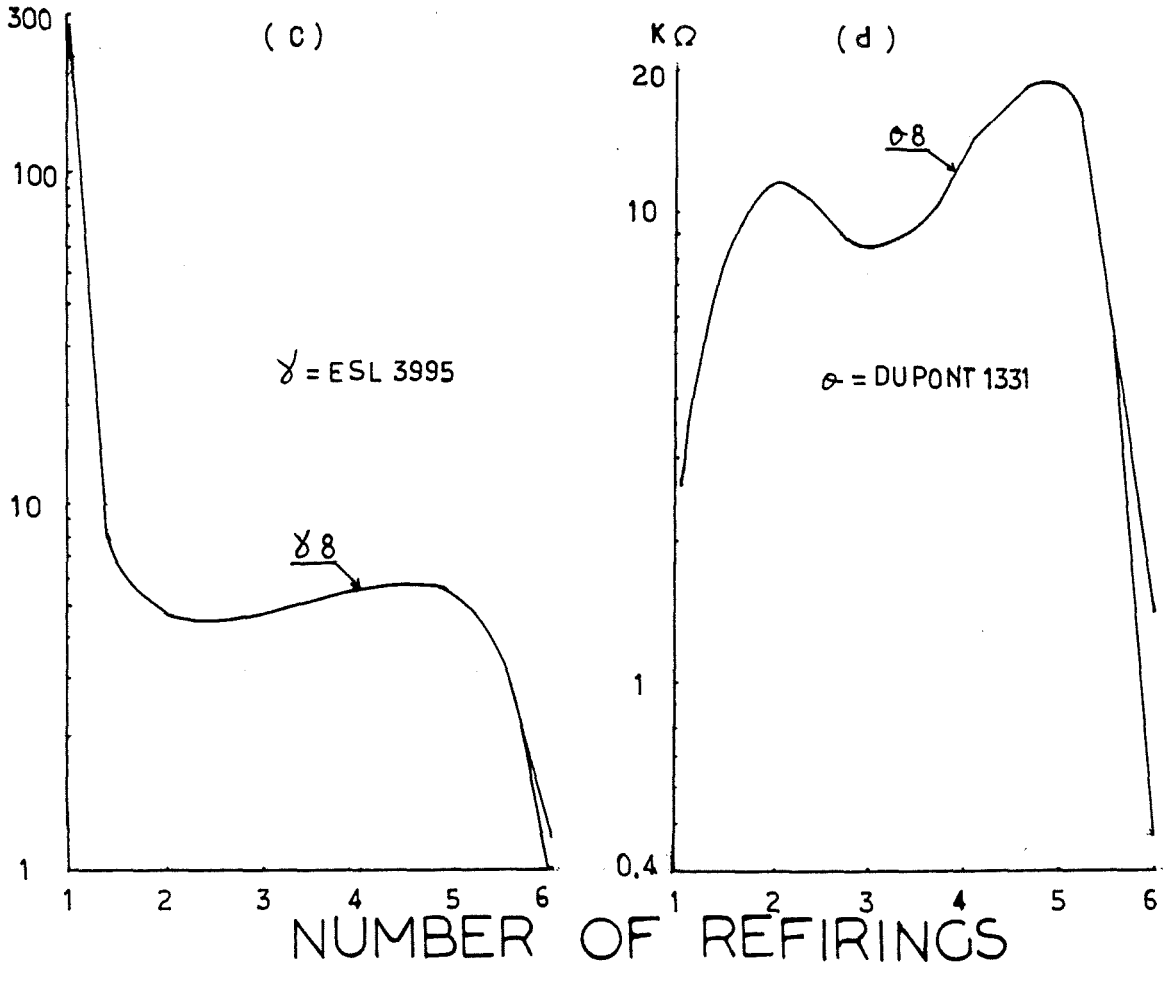


Fig.(4.12) Firing characteristics of resistors α, β, γ and δ with EMCA 9041 dielectric ink.



4.12 DISCUSSION

The existence of the short circuits between the resistor layers gives proof of insufficient insulation provided by the dielectric which results in the interaction between the resistor layers. Graphs of resistors ESL 3912 (α), ESL 3994 (β) and ESL 3995 (γ) in Fig.(4.12) a, b and c indicated a very sharp decrease in resistance after the first dielectric layer was printed on top of the resistor and fired. A second sharp decrease in the value of resistors ESL 3994 (β), ESL 3995 (γ) and Dupont 1331 (δ) was observed when the top resistors were printed and fired.

Although the EMCA 9041 (8) dielectric ink is designed for multilayer applications and despite the fact that firing temperatures in descending order were used, satisfactory results for printing the EMCA 9041 (8) on top of many resistor layers were not obtained. Therefore, the EMCA 9041 (8) was considered to be unsuitable for printing over a resistor layer. However, there was still the possibility that the EMCA 9041 (8) in conjunction with another dielectric material would cause less interaction with the two resistor layers. To examine this possibility, investigation (4) (section 4.13) was arranged and carried out.

4.13 INVESTIGATION (4)

To examine the possibility of using two dielectric materials as the insulating layer between the two resistors of an FDRC network, the EMCA 9041 (8) and the Dupont 9950 (3) which are designed for multilayer applications were selected for use in this investigation. The Dupont 9950 (3) dielectric ink is especially designed to be compatible with Dupont Birox resistors in order to permit the fabrication of resistors over the dielectric. Therefore, the Dupont Birox 1600 series resistor ink was selected for the top (second) resistor in the FDRC network. To save time and substrates, only substrates which had been left over from investigation (2) with the following resistor materials were used:

ESL	3913	(K)
ESL	3914	(L)
ESL	3915	(M)
ESL	2813	(A)
EMCA	5033	(H)

The process stages, considered for printing and firing the consecutive layers, were as follows:

1. Printing and firing one layer of EMCA 9041 (8) dielectric over each of the resistors at 710°C.

2. Refiring the substrates at 850°C the object being to harden the dielectric layer in order to reduce the interaction with the subsequently deposited layers.

3. Printing and firing two layers of Dupont 9950 (3) dielectric succesively, both at 850°C.

4. Printing and firing the conductor terminations for the top resistor at 850°C.

5. Printing and firing Dupont Birox resistor 1600 series at $850^{o}C$.

The resistance changes were recorded after each firing and are given in Table (4.9). In addition to the very sharp changes of resistance after the firing of the EMCA 9041 (8) over the resistors, further abrupt changes and bubbles on the surface were observed when the first layer of Dupont 9950 (3) dielectric was fired. After such a clear indication of interaction and incompatibility between the resistors and the dielectric layers, it was decided not to continue the rest of this investigation. Having tested the combination of EMCA 9041 (8) with a number of resistors with different methods, it was concluded that although the EMCA 9041 (8) was designed for multilayer applications, it could not fulfil the fabrication requirements of the FDRC networks.

Substrate code	First fire	Second fire	Third fire	Fourth fire
K8	1.89	2.16	0.44	0.51
KC	1.88	1.63	1.50	1.48
L8	15.2	79.7	33.8	63.0
LC	15.3	14.8	19.1	20.5
M8	144	47.4	28.9	31.0
MC	131	145	176	195
H8	3.43	1.33	0.54	0.55
HC	3.43	2.98	2.11	1.78
A8	2.29	1.29	0.77	0.91
AC	2.23	2.98	3.76	4.25

Table (4.9) The resistance changes due to refiring, in kΩ.

4.14 INVESTIGATION (5)

It has already been mentioned that the combination of Dupont resistor 1331 (D) with Dupont dielectric 9950 (3) had resulted in the successful fabrication of an FDRC network. In this investigation, further research on the above combination in addition to the combination of resistor (D) with Heraprint IP065 (4) dielectric was carried out. Since the Dupont 9950 (3) dielectric ink is said to be compatible with Dupont Birox resistors investigation on Dupont Birox resistor 1621 (N) with the two dielectric compositions 3 and 4 was also carried out. The Heraprint IP065 (4) dielectric ink was chosen since it had shown a good performance with resistor 1331 (D) in investigations (1) and (2) as shown in Fig.(4.7)d and Fig.(4.10) respectively. Three resistor inks with different sheet resistances were selected from the ESL 3100 series for the top resistors, in order to:

a. evaluate the performance of resistor compositions of different sheet resistances when printed on the resistor-dielectric sandwich of the FDRC devices.

b. evaluate values of ESL3100 resistors of different sheet resistances when fired over a dielectric layer.

c. increase the chance of obtaining the resistor ratio closer to the value of true zero, ie N=0.08627 (see page 31).

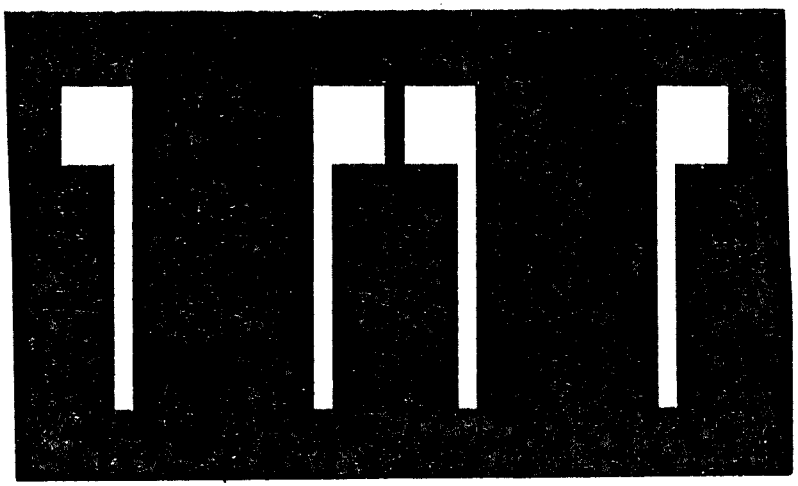
A complete list of the inks used for each FDRC device fabricated in this investigation is presented in Table (4.10).

To study the effect of the physical size upon the performance of the FDRC network, a new pattern with two fully distributed networks of equal sizes for a 1/2" by 1" substrate was designed and is shown

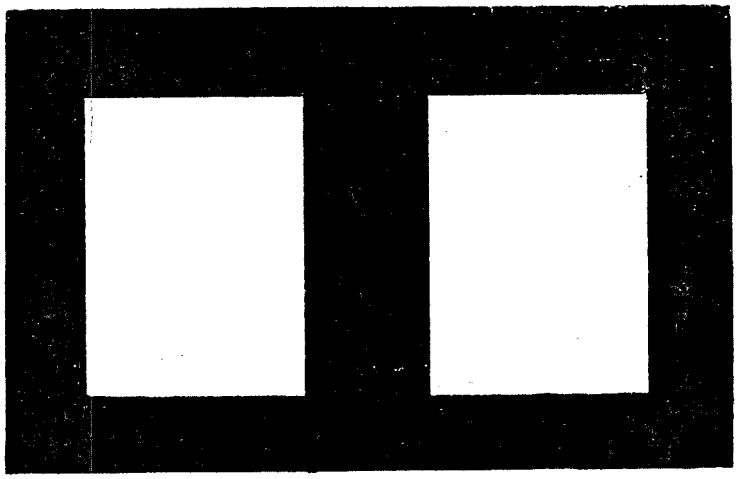
in Fig.(4.13). The screens were prepared and six substrates reserved for each resistor (D & N). Three of these were printed with Dupont 9950 (3) dielectric and the other three with Heraprint IP065 (4). One substrate of each combination was printed with one of the ESL 3100 resistors listed in Table (4.10). The control substrates were also fired the same number of times as the other substrates. After every firing, the resistances were recorded. The graphs of these changes against the corresponding number of firings are shown in Fig.(4.14)a and b. The values of the top and bottom resistors after the last firing, together with the ratio of the two resistors of each device are given in Table (4.11). (The ratios of the resistors are taken in such a way that its numerical value is always less than one).

	Type of Ink	Fired at
Conductor termination for the bottom resistor	Dupont 9061	850°C
The bottom resistor	Dupont 1331(d) and Dupont 1621(N)	850°C 850°C
the dielectric layer	Dupont 9950(3) and Heraprint IP065(4)	850°C 850°C
Conductor termination for the top resistor	ESL 9695	650°C
The top resistor	ESL 3112 (d) ESL 3114 (b) ESL 3116 (e)	625°C 625°C 625°C

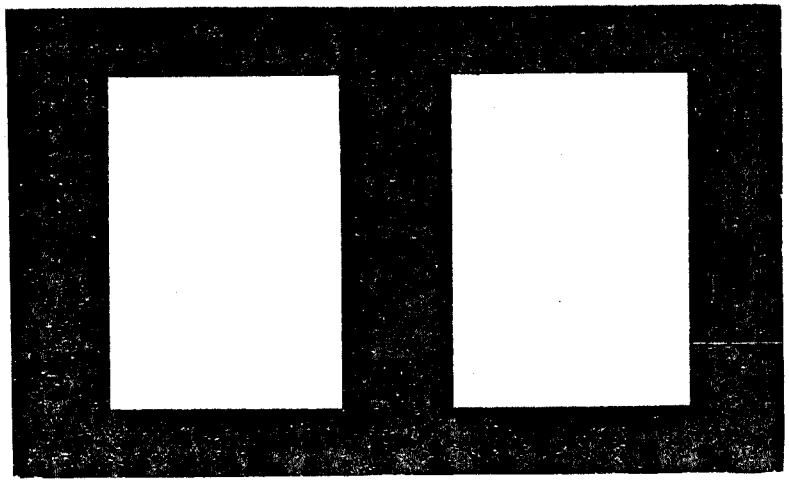
Table (4.10) A complete list of the inks used in investigation (5).



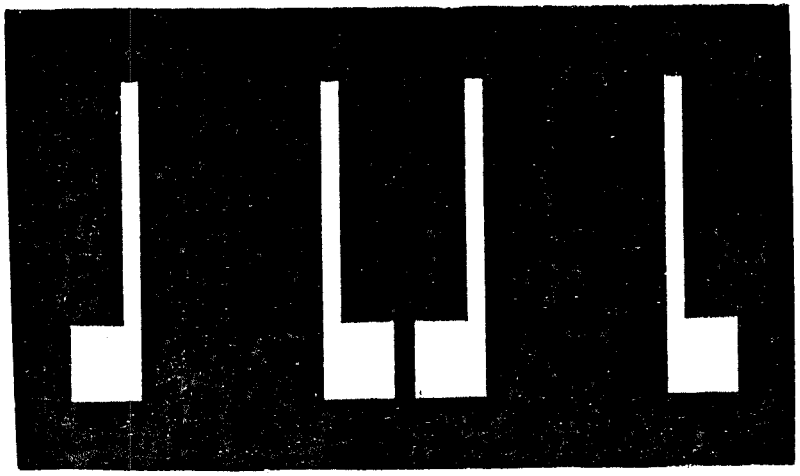
(a) Bottom Terminations



(b) Bottom and Top Resistors



(c) Dielectric insulator



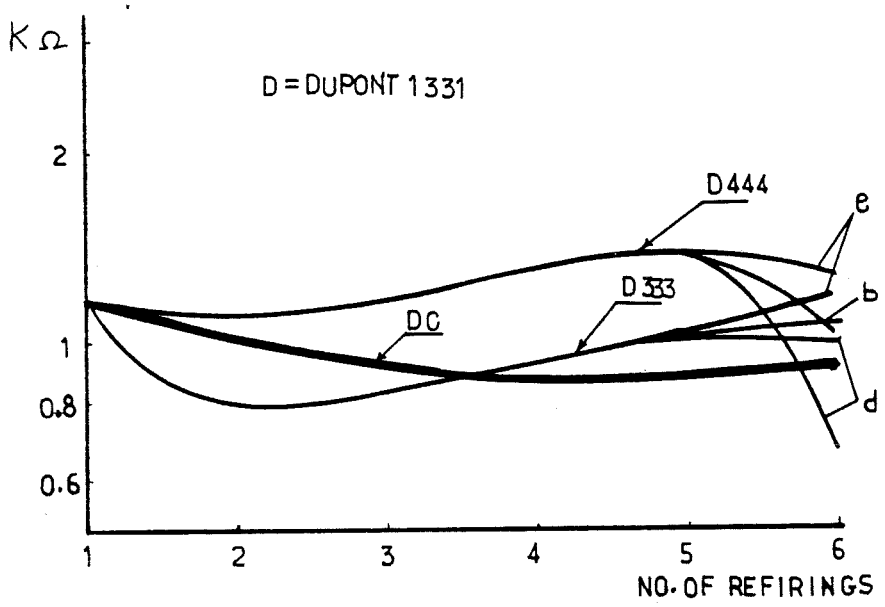
(d) Top Terminations

Fig.(4.13) The pattern designed for investigation (5).

Substrate Code	Bottom Resistor	Top Resistor	Ratio of the Two Resistors
N333 d	202	58	0.287
N333 b	206	560	0.367
N333 e	209	23.6K	0.008
N444 d	108	231	0.467
N444 b	114	11.1K	0.010
N444 e	120	281 K	0.427
D333 d	992	52	0.052
D333 b	1040	657	0.631
D333 e	1130	28.2K	0.040
D444 d	662	179	0.270
D444 b	1030	11.6K	0.094
D444 e	1270	301 K	0.004

Table (4.11) Values of the two resistors of the FDRC networks in Ω.

(a)



(b)

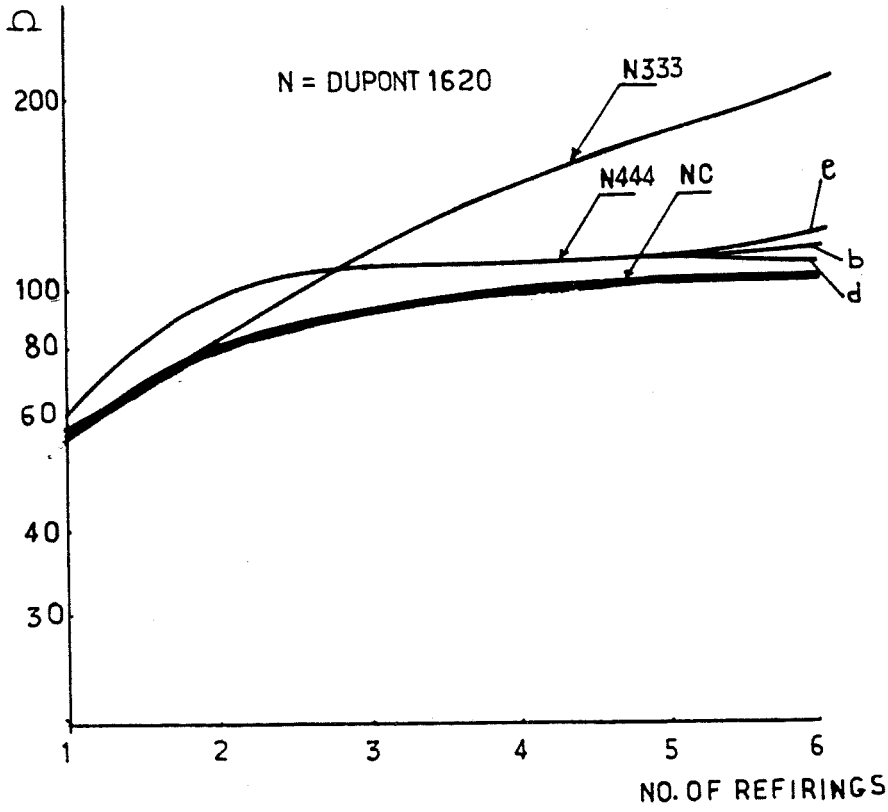


Fig.(4.14) Firing characteristics of resistors D and N with dielectrics 3 and 4.

4.15 DISCUSSION

Referring to the graphs of Fig.(4.14)a, the firing characteristics of both D333 and D444 substrates are quite similar to the control substrate. However, when the ESL 3100 resistors e, b and d (see table 4.10) were printed over the Heraprint IP065 (4) dielectric layer and fired at the sixth firing cycle, some relatively sharp changes in the resistances of the Dupont 1331 (D) (ie the first resistor layer) were observed. This indicates that the presence of the ESL 3100 resistors over Heraprint IP065 (4) has affected the bottom resistor Dupont 1331 (D), causing it to decrease sharply. Substrates with Dupont 9950 (3) dielectric have shown very good compatibility with resistor Dupont 1331 (D) throughout the fabrication process.

The dielectric, Dupont 9950 (3), has shown a better overall compatibility with both the Dupont 1331 (D) (the bottom resistor) and the ESL 3100 resistor (the top resistor) than the Heraprint IP065 (4) dielectric. The results obtained in these combinations confirm the conclusions drawn from investigation (2). From Table (4.11) it can be seen that among the 11 devices fabricated, only the ratio of the resistors of the device D444b is close to the ratio N = 0.08627.

Graphs of Fig.(4.14)b indicate that the resistor Dupont 1620 (N), is more compatible with the dielectric Heraprint IP065 (4) than Dupont 9950 (3). However, the top resistors ESL 3100 e, b and d show less effects on the bottom resistor Dupont 1620 (N) when fired over Dupont 9950 (3) than when fired over Heraprint IP065 (4). This is because the resistor N with dielectric 3 shows a similar change pattern when any of the top resistors e, b and d are printed, see graph of N3 Fig.(4.14)b. Although good isolation is achieved between the first and the second resistors of the FDRC devices fabricated in

this investigation, it appears from the graphs of Fig.(4.14) that the top resistors of lower values tend to reduce the value of the bottom resistors in most cases.

Overall, this investigation resulted in a 100% yield, that is, all the FDRC devices fabricated are free from any short circuits between the two resistor layers and when compared with the corresponding control substrates the firing characteristics of the bottom resistors are quite satisfactory. Therefore, it may be concluded that the fabrication of the smaller size FDRC devices is more successful than that of the larger size devices. Since the two dielectric inks Dupont 9950 (3) and Heraprint IP065 (4) have shown good compatibility with resistor inks Dupont 1331 (D) and Dupont 1620 (N), further research on these inks was carried out in investigation (6).

4.16 INVESTIGATION (6)

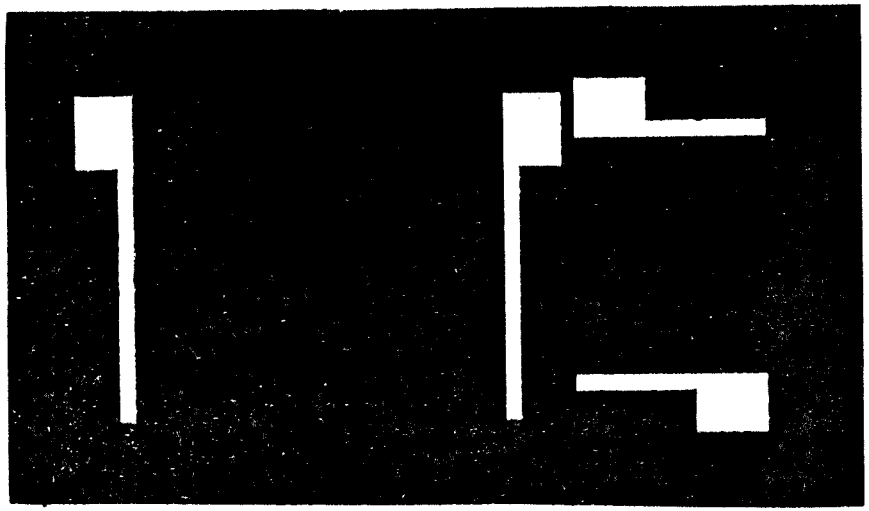
A new pattern of FDRC networks with two different sizes on a 1" by 1/2" substrate was used in this investigation. The pattern for each screen is shown in Fig.(4.15) a, b, c and d respectively. To examine the effects of using the Dupont 9950 (3) and Heraprint IP065 (4) dielectric inks as the insulating layer in the FDRC network, a combination of these dielectric inks in the following sequence was used in this investigation:

1. the first resistor
2. Dupont 9950 (3)
3. Dupont 9950 (3)
4. Heraprint IP 065 (4)
5. the second resistor

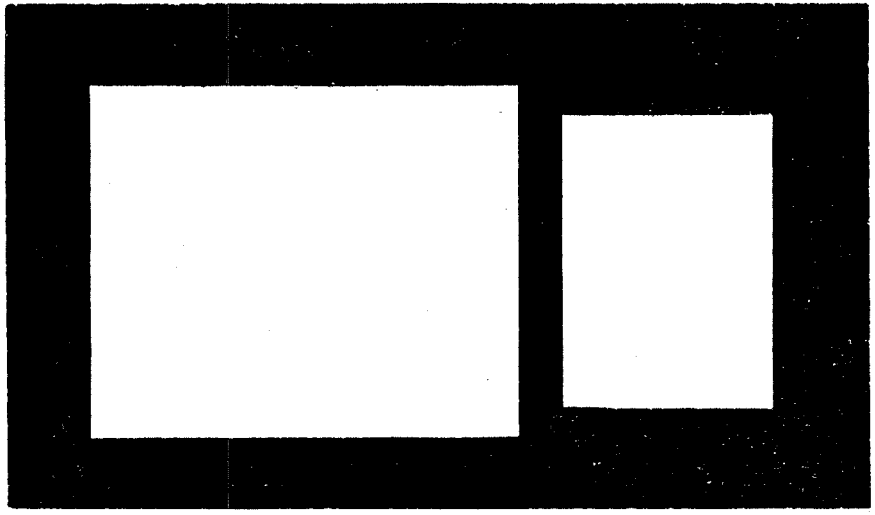
In addition to the inks Dupont 1331 (D) and Dupont 1620 (N), Dupont 1610 (O) was selected as the bottom resistor to examine the feasibility of fabricating an FDRC network with a very low resistance material. The ESL 3100 resistor inks of the following list were selected as the material for the top resistors of the FDRC networks.

I. ESL 3113 (a)
II. ESL 3114 (b)
III. ESL 3115 (c)
IV. ESL 3116 (e)

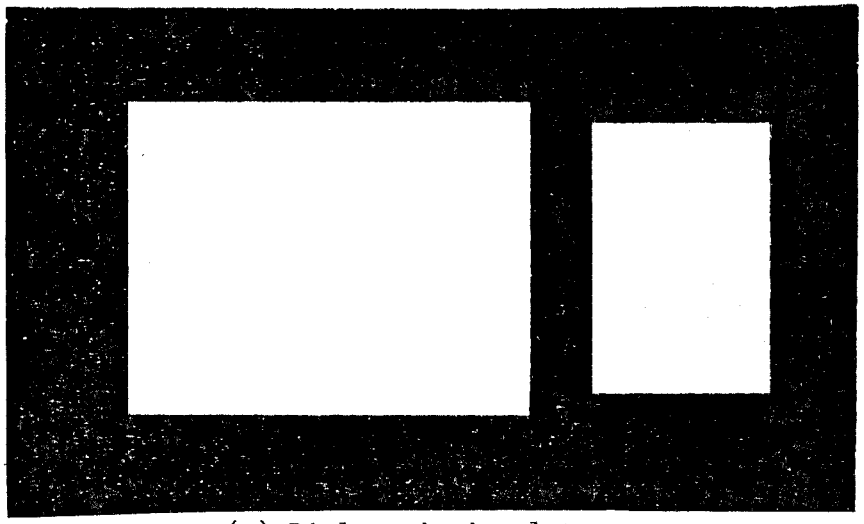
The Dupont 9061 and ESL 9695 Palladium - Silver conductor compositions were used as the first and second resistor's terminals respectively.



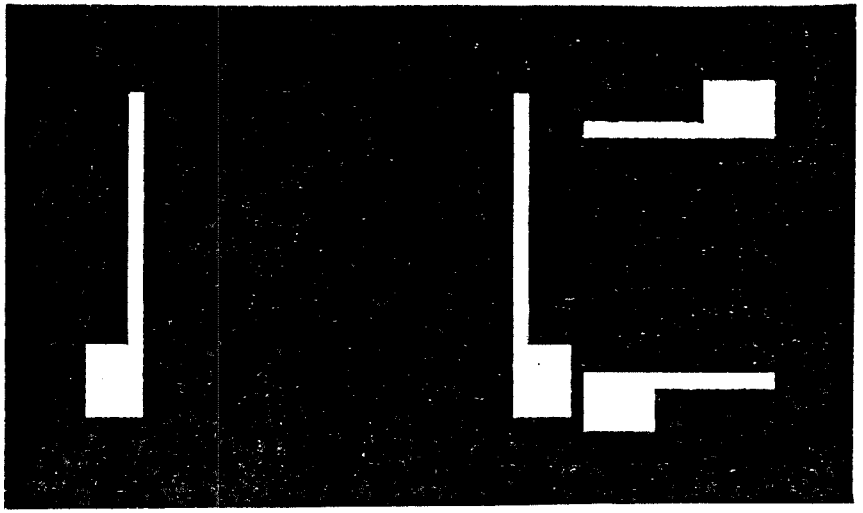
(a) Bottom Terminations



(b) Bottom and Top Resistors



(c) Dielectric insulator



(d) Top Terminations

Fig.(4.15) The pattern designed for investigation (6).

The screens were prepared and the inks were printed and fired in the sequence given in Table (4.12). To reduce the number of firings, the top resistors ESL 3100 were cofired with their conductor terminals ESL 9695. The variations of the first resistors were recorded after each firing and graphs of resistance against the corresponding number of firings for each ink were plotted in Fig.(4.16) a, b and c respectively.

In this investigation, ESL 3100 resistors were also printed on ceramic substrates to act as control substrates in order to observe the change in the value of the top resistor as the result of being printed over the dielectric layer - see Table (4.13). The values of the top and bottom resistor after the last firing together with the ratio of the bottom resistor ivalue over the top resistor value for each device are given in Table (4.14).

Bottom resistor	Dielectric layer 1	Dielectric layer 2	Dielectric layer 3	Top resistor
Dupont 1610(O)	Dupont 9950(3)	Dupont 9950(3)	Heraprint IP065(4)	ESL 3113(a) 3114(b) 3115(c) 3116(e)
Dupont 1620(N)	(3)	(3)	(4)	(a) (b) (c) (e)
Dupont 1331(D)	(3)	(3)	(4)	(a) (b) (c) (e)

Table (4.12) The ink sequence used in investigation (6).

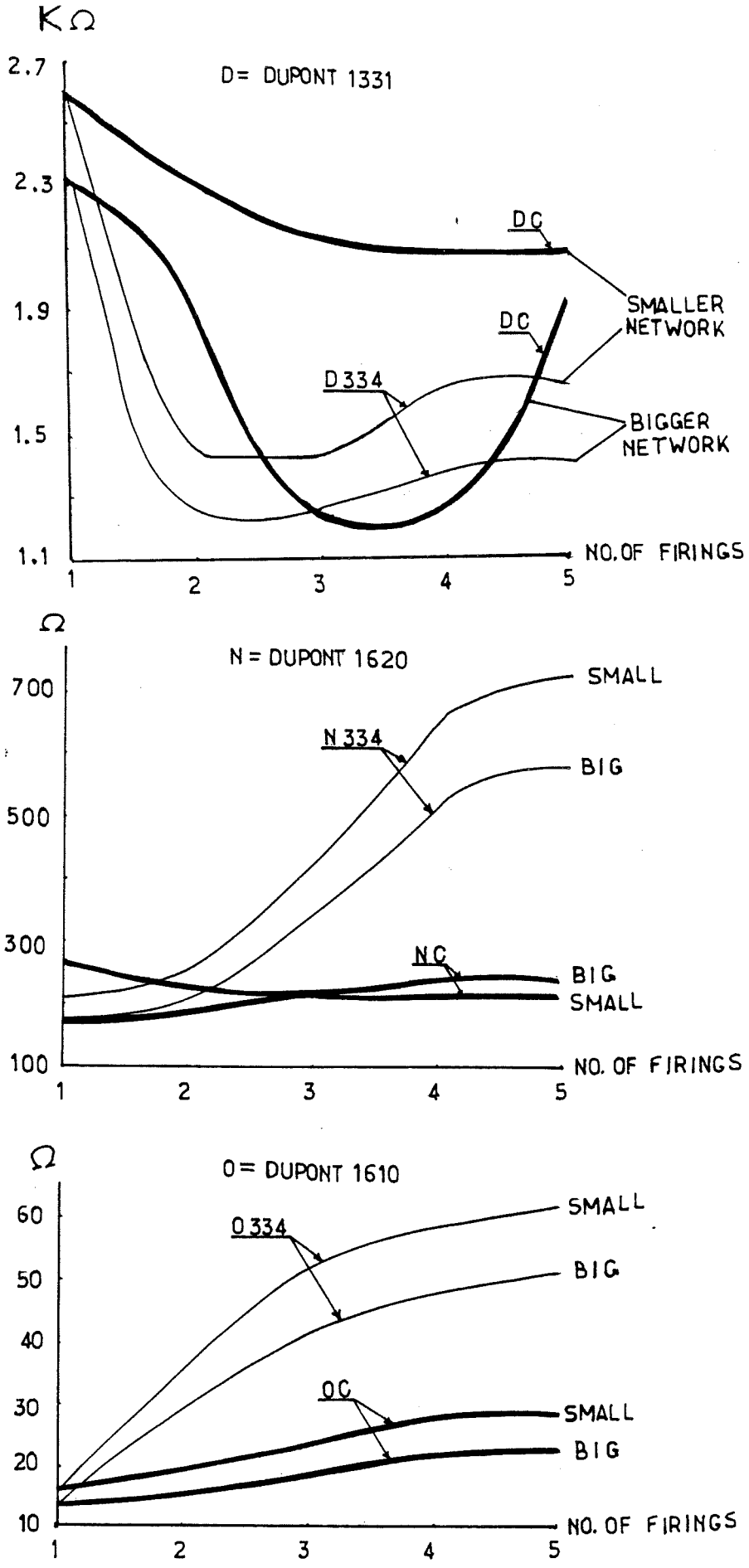


Fig.(4.16) Firing characteristics of resistors D, N and O with combinations of dielectrics 3 and 4.

Substrate code	Top Resistors' compositions	Top Resistors Values over dielectric		Corresponding control resistor	
		large net.	small net.	large net.	small net.
D334 a	ESL 3113 a	7.5 KΩ	8.6 KΩ	6.8 KΩ	7.7 KΩ
N334 a		8.1 KΩ	8.9 KΩ		
O334 a		7.7 KΩ	8.6 KΩ		
D334 b	ESL 3114 b	47 KΩ	59 KΩ	45 KΩ	57 KΩ
N334 b		48 KΩ	64 KΩ		
O334 b		46 KΩ	52 KΩ		
D334 c	ESL 3115 c	1.79M	1.99M	1.43M	1.48M
N334 c		1.72M	2001M		
O334 c		1.40M	1.57M		

Table(4.13) The top resistors values both on dielectric and on substrate.

Substrate code	Large Network resistors values		Small Network resistors values		Ratio of NR/R	
	bottom(NR)	top(R)	bottom(NR)	top(R)	large network	small network
D334 a	1.34k	7.5k	1.61k	8.6k	0.179	0.187
D334 b	1.38k	47 k	1.60k	59 k	0.029	0.027
D334 c	1.37k	1.8M	1.65k	2 M	0.001	0.001
D334 e	1.34k	---	1.59k	---	---	---
N334 a	635	8.5k	767	8.9k	0.0765	---
N334 b	549	48 k	700	64 k	0.011	0.011
N334 c	588	1.7M	746	2 M	0.0003	0.0003
N334 e	571	---	737	---	---	---
O334 a	53	7.7k	64	8.6k	0.007	0.007
O334 b	48	46 k	59	52 k	0.001	0.001
O334 c	52	1.4M	62	1.5M	0.00004	0.00004
O334 e	50	---	61	---	---	---

Table (4.14) Values of the two resistors of the FDRC metworks in Ω.

4.17 DISCUSSION

Graphs of Fig.(4.16) a, b and c show that the firing characteristics of the bottom resistors of the smaller size networks possess the same pattern as the bigger size network in most cases. Only in the case of the Dupont 1331 (D) control resistors the firing characteristics of the small and big networks are very different. The reason for this difference may be due to measurement difficulties.

Looking back at the firing characteristics of Dupont 1331 (D) with Dupont 9950 (3) and of the control resistors in investigation (1), (2) and (5), figures 4.7d, 4.10b and 4.14a respectively, a similar pattern for the firing characteristics is observed. However, the firing characteristics of D333 were different from those of DC in this investigation (ie investigation 6)- see Fig.(4.16)a. The reason for these differences might be any slight change in the fabrication process. This indicates that the parameters of the fabrication process have enormous effects on the firing characteristics of the resistors in an FDRC network. Therefore, it is important to adopt a system of printing and firing, and then try to stick to one procedure when fabricating FDRC networks with different specifications. As above they may be due to faults in the measurements of the control substrates.

Overall, the graphs of Fig.(4.16) do not indicate compatibility between the resistor inks Dupont 1331 (D), 1620 (N), 1610 (O) and combination of two layers of Dupont 9950 (3) and one layer of Heraprint IP065 (4) dielectric inks. However, from Table (4.13), the top resistors (ESL 3100 resistors a, b, c and e) show satisfactory behaviour when printed over the dielectric Heraprint IP065 (4). This means that the resistor values on the dielectric do not differ

significantly from those of the corresponding control substrates. Despite the poor performance of the bottom resistors, all the FDRC devices fabricated in this investigation are free from any interaction between the two resistors of the FDRC. Only in the case of the device 0334c (ie the device with Dupont 1610 (0) and ESL 3115 (c) as the bottom and top resistors respectively) a leakage resistance is measured between the two resistors. This might be due to misaligment of the various layers at the time of printing.

4.18 INVESTIGATION (7)

After the previous six investigations on different resistor - dielectric compositions, it has become clear that only the combination of resistor inks Dupont 1331 (D) with dielectric Dupont 9950 (3) and ESL 3100 resistors had resulted in the best FDRC device. Other resistor - dielectric combinations which had resulted in a relatively good FDRC devices are listed below:

Bottom resistor	Dupont 1331	Dupont 1620	Dupont 1620
Dielectric	Heraprint IP065	Heraprint IP065	Dupont 9950
Top resistor	ESL 3100 series	ESL 3100 series	ESL 3100 series

In investigation (6), the combination of two layers of Dupont 9950 (3) and one layer of Heraprint IP065 (4), as the insulating layer in the FDRC network, was examined and the result was found to be not satisfactory. In this investigation, other combinations of these dielectric inks with resistor inks Dupont 1331 (D) and Dupont 1620 (N) for the bottom resistors and ESL 3100 resistors for the top are examined. A comprehensive list of the inks for each FDRC device fabricated in this investigation is given in Table (4.15).

Bottom Resistor	Dielectri Layers 1st	2nd	3rd	Top Resistor
Dupont 1331 (D)	4*	3+	3	ESL 3115 (c)
(D)	4	4	3	(c)
(D)	4	3	4	(c)
(D)	4	3	3	ESL 3114 (b)
(D)	4	4	3	(b)
(D)	4	3	4	(b)
Dupont 1620 (N)	4	3	3	ESL 3113 (a)
(N)	4	4	3	(a)
(N)	4	3	4	(a)
(N)	4	4	4	(a)
(N)	4	4	4	(a)
(N)	3	4	4	(a)
(N)	3	4	4	(a)
(N)	4	4	4	ESL 3112 (d)
(N)	3	4	4	(d)

* Heraprint IP065 (4)
\+ Dupont 9950 (3)

Table (4.15) The sequence of the inks for each substrate.

The screens of investigation 3 are also used in this examination. The layers of the FDRC devices are printed and fired sequentially as listed in Table (4.1). The values of the bottom resistors are recorded after each firing. The control resistors for both the bottom and top resistors are fired together with the other substrates. Table (4.16) gives the values of the top resistors both on substrates (control resistors) and on the dielectric layers of the devices. The values of the top and bottom resistors after the last firing together with the ratio of the bottom resistor over the top resistor for each device are given in Table (4.17). The firing characteristics of the bottom resistors with the various dielectric combinations are plotted in Fig.(4.17).

Substrate code	Top Resistor composition	Top Resistor Value over dielectric	Corresponding control resistor
D433 c	ESL 3115 c	3.48M	3.03M
D443 c		3.11M	2.53M
D434 c		3.07M	
D433 b	ESL 3114 b	43.7k	46.0k
D443 b		48.1k	46.1k
D434 b		67.2k	
D433 a	ESL 3113 a	11.2k	8.13k
D443 a		10.8k	8.66k
D434 a		9.98k	
N444 a		9.44k	
N444 a		9.72k	
N344 a		9.24k	
N344 a		9.60k	
N444 d	ESL 3112 d	790	710
N344 d		820	750

Table(4.16) The top resistors values on dielectric and on substrate.

Substrate codes	Bottom resistor	top resistor	T/B ratio
D433a	1.19	11.2	0.106
D443a	1.20	10.8	0.111
D434a	1.14	10.1	0.113
D433b	0.95	43.7	0.022
D443b	1.24	48.1	0.259
D434b	1.15	67.2	0.017
D433c	1.16	3.48M	0.0003
D443c	1.18	3.11M	0.0003
D434c	1.12	3.07M	0.0003
N444a	257	9.44	0.027
N444a	322	9.72	0.033
N444d	284	0.79	0.359
N344a	476	9.24	0.515
N344A	530	9.60	0.05
N344d	521	0.82	0.635

Table (4.17) Values of the two resistors of the FDRC networks in kΩ.

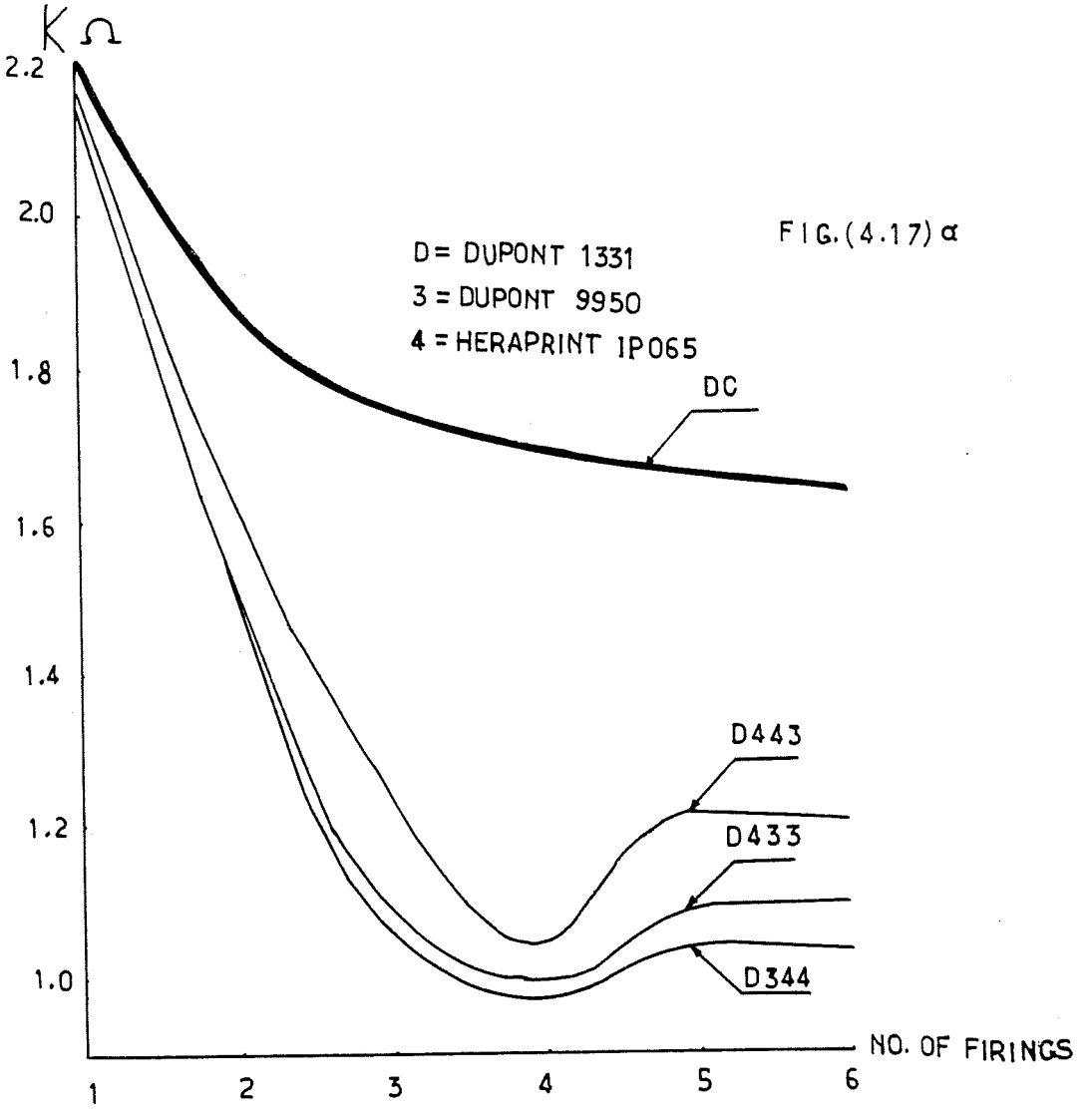


FIG.(4.17) a

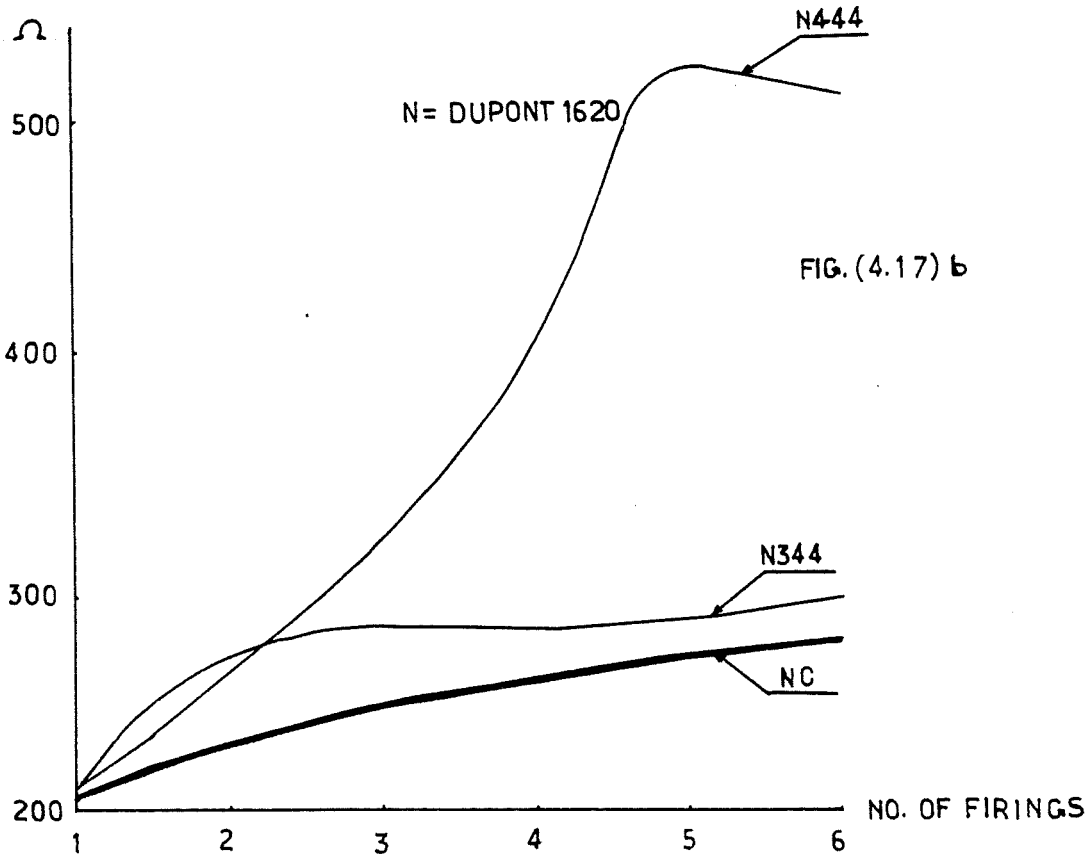


FIG. (4.17) b

Fig.(4.17) Firing characteristics of resistors D and N with some combinations of dielectrics 3 and 4.

4.19 DISCUSSION

It is understood from Table (4.16) that:

a. The values of ESL 3115 (c) as the top resistor over all combinations of the dielectric layers do not differ from the values of corresponding control resistors (ie the resistors on bare substrates).

b. There is only a very slight difference between the values of ESL 3114 (b) resistors over Dupont 9950 (3) (in devices D433b and D443b) and the values of the control resistors. However, the ESL 3114 (b) over Heraprint IP065 (4) in device D434b shows a pronounced difference of about 21k Ω.

c. The values of ESL 3113 (a) resistors over Dupont 9950 (3) in devices D433a and D443a are further away from the values of the control resistors than those of the values of ESL 3113 (a) on Heraprint IP065 (4) in the rest of the devices. However, generally speaking, the values of ESL 3113 (a) over any dielectric are higher than those of the control resistors by an average of 1.5 k Ω.

Despite the attempts made to increase the chance of obtaining a resistance ratio close to the ratio required for the true zero, ie N=0.08627, referring to Table (4.17), a ratio closer than N = 0.1062, ie N = 0.08627 + 0.01993 for device D433a could not be obtained - a fabrication tolerance of +23%.

Despite the compatibility shown in investigation (5) for the combination of resistor Dupont 1331 (D) and dielectrics 3 and 4, graphs of Fig.(4.17)a indicated a poor performance for this combination. The difference in the size of the devices of

investigations (5) and (7) may justify this inconsistency.

The Dupont 1620 (N) composition with one layer of dielectric 3 and two layers of dielectric 4 (N344) behaved similarly to its performance in N444 devices in investigation (5). However, resistor N in the N444 device which has three layers of dielectric 4 did not perform like the resistors of the N444 devices fabricated in inestigation (5). This inconsistency may also be due to the difference in the size of the devices of investigations (5) and (7).

4.20 CONCLUSION FOR CHAPTER (4)

Satisfactory fabrication of FDRC networks was achieved by the following combination: resistor Dupont 1331 (D) as the bottom resistor, three layers of dielectric Dupont 9950 (3) and various resistors of ESL 3100 series as the top resistor. Only small differences were observed between the values of resistors D and those of corresponding control resistors.

However, the values of the bottom resistors of the FDRC networks fabricated using combinations of different resistor and dielectric inks showed pronounced difference when compared with the corresponding control resistors. These combinations are listed in Table(4.18).

Bottom resistor	Dielectric layer			Top Resistor
	1st	2nd	3rd	
Dupont 1331 (D)	3*	3	4+	ESL 3100 series
	4	3	3	
	4	4	3	
	4	3	4	
Dupont 1620 (N)	3	3	4	
	3	4	4	
Dupont 1610 (O)	3	3	4	

* Dupont 9950 (3)

\+ Heraprint IP065 (4)

Table (4.18) The ink combinations which have resulted in fabrication of FDRC networks.

4.21 CAPACITANCE BRIDGE MEASUREMENT

The capacitance between the two resistors of the FDRC devices fabricated in investigation 2 and the value of the (equivalent) capacitor fabricated on the same substrate were measured by a bridge and are given in Table (4.19)a. Similarly, the capacitances of the FDRC devices fabricated throughout the investigations (5), (6) and (7) are measured and listed in Tables (4.19)b, c and d. The key to the substrate coding is given in section 4.5.

The capacitance between the two resistors of the FDRC networks are generally smaller than the capacitances produced by the distribution of two purely conductive electrodes with the same area and the same dielectric insulator. The area of the resistors is not 100% conductive which means less conductive area and therefore less capacitance. This statement is clearly justified by referring to Table (4.19). Table (4.19)a indicates that CE which is the value of the equivalent capacitor, is higher than CD, the capacitance of the FDRC device. Also, from table (4.19) it is seen that the substrates with higher resistances, especially for the top resistors, have lower capacitances.

A comparison between the capacitances of the devices with the same size and resistor layers indicates the difference between the permittivities of the corresponding dielectric layers. For example, the capacitances of the devices D333d 4, D333d 5, D444d 4 and D444d 5 in Table (4.19)b are 140pF, 144pF, 132pF and 125pF respectively. It is seen that the first two capacitances are higher than the second two. Since the size and both resistor layers of these four devices are the same, one of the factors which may cause this difference is the permittivity of the dielectric layers. From this comparison it can be said that the permittivity of the Dupont 9950 (3) is higher than the Heraprint IP065 (4) in this case.

Substrate code	C_D pF	C_D/area pF/mm	C_E pF	C_E/area pF/mm
D333c	230	1.06	587	2.7
D333b	630	2.92	647	3.0

Table (4.19)a Capacitances of the FDRC network and the equivalent capacitors of investigation 2. measured by Wayne Kerr Universal bridge B224.

Substrate code	C_D pF	C_D/area pF/mm
D333b 2	120	1.7
D333b 3	135	1.91
D333d 4	140	1.98
D333d 5	144	2.0
D333e 1	120	1.69
D444b 2	137	1.94
D444d 4	132	1.87
D444d 5	125	1.77
D444e 1	133	1.88
N333b 2	131	1.85
N333d 3	136	1.91
N333e 1	131	1.85
N444b 2	114	1.61
N444d 3	120	1.69
N444e 1	113	1.59

Table (4.19)b Capacitances of the FDRC networks of investigation (5).

Measured by Wayne Kerr Universal bridge B224.

Substrate code	C_D pF	C_D/area pF/mm
D434a	360	1.66
D434b	358	1.65
D434c	350	1.61
D433a	400	1.85
D433b	372	1.72
D443a	360	1.66
N344a	338	1.55
N344d	345	1.60
N444a	326	1.51
N444b	351	1.62

Table (4.19)c Capacitances of the FDRC networks of investigation (7). Measured by Wayne Kerr Universal bridge B224.

Substrate code	Larger network C_D(pF)	C_D/mm	Smaller network C_D(pF)	C_D/mm
D334a	238	1.58	91	1.64
D334b	236	1.57	92	1.67
D334c	90	0.6	65	1.18
D334e	30	0.2	17	0.3
N334a	240	1.60	—	---
N334b	236	1.57	90	1.6
N334c	100	0.66	72	1.3
N334e	27	0.18	16	0.29
O334a	242	1.60	95	1.70
O334b	239	1.59	91	1.65
O334e	22	0.15	10	0.18

Table(4.19)d Capacitances of the FDRC networks of investigation (6). Measured by Wayne Kerr Universal bridge B224.

CHAPTER 5

TRIMMING OF THE DISTRIBUTED RC NETWORK

5.1 INTRODUCTION

The tolerance to which a resistor is manufactured depends on such factors as the method of fabrication, the materials used and the skill of the operator. Thick film resistors can be screened to an as fired tolerance of $\pm$20%. It is an accepted fact in the hybrid circuit industry that in order to achieve films with a tolerance of better than $\pm$1 to 2% (and down to 0.5%) the resistors have to be trimmed in some manner. In a thick film fully distributed FDRC notch filter, the resistors should be given a final adjustment to achieve the notch frequency required.

The techniques of air abrading, the use of abrasive disc or wheels, and laser beam trimming have the common requirements of reasonably accurate mechanical positioning and of accessibility to the surface of the resistor. These techniques are basically destructive in that a portion of the resistor is removed.

However, in our application, the resistors to be trimmed are in a sandwich form, and the shortcomings of these methods are as follows:

1. With these techniques it is not possible to trim only the top or the bottom resistor of the FDRC structure, because, both the top and the bottom resistors receive the same cut

and consequently the resistors cannot be trimmed individually to their respective values.

2. A cut in a uniform FDRC structure leaves it no longer uniform and immediately renders invalid all the results of any mathematical analysis based upon a uniform structure [45]. In general, it can be stated that any trimming techniques which will affect the geometrical shape of the resistor are not suitable for an FDRC distributed notch filter.

OTHER WAYS OF TRIMMING:

The majority of commercially available thick film resistor compositions suffer a permanent change in dc resistance after being subjected to high voltage pulses, either fast or slow, or prolonged stressing under high electrostatic fields [46]. Many workers [46-53] evaluated the performance of several resistor systems after exposure to static discharge. The sensitivity of thick film resistors to high voltages is a phenomenon both useful, as in the case of resistance adjustment, and undesirable, when safeguards to prevent static electricity are not taken during the manufacture of hybrid circuits [52]. Resistor stability under high voltage conditions is not often included in a cursory evaluation because most thick film resistors are used in low voltage hybrid microcircuits.

The techniques of high frequency discharge [53] and electro-chemical trimming [54], both of which are applied to the resistor surface, and also high electrostatic stress and high voltage pulses trimming are non-destructive methods (ie they will not alter the geometrical shape of the resistors). However, they may give some

uneven structural changes. These techniques will be explained in some detail in the sections which follow.

5.2 HIGH FREQUENCY DISCHARGE TRIMMING

The required adjustment in either direction can be achieved by the high frequency trimming methods. The trimming is carried out using an apparatus in which a discharging probe is set close to the surface of the specimen [53] -see Fig.(5.1). Applying 2-10 kV high frequency voltage (500kHz) to the probe, a monopolar discharge is caused to occur between the probe and the specimen and this produces a change in the resistance. Taketa and Haradome [53] have concluded:

1. The maximum negative change in resistance $(\Delta R/R)min$ increases for low sheet resistance and is reduced for high sheet resistances.

2. During the initial stage of continuous high frequency discharging, both TCR and noise characteristics are improved. After this stage, the resistance of doped resistors starts to increase and TCR and noise characteristics start to deteriorate.

3. The $(\Delta R/R)min$ value decreases when:
   a. the sintering period (ie the initial firing) is increased,
   b. the sintering temperature is increased, and
   c. the cooling rate after sintering is decreased.

4. For glass overcoated resistors, the time to attain the $(\Delta R/R)min$ is longer and the value itself is smaller than it is for uncoated resistors.

5. To avoid the unfavourable effects of high frequency trimming on neighbouring resistors, the terminals of the resistor under trimming should be connected to the discharging ground potential terminal.

6. The stability of trimmed resistors is nearly the same as that of untrimmed resistors and is satisfactory.

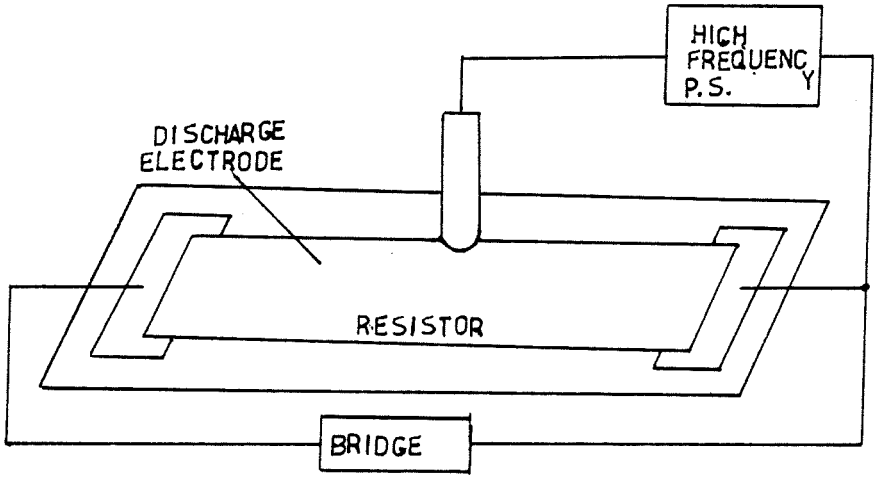


Fig.(5.1) Block diagram of a high frequency resistor trimming.

5.3 ELECTRO-CHEMICAL TRIMMING

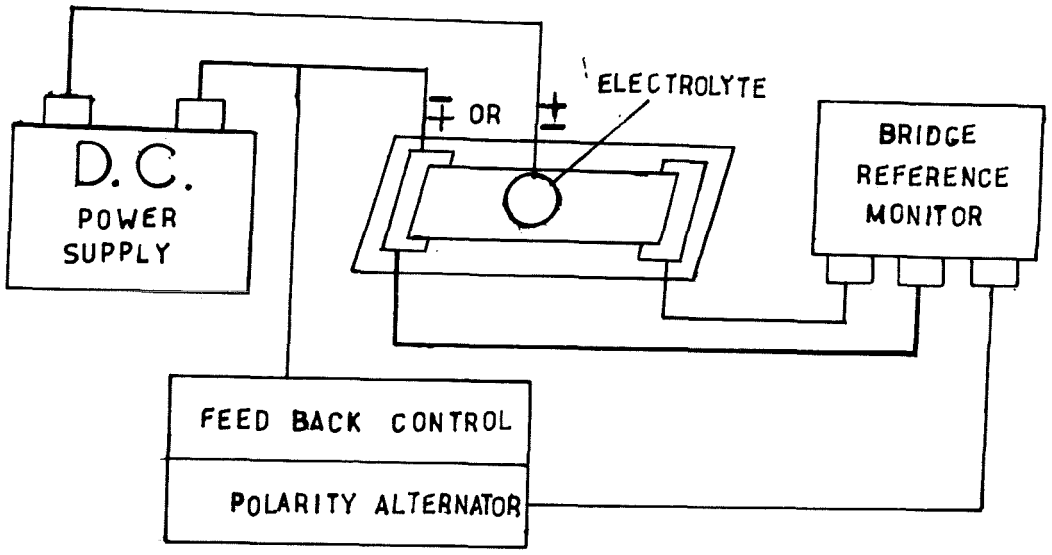


Fig.(5.2) Block diagram of chemical trimming.

The values of thick film resistors, can be reduced by undergoing a simple electro-chemical process [54]. A block diagram of the method is shown in Fig.(5.2). The resistor to be trimmed is connected to a suitable reference monitoring bridge. A moistened (distilled water) felt tip electrode is brought into contact with the resistor body. An ordinary metal probe electrode is connected to one end of the resistor terminations. Both electrodes are connected to a dc power supply. The application of the dc voltage causes a slight electrolysis which in turn generates hydrogen and oxygen depending on

polarity (optional) at the resistor surface -see Fig.(5.3). Hydrogen chemically reduces the resistor film and, at the same time, reduces the value of the resistance. Oxygen, on the other hand, oxidises the film and increases the value of the resistance. Voltage polarity etc can be chosen and automatically controlled so as to permit fast, efficient and accurate bidirectional adjustment of the most commonly employed thick film resistor formulations [54].

The chemical method of trimming requires some means of physical or electrical isolation of the resistor being trimmed. This could be a problem when complex circuitry is involved.

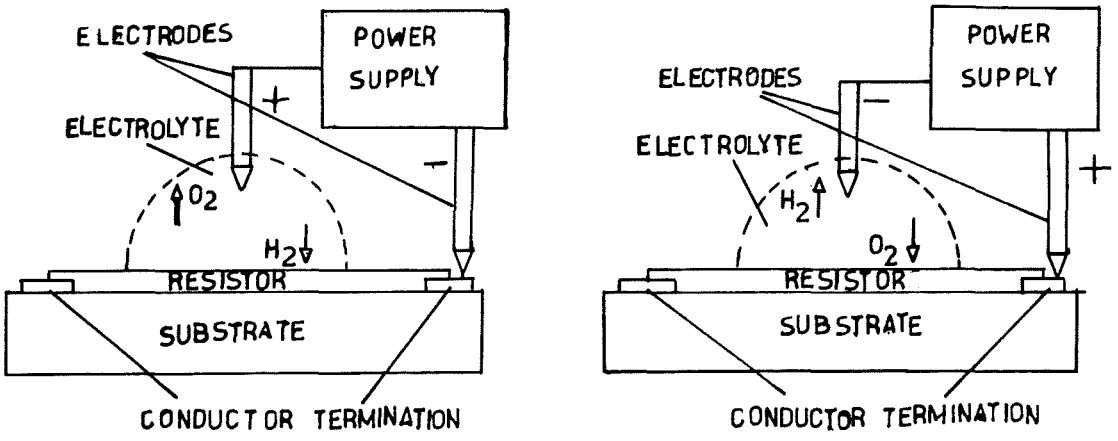


Fig.(5.3) Mechanism of electro-chemical trimming.

5.4 HIGH ELECTROSTATIC STRESS TRIMMING

The magnitude of the resistor change, as well as the manner in which the change is affected over a period of time under high electrostatic stress, varies from manufacturer to manufacturer [55]. Some thick film resistor compositions are fairly stable under high electrostatic stress and suffer no permanent change in dc resistance after prolonged stressing but others are not so stable. A block diagram of this trimming is shown in Fig.(5.4).

In an investigation on the conduction mechanism of thick film resistors under high electrostatic stress, P.W.Polinski* [55] first categorized the compositions in relationship to the physical characteristics of the fired product. All compositions were put into three basic categories according to their conduction mechanism. The first being that in which the conduction mechanism forms throughout the entire volume (thickness) of the fired resistor. The second containing those in which the conduction mechanism forms mainly outside the amorphous binder and close to the resistor- alumina interface. The third being one in which noble metal crystalline growth is stimulated at a fairly high peak firing temperature for a moderately long dwell time and then the growth is limited by the addition of an inert particulate substance such as 0.1 to 0.5 micron aluminum oxide particles. He then hypothesised that if the conduction through the resistor is fairly free of the amorphous binder (ie the dielectric parts of the resistor) a resistor fairly stable to high voltage stresses should result.

* The term electromagnetic stress used by Polinski [55] should in fact be electrostatic stress.

5.4.1 CONDUCTION MECHANISMS UNDER ELECTROSTATIC STRESS

Thick film resistors which are fairly stable under electrostatic stress can be categorized into two groups [55]. The first group includes the compositions in which the conduction mechanism is formed by dense layers of very small particles (less than 0.5 microns in size) and this layer (or layers) is affixed to the alumina substrate by an amorphous substance which is a lead borosilicate glass. The second group is comprised of a substance which is highly filled with very small particle size (less than 0.5 micron) alumina and very little amorphous binder as compared to the other compositions.

Polinski [55] hypothesized that a simple efficient conduction mechanism formed fairly free from the amorphous binder, will exhibit high stability. A simple conduction mechanism is obtained with a maximum of two main conducting elements and a maximum of two dopants to control TCR. Efficient conduction is one whereby practically all the conducting elements in the composition are utilized after the first firing. That is, further decrease in resistivity does not occur by refiring.

He has illustrated that the compositions in which a conduction layer forms under the surface of the glass and not throughout the entire volume, have the highest stability. In compositions where conducting particles are dispersed throughout the amorphous binder, the probability of dielectric barrier breakdown at high sustained stress is maximum and hence these compositions exhibit the greatest instability. Polinski has also reported that the "stable RuO2" resistor compositions gave no indication that the amorphous binder was part of the conduction mechanism since one third of the resistor's thickness could be removed with no change in resistance. This also indicates that the mechanism must have formed near the surface of the substrate.

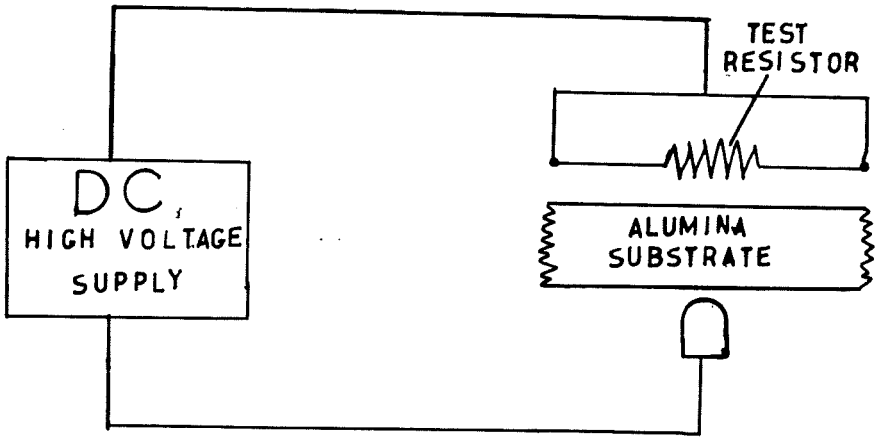


Fig.(5.4) Block diagram of high electrostatic stress trimming.

5.5 HIGH VOLTAGE DISCHARGE TRIMMING

5.5.1 INTRODUCTION

Most thick film resistors, are subject to considerable resistance variation when high-voltage is applied, particularly in the form of high-voltage pulses [48]-[50]. The change of resistance of the thick film resistor caused by the application of high voltage pulses can be utilized to adjust the value of the resistance. On the other hand, for the thick film hybrid IC, which is being used at an ever increasing rate in high voltage circuits of TV sets where very high voltage pulses often occur, improved stability of the thick film resistor to high voltage pulses is strongly desired.

Among thick film resistors on the market the one whose value changes least with applied high voltage is the RuO2:Ir based resistor [49]&[56], but since this type is very expensive, it is not suitable for use in low cost household electric appliances and automotive apparatus. Electric discharge technique for the adjustment of glaze resistors does not require accurate mechanical positioning of the resistor, nor does it require access to the surface of the resistor. It is inherently a non-destructive technique; and after trimming, the geometrical shape of the resistor is left intact; just as it was originally deposited, but having a slightly different value. This is desirable both from the power density stand point and the uniformity of the physical shape of the resistor. Trimming is accomplished by applying a series of high voltage, short duration pulses directly to the terminals of the resistor in question. Two block diagrams of this technique is shown in Fig.(5.5).

In early experiments it had been first suggested that the value of resistances increases on the application of high voltage pulses, then later in an investigation by Pakulski and Touw [50] it was pointed out that, under certain conditions, the resistance value does not increase, but on the contrary actually decreases. Two mechanisms can be considered to be responsible for these results. The first occurs when a large amount of energy is applied to the resistor and results in the destruction of the resistor material, rendering it non-conductive, which as a result increases the overall resistance. The second effect is more subtle, and occurs when the pulse is applied, without destruction of the resistor. It results in a decrease of resistor value by fusing together the metallic particles within the resistor body.

It has been demonstrated [50] that the change in resistor value, when a high voltage pulse is applied across the terminal of the resistor, is caused by the electric field across the resistor, and not simply by the current through the resistor. Furthermore, if the same field is applied to the resistor, the change in the value of the resistor after the first pulse will decrease approximately exponentially with the number of pulses. Thus, for continuous reduction in the resistor value the amplitude of each subsequent pulse must be increased. However, the reduction of the resistance value does not continue indefinitely. This is dependent on the resistor formulation and for a given formulation it depends on the pulse characteristics.

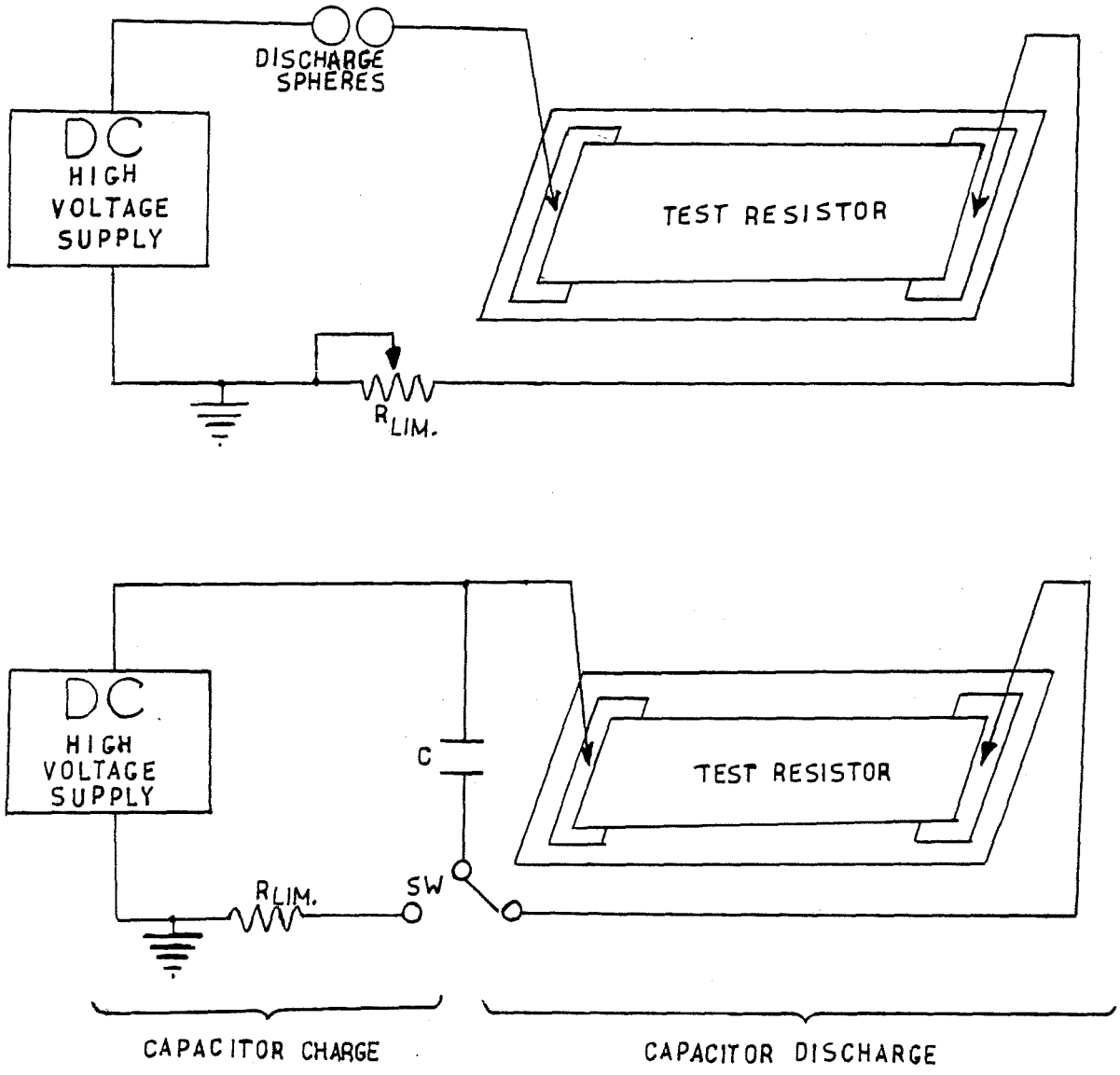


Fig.(5.5) Two diagrams for high voltage pulse trimming.

5.5.2 MECHANISMS OF RESISTANCE CHANGE UNDER HIGH VOLTAGE PULSES

When a high voltage impulse is applied to the glazed resistor, an instantaneous impulse of current flows in the resistor. Supposing that the electrical conduction is mainly performed by the conducting phases which form conducting chains throughout the resistors, see Fig.(5.6) [57]. This impulse of current may indeed produce some changes in the material, depending on the concourses of many circumstances.

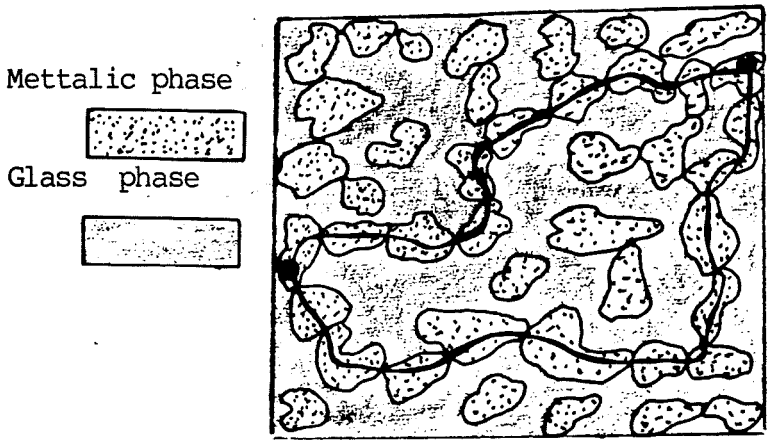


Fig.(5.6) Possible conducting paths connecting two points of the conducting phase.

When a high resistance material $\rho > 1k\Omega/sq.$ undergoes a high voltage impulse, the current flowing in the resistor distributes among the various conducting chains and a corresponding Joule heating effect will develop [57]. This heating effect will be larger in the contact points between the conductive aggregates, than any where else in the chain. As a result in a high conducting chain these contact points are sufficiently large and well distributed so that a negligible contact resistance exists between neighbouring aggregates. The current flowing in this kind of chain produces no substantial

modifications of the contact points, neither in their distribution nor in their section. However, beside the high conducting chains, there are chains which are also constituted by conductive aggregates but owing to imperfect contacts between some neighbouring aggregates, they present a high resistance and they give little contribution. But when a high current impulse is passed through the thick film resistance, a rather high Joule effect will develop in these chains at the sites of the imperfect contacts, where there is a high contact resistance, between neighbouring aggregates. These points will reach and exceed the melting temperature so that a phenomenon of microwelding between contact points belonging to neighbouring aggregates takes place. In this way, chains previously presenting a rather high overall resistance, which did not take part in the conductivity process before, will now present a low resistance path and will increase the number of high conducting chains. This increase of conducting chains produces a fall in the resistivity of the glazed material.

The main difference existing between the high resistance and low resistance materials is that for the same high voltage impulse gradient, the current flowing in a low resistance material is much larger than that in the case of a high resistance material. Therefore, it is expected that new implications will arise for a low resistance material owing to the larger flow of current. In fact, the Joule effect will be important not only at the points of contact between neighouring aggregates but also in the interior of the conductive aggregates themselves, particularly at the smaller aggregates of a given chain [57].

According to the observations of Himmel [48], after repeated pulsing the resistor shows a small increase in temperature for many

materials. Therefore, [57], for low resistance materials, a true melting of the material takes place in certain points of the conductive chain where the section of the aggregates is smaller, and hence, a consequent interruption of the conductive path may happen due to thermal expansion mismatch of the metallic phase and the surrounding glass phase.

In the intermediate resistance range $\rho \approx 1K\Omega/sq$ the two phenomena described before may coexist. Initially there is a decrease in the resistance due to an increase in the number of conductive paths produced by the mechanism already described, but as soon as a certain value of resistance is reached, conditions for a strong heating of the highly conducting paths are made possible with a consequent increase in the resistance, due to the destruction of high conducting paths [57].

Voltage stability of thick film resistors as a whole is also determined largely by the morphology of the conductive phase particles and their uniformity of distribution in the fired film [47]. A homogeneous mixture of glass and conductive phase particles will exhibit the best sintering characteristics. Under these ideal conditions, the printed resistor will sinter uniformly yielding geometrically similar glass-conductor contacts. Under less ideal conditions the glass and conductive phases may have non-uniform particle morphologies so that sintering occurs in a random fashion. The resultant sintered film is non-uniform and the glass-conductor particle contacts are very irregular.

Fig.(5.7) shows a conceptual picture of the ideal and random models presented above [47]. The random model is characterized by a non-uniform network of conductive phase particles. When such a thick film is subjected to an electric field gradient, very high electrical

potentials will exist across some of the junctions, giving rise to voltage breakdown and irreversible resistance changes. In the ideal case, the sintered contacts are all very similar and electric field gradients applied across the resistor will be distributed uniformly, and will result in a greater high voltage stability. For good voltage stability the intergranular region between conductive phase and glass must be as uniform and as thin as possible. Furthermore, the conductive phase must sinter uniformly to give a homogeneous conductive network.

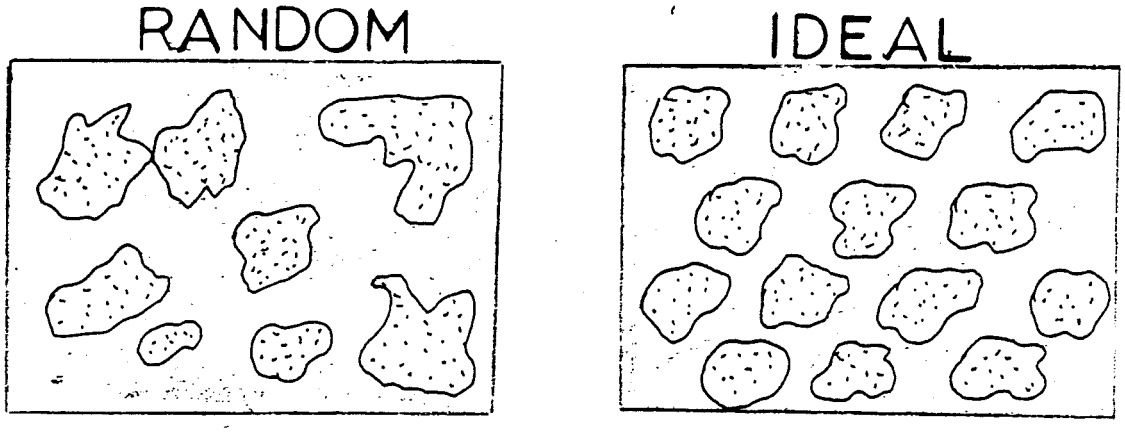


Fig.(5.7) High voltage resistor models [47].

In metal oxide resistors electrical conduction is through a network of interconnected chains of metal oxide particles. The metal oxide particles do not actually touch, but rather they are separated from their neighbours on the chain by a thin glassy layer as schematically illustrated in Fig.(5.8) [17]. This glassy layer is presumed to form during the firing process as a natural feature of liquid phase sintering. Electrical conduction through these layers is by a tunneling process and much, but not all, of the resistance

along a chain is due to these tunnel barriers. The unit of resistance along these segments can be written as a series combination of a metal oxide and a barrier resistance, R = Rm + Rb. The overall thick film resistance depends not only on the unit resistance but also on how the units and chain segments are connected geometrically.

However, this model significantly differs from the simple ideal model. The interparticle barriers contain impurities which affect the conductance barrier. These impurities most likely are introduced from each of the three basic ink ingredients, the organic vehicle, the glass and dissolution of metal oxide in the glass. However, the exact mechanism by which these impurities affect the transmission of charges, is still uncertain.

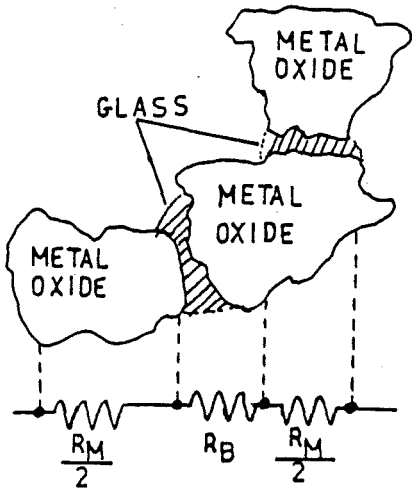


Fig.(5.8) The basic unit of the tunneling barrier model.

5.5.3 HIGH VOLTAGE PULSE APPLICATION

The trimming technique to be used for adjusting the resistors in the FDRC structure must have the ability to trim the bottom and the top resistors to their required values individually. The first three methods that have been explained in sections 5.2 - 5.4 cannot fulfil this requirement since they need accessibility to the surface of the resistor, therefore, the bottom resistor can not be trimmed by those methods. However, since the high voltage technique is applied to the terminals of the resistor it is found to be in agreement with nearly all the necessary requirements, for trimming both the resistors of the FDRC structure.

An electrically controlled apparatus capable of producing high voltage pulses of 2000 volts amplitude with variable widths from 12 μ sec to nearly 100 msec, was designed and constructed by the author, in order to investigate the effects of high voltage pulses on the thick film resistors used to fabricate an FDRC network(see chapter 4). Full details of the high voltage pulse trimmer circuitry are given in sections 5.5.4 - 5.5.6. The pulses are applied one by one directly to the terminals of the resistor, so that the effect of each pulse can be studied individually.

5.5.4 HIGH VOLTAGE PULSE TRIMMER

Figure (5.9) shows the first basic idea of producing the high voltage pulses. The spheres are initially well separated. They are then slowly brought closer together until a spark dischage is initiated between the gap separating them. Some current is drawn from the dc generator through the resistor while the spark lasts. The wider the gap in the spheres, the higher the breakdown voltage and the higher the current associated with the spark and hence the higher the energy of the pulse.

However, since the maximum available current from the generator is very low (8mA), this system does not fulfil the requirments for trimming thick film resistors. Fig.(5.10) shows an improved version of the above system. In this arrangement, one can increase the spark current by storing electrical charge in a capacitor and then discharging the capacitor through the thick film resistor.

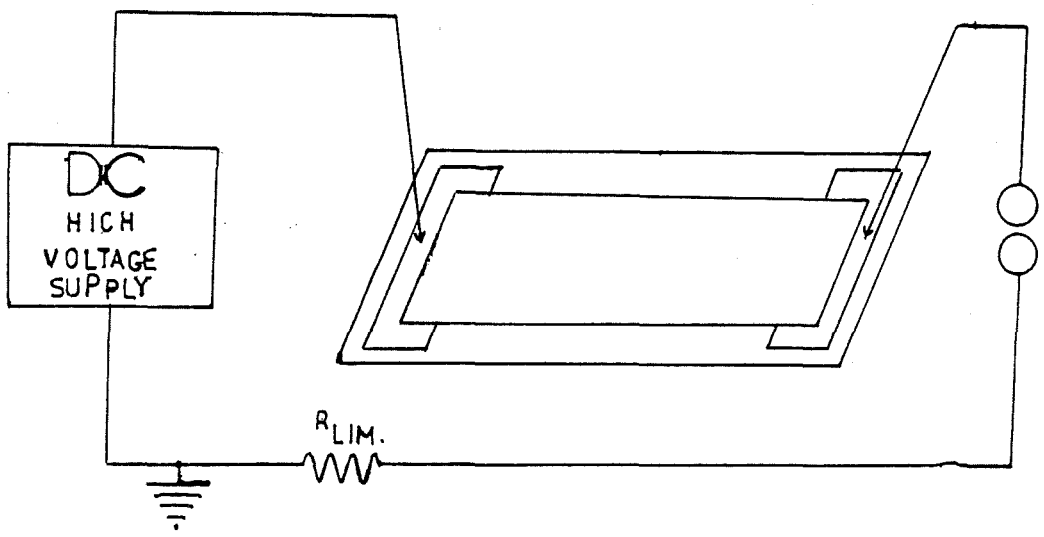


Fig.(5.9) Block diagram of a capacitor discharge arrangement.

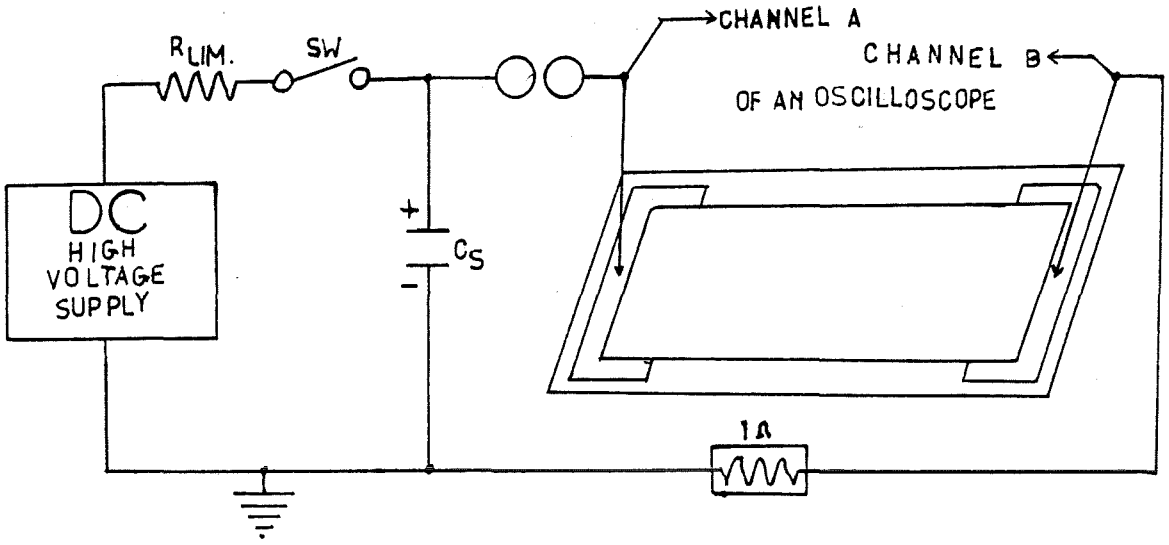


Fig.(5.10) Block diagram of a basic high voltage pulse trimming.

The voltages at the time of the discharge across the thick film resistor and a one ohm resistor were displayed on channels A and B respectively of a storage oscilloscope. The voltage across the one ohm resistor represents the current through the thick film resistor. The function of the resistor R_{lim} is to limit the charging current of the capacitor Cs.

The capacitor Cs cannot be charged to more than a certain voltage which is determined by the distance between the conductor paths on the thick film substrate. If the gap between the conductor paths is smaller than the sparking gap between the spheres, then a voltage breakdown will occur on the substrate rather than across the spheres. In this way, the pattern on the substrate limits the maximum permissible voltage on the capacitor Cs.

Discharging a 0.005 μF capacitor, charged up to 8kV, did not produce enough current to trim the resistor. To increase the current, either the voltage or the capacitance Cs had to be increased. The voltage must not be increased beyond 8kV because higher voltages cause a breakdown across the resistor terminals and /or other conductor paths on the substrate. Therefore, the capacitance was increased to 0.25 μF.

Despite the fact that the pulse energy was increased by increasing the capacitance, no change in resistance was observed. It was then concluded that most of the energy was dissipated in the spark between the spheres. However, to avoid the spark, the spheres were replaced by an electronic switch. Fig.(5.11) shows the circuit connection of an SCR which acts as a switch in series with the capacitor and the thick film resistor.

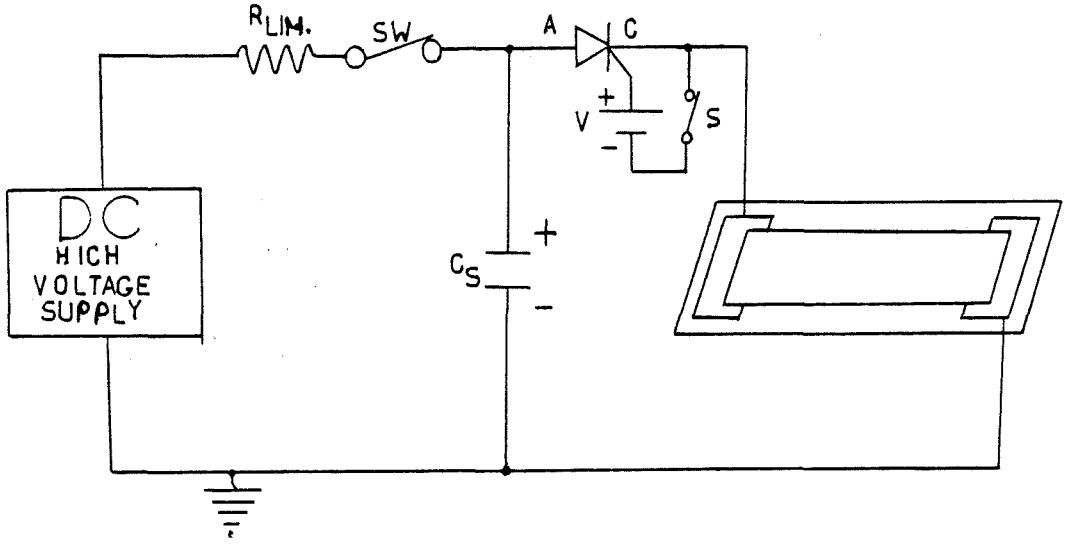


Fig.(5.11) Capacitor discharging circuit with an electronic switch.

THE CIRCUIT OPERATION OF THE SCRs:

When the mechanical switch S closes, the voltage V turns on the SCR (ie A to C becomes short circuit) and hence capacitor Cs discharges into the thick film resistor. The SCR used in the above circuit has a maximum breakdown voltage of 1200V. This voltage is still not high enough for our purpose. To increase the voltage, more SCRs should have been connected in series to withstand the voltage. It must be noted that all the SCRs should have been triggered in synchronism. Triggering one SCR after another causes the maximum voltage to be applied across an individual SCR thereby causing it to blow up. A more sophisticated circuit capable of producing discharges of various time durations was designed by the author and is shown in Fig.(5.12).

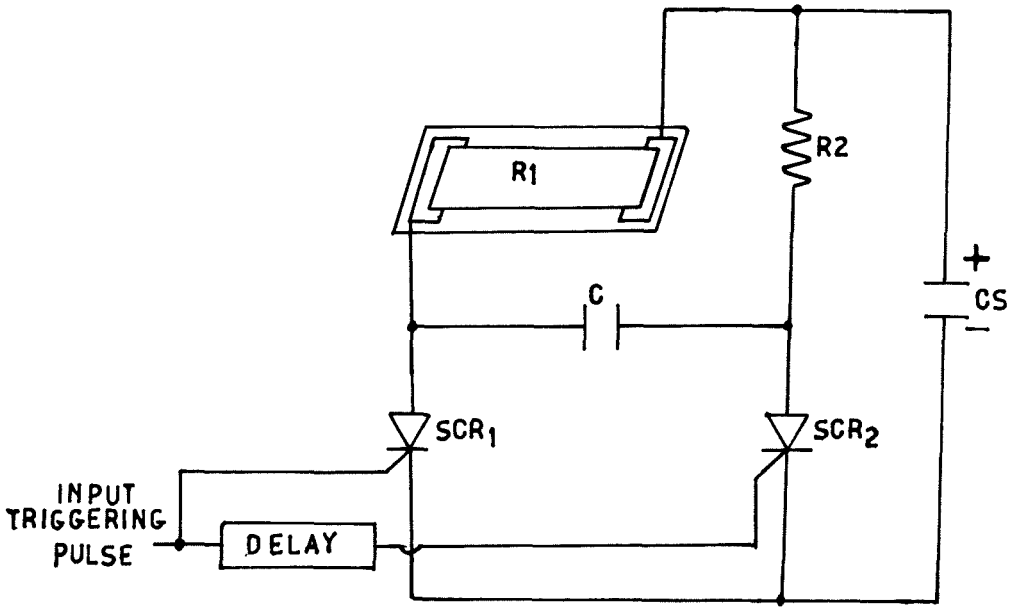


Fig.(5.12) The improved discharge circuit.

OPERATION OF THE MODIFIED CIRCUIT:

When the input triggering pulse appears, SCR_1 turns on and it acts as a short circuit. Capacitor Cs starts to discharge through R_1 and the R_2C paths. Capacitor C charges up through R2. After a predetermined delay, the input triggering pulse reaches the gate of the second SCR and turns it on. As soon as SCR_2 turns on, the positive end of the capacitor C is connected to earth and discharges itself to earth instantaneously, causing the current through SCR_1 to reduce to zero momentarily. Hence, SCR_1 turns off and then Cs discharges through R_2 and the R_1C. The current through R_2 must be much more than the current through R_1C so that Cs discharges through R_2 rather than R_1C. If this condition holds, it can be said that when SCR_2 turns on and SCR_1 turns off, current through R_1 reduces to zero. Fig.(5.13) shows the equivalent of the circuit after the second SCR has been triggered.

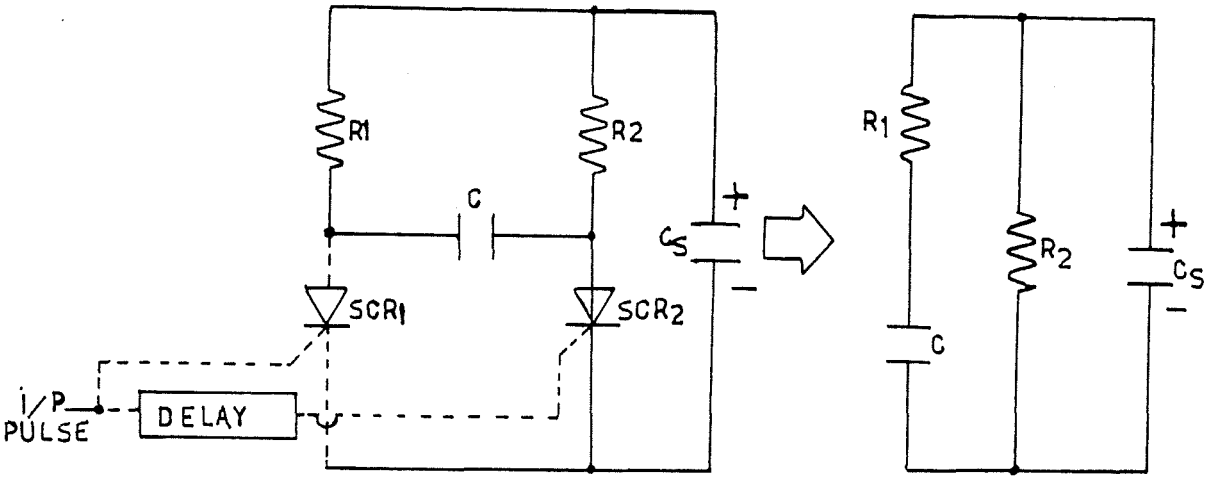


Fig.(5.13) The equivalent circuit to the circuit of Fig.(5.12) after the second SCR is triggered.

The time taken for capacitor C to be discharged through R_2 should be less than the time delay on the gate input triggering pulse of second SCR_2. Therefore, the capacitance can not be too large. On the other hand, the capacitor C should be large enough to store enough charge so that when SCR_2 turns on and the capacitor discharges back to earth, the rate of discharge (ie the current) be at least equal to the current through SCR_1 so that it momentarily reduces the current through SCR_1 to zero.

5.5.5 THE DELAY TIME CIRCUITRY

The SCR_2 gate signal is a replica of the SCR_1 gate signal delayed by some predetermined time. The circuit in Fig.(5.14) was designed to accomplish the desired delay. Fig.(5.15) shows the waveform produced by the circuit in Fig.(5.14).

The first 74121 IC (monostable) is triggered manually through the B input (ie pin number 5). This monostable is triggered at the falling edge of the input pulse and the output Q_1 goes low for a time equal to t_1. Input A_1 (pin 2) of the second monostable is fed by output Q_1 of the first IC (pin 1) and inputs A_2 and B (pin 3 and 5) of the second IC are connected to Vcc. The output Q_2 (pin 1 of the second IC) remains high until the A_1 input of the second IC goes low. Then for a predetermined time t_2, Q_2 stays low. The waveforms of the output states relative to the external input pulse are shown in Fig.(5.15). The two gates of the SCRs are fed by the pulses from Q_1 and Q_2 after passing through an inverting amplifier and two stages of non-inverting current amplifiers. The circuitry of the amplifiers will be explained later.

The times t_1 and t_2 -see Fig.(5.15) - are determined by the external components C_t, R_t and C'_t, R'_t respectively -see Fig.(5.14). t_1 is the time SCR_1 is on and is approximately the time during which the current flows through the thick film resistor R_1. The variations in t_1 corresponding to changes in R_t and C_t are indicated by the graphs of Fig.(5.21) -see section 5.6.1 . These are the results obtained by measurement.

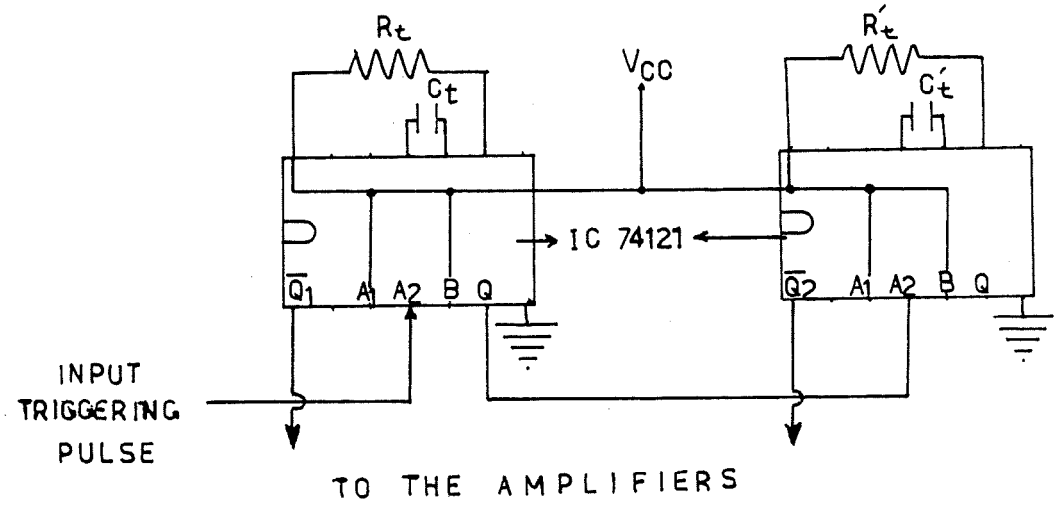


Fig.(5.14) Delay time circuitry.

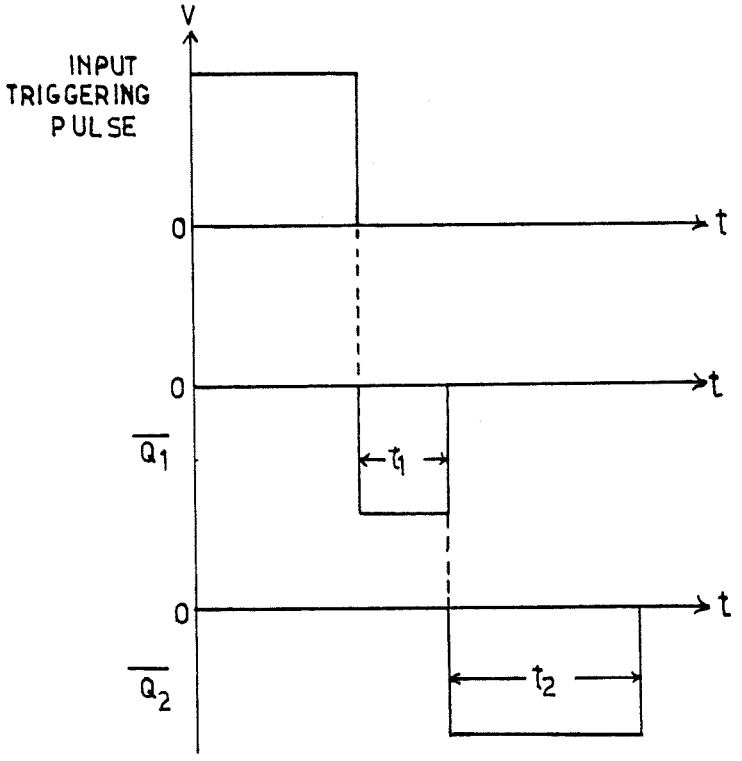


Fig.(5.15) The waveforms produced by circuit of Fig.(5.14).

5.5.6 THE SCR'S GATE DRIVE CIRCUITRY

The circuit in Fig.(5.16) was incorporated into the gate circuit in order to accomplish the desired signal current for the SCR's gates. In this circuit, the first transistor acts as an inverting amplifier to invert and restore the input pulse to 5V. TR_1 is followed by an emitter follower in order to increase the current of the 5V pulse.

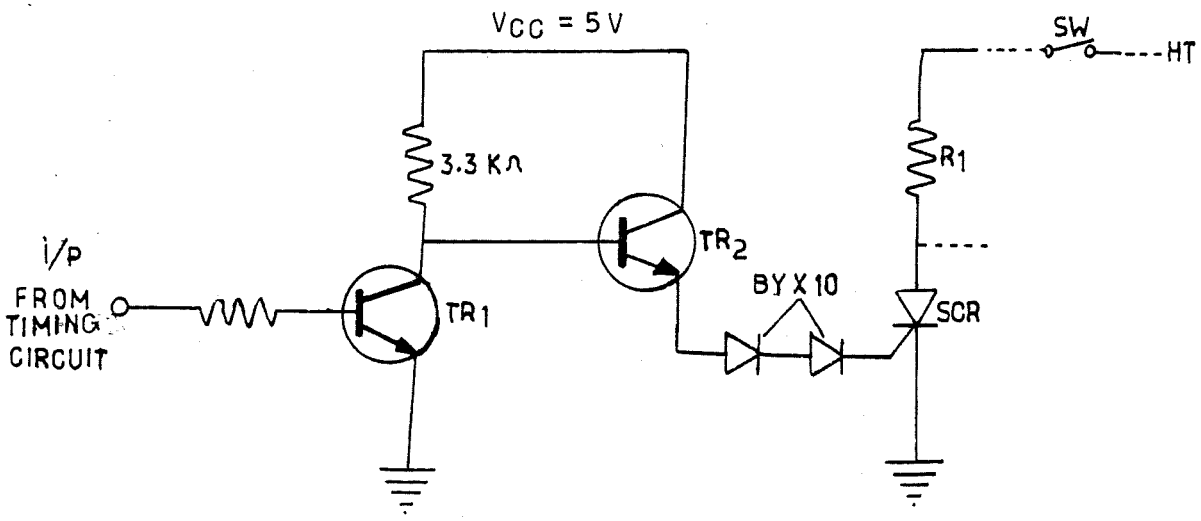


Fig.(5.16) The amplifying circuit for the gate signals.

The output from the emitter follower was connected to the gate of the SCR through two diodes, type BYX10. The object of using the diodes is to oppose any current surge from the anode to the gate when the switch SW closes. The switch SW connects a very high voltage to the anodes of the SCRs. When one diode is employed in the gate circuit of the SCR, the protection is only sufficient for anode voltages up to 700 volts. With two diodes in the gate circuit, the transistor circuit is protected for SCR anode voltages of up to 1200 volts.

The maximum voltage rating between the anode and cathode of the SCRs used is 1200 volts. For higher voltages up to 2400 volts, two SCRs must be connected in series. Fig.(5.17) shows the circuit connection for two SCRs in series.

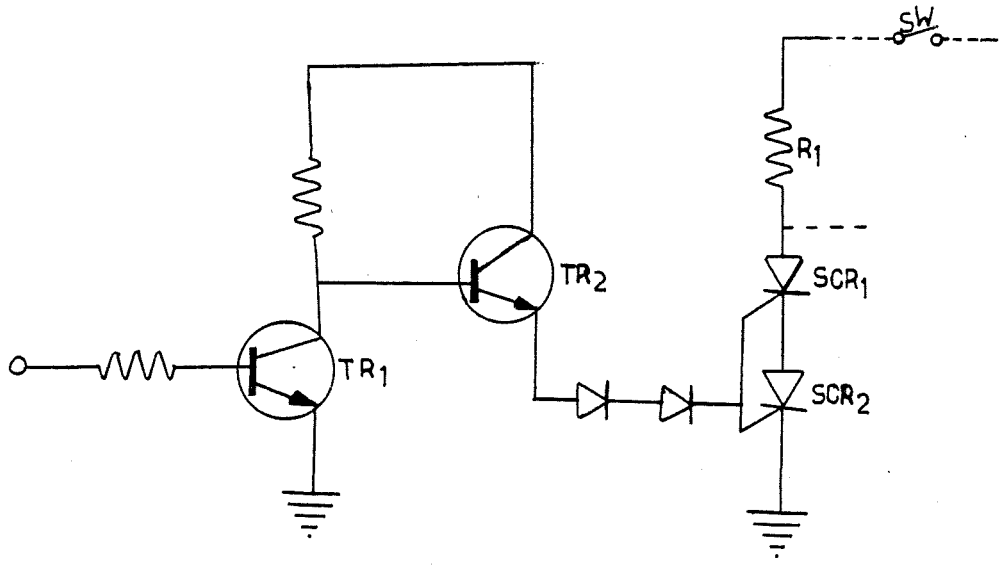


Fig.(5.17) Gate amplifying circuit with two SCRs in series.

It was observed that when the switch SW closes and an HT equal to 1500 volts is applied across the SCRs, the current flows from anode to the gate of SCR_1. After an investigation, the following was concluded: since there is very little resistance between the gate and the cathode of an SCR, the anode of SCR_2 is virtually shorted to its cathode through the gate-cathode junctions of the two SCRs. To avoid the foregoing problem, the two gates should have been isolated from each other by means of a pulse transformer with two secondary windings as shown in Fig.(5.18).

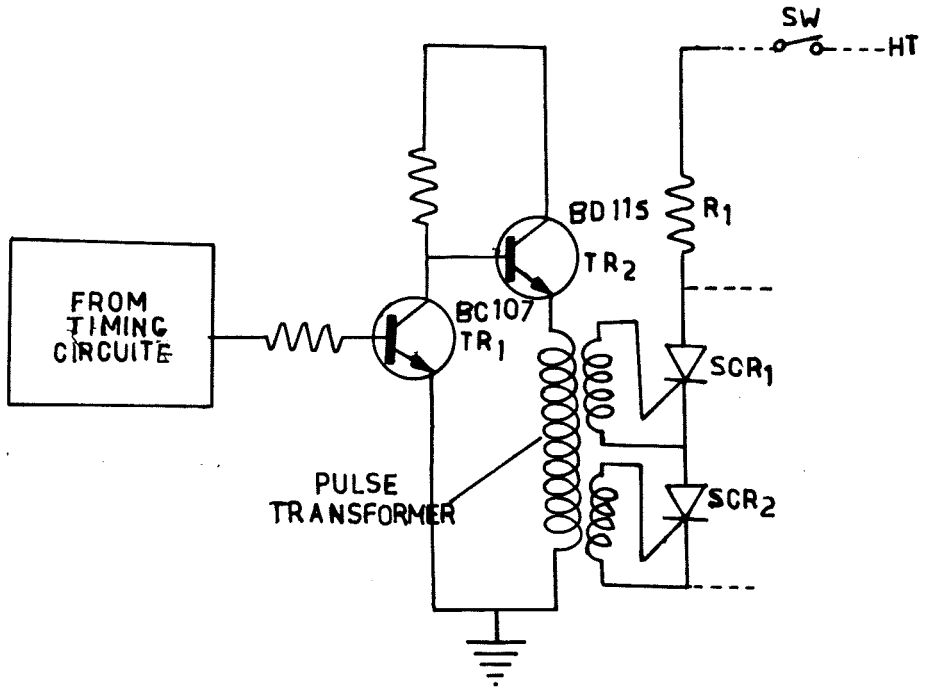


Fig.(5.18) The gates amplifying and isolating circuit.

However, the pulses received across the secondaries do not have enough current (power) to fire the SCRs. To increase the current obtainable from the pulse another stage of emitter follower was cascaded with TR_2 as shown in Fig.(5.19). A complete block diagram of the final circuit is shown in Fig.(5.20). It should be borne in mind that since the pulse obtained by this circuit is generated by the discharge of a series of capacitors, the pulse height is necessarily not constant throughout the pulse.

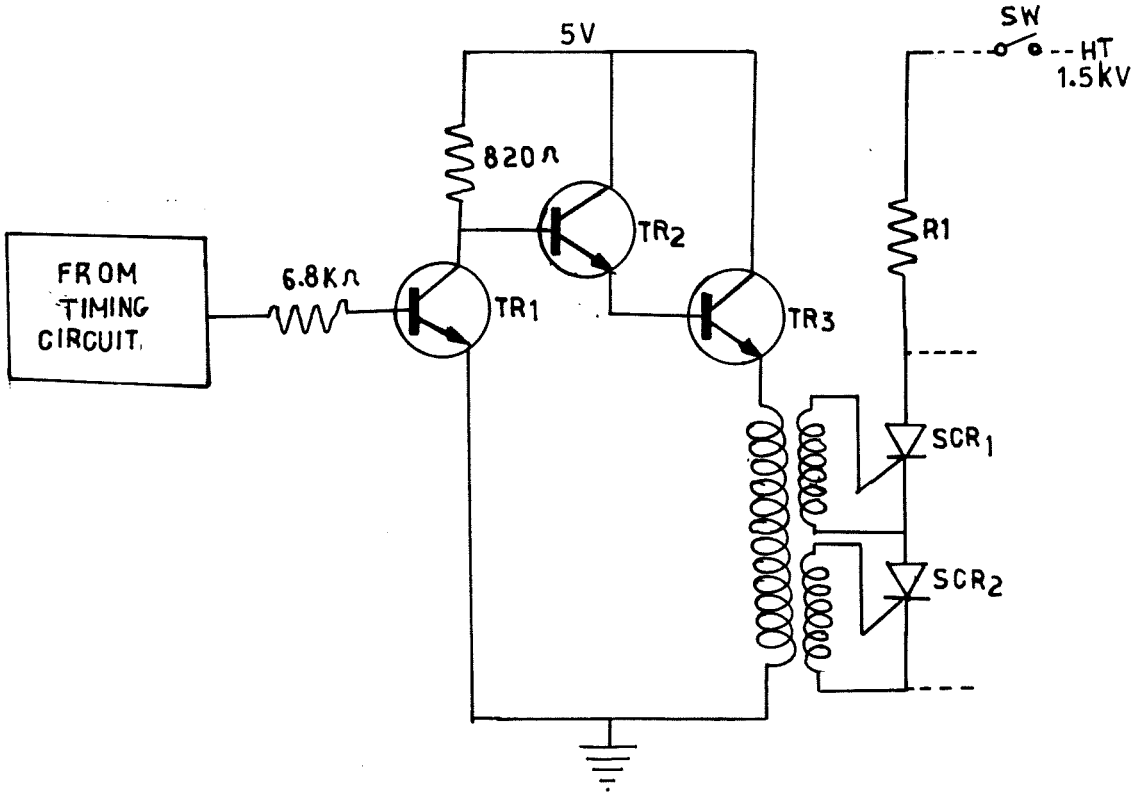


Fig.(5.19) The final gate drive circuit.

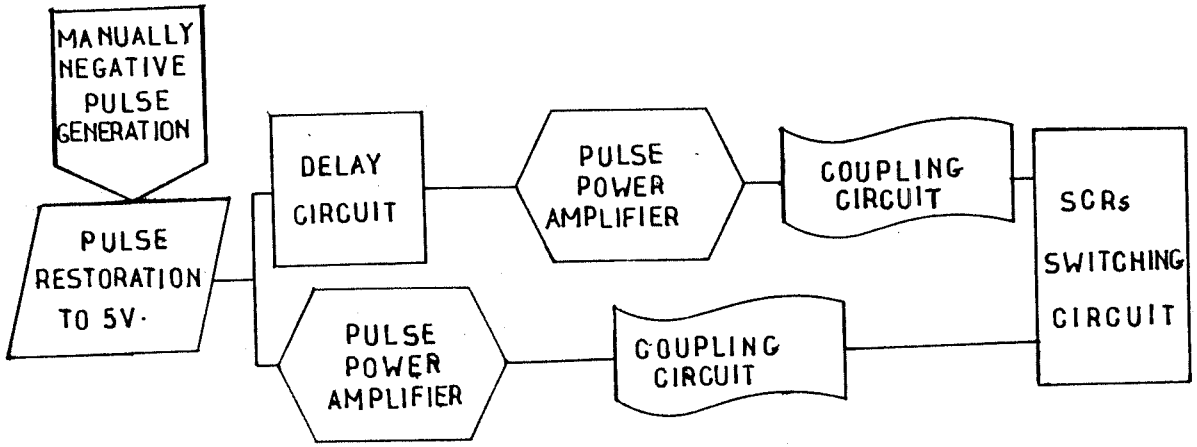


Fig.(5.20) The complete block diagram of the circuit for high voltage pulse trimming, (authors design).

5.6 THE TRIMMING MEASUREMENTS

5.6.1 MEASUREMENTS ON THE TRIMMER

In this section, the results of the measurements on the trimmer are presented. The graphs in Fig.(5.21) indicate the pulse width against variations in R_t for different C_t's. The required values of R_t and C_t for a given pulse width can be obtained by referring to these graphs.

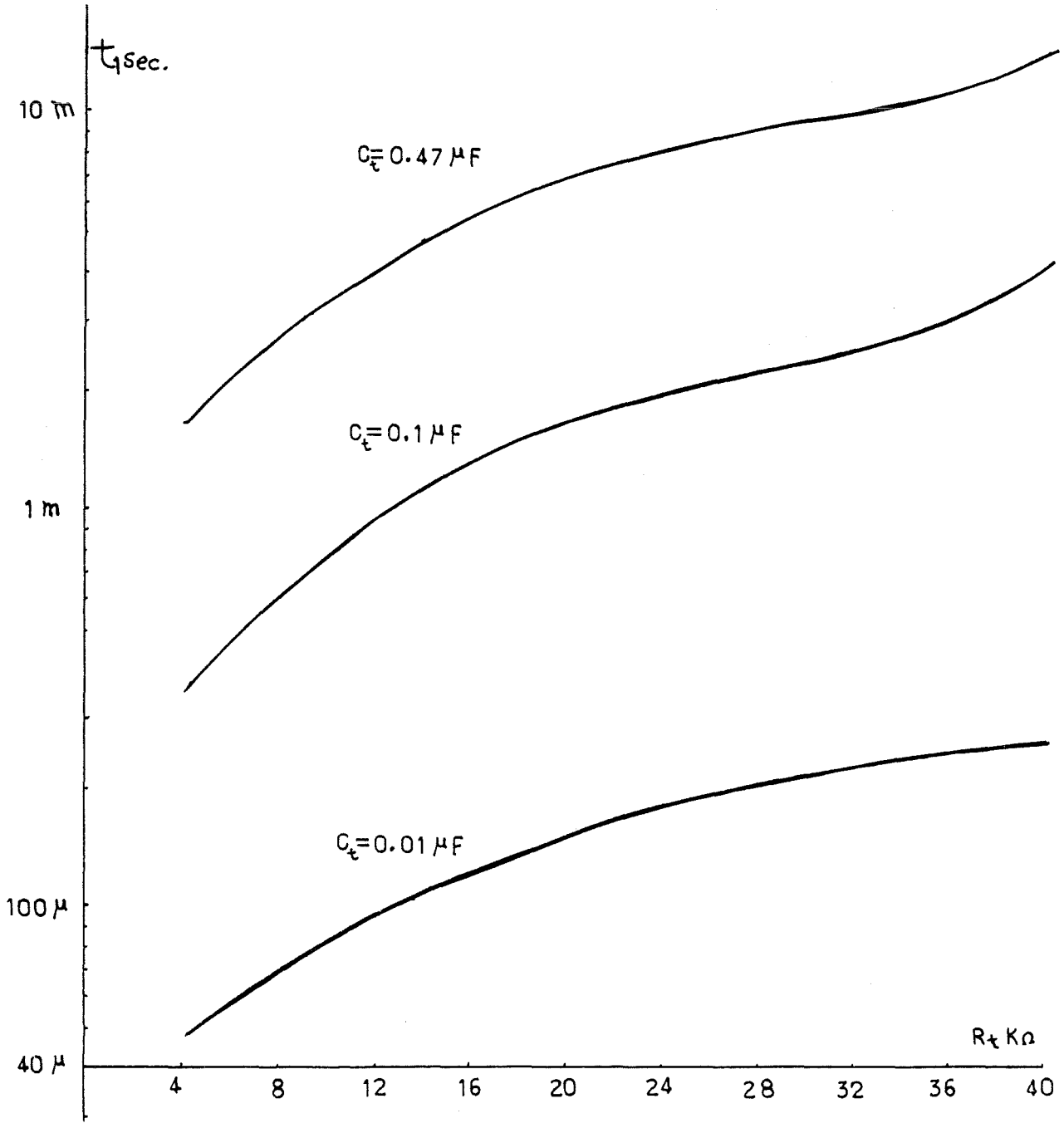


Fig.(5.21) Variation of t_1 against R_t and C_t, see figures 5.14 & 5.15.

5.6.2 THE TRIMMING RESULTS

To investigate the application of the high voltage pulse trimmer, resistors of two different sizes (see sections 4.7 and 4.12), with or without the dielectric layer on top, were put through the high voltage trimming procedure.

The priority was given to the resistors ESL 2813 (A) and the Dupont 1331 (D) for examination in this study because, these resistors have been more compatible with some dielectric inks than other resistors -see sections 4.7 to 4.19. It was thought that, since these resistors are especially designed to be high voltage resistant, they cannot be trimmed by application of high voltage pulses. This was verified by the results of the trimming tests on the resistors A and D -see Fig.(5.22). However, it was then seen that after printing a dielectric layer over the resistors, some of the resistors' properties were changed. This was especially observed on the voltage sensitivity of the resistors, as it was of particular interest for trimming.

A comparison between the graphs of Fig.(5.22) and Fig.(5.23) indicates that the voltage sensitivity of the resistors A and D have decreased due to the presence of the dielectric layer on top. The nature of the resistance change under high voltage pulses is studied in detail in the following sections.

a. VARIATION OF ΔR/R% AGAINST NUMBER OF PULSES APPLIED

Figures 5.22 and 5.23 show the percentage of the resistance change against the number of the pulses applied to the terminals of the resistors. With the pulse voltage at 1.2kV/cm and the constant pulse width of 12μsec, a maximum of 10 pulses were applied to each resistor.

Resistors A and D, with a dielectric layer on top, showed a sudden increase in resistance after several pulses were applied to them -see Fig.(5.23), whereas this effect was not observed when the resistors were not covered by the dielectric layer -Fig.(5.22). This peculiar behaviour is certainly related to the presence of the dielectric layer on top of the resistors. One possible explanation of the effect of the dielectric layer on the resistor layer is as follows.

Since both the resistors A and D are insensitive to high voltages, the constituents of their inks, the glass and the conductive phase particles, are uniformly mixed -see Fig.(5.7). Introduction of a dielectric layer on top of them would disrupt this uniformity and result in a non-uniform network of conductive phase particles. Therefore, the resistors are more susceptible to high voltage pulses as can be seen from Fig.(5.23). The decrease in resistance is due to microwelding between the conductive phase particles. After several pulses are applied, microwelding between small particles produces a number of big conductive aggregates. The sudden increase in resistance after this process is caused by the voltage breakdown between the big aggregates. A picture of this process is shown in Fig.(5.24). A photograph of the structural damage of the thick film resistors, which was caused by the previously explained breakdown, is shown in Fig.(5.25). This shows that there is a limit to the electric field intensity and the number of pulses that can be applied to the resistors.

- Resistors of investigation (1)

× Resistors of investigation (2)

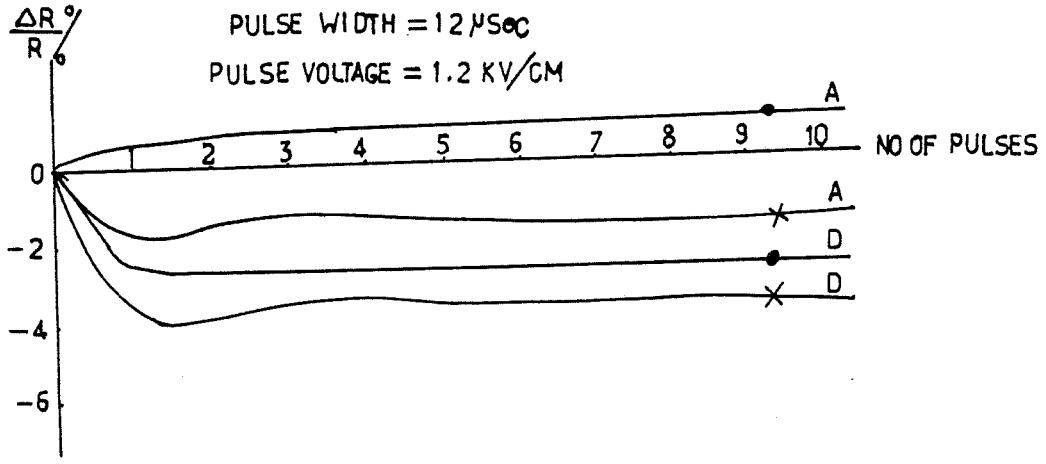


Fig.(5.22) Behaviour of resistors A and D against number of high voltage pulses applied.

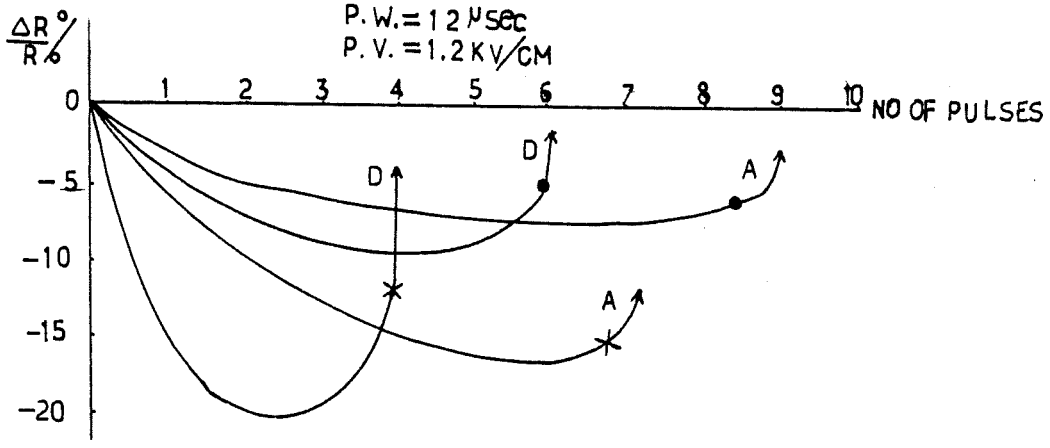
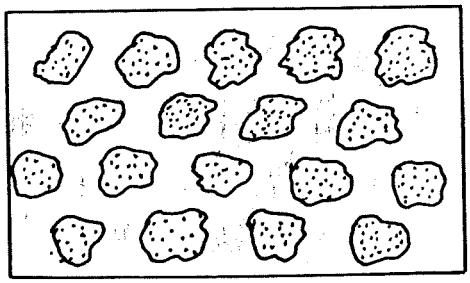
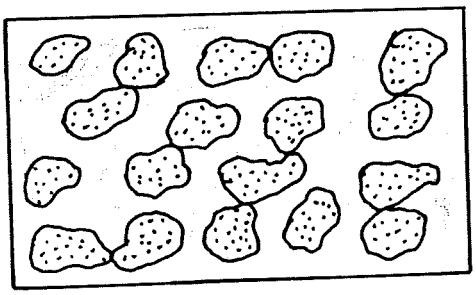


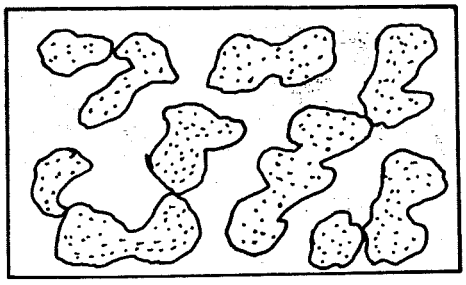
Fig.(5.23) Behaviour of resistors A and D with dielectric layer on top.



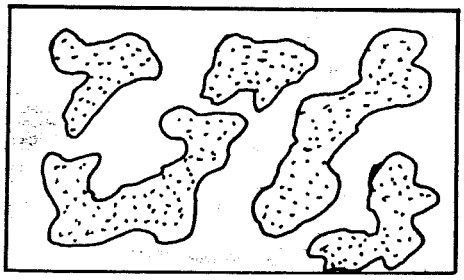
a. The resistor mixture before printing the dielectric layer on top of it.



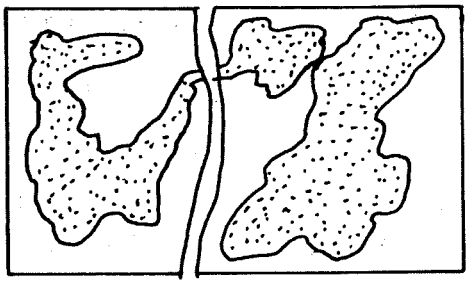
b. The resistor mixture after printing and firing the dielectric layer.



c. The resistor mixture after the application of a few high voltage pulses.



d. The resistor mixture after the application of several high voltage pulses.



e. The complete breakdown of the resistor after the application of an excessive number of high voltage pulses.

Fig.(5.24) The diagramatic illustration of a possible breakdown mechanism of thick film resistors, with dielectric layer on top, under high voltage pulses (explanation suggested by the author).

Metal aggregates 

Glass 

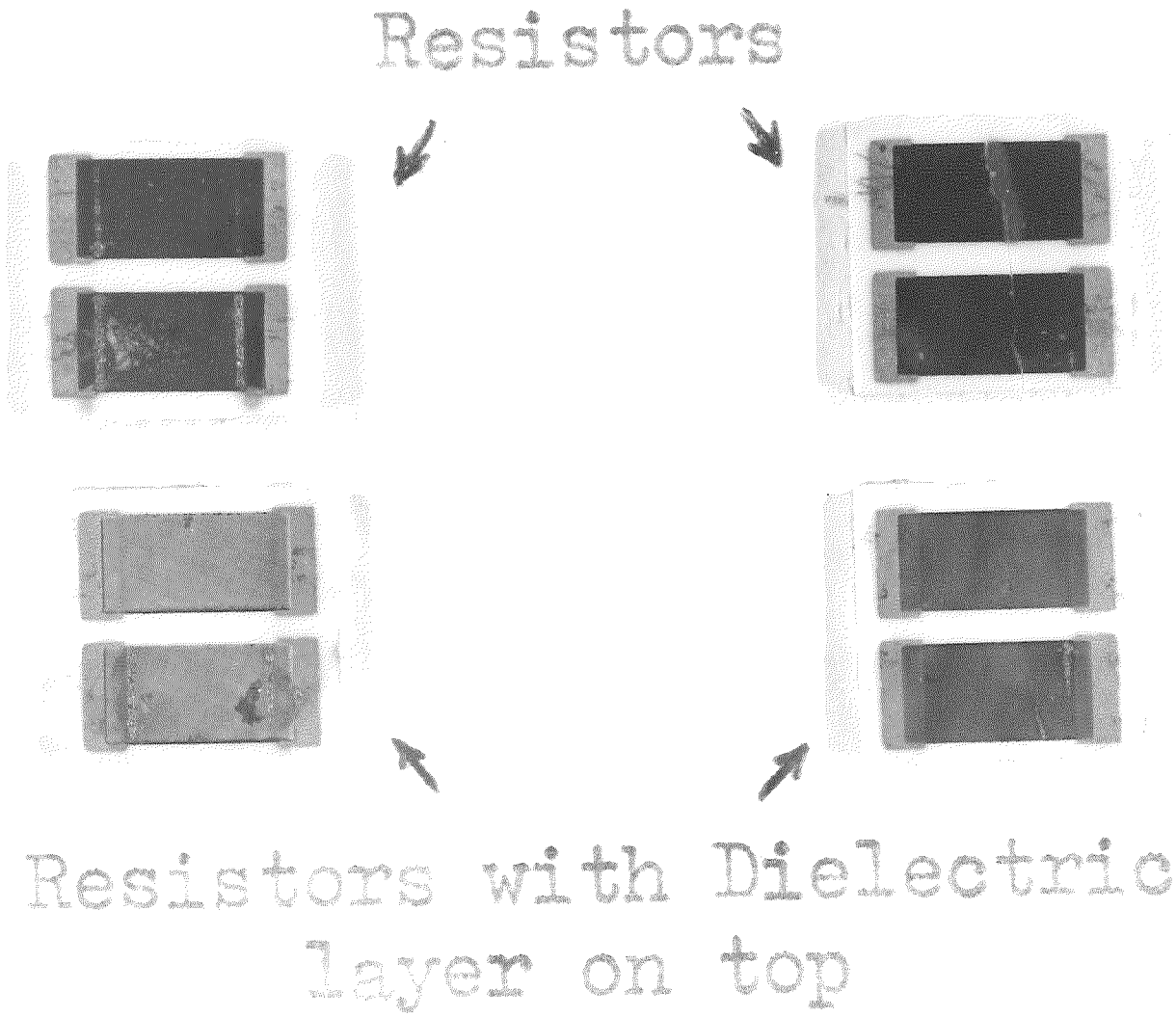


Fig.(5.25) A photograph of the thick film resistors damaged under high voltage pulses .

b. EFFECT OF THE PULSE WIDTH ON MAXIMUM $\Delta R/R\%$

The results of Pakulski's investigation [50] on the relation of pulse widths with the maximum possible amount of trimming showed that a succession of narrower pulses achieves a greater amount of trimming. However, Himmel [48]&[58] found a different result in his investigation in which the discharge time (ie the pulse width) is not critical for the amount of resistance change. These contradictory results show that there is no precise and consistent behaviour. However, in the tests carried out by the author, results similar to those of Himmel's were obtained as illustrated in figures 5.26 and 5.27 for the resistors A & D respectively with dielectric layers on top. Only the application of pulse widths above 30msec caused marked increases in the ratio $\Delta R/R$. This sometimes caused the complete failure of the resistor D with or without a dielectric layer on top and the complete failure of resistor A with a dielectric layer on top. A likely explanation for the increase in resistance for higher pulse widths is the occurrence of partial breakdown of the glass phase due to the heat produced by the pulse. The graphs of figures 5.26 and 5.27 once more indicate the above characteristic of the resistor changes after printing the dielectric layer on top of them.

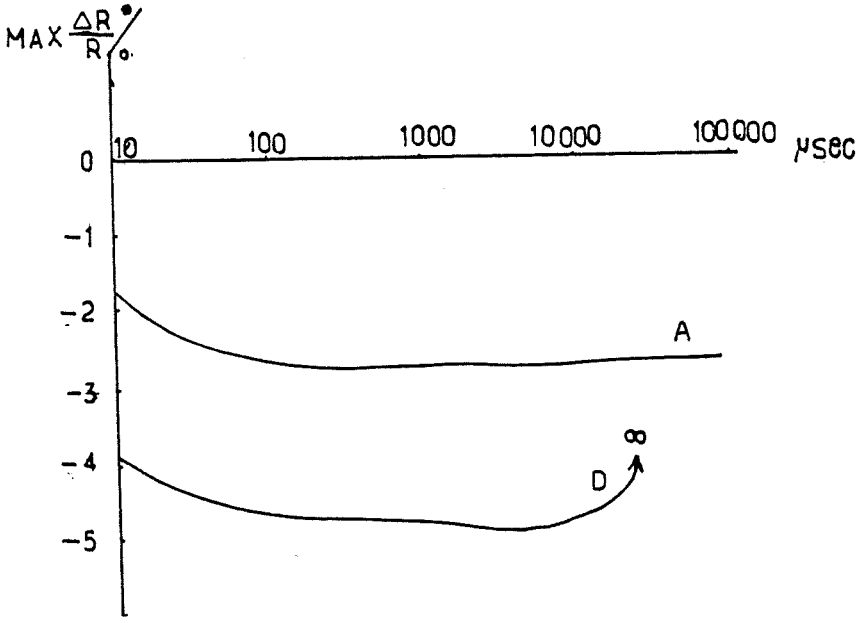


Fig.(5.26) Variations of resistors A and D against the high voltage pulse width.

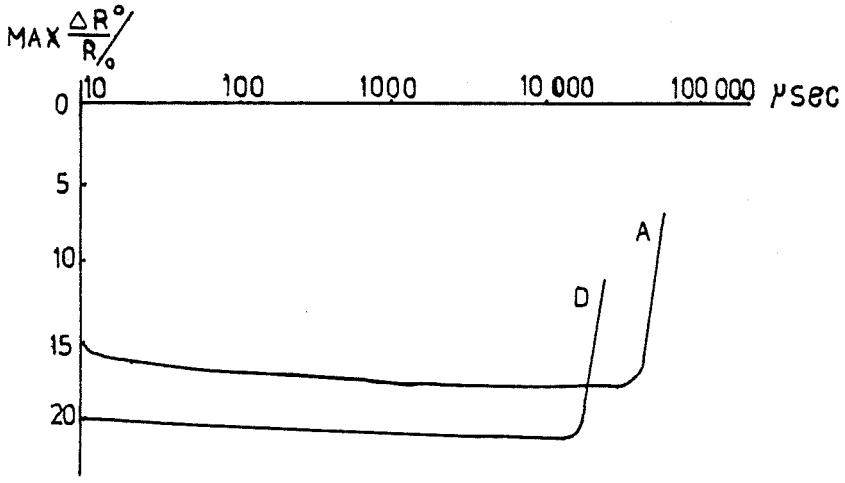


Fig.(5.27) Variations of resistors A and D with dielectric layer on top against the high voltage pulse width.

C. EFFECT OF PULSE VOLTAGE ON MAXIMUM $\Delta R/R\%$

Figures 5.28 and 5.29 show the effects of pulse voltages up to 2.2kV/cm on resistors A and D with and without dielectric layers. As the voltage increases, a drop in resistance occurs. These resistance changes are small for the larger area resistors. In these figures, the symbol ∞ indicates the destruction of the resistors. The significant effect of the dielectric on the resistors can also be observed by comparing Fig.(5.28) with Fig.(5.29). The most likely failure mechanism of the resistors in this test appears to be one with the following sequence:

1. The excessive voltage applied to the resistors will raise the resistors' temperature.

2. The current rises further due to a decrease of resistance caused by either the negative temperature coefficient of resistance, or microwelding between the conductive particles.

3. The resistors reach a new permanent equlibrium or a combination of high temperature and very high local fields causes a breakdown within the glass phase of the resistors. The glass interfaces between the conducting aggregates are destroyed and this causes a catastrophic rise in resistance and structural damages as shown in Fig.(5.27).

● Resistors of investigation (1)

× Resistors of investigation (2)

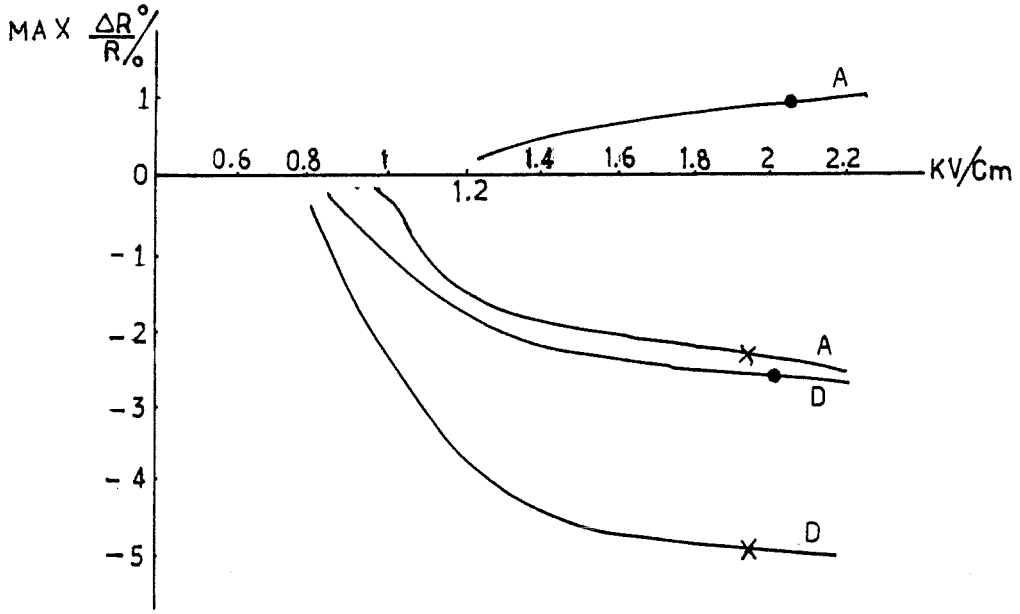


Fig.(5.28) Max. changes of resistor A and D against pulse voltage.

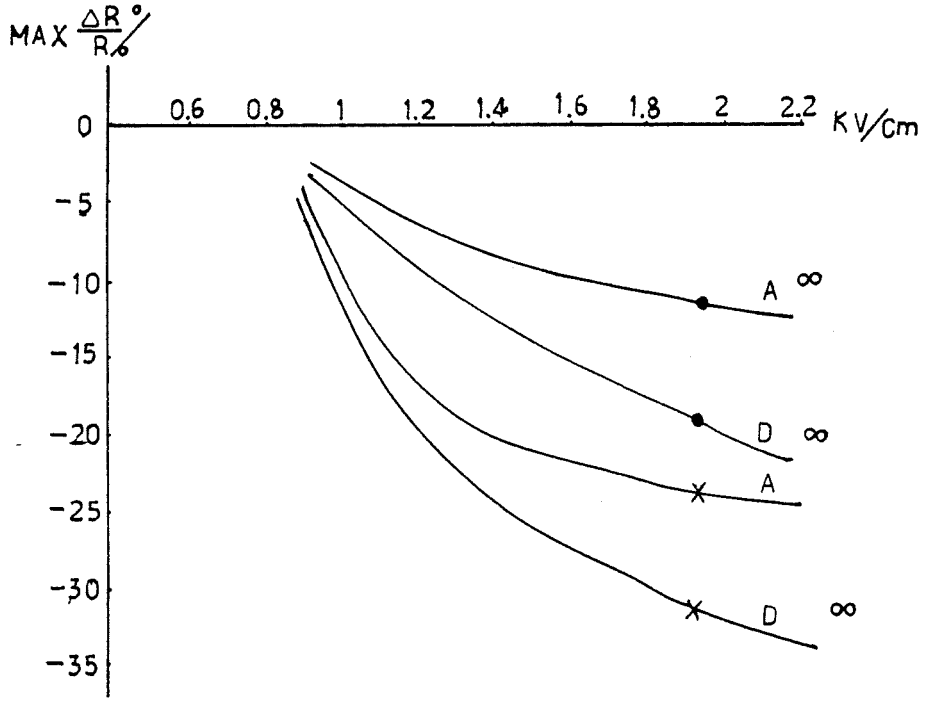


Fig.(5.29) Max. changes of resistor A and D with dielectric layer on top against pulse voltage.

5.7 DISCUSSION ON PREVIOUS WORKS

There are four techniques for trimming thick film resistors without physically removing any resistor parts. The techniques include, high frequency discharge, electro-chemical method, high electrostatic stress and high voltage discharge. The resistor trimming method based on the discharge of a high voltage pulses across the resistor terminal is non-destructive and is the only method which does not need accessibility to the surface of the resistor. Therefore, it is one possible method for trimming the resistors of an FDRC structure. Generally, changes caused by high voltages are of both reversible and irreversible type. Networks with relatively fewer non-tunnelling barriers have a less irreversible change of resistance [59].

Early experiments [60] on trimming techniques for glaze resistors had suggested increasing the resistance value by drawing a spark to the resistor surface. Other investigations [48]&[50] on this effect, however, indicated that the effect is a little more complex than that of simply increasing the value of the resistance. As far as the effect of trimming on TCR is concerned Pakulski [50] has suggested that the TCR becomes smaller as the trim percentage is increased and that the effect is more pronounced for the lower value compositions.

One of the characteristics commonly seen in high value resistors is the successively smaller permanent change in resistance that occurs with repeated high voltage pulsing [61]. At higher applied voltages, the higher dielectric barrier breakdown is responsible for greater permanent changes in resistance [62].

Olivei [57] has postulated two possible mechanisms to account for the behaviour of thick film resistors under high voltages:

1. Disruption of conductive phase paths with heating with the consequent increase in resistance;

2. "Micro-welding" of initially separated conducting regions via field dependent breakdown in the region between conducting areas.

Presumably, the latter mechanism is dominant at higher resistances because of the higher glass concentration. Himmel [48] has generalized the response of a thick film resistor to high voltage pulses as follows:

1. The resistance of the lower resistance materials ($\rho < 100\ \Omega$/sq) increases in value with multiple high voltage pulsing.

2. The higher resistance materials ($\rho \geqslant 500\ \Omega$/sq) showed resistance changes that were initially negative and then became positive.

3. For materials above 1 kΩ/sq, resistance changes were negative.

4. The graphs of resistance against the number of pulses applied follows approximately an exponential curve. No further changes were observed after approximately ten pulses.

5. The effect of increasing voltage while keeping the number of pulses constant was a decrease in resistance for high ρ materials and an increase in resistance for low ρ materials.

6. In many materials, repeated pulsing heated the resistor sufficiently to cause a TCR related change evidenced by a short term drift after pulsing.

5.8 DISCUSSION OF THE WORK ON TRIMMING IN THIS CHAPTER

It was shown in this chapter that it is desirable to use a method of trimming which does not change the resistor film geometry, such as the high voltage pulse trimming. Using the high voltage pulse trimming method, some resistors, both with and without dielectric layers, of two different sizes were examined for trimming.

Graphs of figures 5.22 - 5.29 show the behaviour of the resistors under high voltage pulses. The graphs of Fig.(5.22) indicate that most of the changes due to high voltage pulses occurred during the first few pulses. However, this is not the case when resistors have a layer of dielectric on top. Fig.(5.23) shows that resistors with dielectric layers exhibit coarser changes against the number of pulses applied and, after a certain number of pulses the structure of the resistors breaks down and renders it open circuit. Figures 5.26 and 5.27 also indicate that increasing the pulse width has little effect on the maximum change of resistance. However, at a certain width the resistor structure breaks down. Figures 5.28 and 5.29 show that the sensistivity of resistors to high voltages starts from a certain voltage and increases as the voltage is increased and then becomes steady in an exponential form.

From the trimming experiments reported in section 5.6, it can be concluded that:

1. Resistors with dielectric layers on top are more susceptible to high voltage pulses than the resistors without dielectric layers. In other words, the resistors will lose their voltage standing properties after a dielectric is printed and fired on top of them.

2. The devices of smaller size are more susceptible to high voltage pulses.

3. There is a critical voltage above which a change of resistance commences.

4. Voltages above the critical level cause destruction to resistors and irregular changes in the resistor values.

5. The number of pulses required to produce a significant change in resistance depends on the individual resistor being studied.

However, the exact nature and the extent of pulse induced changes are functions of the manufacturing process, the sheet resistance and the geometry of the resistor. Although some general ideas concerning the mechanism of resistance change under static discharge have been developed [46]&[63], a general formula has not yet been arrived at. However, in general, the following parameters are found to have a considerable effect on the amount of resistance change undergoing high voltage pulse trimming:

1. The base metal particles in resistor compositions.

2. The sheet resistance of the resistors.

3. The thickness of the resistor print [58].

4. The size and the shape of the resistor [64].

5. The presence of a dielectric layer on top of the resistor.

6. The firing temperature of the resistors [58].

7. The pulse shape.

8. Other factors relating to the structure of the resistor for a particular application.

CHAPTER 6

APPLICATIONS OF FDRC NETWORKS

6.1 INTRODUCTION

The thick film FDRC networks fabricated by the author (description in Chapter 4) were used in some of the circuit arrangements described by Kavanaugh [8]. Four circuit applications of FDRC networks that were examined in this research are as follows:

(i) Monostable multivibrator

(ii) Astable multivibrator

(iii) Oscillator

(iv) Notch filter

Details of the experimental work on these circuit applications are given in the following sections.

6.2 MONOSTABLE MULTIVIBRATORS

The lumped element collector-base coupled monostable multivibrator is shown in Fig.(6.1)a.

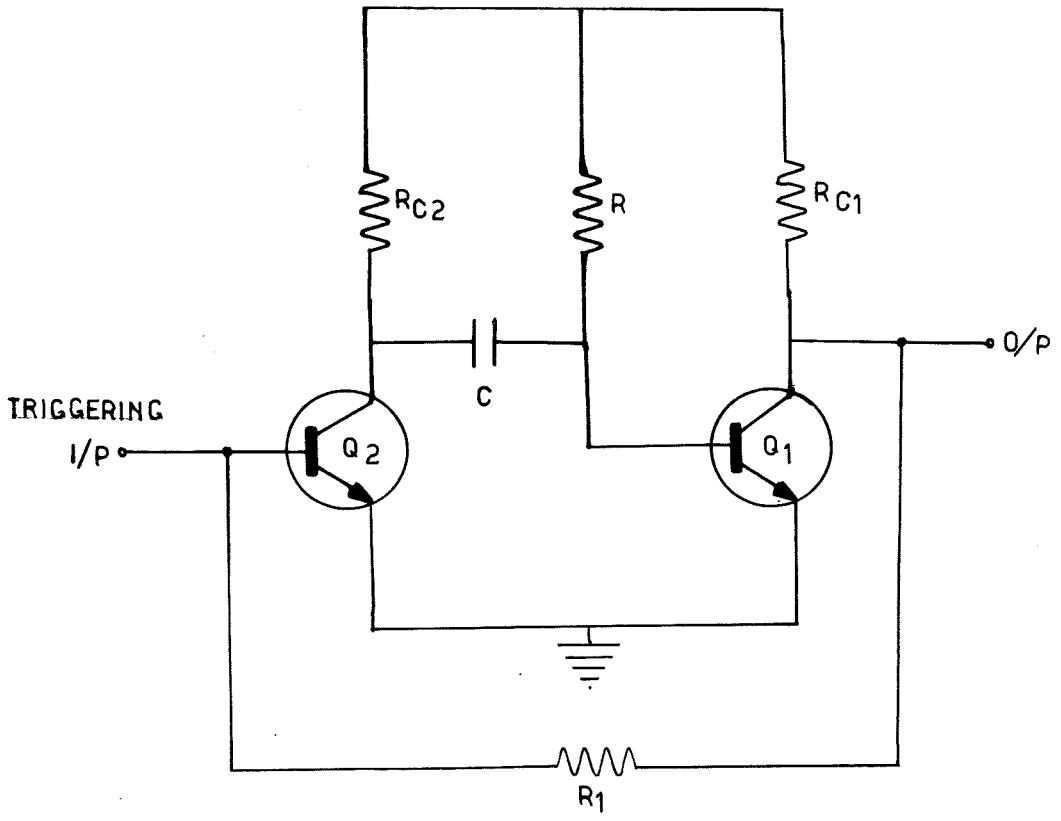


Fig.(6.1)a Lumped element collector base coupled monostable multivibrator.

It is well known that the pulse duration for this circuit is given by [65,p370]:

$$\tau = 0.69\ RC \qquad 6.1$$

where τ is the duration of the quasi-stable state for this circuit.

A similar circuit with the FDRC network replacing the RC timing network, is shown in Fig.(6.1)b.

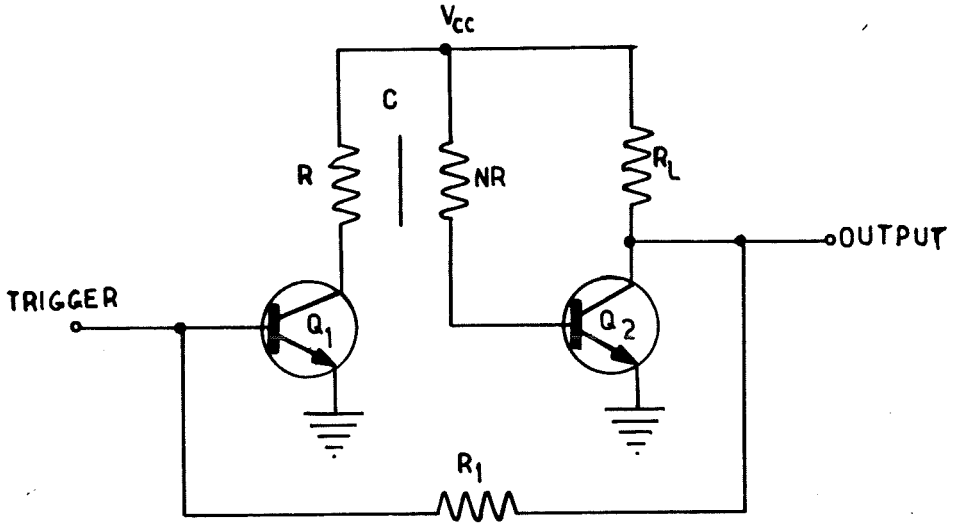


Fig.(6.1)b The FDRC network in a collector-base coupled monostable multivibrator.

The pulse duration for the network of Fig.(6.1)b is given by [66]:

$$\tau = 0.197\ (1+N)\ RC \qquad 6.2$$

Two FDRC devices, fabricated as described in section 4.7 and 4.13 were tried out to test the experimental performance of the circuit arrangement of Fig.(6.1)b. It was found that the circuit performed as expected and working backwards from equation 6.2 it was possible to estimate the value of the FDRC capacitance from the pulse-width obtained. The details of the experimental results are given in Table (6.1).

SUBSTRATE	R KΩ	N	τ μs	R Ω	R KΩ	TRANSISTORS	I/p COUPLING CAPACITOR	FDRC CAPACITANCE
D333b	13	0.146	2	150	10	2N3053	1 μF	1525 pF
D444b	1.3	0.769	0.8	100	10	2N3053	1 μF	1150 pF

Table (6.1) Practical details of the collector-base coupled FDRC monostable multivibrator circuit of Fig.(6.1)b, where is the measured value of the pulse duration.

From the results obtained it is clear that although the circuit appears to work quite satisfactorily for small values of τ (ie $\tau \approx 1\mu$s) the circuit arrangement would be quite unsuitable for use in applications requiring values of τ of the order of say 100 μs, since very large values of FDRC capacitance would then be required.

6.3 ASTABLE MULTIVIBRATOR

The lumped element collector-base coupled astable multivibrator is shown in Fig.(6.2)a. In this case, we have:

$$\tau_1 = 0.69\ R_1C_1 \qquad 6.3$$

$$\tau_2 = 0.69\ R_2C_2 \qquad 6.4$$

where τ_1 and τ_2 are the durations of the pulses at the collectors of Q_1 and Q_2 respectively. And, hence T the period of the wave form at either collector is given by:

$$T = \tau_1 + \tau_2 = 0.69\ (R_1C_1+R_2C_2) \qquad 6.5$$

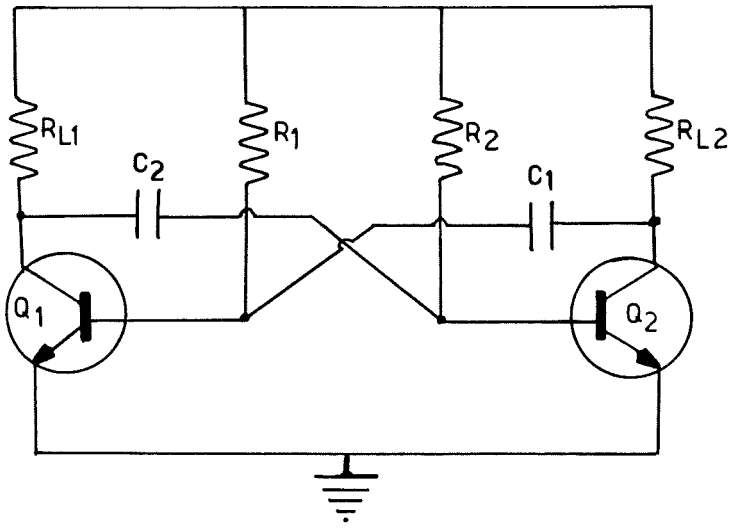


Fig.(6.2)a Lumped element collector-base astable multivibrator.

An analogous astable circuit arrangement using FDRC networks instead of the lumped RC timing networks has also been suggested by Hayes [66] and is shown in Fig.(6.2)b with the corresponding expression for T, the period of the output waveform, given by:

$$T = 0.197\ [(1+N_1)C_1R_1 + (1+N_2)C_2R_2] \qquad 6.6$$

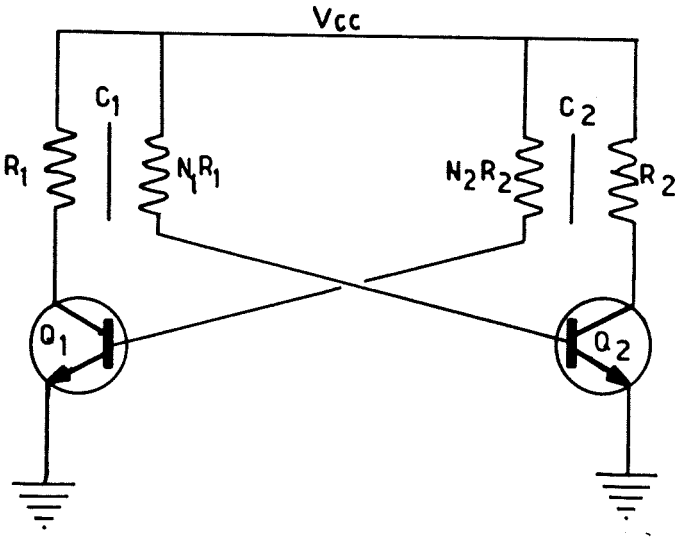


Fig.(6.2)b Collector-base coupled astable multivibrator using two FDRC networks as the timing & coupling elements.

The FDRC networks previously used to construct the monostable circuit described in the foregoing section were now used to implement the circuit arrangement being currently described. The details of the experimental results obtained are given in Table (6.2). T_c in this table is the calculated period using equation 6.5 and T_m is the measured period of the output waveform.

D333b			D444b			Transistors	Vcc volts	T_c μs	T_m μs
R_1 kΩ	C_1 pF	N_1	R_2 kΩ	C_2 pF	N_2	Q_1 & Q_2			
13	1525	0.146	1.3	1150	0.769	2N3053	20	4	0.71

Table(6.2) Practical details of the implementation of the collector-base coupled FDRC astable mulivibrator circuit of Fig.(6.2)b.

From the above results it is evident that $T_c > T_m$, ie the period of the waveform, as measured, was much smaller than that expected as a result of calculation. The reason for this discrepancy was that equation (6.5) has been derived on the assumption that both transistors are saturating, whereas from the amplitude of the observed waveforms it was quite clear that the transistors were nowhere near saturating and when an estimate of the periodic time was recalculated using the much reduced voltage

amplitude (as observed) a much closer agreement between the two values was found to exist.

6.4 OSCILLATORS

Oscillators using distributed RC networks have been described by various workers[7,8,67].

It was thought that it would be interesting to see how the FDRC devices, whose fabrication has been described in chapter 4, would perform when incorporated into one of these oscillator circuits.

The circuit arrangement described by Kavanaugh [8] and shown in Fig.(6.3) was used for this purpose.

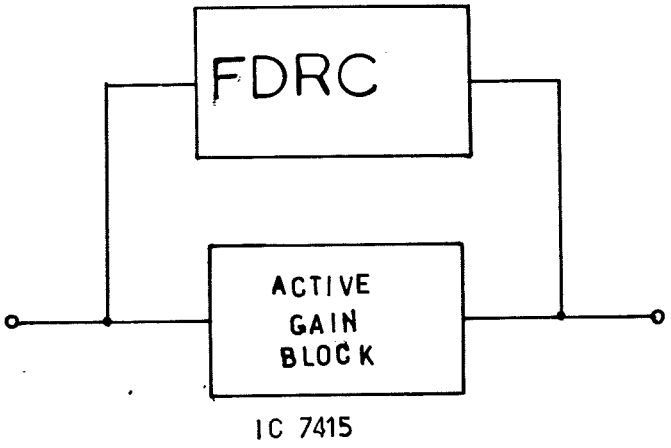


Fig.(6.3) An active amplifier with an FDRC network in the feedback path.

This circuit has been analysed by Kavanaugh [8] who has shown that the frequency of oscillation is given by:

$$f = \frac{30.75}{2\ (1+N)RC} \qquad 6.7$$

An oscillator was constructed using the FDRC device D333b with R = 13KΩ, N = 0.149 and C = 1525pF, substituting these values in equation 6.7 gives:

$$f = 31.4 \text{ kHz} \qquad 6.8$$

The waveform obtained is shown in Fig.(6.4).

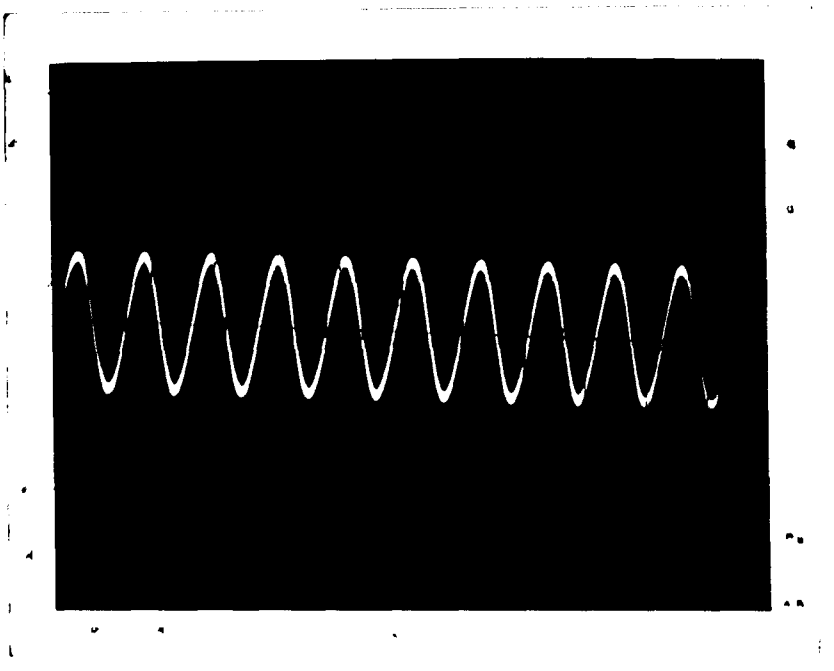


Fig.(6.4) Waveform of the FDRC phase shift oscillator.

VERTICAL SCALE: 20 mV/Cm
HORIZONTAL SCALE: 20 μSec/Cm

6.5 FILTERS

6.5.1 PASSIVE NOTCH FILTERS

The FDRC network as a passive notch filter has been introduced in section 2.4 -page 28. The configuration and analysis of FDRC passive notch filters are the same as those of Fig.(2.10) -see Fig.(6.5) below.

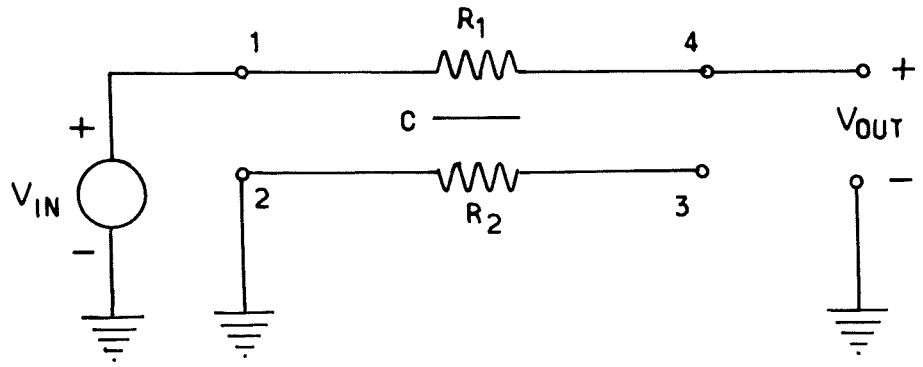


Fig.(6.5) A passive FDRC notch filter circuit.

The notch frequency was given by equation 2.57 which is repeated as equation 6.9 for easy reference.

$$f = \frac{19.75}{2\pi (1+N)RC} \qquad 6.9$$

Using equations (6.15) and (6.16) [page 177] and making the calculation on a computer, the curves shown in Fig.(6.9)a were obtained. These curves demonstrate the effect on the size and the shape of the dip as the value of N is varied, in the range $0.006 \leqslant N \leqslant 0.188$, is clearly even a small deviation from the critical value of $N = 0.086$ has a very profound effect on the magnitude and the sharpness of the dip, although it would appear that acceptable results would be obtained if values of N were confined to the range $0.066 \leqslant N \leqslant 0.166$ thereby allowing a massive tolerance of +93% to -23%.

In this section, three FDRC devices D444b, N334a and N344a which were fabricated in sections 4.14, 4.16 and 4.18 respectively, were each connected as a notch filter of the type shown in Fig.(6.5) and their frequency responses were measured. The method of section 2.5, ie using the notch frequency obtained for each device and also equation 6.9, is used to determine the capacitance of each device. For comparison, these capacitances together with the corresponding values estimated by bridge measurement in section 4.20 are listed below:

	D444b	N334a	N344a
capacitances obtained from notch frequency	Cc=131pF	Cc=224pF	Cc=325pF
capacitances estimated by bridge	Cm=137pF	Cm=238pF	Cm=310pF

The graphs of the measured responses of the FDRC notch filters together with the responses obtained from calculations are drawn by computer and presented in section 6.5.4.

It will be noticed that only a very rough estimate of the capacitance value can be obtained by bridge measurement methods. [This particular type of measurement has been investigated and shown to be only partially valid for distributed filters.]*

* Dr. A.J. Walton, University of Edinbrough. (Private communication).

6.5.2 ACTIVE BANDPASS FILTERS

An active bandpass filter [7] using an FDRC and a high gain operational amplifier is shown in Fig.(6.6). Kavanaugh [8] has analysed this circuit and has suggested a design procedure.

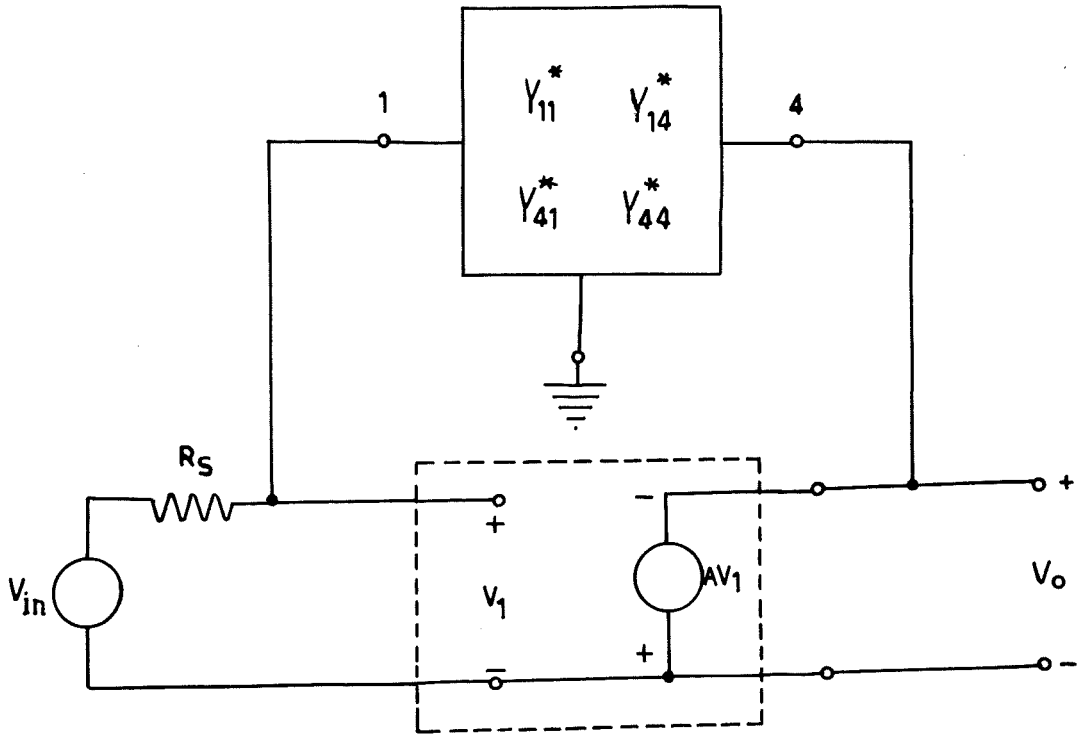


Fig.(6.6) An active bandpass filter using an FDRC network with the ports connections as shown in Fig.(6.5)

The design procedure proposed by Kavanaugh [8] is only applicable to the design of band-pass filters when the value of N (ie the ratio of the two resistors of the FDRC network) is 0.08627, which is the value of N for true zero, -see page 31. The ratio of the values of the two resistors of the FDRC network, when it is fabricated on thick film ceramic, is not controllable with the accuracy needed. Since the trimming method for the FDRC structure is not yet fully established, the resistors cannot be trimmed to the exact value to give N = 0.08627. Therefore, using the FDRC device N344a which had been fabricated in section 4.18, an active band- pass filter with no predetermined specification was implemented as shown in Fig.(6.7).

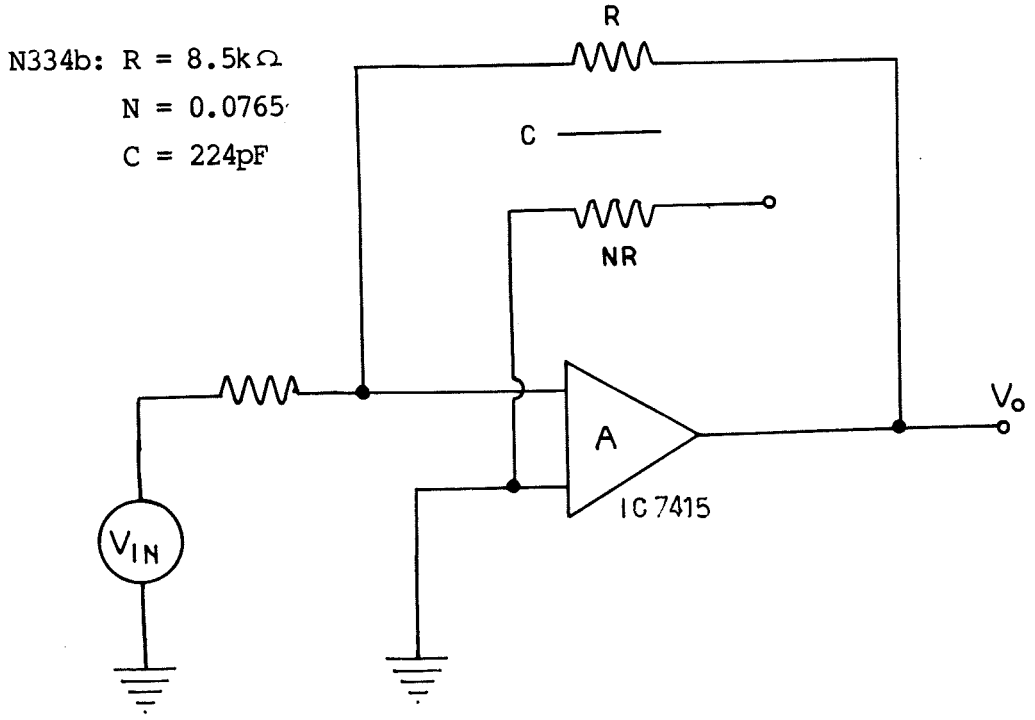
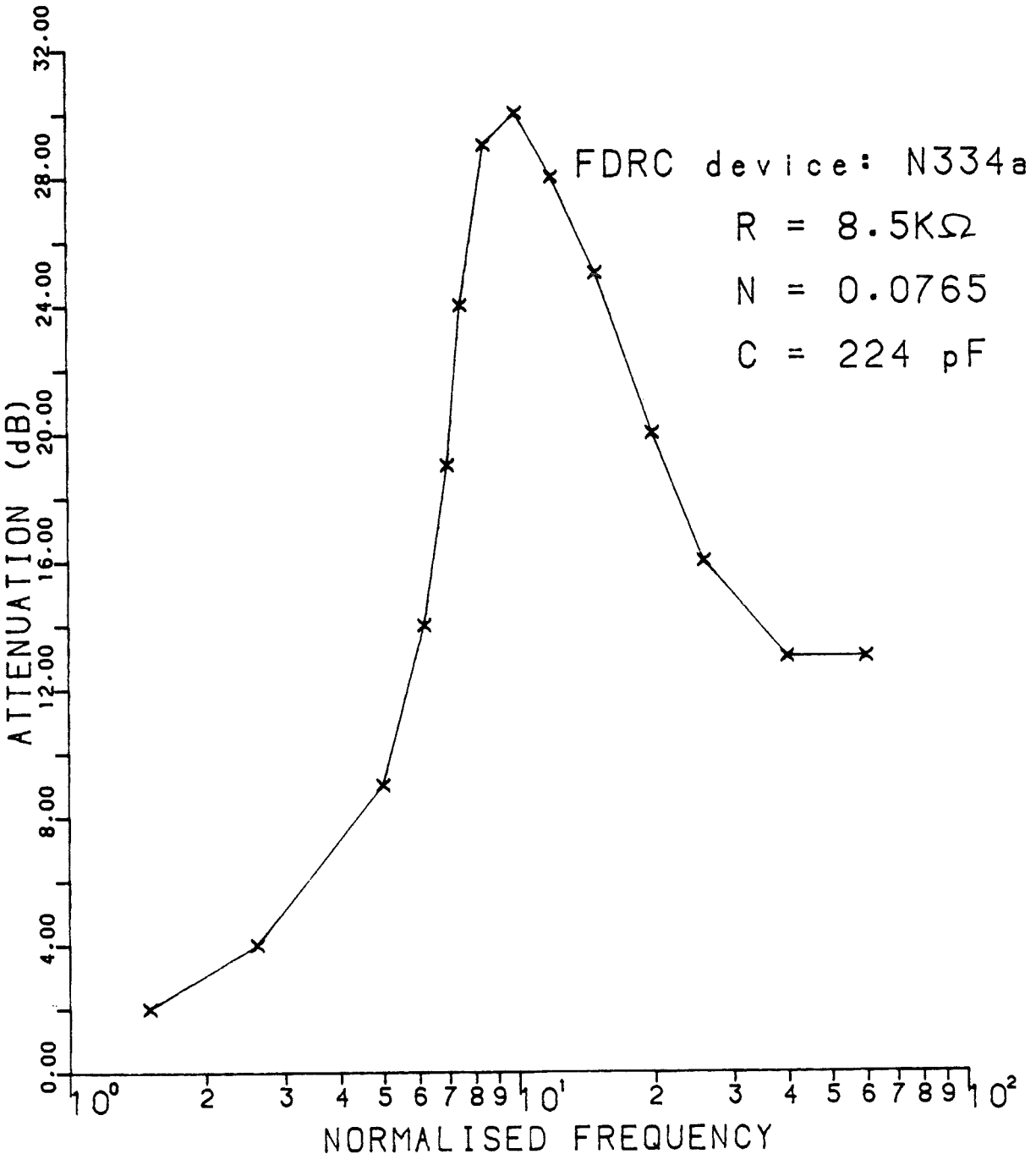


Fig.(6.7) An active bandpass filter using the N334 FDRC device fabricated as described in section 4.18.

The frequency response of the filter was measured and, by the use of the programme in Appendix 2, was plotted by computer as shown in Fig.(6.8). The comparison between the graphs of Fig.(6.8) and (6.11)c indicate that the notch frequency and depth of the passive FDRC filter are very similar to the corresponding values of the band- width and amplitude of the active filter.

FIG. (6.8)

THE ACTIVE FDRC FILTER
MEASURED FREQUENCY RESPONSE



6.5.3 COMPUTER ANALYSIS

In this section, the computer analysis of the frequency response of a number of FDRC networks in the notch configuration of Fig.(6.5) is presented as a set of graphs of gain against frequency for a series of different values of N. To find a suitable form of the gain equation for computer programming, the following modifications of the relevant formulae are made. From page 31 we have:

$$u = \sqrt{\frac{\omega}{2\omega_o}} = \pm \pi$$

substituting for ω_o from equation 2.56:

$$\omega = 2\pi^2 \frac{1}{(1+N)RC} \qquad 6.10$$

But for the true notch, from equation 2.59

$$N = \frac{1}{\cosh(\pi)} \qquad 6.11$$

substituting for N from 6.11 into 6.10 and let us denote this frequency by ω_r, thus:

$$\omega_r = \frac{2\pi^2}{\left(1+\frac{1}{\cosh(\pi)}\right)RC} \qquad 6.12$$

recalling θ form page 30:

$$\theta = \sqrt{j\omega(1+N)RC} \qquad 6.13$$

From equation 2.52, equation 6.13 can be writen as:

$$\theta = \sqrt{\omega(1+N)RC}\ (1+j) \qquad 6.14$$

Let us now substitute for RC from equation 6.12 into equation 6.14. Therefore,

$$\theta = \sqrt{(1+N)\left(\frac{2\pi^2}{1+\frac{1}{\cosh\pi}}\right)\left(\frac{\omega}{\omega_r}\right)}\ (1+j) \qquad 6.15$$

But from equation 2.50

$$\frac{V_o}{V_i} = \frac{1+N\cosh\theta}{(1+N)\cosh\theta} \qquad 6.16$$

Using equations 6.15 and 6.16, a computer plotting programme was written, through which the graphs of attenuation in dB against the normalized frequency $\frac{\omega}{\omega_r}$ for different values of N were plotted as shown in Fig.(6.9)a & b. The details of the programme are given in Appendix 3. By modifying this programme an attenuation graph was plotted for the "true zero" value of N, (which is from equation 6.11, N = 0.086266). This graph is shown in Fig.(6.10). The modified programme is also given in Appendix 3.

FIG. (6. 9) a

COMPUTER ANALYSIS

The FDRC Filter Characteristic

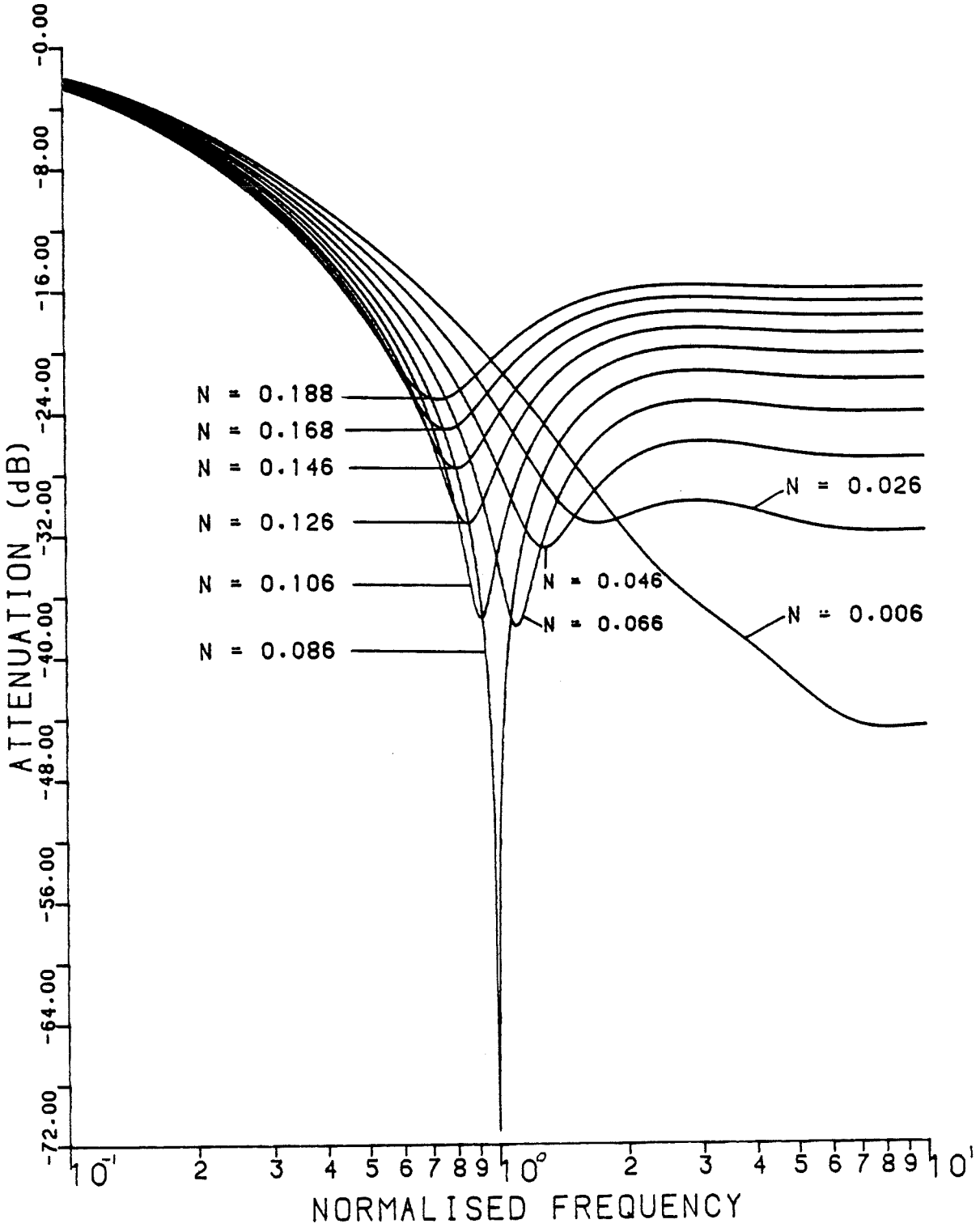
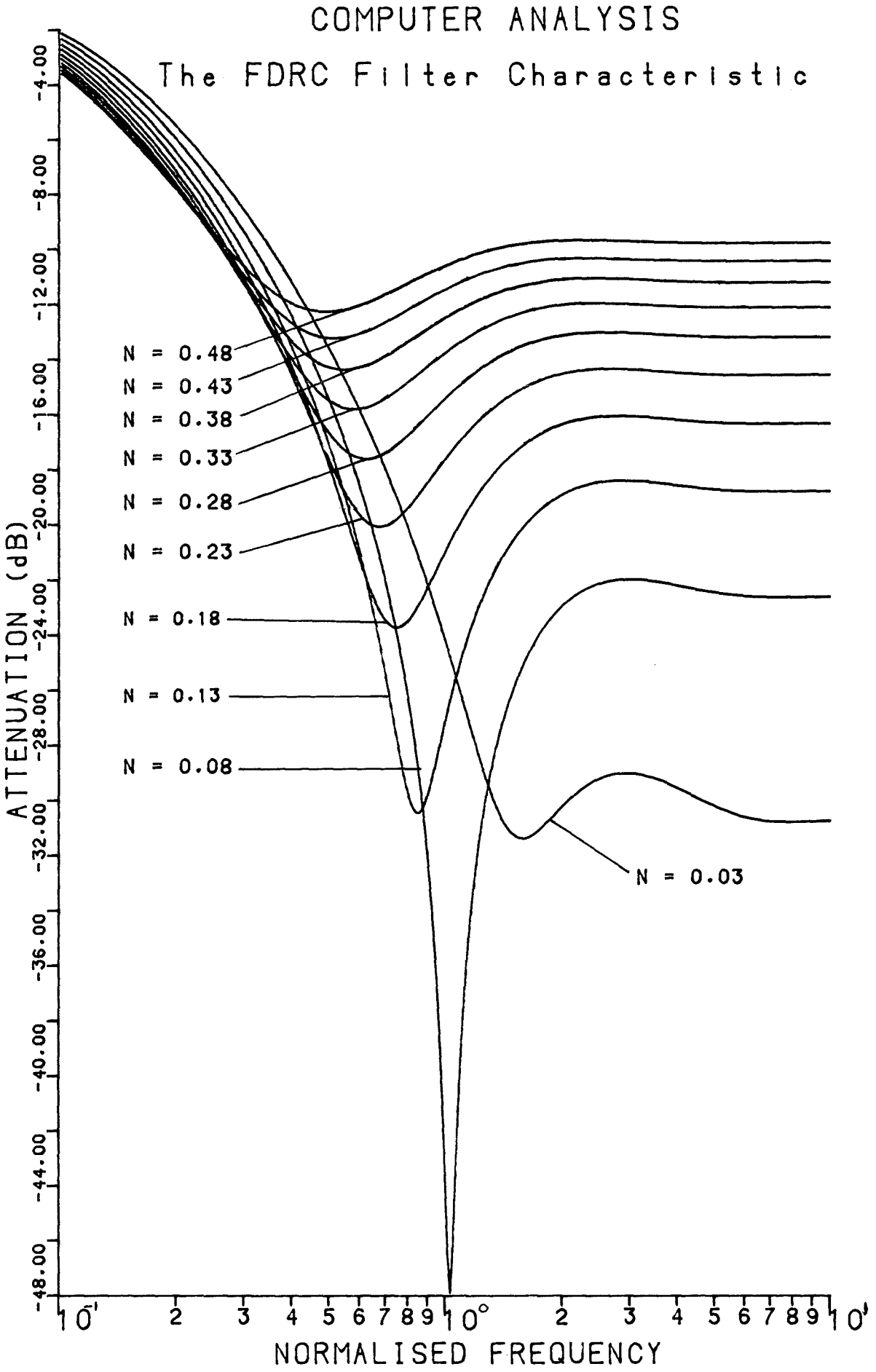


FIG. (6. 9) b


COMPUTER ANALYSIS
The FDRC Filter Characteristic
ATTENUATION (dB)
-4.00
-8.00
-12.00
-16.00
-20.00
-24.00
-28.00
-32.00
-36.00
-40.00
-44.00
-48.00
N = 0.48
N = 0.43
N = 0.38
N = 0.33
N = 0.28
N = 0.23
N = 0.18
N = 0.13
N = 0.08
N = 0.03
10'
2
3
4
5
6
7
8
9
10°
2
3
4
5
6
7
8
9
10'
NORMALISED FREQUENCY

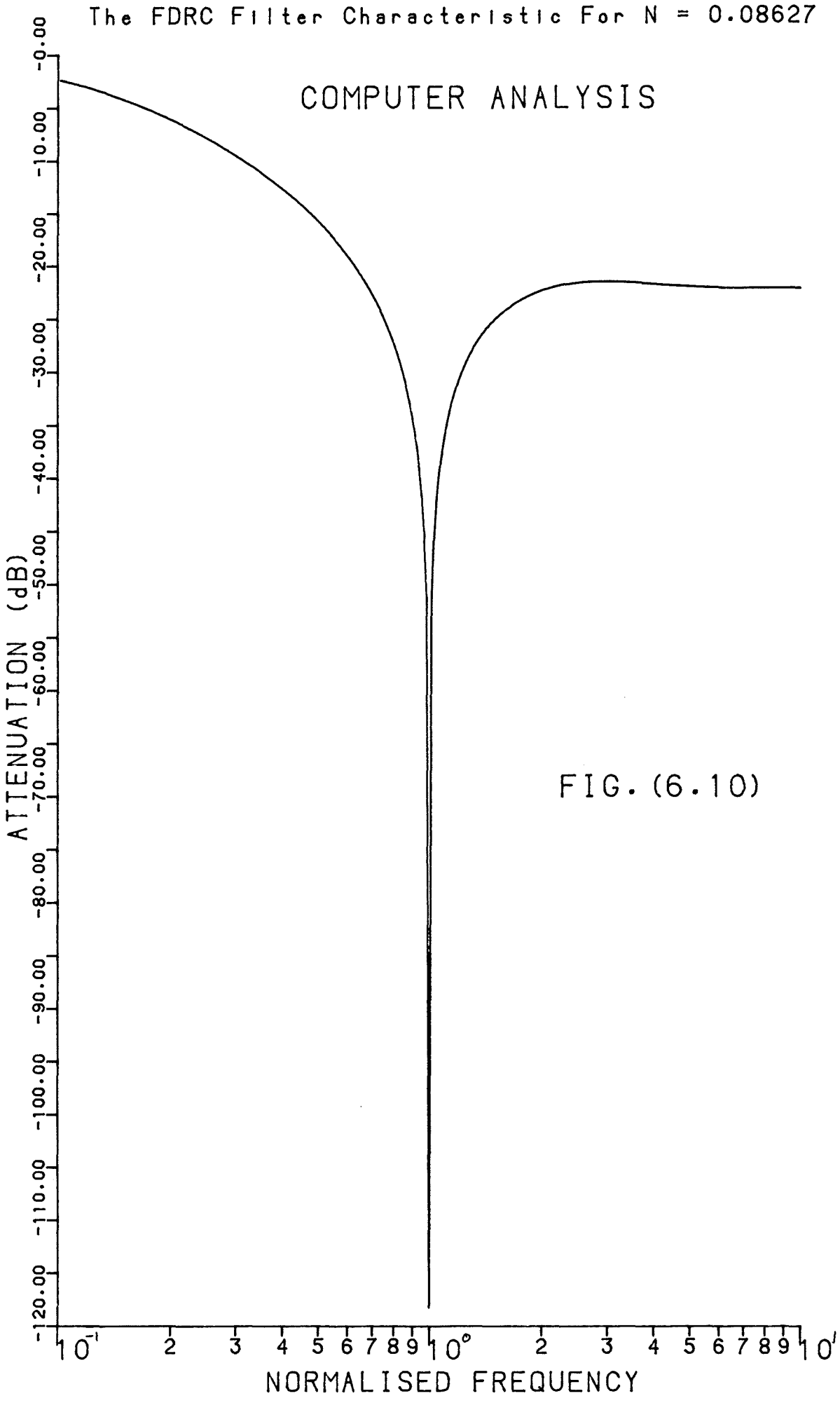

The FDRC Filter Characteristic For N = 0.08627
COMPUTER ANALYSIS
ATTENUATION (dB)
-0.00
-10.00
-20.00
-30.00
-40.00
-50.00
-60.00
-70.00
-80.00
-90.00
-100.00
-110.00
-120.00
10⁻¹ 2 3 4 5 6 7 8 9 10⁰ 2 3 4 5 6 7 8 9 10¹
NORMALISED FREQUENCY

FIG. (6.10)

6.5.4 COMPARISON

In order to compare the measured frequency response of the FDRC passive notch filters D444b, N334a and N344a with the theoretical frequency response, the frequency response of the device as a passive notch filter configuration (see Fig.6.5) was measured using the approprate measuring equipment, using equations 6.15 and 6.16, and substituting the value of N for each device, the theoretical responses of the devices were computed and together with the responses measured in section 6.5.1 are plotted by computer and shown in Fig.(6.11)a, b and c respectively. The frequency axes are normalized to ω_r, where ω_r is the notch frequency measured for each device. Detail of the programs are given in Appendix 4.

FIG. (6.11) a

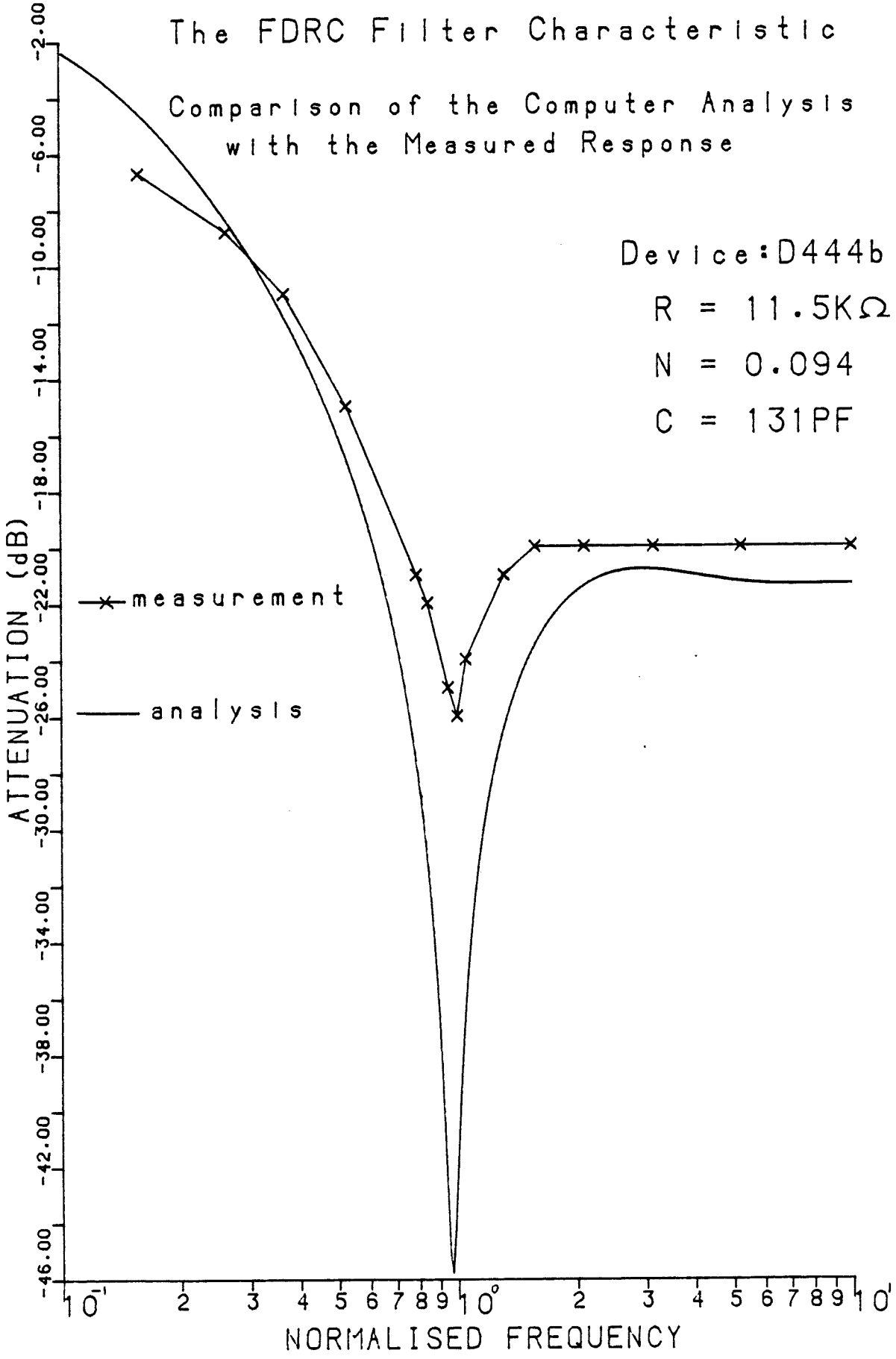

The FDRC Filter Characteristic
Comparison of the Computer Analysis with the Measured Response
Device: D444b
R = 11.5KΩ
N = 0.094
C = 131PF
measurement
analysis
ATTENUATION (dB)
-2.00
-6.00
-10.00
-14.00
-18.00
-22.00
-26.00
-30.00
-34.00
-38.00
-42.00
-46.00
10⁻¹ 2 3 4 5 6 7 8 9 10⁰ 2 3 4 5 6 7 8 9 10¹
NORMALISED FREQUENCY

FIG. (6.11) b

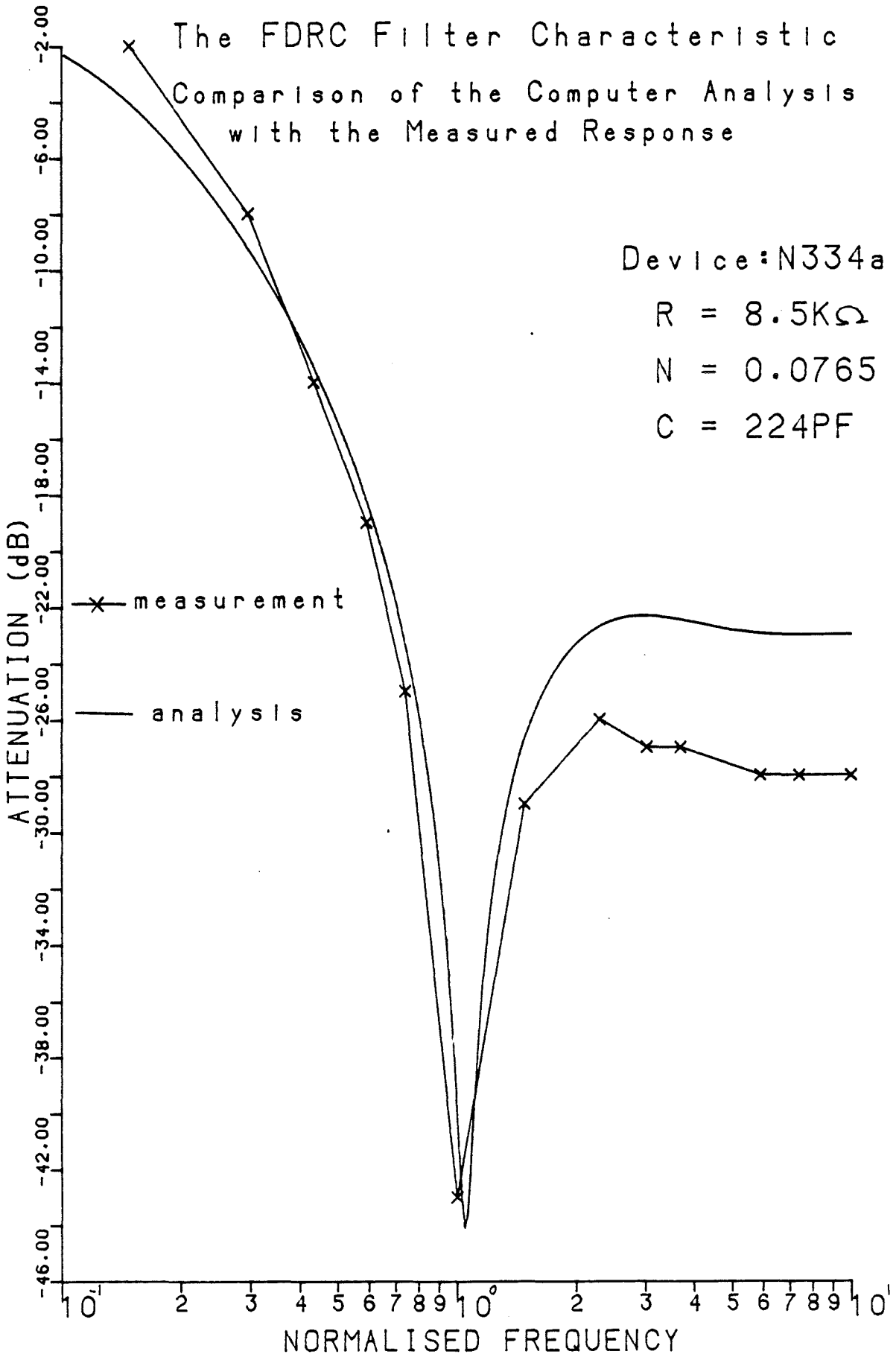
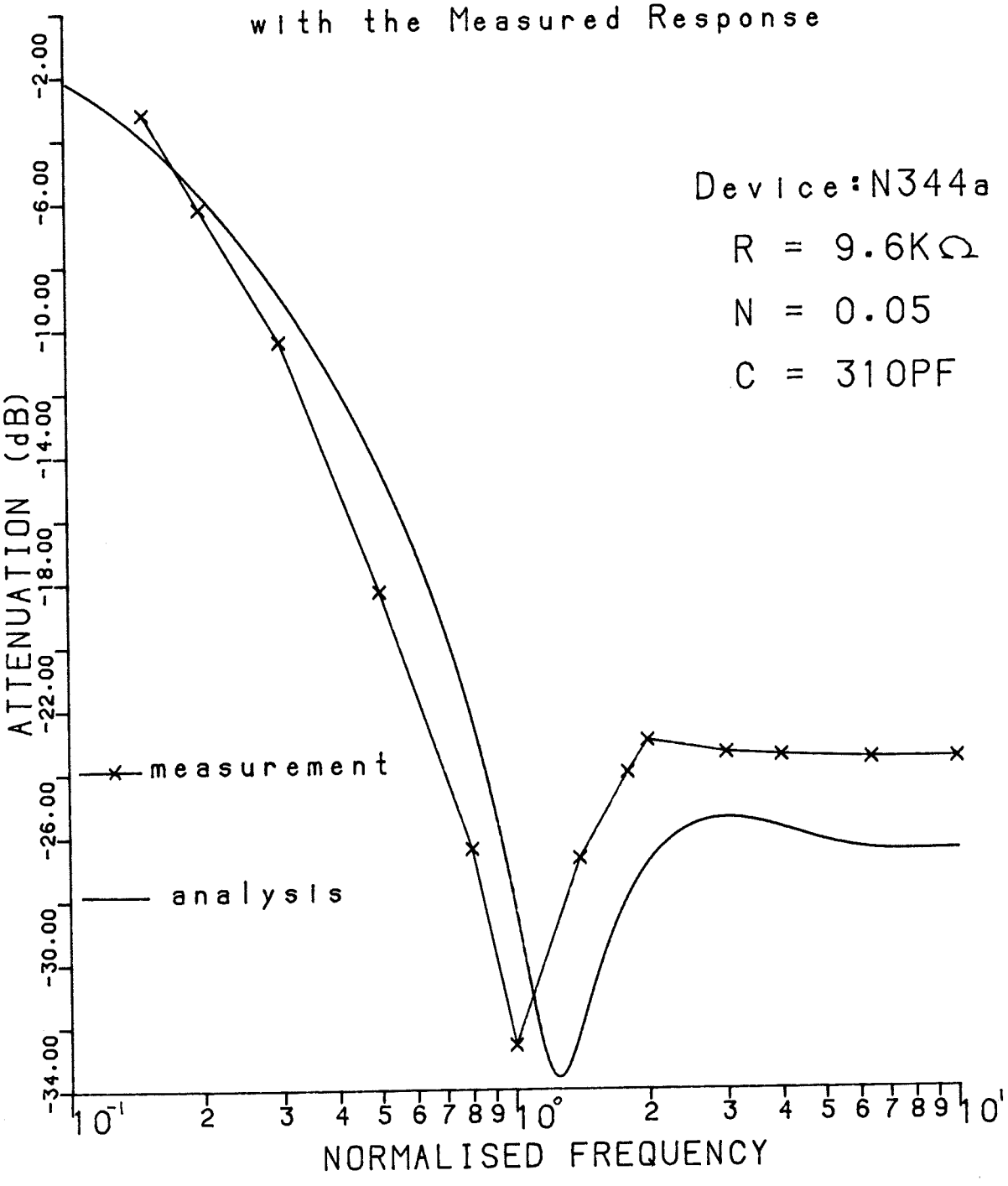

The FDRC Filter Characteristic
Comparison of the Computer Analysis
with the Measured Response
Device: N334a
R = 8.5KΩ
N = 0.0765
C = 224PF
measurement
analysis
ATTENUATION (dB)
-2.00
-6.00
-10.00
-14.00
-18.00
-22.00
-26.00
-30.00
-34.00
-38.00
-42.00
-46.00
10⁻¹ 2 3 4 5 6 7 8 9 10⁰ 2 3 4 5 6 7 8 9 10¹
NORMALISED FREQUENCY

FIG. (6.11) c

The FDRC Filter Characteristic

Comparison of the Computer Analysis with the Measured Response



6.5.5 COMMENTS ON THE ATTENUATION GRAPHS

The graphs of Fig.(6.9)a indicate that the notch frequency and depth are both very sensitive to slight changes in the value of N (as small as 0.02). However, as the value of N departs form the true zero value (ie N = 0.086266), the chages in the notch frequency and depth, for different values of N, are not much.

Figure (6.9)b presents the FDRC passive notch filter frequency response for larger changes in the value of N. The rapid change in the notch depth for different values of N, can also be observed form these graphs. However, it is more clear that with N values higher than the "true zero" value, which is N=0.086266, the responses of the filters have a notch shape, but, for N values lower than N=0.086266 the notch loses the shape and, therefore, the notch filter configuration of Fig.(6.5) is no longer valid as a notch filter.

Figure (6.10) shows the attenuation graph of an FDRC notch filter for the "true zero" value of N, which is N=0.086266. The graph indicates that a notch depth as deep as -120 dB can be obtained when N is equal to the "true zero" value.

Figures (6.11)a, b and c present both the measured and the theoretically obtained frequency responses of the D444b, N334a and N344an FDRC devices fabrication in investigations 5, 6 and 7 respectively, which are reported in sections 4.14, 4.16 and 4.18 respectively. The notch depth computed

for the D444b device is about 20 dB deeper than the notch depth measured, see Fig.(6.11)a. However, the notch frequencies of both the graphs are consistent. The graphs of Fig.(6.11)b indicate similarity between the measured and the computed frequency responses for the FDRC N334a device. This may be due to the fact that the value of N for this device is very close to the "true zero" value, (ie differing only by about $\pm$0.01).

The graphs of Fig.(6.11)c also indicate a similar notch shape for both the responses. However, the notch frequencies are more apart for this device. It can be concluded from Fig.(6.11)a, b & c that as the value of N gets higher than the true zero value, the notch frequencies of both the measured and the computed responses are more similar to each other, and as N gets lower than the "true zero" the differences between the notch frequencies of the two responses become larger.

CHAPTER 7

7.1 CONCLUSION

In conjunction with the rising interest in microelectronics and integrated circuits, much interest has been displayed in distributed- parameter networks. Thick films offer many advantages over vacuum evaporation thin films and silicon integrated circuits.

From the work that had been reported on the fabrication of distributed RC (DRC) networks onto thick film substrates, some of the problems likely to be encountered were known. This dissertation attempts to give details of a fabrication technique for a Fully Distributed RC (FDRC) network using thick film technology.

In order to cater for the special requirements of FDRC networks, several thick film resistor trimming methods were studied from which the high voltage pulse trimming was chosen as the preferred method. A high voltage pulse trimmer was designed the full design procedure and operation of which have been explained in detail. The successfully fabricated FDRC networks were used in several electronic circuits such as the monostable multivibrators, the phase shift oscillators and band pass and notch filters.

The implementation of FDRC networks included printing and firing of dielectric ink over a fired resistor which had not been attempted before. Fabrication of these networks also involved

printing resistor ink over a fired dielectric which had already been discussed in fabrication of DRC networks by previous workers. The problems of resistor- ink compatibility associated with the fabrication of thick film FDRC networks were identified and subsequently successfully resolved. Conditions for compatibility were considered to be as follows:

1. The inks should have the same temperature coefficient of expansion in order to avoid cracks of the FDRC structure during the last firing cycles.

2. After successive firings the upper layers should not diffuse or penetrate into the lower layers, ie there should be no interaction between the successive layers.

3. The first resistor must keep its parameters unchanged when the successive layers are fired over it several times.

To resolve the problem of interaction caused by refiring, a successive decrease in firing temperatures for the successive layers was considered (section 4.12). Although this practise was not found to be a definite solution to the problem, it was maintained throughout the investigations.

The resistors, both with and without dielectric layers on top, as a whole showed changes in resistance when refired several times. However, the changes were sometimes more pronounced for a particular resistor - dielectric ink combination. In fact, refiring has also some effect on other resistor parameters such as temperature coefficient, voltage coefficient etc which are inevitable with most of the present materials available for thick film work.

Despite the inevitable effects of refiring on the resistor parameters, a number of FDRC networks were successfully fabricated. This indicates that the problem of interaction between the resistor and dielectric layers may be successfully eliminated by choosing the right resistor - dielectric ink combination.

Trimming the resistors of the FDRC device is an important part of the process. The usual and ordinary means of trimming are not suitable and applicable to the thick film FDRC networks. The common methods of trimming would require accessibility to the surface of the resistor and many of them involve some physical removal of the resistor body.

Trimming of the resistors in the FDRC device must be performed when the device fabrication is completed because there would be further changes in the first resistor due to refiring. The high voltage pulse trimming technique seemed to be the only method known which satisfied the trimming requirements.

After extensive investigations, a high voltage pulse trimmer, ie a system capable of producing high voltage pulses of 2000 volts amplitude with variable widths of 12 μ sec to nearly 100m sec, was constructed. Two resistors, both with and without dielectric layer on top in two different sizes were examined for trimming. It was found that the larger resistors were less sensitive to high voltage pulses than the smaller ones. This means that the power applied per square of the resistor area is what one should consider rather than the power applied across the terminals of the resistor. Also, resistors with dielectric layers on top are found to be more susceptible to high voltage pulses than the resistors without the dielectric layer. This indicates that the process of printing and firing dielectric and the other successive layers over the bottom

firing dielectric and the other successive layers over the bottom resistor of the FDRC network has a definite effect on the voltage resistance of the resistor.

Of the two resistors ESL 3113 (A) and Dupont 1331 (D) which were used for trimming, resistor D was less sensitive to the high voltage pulses. This could have been predicted from the manufacturing specifications on voltage resistance for both resistors. The interesting point is that resistor D has also been more compatible with the dielectric inks than resistor A has been. Therefore, it may be concluded that the special treatment in the design and manufacturing of high voltage resistor inks [47] is also what is required for a resistor to be compatible with dielectric materials.

In general, the high voltage pulses have a definite effect on the resistors. However, in order to use this method for trimming the resistors of thick film FDRC structures, the manner in which the resistor values change under high voltage pulses must be studied more extensively. Hence, the resistors, both with and without dielectric layers on top, must be categorized for their susceptibility to high voltage pulses in terms of the constituents of the resistors.

Turning to the theory of FDRC networks, the computer analysis of the notch filter showed a marked sensitivity of the notch depth with the deviation of N (the ratio of the resistors) from the value of $N = 0.086266$ which is the value required for a true notch. However, obtaining the exact value for N has so far proved to be impractical and, therefore, the notch depth is usually not very deep (ie not less than -50dB).

Some of the FDRC devices fabricated were used in some electronic circuits. The work on monostables, phase shift oscillators and filters showed that these FDRC devices perform as the analysis of the circuits has suggested.

7.2 SUGGESTIONS FOR FURTHER RESEARCH

Several authors have reported sharper roll - off characteristics obtained in low pass filters by using exponentially tapered RC distributed networks. Perhaps for some specific applications a smaller total capacitance is required by using one of the tapered networks. One suggestion is to fabricate tapered thick film FDRC networks.

Another problem is the determination of the exact nature of the FDRC network. In other words, the design may specify a uniformly distributed network, but the fabrication process may yield a network with some slight deviation. Does this deviation radically change the performance of the distributed network? Considerable work needs to be done in the area of sensitivity to parameters variations.

The assumption in this research was that the networks exhibit no inductive effects along the resistor layers and that the dielectric has no loss. However, due to the geometry of the resistor layers, at high frequencies the inductance becomes appreciable, perhaps even to the extend of resonating with the capacitance layer. Effects of this sort need to be investigated further.

The high voltage pulse trimming method has been explored after constructing a high voltage pulse trimmer device. A number of resistors were tested for trimming and the effect of various parameters of high voltage pulses on the amount resistance change were investigated. However a great deal of experimental work remains to be carried out before it becomes possible to establish general formulae for high voltage pulse trimming.

Application of thick film FDRC devices in different types of filters, oscillators and amplifier circuits should be more extensively studied. There is also a need for thick film materials especially designed for the fabrication of FDRC networks.

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APPENDIX 1

THE MAGNITUDE AND ANGLE DERIVATION

FROM PAGE 20:

$$\frac{Z}{R} = \frac{\tanh \sqrt{j\omega RC}}{\sqrt{j\omega RC}} \qquad 1$$

Let $$\omega RC = \eta \qquad 2$$

and $$\tanh \sqrt{j\omega RC} = X \qquad 3$$

Therefore $$X = \frac{\sinh \sqrt{j\eta}}{\cosh \sqrt{j\eta}} \qquad 4$$

but $$\sqrt{j\eta} = \pm \left(\sqrt{\frac{\eta}{2}} + j \sqrt{\frac{\eta}{2}} \right)$$

Let $$\sqrt{\frac{\eta}{2}} = \alpha \qquad 5$$

substituting for η in equation 4

$$X = \pm \frac{\sinh (\alpha + j\alpha)}{\cosh (\alpha + j\alpha)} \qquad 6$$

We know that: $\sinh (A+B) = \cosh A \sinh B + \cosh B \sinh A$

$\cosh (A+B) = \cosh A \cosh B + \sinh A \sinh B$

$\sinh jC = j \sin C$ and $\cosh jC = \cos C$

Using the above identities, equation 6 can be written as:

$$X = \pm \frac{j \cosh\alpha \sin\alpha + \cos\alpha \sinh\alpha}{\cosh\alpha \cos\alpha + j \sinh\alpha \sin\alpha} \qquad 7$$

THE MAGNITUDE DERIVATION

$$|X| = \frac{|N|}{|D|} = \sqrt{\frac{\cosh^2\alpha \sin^2\alpha + \sinh^2\alpha \cos^2\alpha}{\cosh^2\alpha \cos^2\alpha + \sinh^2\alpha \sin^2\alpha}} \qquad 8$$

Using the following double angle identities:

$$\cosh^2\alpha = \frac{\cosh 2\alpha + 1}{2}$$

$$\sinh^2\alpha = \frac{\cosh 2\alpha - 1}{2}$$

$$\sin^2\alpha = \frac{1 - \cos 2\alpha}{2}$$

$$\cos^2\alpha = \frac{\cos 2\alpha - 1}{2}$$

equation 8 can be written as:

$$|X| = \sqrt{\frac{(\cosh 2\alpha - 1)(\cos 2\alpha + 1) + (\cosh 2\alpha + 1)(1 - \cos 2\alpha)}{(\cosh 2\alpha + 1)(\cos 2\alpha + 1) + (\cosh 2\alpha - 1)(1 - \cos 2\alpha)}} \qquad 9$$

Substituting for α from equation 5, and simplifying equation 9.

$$|X| = \left[\frac{\cosh\sqrt{2\eta} - \cos\sqrt{2\eta}}{\cosh\sqrt{2\eta} + \cos\sqrt{2\eta}}\right]^{\frac{1}{2}} \qquad 10$$

rewriting equation 1 as:

$$\frac{Z}{R} = \frac{X}{\sqrt{j\omega RC}} \qquad 11$$

Therefore

$$\left|\frac{Z}{R}\right| = \frac{|X|}{\left|\sqrt{j\omega RC}\right|} \qquad 12$$

but

$$\left|\sqrt{j\omega RC}\right| = \sqrt{\omega RC}$$

Substituting for $|X|$ from equation 10 in equation 12, we get:

$$\left|\frac{Z}{R}\right| = \frac{1}{\sqrt{\omega RC}}\left[\frac{\cosh\sqrt{2\eta} - \cos\sqrt{2\eta}}{\cosh\sqrt{2\eta} + \cos\sqrt{2\eta}}\right]^{\frac{1}{2}}$$

THE ANGLE DERIVATION

Multiplying both the numerator and the denumerator of equation 7 by the complex conjugate of the denomirator, we get:

$$X = \pm \frac{\cosh\alpha \sinh\alpha \cos^2\alpha + \cosh\alpha \sinh\alpha \sin^2\alpha + j(\cosh^2\alpha \sin\alpha\cos\alpha - \sinh^2\alpha \sin\alpha\cos}{\alpha}$$

substituting for X in equation 11 and rearranging it:

$$\frac{Z}{R} = \frac{X}{\sqrt{j\omega RC}} = \frac{(1-j)(\cosh\alpha \sinh\alpha + j\sin\alpha\cos\alpha)}{D}$$

$$= \frac{\sinh 2\alpha + \sin 2\alpha + j(\sin 2\alpha - \sinh 2\alpha)}{D}$$

Now the angle of complex number $\left(\frac{Z}{R}\right)$ is:

$$\angle\frac{Z}{R} = \text{ARC}\tan\left[\frac{\sin 2\alpha - \sinh 2\alpha}{\sin 2\alpha + \sinh 2\alpha}\right]$$

APPENDIX 2

```
C         THIS PROGRAMM IS FOR A PLOT OF ATTEN./FREQ. FOR A BAND-PASS FILTER
       DIMENSION X(16),Y(16),ITX1(10),ITX2(8),ITX3(11),
      1   ITX4(14),ITX5(5),ITX6(9),ITX7(5),ITX8(7),ITX9(5)
$INSERT SYSCOM⅛KEYS.F
       DATA ITX1/'NORMALISED FREQUENCY'/,
      1    ITX2/'ATTENUATION (dB)'/,
      2    ITX3/'THE ACTIVE FDRC FILTER'/,
      3    ITX4/'MEASURED FREQUENCY RESPONSE '/,
      4    ITX5/'FIG.(6.13)'/,ITX6/'FDRC device: N334a'/,
      5    ITX7/'R = 8.5K  '/,ITX8/'C = 224 pF    '/,
      6    ITX9/'N = 0.0765'/
       CALL SRCH$$(K$READ,'DATA',4,1,IT,ICODE)
       IF          (ICODE.NE.0) GO TO 500
       READ(5,20) (X(I),Y(I),I=1,14)
20     FORMAT      (F7.4,I3)
       CALL SRCH$$(K$CLOS,'DATA',4,1,IT,ICODE)
       CALL PLOTS (0,0,4)
       CALL FACTOR(1.0)
       CALL SCALG (X,14.0,14,1)
       CALL SCALES(Y,16.0,14,1)
       CALL LGAXS (0.0,0.0,ITX1,-20,14.0,0.0,X(15),X(16))
       CALL AXIS  (0.0,0.0,ITX2,16,16.0,90.0,Y(15),Y(16))
       CALL LGLIN (X,Y,14,1,1,4,-1)
       CALL SYMBOL(5.0,19.0,0.4,ITX5,0.0,10)
       CALL SYMBOL(3.0,18.0,0.32,ITX3,0.0,22)
       CALL SYMBOL(2.5,17.3,0.32,ITX4,0.0,28)
       CALL SYMBOL(8.0,14.0,0.4,ITX6,0.0,18)
       CALL SYMBOL(10.5,13.0,0.4,ITX7,0.0,10)
       CALL SYMBOL(10.5,12.0,0.4,ITX9,0.0,10)
       CALL SYMBOL(10.5,11.0,0.4,ITX8,0.0,14)
       CALL PLOT  (24.0,0.0,999)
       STOP
500    WRITE       (1,1)
1      FORMAT      ( ' ERROR IN OPENING THE FILE')
       CALL EXIT
       END
```

APPENDIX 3

Programme 1

```
C       PROGRAMM FOR PLOTS OF ATTEN./FREQ. FOR A NUMBER OF
C       FDRC NOTCH FILTERS
        DIMENSION OMEG(3000),OMG1(302),ATENDB(3002),ITEXT1(10),ITEXT2(8)
     1 ,ITEXT3(15),ITEXT4(9),ITX1(5),ITX2(5),ITX3(5),ITX11(6)
     2 ,ITX4(5),ITX5(5),ITX6(5),ITX7(5),ITX8(5),ITX9(5),ITX10(5)
        COMPLEX CN,CD,CEO,CJ
        DATA ITEXT1/'NORMALISED FREQUENCY'/,ITEXT2/'ATTENUATION (dB)'/,
     1    ITEXT3/'The FDRC Filter Characteristic'/,ITX11/'FIG.(6.15)a '/
     2    ,ITEXT4/'COMPUTER ANALYSIS '/,ITX10/'N = 0.006 '/,ITX9/
     3    'N = 0.026 '/,ITX8/'N = 0.046 '/,ITX7/'N = 0.066 '/,ITX6/
     4    'N = 0.086 '/,ITX5/'N = 0.106 '/,ITX4/'N = 0.126 '/,
     5    ITX3/'N = 0.146 '/,ITX2/'N = 0.168 '/,ITX1/'N = 0.188 '/
        CALL PLOTS (0,0,4)
        CALL FACTOR (1.0)
        CJ=(0.0,1.0)
        PI=3.1415926
        AN=0.006
        I=0
200     CONTINUE
        J=0
        E=-1.0
300     E=E+2.0/300.0
        J=J+1
        OMEGA=10.0**E
        OMG=10.0*OMEGA
        OMG1(J)=OMG
        GAMMA=PI*SQRT((1.0+AN)*(OMEGA)*((EXP(PI)+EXP(-PI))/2.0)
     1/(1.0+((EXP(PI)+EXP(-PI))/2.0)))
        I=I+1
        X=((EXP(GAMMA)+EXP(-GAMMA))/2.0)*COS(GAMMA)
        Y=((EXP(GAMMA)-EXP(-GAMMA))/2.0)*SIN(GAMMA)
        CN=CMPLX(1.,0.)+CMPLX(AN,0.)*CMPLX(X,Y)
        CD=CMPLX(1.+AN,0.)*CMPLX(X,Y)
        CEO=CN/CD
        ABSCEO=CABS(CEO)
        ATENDB(I)=20.0*ALOG10(ABSCEO)
        IF(E.LT.0.994)GO TO 300
        AN=AN+0.02
        IF (I.LT.3000) GO TO 200
        CALL SCALG (OMG1,14.0,300,1)
        CALL SCALES (ATENDB,18.0,I,1)
        CALL LGAXS (0.0,0.0,ITEXT1,-20,14.0,0.0,OMG1(301),OMG1(302))
        CALL AXIS(0.0,0.0,ITEXT2,16,18.0,90.0,ATENDB(I+1),ATENDB(I+2))
```

```
C       put aside the scale factors which we will use several times
        SCY1=ATENDB(I+1)
        SCY2=ATENDB(I+2)
        DO 40 M=1,10
        I=(M-1)*300+1

C       save the two locations which will hold the scaling info
        SY51=ATENDB(I+300)
        SY52=ATENDB(I+301)

C       now put in the scale factors in the appropriate places
        ATENDB(I+300)=SCY1
        ATENDB(I+301)=SCY2

C       now do the line
        CALL LGLIN (OMG1,ATENDB(I),300,1,0,0,-1)

C       now put back the values to be plotted
        ATENDB(I+300)=SY51
        ATENDB(I+301)=SY52
40      CONTINUE
        CALL SYMBOL(1.8,20.3,0.4,ITEXT3,0.0,32)
        CALL SYMBOL(4.6,21.5,0.4,ITEXT4,0.0,17)
        CALL SYMBOL(2.2,12.2,0.25,ITX1,0.0,10)
        CALL SYMBOL(2.2,11.6,0.25,ITX2,0.0,10)
        CALL SYMBOL(2.2,11.0,0.25,ITX3,0.0,10)
        CALL SYMBOL(2.2,10.1,0.25,ITX4,0.0,10)
        CALL SYMBOL(2.2,9.1,0.25,ITX5,0.0,10)
        CALL SYMBOL(2.2,8.0,0.25,ITX6,0.0,10)
        CALL SYMBOL(7.8,8.4,0.22,ITX7,0.0,10)
        CALL SYMBOL(7.8,9.1,0.22,ITX8,0.0,10)
        CALL SYMBOL(11.8,8.5,0.25,ITX10,0.0,10)
        CALL SYMBOL(11.8,10.6,0.25,ITX9,0.0,10)
        CALL SYMBOL(4.5,22.8,0.4,ITX11,0.0,12)
        CALL PLOT  (12.0,0.0,999)
        STOP
        END
```

Programme 2

```
C       PROGRAMM FOR PLOTS OF ATTEN./FREQ. FOR A NUMBER OF
C       FDRC NOTCH FILTERS
        DIMENSION OMEG(3000),OMG1(302),ATENDB(3002),ITEXT1(10),ITEXT2(8)
      1 ,ITEXT3(15),ITEXT4(9),ITX1(5),ITX2(5),ITX3(5),ITX11(6)
      2 ,ITX4(5),ITX5(5),ITX6(5),ITX7(5),ITX8(5),ITX9(5),ITX10(5)
        COMPLEX CN,CD,CEO,CJ
        DATA ITEXT1/'NORMALISED FREQUENCY'/,ITEXT2/'ATTENUATION (dB)'/,
      1    ITEXT3/'The FDRC Filter Characteristic'/,ITX11/'FIG.(6.15)b'/,
      2    ITEXT4/'COMPUTER ANALYSIS '/,ITX10/'N = 0.03  '/,ITX9/
      3    'N = 0.08  '/,ITX8/'N = 0.13  '/,ITX7/'N = 0.18  '/,ITX6/
      4    'N = 0.23  '/,ITX5/'N = 0.28  '/,ITX4/'N = 0.33  '/,
      5     ITX3/'N = 0.38  '/,ITX2/'N = 0.43  '/,ITX1/'N = 0.48  '/
        CALL PLOTS (0,0,4)
        CALL FACTOR (1.0)
        CJ=(0.0,1.0)
        PI=3.1415926
        AN=0.03
        I=0
200     CONTINUE
        J=0
        E=-1.0
300     E=E+2.0/300.0
        J=J+1
        OMEGA=10.0**E
        OMG=10.0*OMEGA
        OMG1(J)=OMG
        GAMMA=PI*SQRT((1.0+AN)*(OMEGA)*((EXP(PI)+EXP(-PI))/2.0)
      1/(1.0+((EXP(PI)+EXP(-PI))/2.0)))
        I=I+1
        X=((EXP(GAMMA)+EXP(-GAMMA))/2.0)*COS(GAMMA)
        Y=((EXP(GAMMA)-EXP(-GAMMA))/2.0)*SIN(GAMMA)
        CN=CMPLX(1.,0.)+CMPLX(AN,0.)*CMPLX(X,Y)
        CD=CMPLX(1.+AN,0.)*CMPLX(X,Y)
        CEO=CN/CD
        ABSCEO=CABS(CEO)
        ATENDB(I)=20.0*ALOG10(ABSCEO)
        IF(E.LT.0.994)GO TO 300
        AN=AN+0.05
        IF (I.LT.3000) GO TO 200
        CALL SCALG (OMG1,14.0,300,1)
        CALL SCALES (ATENDB,23.0,I,1)
        CALL LGAXS (0.0,0.0,ITEXT1,-20,14.0,0.0,OMG1(301),OMG1(302))
        CALL AXIS(0.0,0.0,ITEXT2,16,23.0,90.0,ATENDB(I+1),ATENDB(I+2))
```

```
C       put aside the scale factors which we will use several times
        SCY1=ATENDB(I+1)
        SCY2=ATENDB(I+2)
        DO 40 M=1,10
        I=(M-1)*300+1

C       save the two locations which will hold the scaling info
        SY51=ATENDB(I+300)
        SY52=ATENDB(I+301)

C       now put in the scale factors in the appropriate places
        ATENDB(I+300)=SCY1
        ATENDB(I+301)=SCY2

C       now do the line
        CALL LGLIN (OMG1,ATENDB(I),300,1,0,0,-1)

C       now put back the values to be plotted
        ATENDB(I+300)=SY51
        ATENDB(I+301)=SY52
40      CONTINUE
        CALL SYMBOL(1.8,22.0,0.4,ITEXT3,0.0,30)
        CALL SYMBOL(4.6,23.0,0.4,ITEXT4,0.0,17)
        CALL SYMBOL(1.2,17.0,0.25,ITX1,0.0,10)
        CALL SYMBOL(1.2,16.4,0.25,ITX2,0.0,10)
        CALL SYMBOL(1.2,15.8,0.25,ITX3,0.0,10)
        CALL SYMBOL(1.2,15.1,0.25,ITX4,0.0,10)
        CALL SYMBOL(1.2,14.3,0.25,ITX5,0.0,10)
        CALL SYMBOL(1.2,13.4,0.25,ITX6,0.0,10)
        CALL SYMBOL(1.2,12.2,0.22,ITX7,0.0,10)
        CALL SYMBOL(1.2,10.8,0.22,ITX8,0.0,10)
        CALL SYMBOL(1.2,9.5,0.25,ITX9,0.0,10)
        CALL SYMBOL(10.5,7.5,0.25,ITX10,0.0,10)
        CALL SYMBOL(6.0,24.3,0.4,ITX11,0.0,12)
        CALL PLOT(12.0,0.0,999)
        STOP
        END
```

Programme 3

```
C      THIS PROGRAMM IS FOR A PLOT OF ATTEN./FREQ. FOR N=0.08627.
       DIMENSION OMEG(300),OMG1(302),ATENDB(302),ITEXT1(10),ITEXT2(8)
     1 ,ITEXT3(23),ITEXT4(9),ITX9(6)
       COMPLEX CN,CD,CEO,CJ
       DATA ITEXT1/'NORMALISED FREQUENCY'/,ITEXT2/'ATTENUATION (dB)'/,
     1    ITEXT3/'The FDRC Filter Characteristic For N = 0.08627'/,
     2    ITEXT4/'COMPUTER ANALYSIS '/,ITX9/'FIG.(6.16) '/
       CALL PLOTS (0,0,4)
       CALL FACTOR (1.0)
       CJ=(0.0,1.0)
       PI=3.1415926
       AN=0.086266
       J=0
       E=-1.0
300    E=E+2.0/300.0
       J=J+1
       OMEGA=10.0**E
       OMG=10.0*OMEGA
       OMG1(J)=OMG
       GAMMA=PI*SQRT((1.0+AN)*(OMEGA)*((EXP(PI)+EXP(-PI))/2.0)
     1/(1.0+((EXP(PI)+EXP(-PI))/2.0)))
       X=((EXP(GAMMA)+EXP(-GAMMA))/2.0)*COS(GAMMA)
       Y=((EXP(GAMMA)-EXP(-GAMMA))/2.0)*SIN(GAMMA)
       CN=CMPLX(1.,0.)+CMPLX(AN,0.)*CMPLX(X,Y)
       CD=CMPLX(1.+AN,0.)*CMPLX(X,Y)
       CEO=CN/CD
       ABSCEO=CABS(CEO)
       ATENDB(J)=20.0*ALOG10(ABSCEO)
       IF(E.LT.0.994)GO TO 300
       CALL SCALG (OMG1,14.0,300,1)
       CALL SCALES (ATENDB,24.0,300,1)
       CALL LGAXS (0.0,0.0,ITEXT1,-20,14.0,0.0,OMG1(301),OMG1(302))
       CALL AXIS(0.0,0.0,ITEXT2,16,24.0,90.0,ATENDB(301),ATENDB(302))
       CALL LGLIN (OMG1,ATENDB,300,1,0,0,-1)
       CALL SYMBOL(0.6,24.6,0.3,ITEXT3,0.0,46)
       CALL SYMBOL(4.6,23.0,0.4,ITEXT4,0.0,18)
       CALL SYMBOL (9.5,10.0,0.4,ITX9,0.0,12)
       CALL PLOT(24.0,0.0,999)
       STOP
       END
```

APPENDIX 4

Programme 1

```
C       PROGRAMM FOR PLOTTING THE MEASURED AND THE ANALYSED
C       FREQUENCY RESPONSES
C       FOR DEVICE D444b
        DIMENSION OMG1(302),ATENDB(302),ITEXT1(10),ITEXT2(8)
     1 ,ITEXT3(15),ITEXT4(18),ITX1(6),ITX2(4),ITX9(6)
     2 ,ITEXT5(13),XM(17),YM(17),ITX3(6),ITX4(7),ITX5(7),ITX6(7)
        COMPLEX CN,CD,CEO,CJ
$INSERT SYSCOM$KEYS.F
        DATA ITEXT1/'NORMALISED FREQUENCY'/,ITEXT2/'ATTENUATION (dB)'/,
     1    ITEXT3/'The FDRC Filter Characteristic'/,
     2    ITEXT4/'Comparison of the Computer Analysis '/,
     3    ITEXT5/'with the Measured Response'/,
     4    ITX1/'measurement'/,ITX2/'analysis'/,ITX3/'Device:D444b'/,
     5    ITX4/'    R = 11.5K '/,ITX5/'    N = 0.094 '/,ITX9/
     6    'FIG.(6.17)a '/,ITX6/'    C = 131PF '/
        CALL SRCH$$(K$READ,'DATA',4,1,IT,ICODE)
        IF(ICODE.NE.0) GO TO 500
        READ(5,20)(XM(I),YM(I),I=1,15)
20      FORMAT(F7.2,F7.1)
        CALL SRCH$$(K$CLOS,'DATA',4,1,IT,ICODE)
        CALL PLOTS (0,0,4)
        CALL FACTOR (1.0)
        CJ=(0.0,1.0)
        PI=3.1415926
        AN=0.094
        J=0
        E=-1.0
300     E=E+2.0/300.0
        J=J+1
        OMEGA=10.0**E
        OMG=10.0*OMEGA
        OMG1(J)=OMG
        GAMMA=PI*SQRT((1.0+AN)*(OMEGA)*((EXP(PI)+EXP(-PI))/2.0)
     1/(1.0+((EXP(PI)+EXP(-PI))/2.0)))
        X=((EXP(GAMMA)+EXP(-GAMMA))/2.0)*COS(GAMMA)
        Y=((EXP(GAMMA)-EXP(-GAMMA))/2.0)*COS(GAMMA)
        CN=CMPLX(1.,0.)+CMPLX(AN,0.)*CMPLX(X,Y)
        CD=CMPLX(1.+AN,0.)*CMPLX(X,Y)
        CEO=CN/CD
        ABSCEO=CABS(CEO)
        ATENDB(J)=20.0*ALOG10(ABSCEO)
        IF(E.LT.0.994)GO TO 300
        CALL SCALG (OMG1,14.0,300,1)
        CALL SCALES (ATENDB,22.0,300,1)
        CALL LGAXS (0.0,0.0,ITEXT1,-20,14.0,0.0,OMG1(301),OMG1(302))
        CALL AXIS(0.0,0.0,ITEXT2,16,22.0,90.0,ATENDB(301),ATENDB(302))
        CALL LGLIN (OMG1,ATENDB,300,1,0,0,-1)
```

```
      CALL SYMBOL(2.0,22.0,0.4,ITEXT3,0.0,30)
      CALL SYMBOL(2.0,20.7,0.35,ITEXT4,0.0,36)
      CALL SYMBOL(3.0,20.0,0.35,ITEXT5,0.0,26)
      CALL SYMBOL (1.3,12.0,0.35,ITX1,0.0,12)
      CALL SYMBOL (1.6,10.0,0.35,ITX2,0.0,8)
      CALL SYMBOL (10.0,18.0,0.4,ITX3,0.0,12)
      CALL SYMBOL (9.0,17.0,0.4,ITX4,0.0,14)
      CALL SYMBOL (9.0,16.0,0.4,ITX5,0.0,14)
      CALL SYMBOL (9.0,15.0,0.4,ITX6,0.0,14)
      CALL SYMBOL (5.0,23.5,0.4,ITX9,0.0,12)
      XM(16)=OMG1(301)
      XM(17)=OMG1(302)
      YM(16)=ATENDB(301)
      YM(17)=ATENDB(302)
      CALL LGLIN(XM,YM,15,1,1,4,-1)
      CALL PLOT(12.0,0.0,999)
      STOP
500   WRITE(1,1)
1     FORMAT( ' ERROR IN OPENING THE FILE')
      CALL EXIT
      END
```

Programme 2

```
C       PROGRAMM FOR PLOTTING THE MEASURED AND THE ANALYSED
C       FREQUENCY RESPONSES
        DIMENSION OMG1(302),ATENDB(302),ITEXT1(10),ITEXT2(8)
     1 ,ITEXT3(15),ITEXT4(18),ITX1(6),ITX2(4),ITX9(6)
     2 ,ITEXT5(13),XM(15),YM(15),ITX3(6),ITX4(7),ITX5(7),ITX6(7)
        COMPLEX CN,CD,CEO,CJ
$INSERT SYSCOM3/8KEYS.F
        DATA ITEXT1/'NORMALISED FREQUENCY'/,ITEXT2/'ATTENUATION (dB)'/,
     1    ITEXT3/'The FDRC Filter Characteristic'/,
     2    ITEXT4/'Comparison of the Computer Analysis '/,
     3    ITEXT5/'with the Measured Response'/,
     4    ITX1/'measurement'/,ITX2/'analysis'/,ITX3/'Device:N334a'/,
     5    ITX4/'    R = 8.5K  '/,ITX5/'    N = 0.0765'/,
     6    ITX6/'    C = 224PF '/,ITX9/'FIG.(6.17)b '/
        CALL SRCH$$(K$READ,'DATA',4,1,IT,ICODE)
        IF(ICODE.NE.0) GO TO 500
        READ(5,20)(XM(I),YM(I),I=1,13)
 20     FORMAT(F7.2,I5)
        CALL SRCH$$(K$CLOS,'DATA',4,1,IT,ICODE)
        CALL PLOTS (0,0,4)
        CALL FACTOR (1.0)
        CJ=(0.0,1.0)
        PI=3.1415926
        AN=0.07647
        J=0
        E=-1.0
300     E=E+2.0/300.0
        J=J+1
        OMEGA=10.0**E
        OMG=10.0*OMEGA
        OMG1(J)=OMG
        GAMMA=PI*SQRT((1.0+AN)*(OMEGA)*((EXP(PI)+EXP(-PI))/2.0)
     1/(1.0+((EXP(PI)+EXP(-PI))/2.0)))
        X=((EXP(GAMMA)+EXP(-GAMMA))/2.0)*COS(GAMMA)
        Y=((EXP(GAMMA)-EXP(-GAMMA))/2.0)*SIN(GAMMA)
        CN=CMPLX(1.,0.)+CMPLX(AN,0.)*CMPLX(X,Y)
        CD=CMPLX(1.+AN,0.)*CMPLX(X,Y)
        CEO=CN/CD
        ABSCEO=CABS(CEO)
        ATENDB(J)=20.0*ALOG10(ABSCEO)
        IF(E.LT.0.994)GO TO 300
        CALL SCALG (OMG1,14.0,300,1)
        CALL SCALES (ATENDB,22.0,300,1)
        CALL LGAXS (0.0,0.0,ITEXT1,-20,14.0,0.0,OMG1(301),OMG1(302))
        CALL AXIS(0.0,0.0,ITEXT2,16,22.0,90.0,ATENDB(301),ATENDB(302))
        CALL LGLIN (OMG1,ATENDB,300,1,0,0,-1)
```

```
      CALL SYMBOL(2.0,22.0,0.4,ITEXT3,0.0,30)
      CALL SYMBOL(2.0,21.0,0.35,ITEXT4,0.0,36)
      CALL SYMBOL(3.0,20.3,0.35,ITEXT5,0.0,26)
      CALL SYMBOL (1.3,12.0,0.35,ITX1,0.0,12)
      CALL SYMBOL (1.6,10.0,0.35,ITX2,0.0,8)
      CALL SYMBOL (10.0,18.0,0.4,ITX3,0.0,12)
      CALL SYMBOL (9.0,17.0,0.4,ITX4,0.0,14)
      CALL SYMBOL (9.0,16.0,0.4,ITX5,0.0,14)
      CALL SYMBOL (9.0,15.0,0.4,ITX6,0.0,14)
      CALL SYMBOL (5.0,23.5,0.4,ITX9,0.0,12)
      XM(14)=OMG1(301)
      XM(15)=OMG1(302)
      YM(14)=ATENDB(301)
      YM(15)=ATENDB(302)
      CALL LGLIN(XM,YM,13,1,1,4,-1)
      CALL PLOT(12.0,0.0,999)
      STOP
500   WRITE(1,1)
1     FORMAT( ' ERROR IN OPENING THE FILE')
      CALL EXIT
      END
```

Programme 3

```
C       PROGRAMM FOR PLOTTING THE MEASURED AND THE ANALYSED
C       FREQUENCY RESPONSES
        DIMENSION OMG1(302),ATENDB(302),ITEXT1(10),ITEXT2(8)
     1 ,ITEXT3(15),ITEXT4(18),ITX1(6),ITX2(4),ITX9(6)
     2 ,ITEXT5(13),XM(15),YM(15),ITX3(6),ITX4(7),ITX5(7),ITX6(7)
        COMPLEX CN,CD,CEO,CJ
$INSERT SYSCOM¾KEYS.F
        DATA ITEXT1/'NORMALISED FREQUENCY'/,ITEXT2/'ATTENUATION (dB)'/,
     1    ITEXT3/'The FDRC Filter Characteristic'/,
     2    ITEXT4/'Comparison of the Computer Analysis '/,
     3    ITEXT5/'with the Measured Response'/,
     4    ITX1/'measurement'/,ITX2/'analysis'/,ITX3/'Device:N344a'/,
     5    ITX4/'    R = 9.6K  '/,ITX5/'    N = 0.05  '/,
     6    ITX6/'    C = 310PF '/,ITX9/'FIG.(6.17)c '/
        CALL SRCH$$(K$READ,'DATA',4,1,IT,ICODE)
        IF(ICODE.NE.0) GO TO 500
        READ(5,20)(XM(I),YM(I),I=1,13)
20      FORMAT(F6.1,F7.1)
        CALL SRCH$$(K$CLOS,'DATA',4,1,IT,ICODE)
        CALL PLOTS (0,0,4)
        CALL FACTOR (1.0)
        CJ=(0.0,1.0)
        PI=3.1415926
        AN=0.05
        J=0
        E=-1.0
300     E=E+2.0/300.0
        J=J+1
        OMEGA=10.0**E
        OMG=10.0*OMEGA
        OMG1(J)=OMG
        GAMMA=PI*SQRT((1.0+AN)*(OMEGA)*((EXP(PI)+EXP(-PI))/2.0)
     1/(1.0+((EXP(PI)+EXP(-PI))/2.0)))
        X=((EXP(GAMMA)+EXP(-GAMMA))/2.0)*COS(GAMMA)
        Y=((EXP(GAMMA)+EXP(-GAMMA))/2.0)*COS(GAMMA)
        CN=CMPLX(1.,0.)+CMPLX(AN,0.)*CMPLX(X,Y)
        CD=CMPLX(1.+AN,0.)*CMPLX(X,Y)
        CEO=CN/CD
        ABSCEO=CABS(CEO)
        ATENDB(J)=20.0*ALOG10(ABSCEO)
        IF(E.LT.0.994)GO TO 300
1001    FORMAT(I6,F10.5,F12.6)
C       WRITE(1,1001)((K,OMG1(K),ATENDB(K)),K=1,300)
C       WRITE(1,30)(XM(I),YM(I),I=1,15)
30      FORMAT(F5.1,10X,F5.1)
        CALL SCALG (OMG1,14.0,300,1)
        CALL SCALES (ATENDB,17.0,300,1)
        CALL LGAXS (0.0,0.0,ITEXT1,-20,14.0,0.0,OMG1(301),OMG1(302))
        CALL AXIS(0.0,0.0,ITEXT2,16,17.0,90.0,ATENDB(301),ATENDB(302))
        CALL LGLIN (OMG1,ATENDB,300,1,0,0,-1)
```

```
      CALL SYMBOL(2.0,19.0,0.4,ITEXT3,0.0,30)
      CALL SYMBOL(2.0,17.5,0.35,ITEXT4,0.0,36)
      CALL SYMBOL(3.0,16.7,0.35,ITEXT5,0.0,26)
      CALL SYMBOL (1.3,5.0,0.35,ITX1,0.0,12)
      CALL SYMBOL (1.6,3.0,0.35,ITX2,0.0,8)
      CALL SYMBOL (10.0,14.0,0.4,ITX3,0.0,12)
      CALL SYMBOL (9.0,13.0,0.4,ITX4,0.0,14)
      CALL SYMBOL (9.0,12.0,0.4,ITX5,0.0,14)
      CALL SYMBOL (9.0,11.0,0.4,ITX6,0.0,14)
      CALL SYMBOL (4.5,20.5,0.4,ITX9,0.0,12)
      XM(14)=OMG1(301)
      XM(15)=OMG1(302)
      YM(14)=ATENDB(301)
      YM(15)=ATENDB(302)
      CALL LGLIN(XM,YM,13,1,1,4,-1)
      CALL PLOT(12.0,0.0,999)
      STOP
500   WRITE(1,1)
1     FORMAT( ' ERROR IN OPENING THE FILE')
      CALL EXIT
      END
```

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