# Model Predictive Current Control for a Low-Cost Shunt Active Power Filter

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***Abstract*—Performance of a three-phase shunt active power filter (SAPF) relies on the capability of the controller to track the reference current. Therefore, designing an accurate current controller is crucial to guarantee satisfactory SAPF operation. This paper presents a model predictive current controller (MPCC) for a low-cost, four switch, shunt active power filter for power quality improvement. A four switch, B4, converter topology is adopted as an SAPF, hence offering a simple, robust, and low-cost solution. In addition, to further reduce the overall cost, only two interfacing filter inductors, instead of three, are used to eliminate switching current ripple. The proposed SAPF model MPCC is detailed for the implementation, where simulation and experimental results validate the effectiveness of the proposed control algorithm showing a 20% improvement in total harmonic distortion compared with a conventional hysteresis band current controller.**

***Index Terms*—Four-switch converter, harmonic distortion, model predictive current control, power quality, shunt active power filter.**

LIST OF ABBREVIATIONS

| | |
|---|---|
| FCS | Finite Control Set |
| HBCC | Hysteresis Band Current Control |
| MPCC | Model Predictive Current Control |
| PCC | Point of Common Coupling |
| PLL | Phase Locked Loop |
| PI | Proportional-Integral |
| PWM | Pulse Width Modulation |
| SAPF | Shunt Active Power Filter |
| SVM | Space Vector Modulation |
| THD | Total Harmonic Distortion |

## I. INTRODUCTION

THE growth in the utilization of nonlinear loads, which draw non-sinusoidal currents, has increased in recent decades. These nonlinear loads are the main source of harmonics which affect system power quality [1] - [3]. Traditionally, passive filters were used to solve power quality problem [4]. Unfortunately, passive filters have a bulky structure and can only filter the frequencies they were tuned for.

A shunt active power filter (SAPF) is an attractive solution to improve electrical network power quality [5]. Compact size, flexibility and excellent filtering performance are some SAPF merits. Generally, the SAPF is a three-phase current controlled voltage source inverter with a storage capacitor on the DC side and interfacing filter inductors on the AC side. The SAPF acts as a current source injecting the required current harmonic components and the reactive power needed by the load to ensure balanced three phase supply currents with pure sinusoidal waveforms.

SAPF operation has two main aspects; first is the generation of reference currents and second, the current control technique, i.e., tracking of the reference currents. Several methods have been proposed for reference current extraction [6]: synchronous reference frame, capacitor voltage control, neural networks, Fourier series, Kalman filter [7] and *pq* theory [8].

The most common current tracking approaches are hysteresis, linear pulse width modulation (PWM), and deadbeat current control techniques [9]. Hysteresis is a non-linear current control approach where the current error is handled by a hysteresis band controller. Switching signals are changed when the error in current transgresses out with a certain predefined band. But a narrow hysteresis band is required to guarantee accurate current tracking, resulting in high switching frequency. PWM is a linear control approach which uses a proportional-integral (PI) controller to generate the reference voltage signals. Then a modulating stage is required, either through carrier triangular waveforms or space vector modulation (SVM), to generate the required gating signals. However, PI control, in the stationary reference frame, results in unsatisfactory, slow response with poor tracking capability due to the wide frequency spectrum of the harmonic content [10]. Deadbeat current control replaces the PI controller with a deadbeat controller where the controller generates the required voltage vector that results in zero current error in the next sampling instant. But the deadbeat controller is severely affected by system parameter variation, noise in measured signals and calculation delay requiring an excessively high sampling frequency [11].

Due to these shortcomings in classical control techniques, finite control set model predictive current control (FCS-MPCC) emerged as an excellent current control alternative [12]. As opposed to PWM and deadbeat control techniques, MPCC does not require a modulating stage [13]. MPCC is based on a different control philosophy, being a proactive approach rather than being reactive. Action is taken before the error in current occurs [14]. MPCC has better transient and steady state performance compared with classical control approaches [15]. Moreover, MPCC can incorporate constraints in the cost function, hence satisfying multi objectives control targets [16]. MPCC covers a wide range of power converter applications including inverters as well as active power filters [17].

Conventionally, two-level, three-legs, six-switch (B6) voltage source inverters are utilized in SAPF applications. In an attempt to reduce the converter cost, the four switch (B4) converter was proposed, initially for drive applications [18-20] thence for SAPF [21]. The B4 inverter utilizes only four power semiconductor switches, diodes, and gate drivers instead of six. This reduces the overall converter cost and minimizes conduction losses. Additionally, inverter reliability improves but at the expense of fewer switch states and higher semiconductor voltage rating.

In [22], traditional triangular PWM is utilized to generate the required gating signals for the power switches. However, in the analysis, two capacitor voltages are assumed equal. Also, four PI controllers are required for generating and tracking the reference current. A different control approach is adopted in [23], where the supply currents are controlled instead of the SAPF currents. This eliminates two current sensors. But reference current generation is based on tuning a PI controller which inherently has slow response, along with requiring a linear plant model for parameter tuning. Also, a phase locked loop (PLL) is needed to detect the voltage phase at the point of common coupling (PCC).

In [24], one cycle control is proposed but the control is complex. In addition, modelling is based on considering the load as a linear lagging type. Thus, performance deteriorates when the linear load is replaced with a nonlinear load with high harmonic content. This control approach does not require voltage sensors at the PCC, but performance deteriorates with a distorted supply voltage. In [25], SVM based on coordinate transformation is proposed to simplify trigonometric calculations but a linear plant model is required to tune current controller gains. The absence of a zero-voltage vector along with a high frequency carrier signal is required for capacitor voltage balancing, which increases switching loss. Variable parameter PWM is introduced in [26] for improved current tracking. Yet, the two parameters of the proposed PWM require tuning by experimentation. Moreover, capacitors voltages balancing is not considered. In addition, a y/y transformer is required to match the voltage between the SAPF AC side and the PCC.

In [27], a PI plus Vector PI controller is proposed to control the supply current. Control is complex; a fourth order plant model is required, no controller tuning method is given, the discrete time model involves a trigonometric part which requires long execution times, and finally the problem of capacitor imbalance is not considered. Double band HCC is proposed in [28], [29] to reduce switching loss. But the control approach results in unequal voltage stress on the switching devices, resulting in converter switching devices with a higher voltage rating. In [30] an SVM technique is proposed for a fault tolerant converter to reduce the computational burden. The converter requires six switches and six contactors which significantly increase cost.

A variable modulation index is proposed in [31], [32] to improve current tracking performance. This results in an increased switching frequency. In addition, the capacitor voltages balancing is not addressed and no experimental results are given to validate the proposed control approach.

In this paper, a finite control set model predictive current control FCS-MPCC approach is proposed to accurately track the B4 SAPF reference currents. The cost function is modified to account for capacitors' voltage balancing accordingly. Only two shunt filter interfacing inductors are required which further reduces the overall cost. Comparison of the proposed approach against conventional HBCC is highlighted. The paper contribution is:

- Two interfacing filter inductors are deployed instead of three which reduces converter cost.
- An FCS-MPCC approach is proposed which improves the SAPF performance by more than 20% over the conventional HBCC.

The paper is organized as follows; section II discusses the proposed converter highlighting basic SAPF operating principles along with a detailed mathematical model of the proposed converter. The concept of FCS-MPCC applied to the B4 SAPF is investigated in section III. Section IV addresses the problem imbalance of two DC side capacitor. Simulation results of the proposed control approach, along with a comparison with conventional approaches, are illustrated in section V. Experimental results, validating the proposed concept, are given in section VI. Conclusion form section VII.

## II. The Proposed B4 SAPF

This section discusses and analyzes the proposed low-cost B4 SAPF. Fig. 1 shows a three-phase power supply feeding a balanced three-phase nonlinear load. At the PCC, the four-switch SAPF is connected through two interfacing inductors. The shunt converter has only four switches instead of the conventionally six. Phase '$a$' is connected to the center point of the two DC side series connected capacitors. Only two interfacing filter inductors, $L_f$, are required to filter out switching current ripple. Thus, the SAPF acts as a current source supplying the required current harmonic content and reactive power to the load, resulting in pure balanced three-phase sinusoidal grid currents as seen in Fig. 1. The basic operation of the SAPF along with reference current generation are briefly highlighted. A detailed mathematical model of the proposed converter is illustrated.

### *A. Reference Current Generation*

The first step in SAPF operation is reference current generation. A dominant technique for reference current generation is the instantaneous active and reactive power (*pq*) theory proposed by Akagi in 1983 which deals with the three-phase system as one entity. The *pq* method involves simple algebraic expressions, so it can be implemented using ordinary processors, which is a main advantage of the technique. Also, the method can be applied to any three-phase system balanced or unbalanced, with or without a neutral. The method is also valid for both transient and steady state cases.

The PCC voltages, DC side capacitor voltage, and the load currents are measured. The *pq* theory is applied to extract the undesired components of the power, to generate the reference currents.

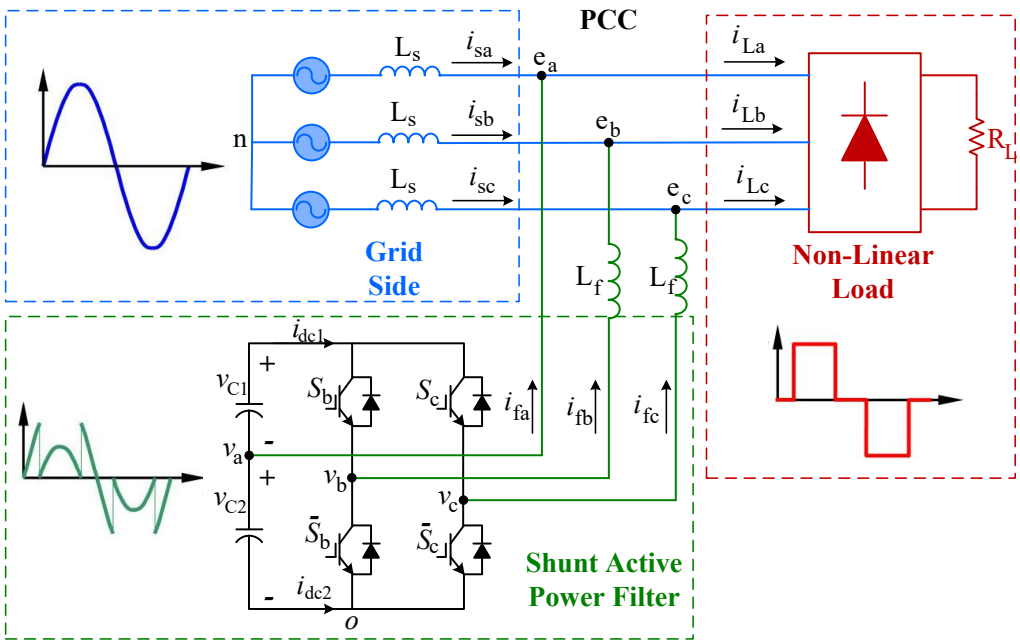


**Fig. 1.** Proposed B4 SAPF.

These reference currents represent the harmonic content and the reactive power required by the load, therefore the SAPF must synthesize these reference currents. Since the system is a balanced, only two voltages at the PCC along with two load currents need to be measured.

The theory is based on Clarke's transformation where the voltages and currents are transformed from '*abc*' to '*αβ*' coordinates using (1).

$$\begin{bmatrix} x_\alpha \\ x_\beta \end{bmatrix} = \sqrt{2/3}\begin{bmatrix} 1 & -1/2 & -1/2 \\ 0 & 1/2\sqrt{3} & -1/2\sqrt{3} \end{bmatrix}\begin{bmatrix} x_a \\ x_b \\ x_c \end{bmatrix} \tag{1}$$

where $x$ represents the voltage and current. The factor $\sqrt{2/3}$ is for invariant power transformation.

After the voltages and currents are transformed, the instantaneous values of the real power, $p$, and the imaginary power, $q$, are calculated from (2).

$$\begin{bmatrix} p \\ q \end{bmatrix} = \begin{bmatrix} v_\alpha & v_\beta \\ -v_\beta & v_\alpha \end{bmatrix}\begin{bmatrix} i_\alpha \\ i_\beta \end{bmatrix} \tag{2}$$

Each power component consists of two parts; the mean (DC) part and the alternating part. The mean value of instantaneous real power, $\bar{p}$, corresponds to the energy per unit time transferred from the power supply to the load through the three phases, hence represents the effective (useful) desired power. The other power components (i.e., the alternating part of the real power, $\tilde{p}$, and the imaginary power, $q$) represent the harmonic content and the reactive power. These power components are undesirable power components, hence will be supplied to the load by the SAPF. Thus, the compensating powers are defined by (3).

$$\begin{aligned} p_c &= \tilde{p} - p_{reg} \\ q_c &= q \end{aligned} \tag{3}$$

where $p_{reg}$ represents the switching power loss.

The switching power loss is supplied by the capacitor causing voltage drop in the DC side capacitor voltage. The grid must supply the DC side capacitor with an amount equal to power loss, so the DC side capacitor voltage is kept constant using a PI controller.

After the compensated powers are calculated as given by (3), the reference currents can be generated by inverting (2) as given by (4).

$$\begin{bmatrix} i^*_{f\alpha} \\ i^*_{f\beta} \end{bmatrix} = \frac{1}{v_\alpha^2 + v_\beta^2}\begin{bmatrix} v_\alpha & -v_\beta \\ v_\beta & v_\alpha \end{bmatrix}\begin{bmatrix} p_c \\ q_c \end{bmatrix} \tag{4}$$

Now the reference currents in '*αβ*' coordinates are known and are transformed back to the '*abc*' coordinates using an inverse Clarke's transformation given by (5).

$$\begin{bmatrix} i^*_{fa} \\ i^*_{fb} \\ i^*_{fc} \end{bmatrix} = \sqrt{2/3}\begin{bmatrix} 1 & 0 \\ -1/2 & 1/2\sqrt{3} \\ -1/2 & -1/2\sqrt{3} \end{bmatrix}\begin{bmatrix} i^*_\alpha \\ i^*_\beta \end{bmatrix} \tag{5}$$

### *B. Modelling of The Proposed B4 SAPF*

To establish the second SAPF operational step, current tracking, accurate modelling of the system is required. Referring to Fig. 1, the converter voltages with respect to the converter reference, $o$, are given by (6).

$$\begin{aligned} v_{ao} &= v_{c2} \\ v_{bo} &= s_b(v_{c1} + v_{c2}) \\ v_{co} &= s_c(v_{c1} + v_{c2}) \end{aligned} \tag{6}$$

where $v_{c1}$, and $v_{c2}$ are the upper and lower capacitor voltages respectively, while $s_b$ and $s_c$ are the upper switches of phases *b*, and *c* respectively. (1 represents switch ON, and 0 represents switch OFF).

Table I summarizes the converter possible switching states and the corresponding output voltages.

TABLE I
SWITCHING STATES AND CORRESPONDING VOLTAGES

| State | | Output voltage | | |
|---|---|---|---|---|
| $s_b$ | $s_c$ | $v_{ao}$ | $v_{bo}$ | $v_{co}$ |
| 0 | 0 | $v_{c2}$ | 0 | 0 |
| 0 | 1 | $v_{c2}$ | 0 | $v_{c1}+v_{c2}$ |
| 1 | 0 | $v_{c2}$ | $v_{c1}+v_{c2}$ | 0 |
| 1 | 1 | $v_{c2}$ | $v_{c1}+v_{c2}$ | $v_{c1}+v_{c2}$ |

The converter voltages with respect to the grid neutral, *n*, are given by:

$$\begin{aligned} v_{an} &= v_{ao} - v_{no} = e_{an} \\ v_{bn} &= v_{bo} - v_{no} = e_{bn} + R_f i_{fb} + L_f \frac{di_{fb}}{dt} \\ v_{cn} &= v_{co} - v_{no} = e_{cn} + R_f i_{fc} + L_f \frac{di_{fc}}{dt} \end{aligned} \tag{7}$$

Adding these three components, for a balanced three-phase system, (8) holds:

$$\begin{aligned} e_{an} + e_{bn} + e_{cn} &= 0 \\ i_{fa} + i_{fb} + i_{fc} &= 0 \end{aligned} \tag{8}$$

Hence, the potential difference between the grid neutral, *n*, and the converter reference, *o*, is defined by (9).

$$\begin{aligned} v_{no} = \tfrac{1}{3}\Big\{ & v_{c2} + s_b(v_{c1}+v_{c2}) + s_c(v_{c1}+v_{c2}) \\ & + R_f i_{fa} + L_f \frac{di_{fa}}{dt}\Big\} \end{aligned} \tag{9}$$

Substituting (9) into (8), the converter continuous time model is defined by (10).

$$\begin{aligned} R_f i_{fa} + L_f \frac{di_{fa}}{dt} &= v_{c1}(-s_b - s_c) \\ &\quad + v_{c2}(-s_b - s_c + 2) - 3e_{an} \\ R_f i_{fb} + L_f \frac{di_{fb}}{dt} &= v_{c1}(s_b) + v_{c2}(s_b - 1) - 2e_{bn} \\ &\quad - e_{cn} \\ R_f i_{fc} + L_f \frac{di_{fc}}{dt} &= v_{c1}(s_c) + v_{c2}(s_c - 1) - 2e_{cn} \\ &\quad - e_{bn} \end{aligned} \tag{10}$$

Currents in the upper and the lower DC side capacitors are defined by the switching states of switches $s_b$, and $s_c$ along with the filter currents $i_{fb}$, and $i_{fc}$ as given by (11).

$$\begin{aligned} i_{dc1} &= s_b i_{fb} + s_c i_{fc} \\ i_{dc2} &= (1 - s_b) i_{fb} + (1 - s_c) i_{fc} \end{aligned} \tag{11}$$

The capacitor voltages are defined by (12).

$$\begin{aligned} v_{C1} &= V_1 + \frac{1}{C}\int_{t_0}^{t} -i_{dc1}\,dt \\ v_{C2} &= V_2 + \frac{1}{C}\int_{t_0}^{t} i_{dc2}\,dt \end{aligned} \tag{12}$$

where *C* is the value of each capacitor, and $V_1$ and $V_2$ are the initial voltages on the upper and lower capacitors, respectively.

## III. FINITE CONTROL SET MODEL PREDICTIVE CURRENT CONTROL

FCS-MPCC is an advanced, and accurate current control technique widely used for power converters. The aim is to use the plant discrete time model to predict all its possible future behavior, then select the optimal control action which minimizes a predefined cost function in the next sampling instant. The cost function may be a single objective (minimizing the error in current), or multi-objective (by including a secondary objective function).

Compared with conventional current control approaches, FCS-MPCC eliminates the requirement of a modulating stage, does not require a linear plant model, and allows the inclusion of constraints (balancing of DC side capacitors' voltages). Also, it uses a different philosophy, where control action is taken before the error in current occurs.

Since FCS-MPCC deals with a plant discrete time model. Hence, the SAPF first order continuous time model, described in section II by (9) – (13), is discretized using Euler's method.

The SAPF predicted currents in discrete time domain at sample (k+1) are defined by

$$i_{fy}^{p}(k+1) = \left(1 - \frac{R_f}{L_f}T_s\right) i_{fy}(k) + \frac{T_s}{L_f} V_y(k) \tag{13}$$

where *y* represents the phase (*a, b* and *c*), $T_s$ is the sampling time, and $V_y$ is the voltage for each phase, defined by (14).

$$\begin{aligned} V_a(k) &= v_{c1}(k)\{-s_b - s_c\} + v_{c2}(k)\{-s_b - s_c + 2\} \\ &\quad - 3e_{an}(k) \\ V_b(k) &= v_{c1}(k)\{s_b\} + v_{c2}(k)\{s_b - 1\} - 2e_{bn}(k) \\ &\quad - e_{cn}(k) \\ V_c(k) &= v_{c1}(k)\{s_c\} + v_{c2}(k)\{s_c - 1\} - 2e_{cn}(k) \\ &\quad - e_{bn}(k) \end{aligned} \tag{14}$$

The voltages vary according to the switch states along with the voltage values of the DC side capacitors, and the PCC. Table II summarizes the voltages for the four possible switching states.

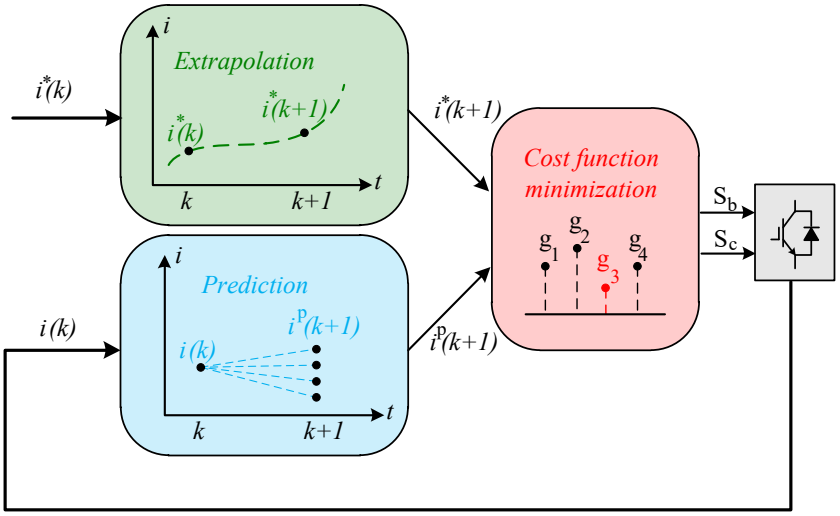


**Fig. 2.** Illustration of FCS-MPCC.

TABLE II
SWITCHING STATES AND CORRESPONDING VOLTAGES

| State | | Output voltage | | |
|---|---|---|---|---|
| $s_b$ | $s_c$ | $V_a(k)$ | $V_b(k)$ | $V_c(k)$ |
| 0 | 0 | $2v_{c2}(k) - 3e_{an}(k)$ | $-v_{c2}(k) - 2e_{bn}(k) - e_{cn}(k)$ | $-v_{c2}(k) - 2e_{cn}(k) - e_{bn}(k)$ |
| 0 | 1 | $v_{c2}(k) - v_{c1}(k) - 3e_{an}(k)$ | $-v_{c2}(k) - 2e_{bn}(k) - e_{cn}(k)$ | $v_{c1}(k) - 2e_{cn}(k) - e_{bn}(k)$ |
| 1 | 0 | $v_{c2}(k) - v_{c1}(k) - 3e_{an}(k)$ | $v_{c1}(k) - 2e_{bn}(k) - e_{cn}(k)$ | $-v_{c2}(k) - 2e_{cn}(k) - e_{bn}(k)$ |
| 1 | 1 | $-2v_{c1}(k) - 3e_{an}(k)$ | $v_{c1}(k) - 2e_{bn}(k) - e_{cn}(k)$ | $v_{c1}(k) - 2e_{cn}(k) - e_{bn}(k)$ |

FCS-MPCC is accomplished through five steps:

1) Extrapolating the reference current (calculated in section II and given by (5)) using the Lagrange method defined by (15).

$$i_{fy}^*(k+1) = 3i_{fy}^*(k) - 3i_{fy}^*(k-1) + i_{fy}^*(k-2) \quad (15)$$

where y represents the phase (*a, b* and *c*),

2) Measuring the SAPF currents $i_{fb}(k)$, $i_{fb}(k)$ and $i_{fc}(k)$. (Two currents are sufficient in a balanced system).
3) Calculating all the possible voltages using Table II.
4) Calculate the predicted SAPF currents defined by (13)
5) Evaluate the cost function given by (16) which represents the absolute error between the reference current and the predicted actual current.

$$g(k) = \sum_{y=a}^{c} \left| i_{fy}^*(k+1) - i_{fy}^p(k+1) \right| \quad (16)$$

The switching state, which minimizes the cost function, is selected and applied to the converter. Fig. 2 illustrates the operation of FCS-MPCC.

## IV. BALANCING OF DC SIDE CAPACITOR VOLTAGES

In the B4 configuration (either operating as an inverter or a SAPF), one phase is connected to the mid-pint of the split DC link capacitor. This configuration can result in voltage imbalance of the two capacitors. If the problem of capacitor voltage imbalance is not resolved, unequal voltage stress will be applied on the switching devices leading to possible failure unless overrated. Conventionally, extra PI controllers are required to balance the DC side capacitor voltages.

But an FCS-MPCC advantage is the possibility of handling multi-objectives, where the primary objective is current control, while the secondary objective could be minimization of the switching frequency, peak current limitation, reduction of the common mode voltage or reactive power or balancing the split DC link capacitor voltages, as in this case. Each objective defined in the cost function is multiplied by a weighting factor to reflect its relative importance.

To balance the DC side capacitor voltages, the discrete time model of capacitor voltages and currents must be defined.

The DC side capacitor currents are defined by (17).

$$\begin{aligned} i_{dc1}(k) &= s_b i_{fb}(k) + s_c i_{fc}(k) \\ i_{dc2}(k) &= \{1 - s_b\} i_{fb}(k) + \{1 - s_c\} i_{fc}(k) \end{aligned} \quad (17)$$

The predicted capacitor voltages are:

$$\begin{aligned} v_{c1}^p(k+1) &= v_{c1}(k) - \frac{1}{C} i_{dc1}(k) \\ v_{c2}^p(k+1) &= v_{c2}(k) + \frac{1}{C} i_{dc2}(k) \end{aligned} \quad (18)$$

Hence, the cost function is modified to account for capacitor imbalance as defined by (19).

$$g(k) = \lambda_i \sum_{y=a}^{c} \left| i_{fy}^{*}(k+1) - i_{fy}^{p}(k+1) \right| + \lambda_v \left| v_{c2}^{p}(k+1) - v_{c1}^{p}(k+1) \right| \tag{19}$$

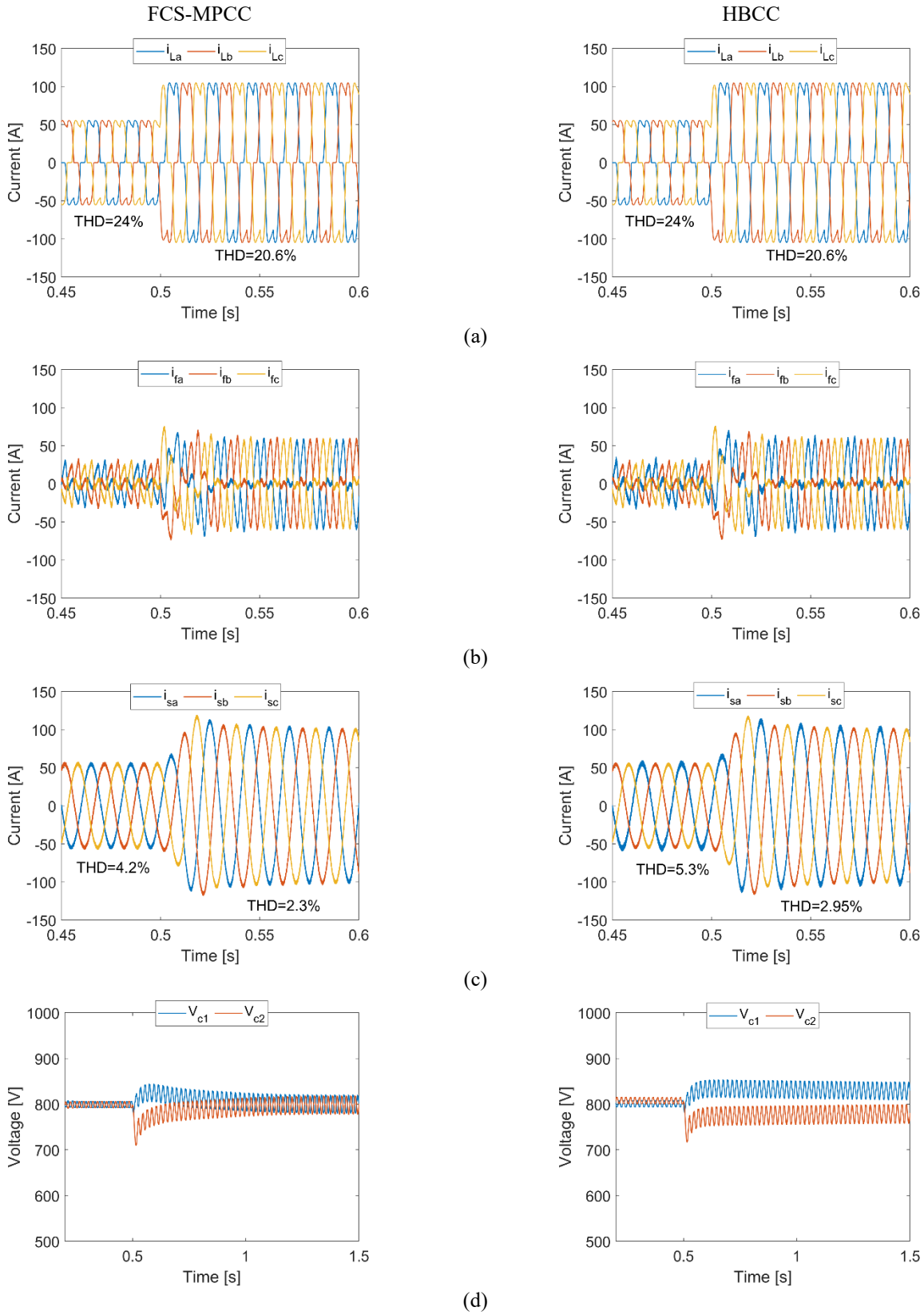


**Fig. 3.** SAPF simulation results using FCS-MPCC and HBCC: (a) Load current, (b) Filter current, (c) Supply current, and (d) DC side capacitor voltages.

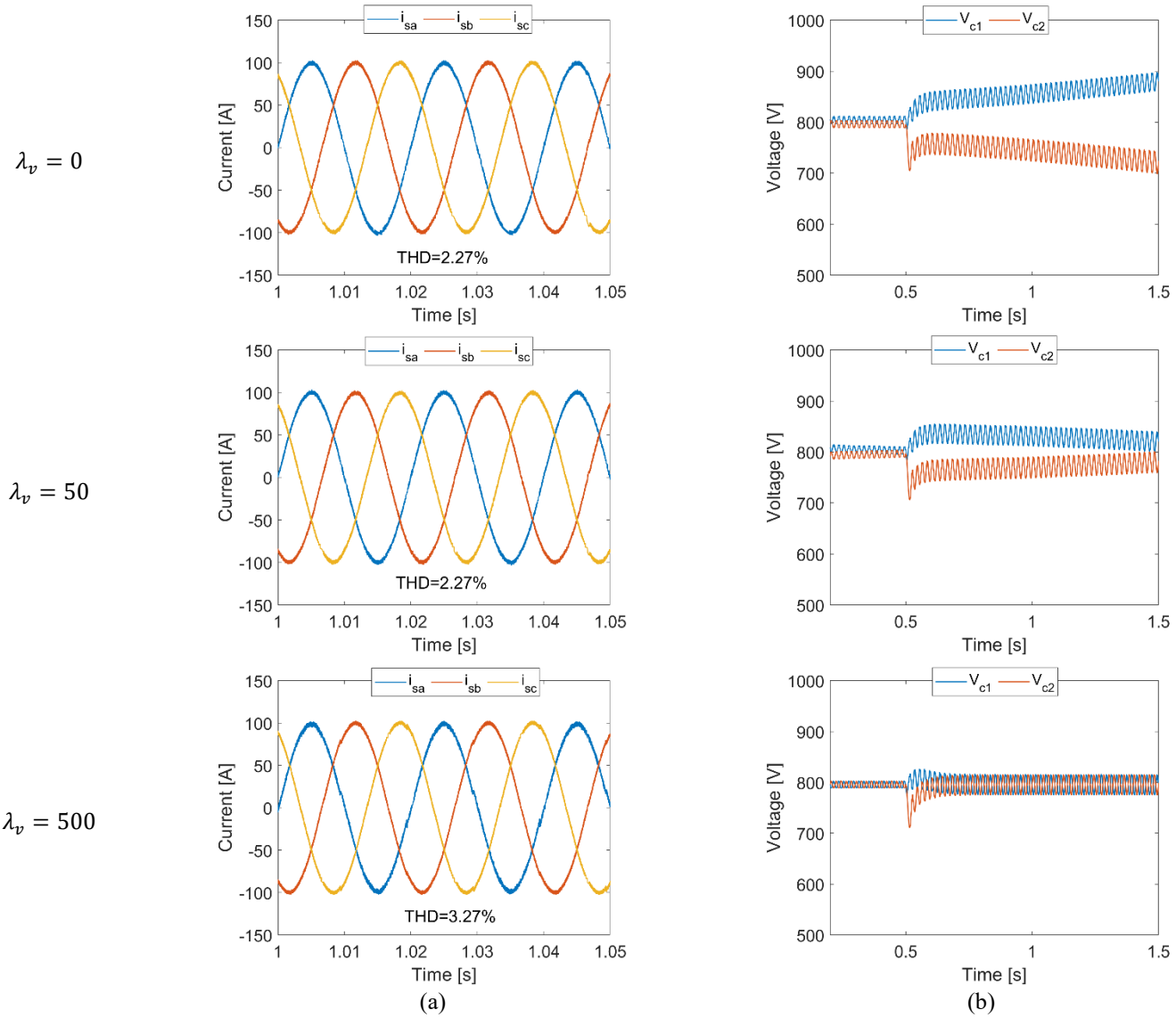


**Fig. 4.** Effect of varying $\lambda_v$: (a) Supply current and (b) DC side capacitor voltages.

where $\lambda_i$ and $\lambda_v$ are the weighting factors for current and voltage balancing, respectively. Changing the weighting factor values offers flexibility resulting in adjustable performance. That is if $\lambda_v$ is set to zero, the cost function will become a single objective with current control only, without considering capacitor voltage imbalance. On the other hand, setting a non-zero value of $\lambda_v$ will introduce the secondary objective into the cost function. Several methods are available for selecting the weighting factors, like heuristic approaches, per unit method, and a look-up table [33]. Using (19), the switching state which ensures optimal current tracking along with balancing the DC side capacitor voltages, is selected.

In this paper a heuristic approach is adopted, where the current weighting factor $\lambda_i$ is set to unity, while the voltage balancing weighting factor $\lambda_v$ is changed gradually and the performance is monitored until satisfactory performance is achieved. Note that the importance of the specific secondary objective implies the initial value of the secondary weighting factor. Since, DC link capacitor voltage balancing is equally important to current tracking, the initial start value of $\lambda_v$ should be high, decreasing gradually. On the other hand, if the secondary objective is not of prime importance, like common mode voltage reduction, the initial start of $\lambda_v$ is set to zero and increased gradually.

## V. Simulation Results

In this section, the simulation results of the proposed current control approach are presented and compared with the results of the HBCC (hysteresis control is selected for comparison as it offers the best performance amongst conventional current control approaches).

The SAPF feeds a diode rectifier load of resistance 10Ω. At 0.5s the load resistance is halved by connecting another 10Ω in parallel. A small hysteresis band (0.5A) is selected to improve HBCC performance, for fair comparison.

Table III illustrates the simulation parameters.

TABLE III
SAPF PARAMETERS (SIMULATION RESULTS)

| Parameter | Value |
|---|---|
| Frequency | 50Hz |
| Line to line voltage, rms | 400V |
| DC link voltage | 1600V |
| Diode rectifier load resistance | 10Ω//10Ω |
| Filter inductance | 2x3mH |
| DC side capacitance | 2x3.3mF |
| Sampling time | 10µs |

Fig. 3 shows the performance comparison between both approaches. Fig. 3a shows the load current with high harmonic content, hence with high total harmonic distortion (THD). The THD is severely pronounced at light loads as the value of the current fundamental component is low.

Fig. 3b shows the SAPF current for both approaches. While Fig. 3c demonstrates the supply current waveform where balanced three-phase sinusoidal current waveforms are achieved by both approaches. For the operation up to 0.5s (when the connected load is 10Ω), FCS-MPCC produces 4.2% THD as opposed to 5.3% for the HBCC (a 21% improvement). But when the rectifier load resistance is halved (increasing the current fundamental component) the THD is 2.3% and 2.95% for the FCS-MPCC and the HBCC respectively (a 22% improvement).

For proper B4 inverter/SAPF operation, balancing of the split DC capacitors is vital. Owing to FCS-MPCC versatility, the cost function is easily updated, according to (19), to account for the DC side capacitor voltage balancing. The value of $\lambda_i$ is set to unity, while $\lambda_v$ is 150. Hence, satisfactory performance is achieved as seen in Fig. 3d, where the split dc link capacitor voltages are balanced.

To further investigate the effect of varying $\lambda_i$ and $\lambda_v$, Fig. 4 demonstrates FCS-MPCC performance at different voltage balancing weighting factors $\lambda_v$, while keeping the current weighting factor $\lambda_i$ at unity in all cases. Fig. 4a shows the supply current waveforms, while Fig. 4b shows the DC side capacitors' voltages. When ignoring voltage balancing ( $\lambda_v = 0$), the split DC side capacitor voltages deviate after changing the load condition at 0.5s. But when $\lambda_v$ is set to a non-zero value, balancing of capacitors' voltages is achieved almost with the same supply current THD. Although voltage balancing is quickly achieved with an exaggerated value ($\lambda_v = 500$), the harmonic content in supply current increases.

Fig. 5 studies the dynamic response of the system, where Fig. 5a illustrates the three-phase supply currents at startup where balanced three-phase sinusoidal currents are achieved after two cycles. Fig. 5b shows balanced split DC link capacitor voltages. As highlighted previously, the value of the voltage balancing weighting parameter affects the time required for the capacitor voltages to balance.

Both FCS-MPCC and HBCC have variable switching frequencies. With $10\mu s$ sampling time, the switching frequency for both does not exceed 25kHz. Fig. 6 shows the switching pulses for both approaches - showing similar switching frequencies.

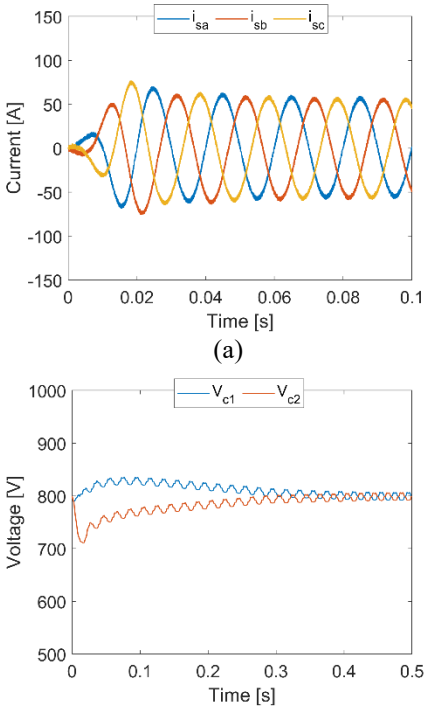


**Fig. 5.** Dynamic response of the proposed SAPF: (a) Three-phase supply currents and (b) Split DC link capacitor voltages.

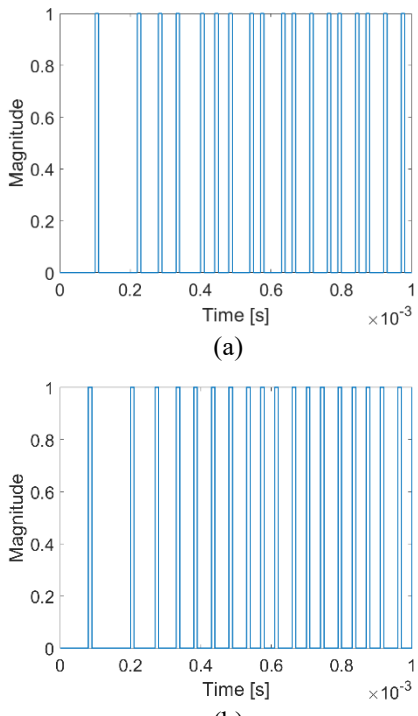


**Fig. 6.** Gating signals: (a) FCS-MPCC and (b) HBCC

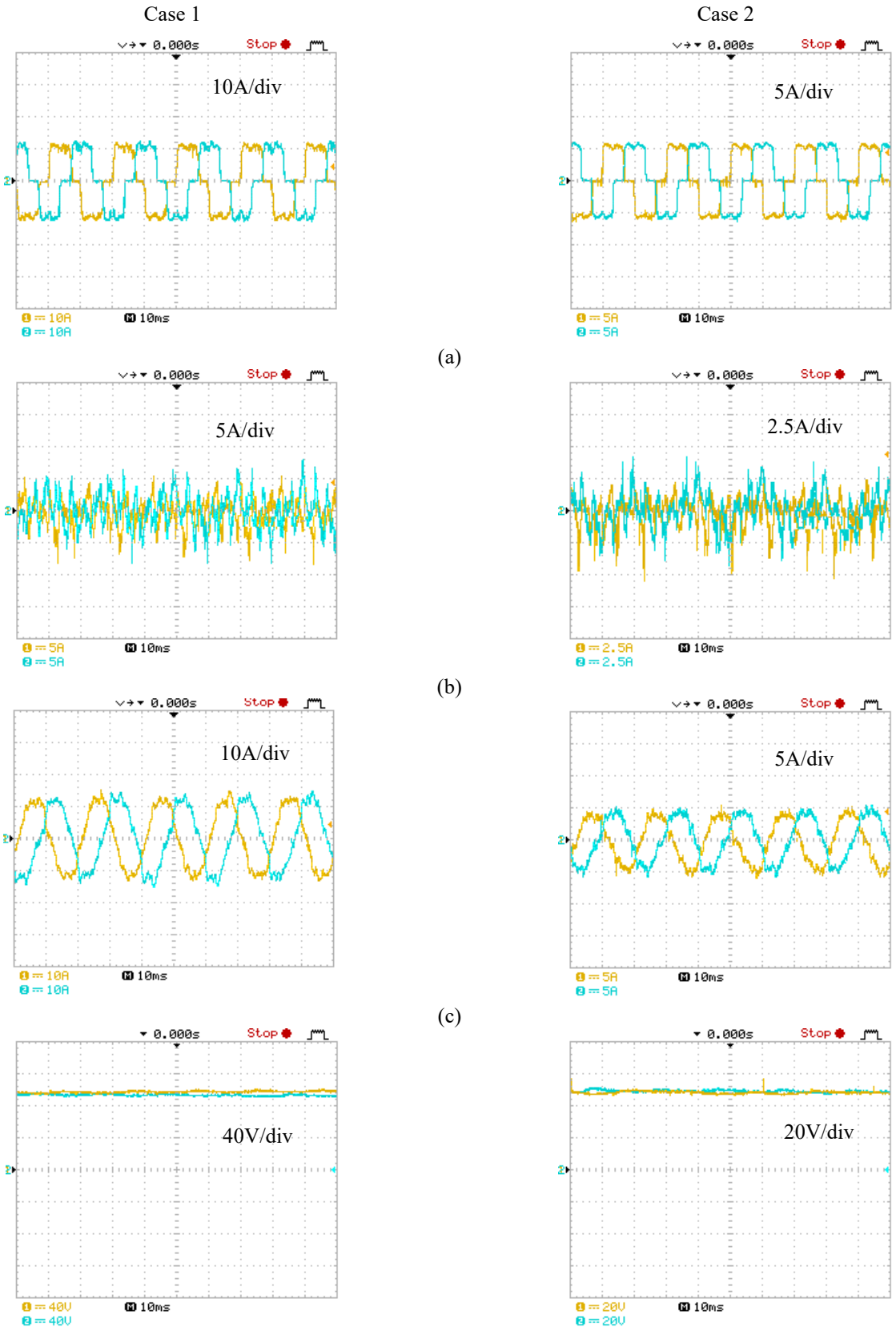


**Fig. 7.** SAPF experimental results using FCS-MPCC: (a) Load current, (b) Filter current, (c) Supply current, and (d) DC side capacitor voltages.

Table IV summarizes the simulation results showing the THD for different voltage balancing weighting factors along with the time required ($t_{bal}$) for the split dc link capacitor voltages to balance.

TABLE IV
THD AND BALANCING TIME FOR DIFFERENT $\lambda_v$

| $\lambda_v$ | THD (%) | $t_{bal}$ $(s)$ |
|---|---|---|
| 0 | 2.27 | $\infty$ |
| 50 | 2.27 | 1.5 |
| 150 | 2.3 | 0.4 |
| 500 | 3.27 | 0.1 |

## VI. EXPERIMENTAL RESULTS

The experimental results of the proposed current control approach are presented in this section. The experimental test rig used to confirm the findings is shown in the Appendix. Table V shows the parameters experimental used. Results for two cases are presented: 200V DC link voltage and 100V dc to show that the proposed control approach is suitable for different voltage and current levels. The SAPF feeds a diode rectifier load of resistance 4.7Ω. Results are illustrated in Fig. 7

Fig. 7a shows the load currents, where nonsinusoidal current waveforms with high THD are found due to the nonlinear diode rectifier load (see Fig. 3a for simulation results). Fig. 7b shows SAPF currents, where these currents represent the harmonic content and reactive power required by the nonlinear load (see Fig. 3b for simulation results). Supply current waveforms are illustrated in Fig. 7c, where balanced sinusoidal waveforms are achieved (see Fig. 3c for simulation results). Note that only two currents are presented for the load, the filter and the supply since the system is a 3φ balanced system. This allows the utilization of fewer voltage and current sensors. Finally, Fig. 7d illustrates balanced DC side split capacitor voltages (see Fig. 3d for simulation results), where the proposed FCS-MPCC approach balances the capacitors' voltages.

TABLE V
SAPF PARAMETERS (EXPERIMENTAL RESULTS)

| Parameter | Value | |
|---|---|---|
| | Case 1 | Case 2 |
| Frequency | 50Hz | 50Hz |
| Line to line voltage, rms | 50V | 25V |
| DC link voltage | 200V | 100V |
| Diode rectifier load resistance | 4.7Ω | 4.7Ω |
| Filter inductance | 2x3mH | 2x3mH |
| DC side capacitance | 2x3.3mF | 2x3.3mF |
| Sampling time | 25μs | 25μs |

## VII. CONCLUSION

This paper presented a finite control set model predictive current control (FCS-MPCC) approach for a low cost, reduced size, four-switch (B4) shunt active power filter (SAPF). In addition, two filter inductors instead of conventional three inductors are utilized to filter out the switching harmonics. A detailed mathematical model was presented in both the continuous and discrete time domains. The problem of split DC side capacitor imbalance is readily handled by modifying the cost function, where weighting factors are adjusted to satisfy the primary objective (current tracking), and the secondary objective (balancing DC side split capacitor voltages). The FCS-MPCC approach was illustrated for accurate reference current tracking. Comparison of the proposed control approach against a conventional, widely used hysteresis band current control (HBCC) approach showed the superior performance of the proposed FCS-approach, with more than a 20% improvement. Experimental results validate the proposed control approach.

## APPENDIX

Fig. 8 shows the experimental test rig used to validate the simulation results.

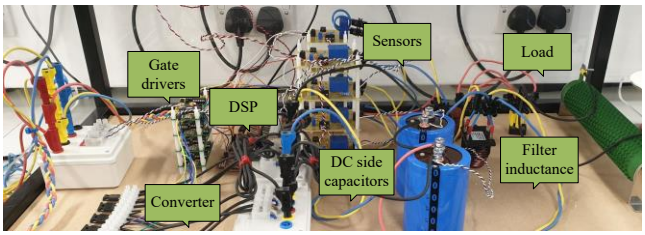


**Fig. 8.** Experimental test rig.

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