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DESIGN OF POWER CONVERTERS WITH EMBEDDED ENERGY STORAGE FOR HYBRID DC-AC APPLICATIONS

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Thesis submitted to the Pontificia Universidad Católica de Chile in partial fulfilment of the requirements for the degree of Doctor in Engineering Sciences

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Santiago de Chile, June 2023

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Gratefully to my family

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ABSTRACT

The high penetration of renewable energies into power systems is leading to a revolution in the structure of modern power grids. In this context, the present thesis investigates the design of power electronics converters with extended capabilities due to the embedding of energy storage within the topologies. Thus, the research objective is to propose power converters with capabilities of integrating energy storage technologies to provide further services required for the operation of hybrid dc-ac systems. The thesis contains two parts, first part shows the work developed for low- and medium-power applications, while the second part describes the investigation performed for high-power systems.

The first part of this thesis explains the design and operation of a three-port dc-dc-ac converter developed for integrating energy storage into hybrid dc-ac applications. The topology is based on a conventional two-level dc-ac converter, and it uses a single power conversion stage to control the power flow between three ports, minimising the required components. Simulation and experimental results validate the operation of the proposal, showing that a multi-variable control system allows exploiting the degrees of freedom to manage power interactions of multiple elements without needing extra power converters. Furthermore, a comparative analysis is carried on to showcase the advantages and limitations of the proposal as opposed to state-of-the-art solutions in the same context. The study concludes that the proposed topology is suitable for low- and medium-power systems with bidirectional power flow capabilities among all ports and limited voltage boost needs. Simulation analysis shows that efficiencies up to 95.94% can be reached for a 3 kW design, which compares to efficiencies of similar state-of-the-art topologies. Moreover, the operation is also validated in a reduced-scale prototype allowing to test the multi-variable control scheme in a real-time implementation.

The second part of the thesis focuses on the design and operation of a Modular Multilevel Converter (MMC) topology with integrated energy storage using new parallel branches

in the phases of the converter. This topology allows the integration of partially-rated Energy Storage Systems (ESS) to decouple the ac and dc sides of a High Voltage Direct Current (HVDC) substation. Thus, it enables the provision of ancillary services such as fast frequency response, black-start capabilities and load-levelling, which are required by modern hybrid dc-ac power grids. Results show that the proposal allows the addition of up to 37% power from the ESS considering similarly rated power semiconductors in a simulated 1 GW MMC substation. Analysis shows that extra device losses remain under 1% for an additional $\pm 10\%$ of ESS power on top of the nominal substation-rated power. Furthermore, a laboratory-scale experimental rig was built to demonstrate the operation of the proposed design.

In conclusion, two different topologies are proposed and analysed for integrating energy storage into hybrid dc-ac applications depending on the power rating required. The study is supported by simulation and experimental results obtained during the project to validate both proposals.

Keywords: DC-AC Power Conversion, Multi-port Converters, Modular Multilevel Converters (MMC), Energy Storage Systems (ESS), Hybrid Power Integration, Multi-variable Control Systems.

RESUMEN

La creciente inclusión de energías renovables en los sistemas eléctricos está provocando una revolución en la estructura de las redes eléctricas modernas. En este contexto, la presente tesis investiga el diseño de conversores de potencia con capacidades extendidas debido a la incorporación de almacenamiento de energía dentro de las topologías. Así, el objetivo de la investigación es proponer conversores de potencia con capacidades de integración de tecnologías de almacenamiento de energía para brindar servicios adicionales requeridos para la operación de sistemas híbridos CC-CA. La tesis consta de dos partes, la primera parte muestra el trabajo desarrollado para aplicaciones de baja y media potencia, mientras que la segunda parte describe la investigación realizada para sistemas de alta potencia.

La primera parte de esta tesis explica el diseño y operación de un conversor CC-CC-CA de tres puertos desarrollado para integrar el almacenamiento de energía en aplicaciones híbridas CC-CA. La topología se basa en un convertidor CC-CA convencional de dos niveles y utiliza una sola etapa de conversión de energía para controlar el flujo de energía entre tres puertos, lo que minimiza los componentes necesarios. Los resultados de simulación y experimentales validan el funcionamiento de la propuesta, mostrando que un sistema de control multivariable permite explotar los grados de libertad para gestionar interacciones de potencia de múltiples elementos sin necesidad de conversores de potencia adicionales. Además, se realiza un análisis comparativo para mostrar las ventajas y limitaciones de la propuesta frente a soluciones de vanguardia en el mismo contexto. El estudio concluye que la topología propuesta es adecuada para sistemas de potencia media con capacidades de flujo de potencia bidireccional entre todos los puertos y necesidades limitadas de aumento de voltaje.

La segunda parte de la tesis se centra en el diseño y operación de una topología de Conversor Modular Multinivel (MMC) con almacenamiento de energía integrado utilizando nuevas ramas paralelas en las fases del conversor. Esta topología permite la integración

de sistemas de almacenamiento de energía (ESS) de potencia limitada para desacoplar los lados de CA y CC de una subestación HVDC. Por lo tanto, permite la provisión de servicios auxiliares como respuesta de frecuencia rápida, capacidades de arranque en negro y nivelación de carga, que son requeridos por las redes eléctricas híbridas de CC-CA. Los resultados muestran que la propuesta permite agregar hasta un 37% de potencia desde el ESS considerando semiconductores de potencia de clasificación similar en una subestación MMC simulada de 1 GW. El análisis muestra que las pérdidas de dispositivos adicionales se mantienen por debajo del 1% por un $\pm 10\%$ adicional de energía desde ESS.

En conclusión, esta tesis propone y analiza dos topologías diferentes para integrar el almacenamiento de energía en aplicaciones híbridas de CC-CA según la potencia nominal requerida. El estudio se apoya en resultados de simulación y experimentales obtenidos durante el proyecto para validar ambas propuestas.

Palabras Claves: Conversión de energía CC-CA, Conversores Multipuerto, Conversores Modulares Multinivel (MMC), Sistemas de Almacenamiento de Energía (ESS), Sistemas Híbridos de Potencia, Sistemas de Control Multivariable.

1. INTRODUCTION

The energy transition towards a carbon-neutral world is key to the sustainability of humanity and also, and urgent need due to accelerated climate changes. Thus, most countries around the world aim to reach the carbon-neutral goal by 2050 (Evans et al., 2022; Guterres, 2020; McKinsey & Company, 2022). Consequently, there is a growing need for the inclusion of renewable energies into the grid at both industrial and residential levels. Additionally, the electrification of final energy uses, such as heating and transport, also needs to increase drastically to achieve the Net-Zero goal. Specifically, renewable participation in electricity generation should rise to 86% and electrification of end uses should go from the current 20% to around 50% by 2050 to achieve the goal (International Renewable Energy Agency (IRENA), 2020), as shown in Fig. 1.1. Therefore, the development of power converters for using renewable sources and replacing fossil fuel systems achieving high density, efficiency and reliability is one of the main challenges in reaching the zero net emissions goal.

The use of power converters is fundamental to increase electrification based on renewable energies, as this challenge imposes the use of Direct Current (DC) technologies in

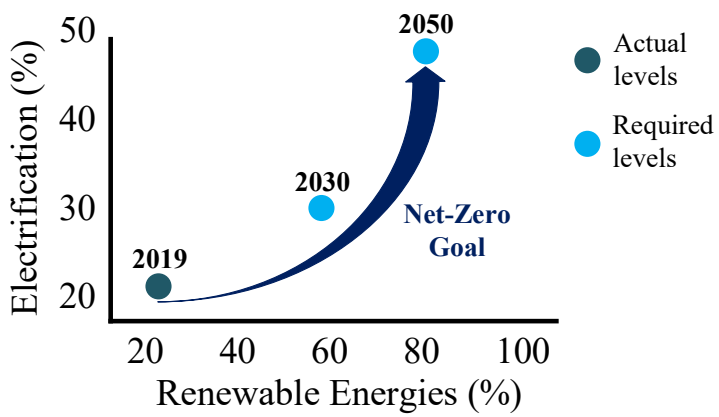


FIGURE 1.1. Required electrification and renewable generation share to achieve Net-Zero goal.

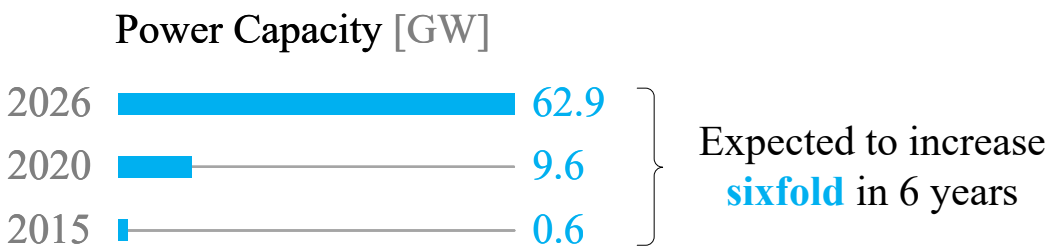


FIGURE 1.2. Battery Energy Storage Systems Worldwide Installed Capacity.

conjunction with the existing Alternate Current (AC) systems (Rodriguez et al., 2009). Examples of these hybrid DC-AC systems requiring power converters are solar photovoltaic (PV) generation connected to the AC grid, HVDC interconnections between two or more AC grids and Electric Vehicles (EV) powertrains (Clement-Nyns et al., 2010; Eftekharnejad et al., 2013; Kroposki et al., 2017; MacDowell et al., 2019; Shen et al., 2019). However, the inclusion of power converters raises a stability problem for the grids, as inherently these technologies do not contribute to the system inertia as large synchronous generators (Gevorgian et al., 2015; Lasseter et al., 2020; Y. Liu et al., 2017). Thus, the latest research trends have focused on implementing grid-forming capabilities in power converters to address the stability issues on small and large-scale systems (Fang et al., 2019; Rathnayake et al., 2021; Serban & Marinescu, 2014). The lack of kinetic energy in power converter systems leads to the use of different energy storage sources (Batteries, super-capacitors and hydrogen-based systems) to provide the required services maintaining the grid operation (Fang et al., 2018; Renaudineau et al., 2022). Therefore, the use of Energy Storage Systems (ESS) has increased rapidly in the last years, with studies showing a growth factor of 6 for utility-scale ESS to 2026 (International Energy Agency (IEA), 2021), as shown in Fig. 1.2.

Consequently, the transformation of power systems to comply with a sustainable development path presents two main technical challenges to be tackled with the use of power electronics systems:

- Co-existence of AC and DC technologies to increase the electrification of all sectors based on renewable energy sources.

- Integration of ESS into hybrid DC-AC systems to support the operation, addressing the variability of renewable resources and replacing fossil fuel-powered technologies.

1.1. Hybrid DC-AC Applications with Energy Storage

Different technologies will drive the transformation of modern power systems to face the rising inclusion of clean energy sources and decommissioning of fossil fuel systems. Applications can be classified according to their operation characteristics, such as power and voltage levels, as these define the requirements for the needed power conversion stage. Thus, this section will describe the main hybrid DC-AC technologies playing a role in the energy transition to a carbon-neutral society according to their power levels.

1.1.1. Low and Medium Power Applications

The inclusion of Distributed Energy Resources (DER) is a major change in the operation of modern electrical grids, which used to be highly unidirectional and dominated by utility-scale generators. DERs consist of units located close to the end-users that are able to generate, store and use energy in a controlled manner. Thus, they cover a wide spectrum of technologies as PV generation, ESS (based on batteries, supercapacitors or hydrogen systems) and EVs. These applications usually connect to the grid at the distribution level with rated powers of less than 10 MW. Then, DERs play a fundamental role in the electrification of different sectors and the integration of renewable energy sources into the grid. Additionally, analysis shows that they allow avoiding and/or deferring investment in network infrastructure when used in highly saturated areas at the distribution level (Energy Networks Australia, 2017; National Renewable Energy Laboratory (NREL), 2021). Therefore, the inclusion of DERs has been increasing in the later years and it is projected to keep the trend in the following years, as it is shown in Fig. 1.3.

Distributed PV systems are a well-deployed technology, with significant participation on the renewable generation matrix during the last 10 years. Therefore, the technology seems mature with continuously decreasing prices and a set of relevant actors providing

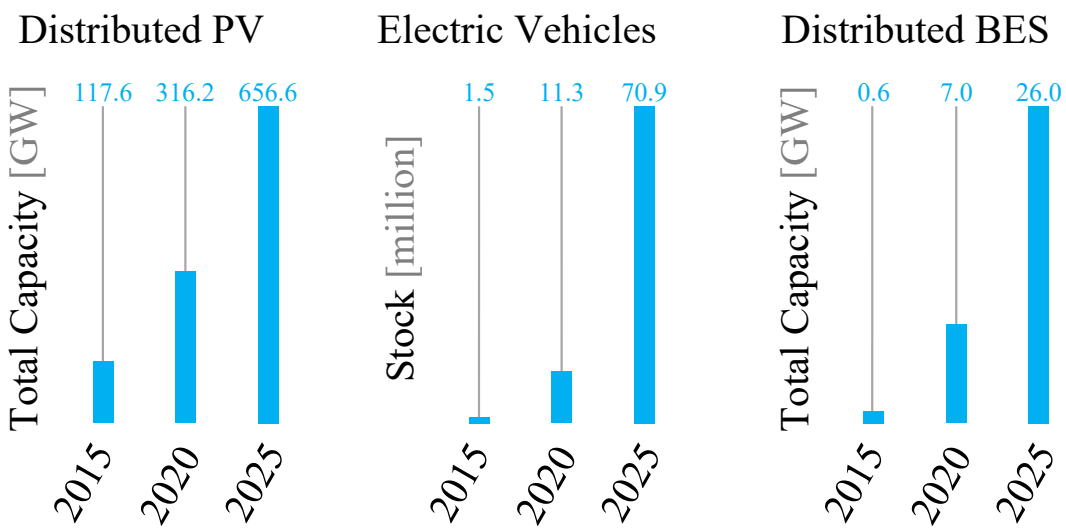


FIGURE 1.3. Inclusion trend of main DERs technologies.

power electronics solutions to connect the PV arrays to the grid. However, there is an opportunity for innovation due to the trend of complementing solar installations with energy storage. This integration allows for improving the overall performance of the system by enabling extra frequency and voltage regulation services using the battery as an energy buffer (Kouro et al., 2015). The penetration of this hybrid configuration is increasing, with countries such as Germany and Hawaii having close to 50% and 100% respectively of their residential solar installed capacity with energy storage units (Bloomberg NEF, 2022).

The share of EVs in the transport market has also increased rapidly in the last years, with projections showing that they should represent more than 60% of the sold vehicles by 2030 (IEA, 2022b). EVs are classified into two major groups, Battery Electric Vehicles (BEV) and Plug-in Hybrid Electric Vehicles (PHEV) depending on the energy source of the powertrain (Habib et al., 2018; Martinez et al., 2017). BEVs power the traction motor exclusively from a battery and dominate the market reaching 68% of the EVs share by 2021 (IEA, 2022a). However, IEA also projects a continuous increment in the PHEV use, having a stock 10 times bigger by 2030 from the present numbers. PHEVs use more than

one energy source, with vehicles using hydrogen fuel cells together with Li-ion batteries showing a promising example for future models.

1.1.2. High Power Applications

The principal change driving the modernisation of the electrical grid at a high-power level is the inclusion of HVDC links in the transmission system. This technology allows integrating remotely located renewable energy sources with the main loads of the grid and also interconnecting different asynchronous AC systems (Barnes et al., 2017; X. Chen et al., 2011; Feng et al., 2014; Flourentzou et al., 2009; L. Zhang et al., 2017). The technical advantages supporting the inclusion of HVDC links into AC systems are the elimination of reactive power, higher power transfer density and the ability to connect asynchronous systems (European Network of Transmission System Operators for Electricity (ENTSO-E), 2019). Therefore, it is projected that the installed capacity of HVDC links evolves from 277 GW in 2017 to over 500 GW by 2025 (Alassi et al., 2019; IEA, 2016).

The main importance of HVDC links is related to enabling the deployment of hybrid DC-AC grids and the connection of large-scale offshore wind energy supplies to the grid, which are two of the flagships defined in the Research, Development, and Innovation Roadmap to 2030 stated by ENTSO-E (2020). Additionally, they should also be able to provide ancillary services to the grid to face the stability issues generated by the decommissioning of fossil fuel-based rotating plants (Aouini et al., 2016; Junyent-Ferr et al., 2015; H. Liu & Chen, 2015). In this regard, the inclusion of energy storage sources appears as a suitable alternative to enable the provision of these services and increase the flexibility of the hybrid DC/AC grids (Errigo, Morel, et al., 2022).

1.1.3. Energy Storage Systems

Energy storage systems appear as a fundamental technology enabling the modernisation of power grids to include the required renewable energy sources and to increase the electrification of end-user applications. ESS work at all power levels providing services to

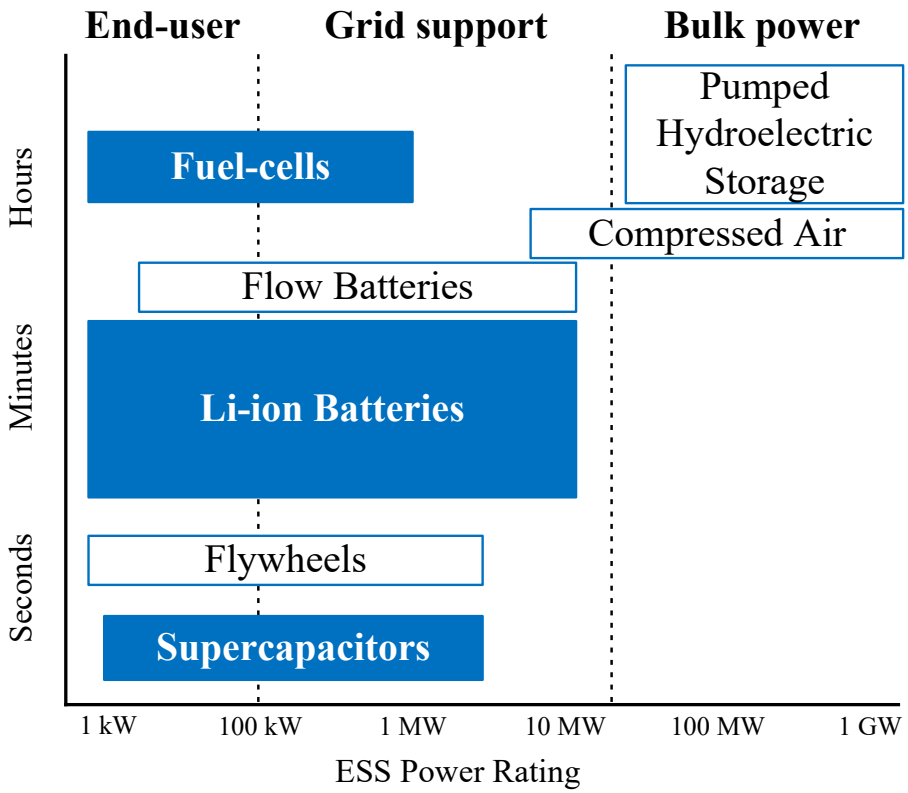


FIGURE 1.4. ESS technologies with power ratings and energy capacity.

improve the grid resilience and add more flexibility to the grid operation. The main principle is to store generated energy from any source into the unit, to then be able of using it when the system requires to. Thus, the main parameters defining the ES units are power rating and the energy capacity defining for how long they can provide the rated power. These parameters vary depending on the selected energy storage technology, as shown in Fig. 1.4 (Boicea, 2014; Farhadi & Mohammed, 2016; Grainger et al., 2014; Stynski et al., 2020). The figure also shows that different ESS technologies are suitable for providing different services, depending on the power and energy capacity. Furthermore, the main three technologies related to the development of the converters in this research are highlighted: Li-ion batteries, supercapacitors and fuel cells.

Li-ion batteries are the most mature energy storage technology and it is expected for them to keep increasing their penetration into power systems, as illustrated in Fig. 1.2 and Fig. 1.3. The main advantages of these batteries are high energy density, fast response, low self-discharge and continuously decreasing manufacturing costs (Lukic et al., 2008; Vazquez et al., 2010). The main applications for Li-ion batteries are EVs, residential ESS, and utility-scale ESS providing regulation services to the grid.

Supercapacitors (SCs) stand out in ES technologies because of their very high power density (1000-10000 W/kg), energy efficiency up to 95% and long cycle life (>50000 cycles) (Fang et al., 2019; Vazquez et al., 2010). Therefore, industry vendors have already started implementing systems based on SCs to provide grid services (ABB, 2012). The main downside of SCs is the reduced energy density compared to other ES technologies, limiting their use for applications with short operational times. However, the latter has motivated the research for hybrid systems, aiming to complement the high power capabilities of SCs with high energy technologies as batteries or fuel cells (Choi et al., 2012; Fang et al., 2018; Thounthong et al., 2007; L. Zhang et al., 2019). Thus, the main use for SCs is related to hybrid EV powertrains and low-energy demanding grid services, such as voltage regulation.

Finally, hydrogen-based ESS are meant to play an important role in the decarbonisation of sectors where fossil-fuel systems are still the standard, such as heavy-duty transport and heavy industry (IEA, 2021). Additionally, hydrogen appears as an emerging technology for seasonal storage of renewable energy due to it very high energy density. The operation of low-emissions hydrogen ESS is based on two main elements: the electrolysers for producing hydrogen from renewable sources, such as PV systems (Renaudineau et al., 2022); and the fuel-cells to generate electricity from the generated hydrogen. The fuel-cell technology has been developed in the last decade, with its main use related to EVs (Bauman & Kazerani, 2008; Zandi et al., 2011).

The common characteristic for the three ES technologies presented is that they operate in DC, therefore they require the use of power converters to be connected to conventional

AC grids and loads. Thus, for the purpose of the present research project, the ESS sources will be modelled as DC power supplies indicating the operational power and energy parameters when required.

1.2. Power Electronics for Hybrid DC-AC Applications with Energy Storage

This section provides a review of the state-of-the-art Power Electronics (PE) systems that have been proposed to address the challenges presented by the applications of the last section. The inclusion of the described applications to enable the net-zero goal by 2050 is strongly attached to the development of new PE topologies. Therefore, research has focused on developing efficient, reliable, and power-dense solutions for these systems in the latter years. The topologies are presented in two different groups, according to their power levels.

1.2.1. Low and Medium Power Topologies

The PE technology to connect DC systems with AC ones is mature, with the Voltage Source Converters (VSC) having crucial importance in the integration of DC technologies to the existing AC grids. For low- and medium-power applications, the most accepted topologies are the two or three-levels converters shown in Figure 1.5. However, section 1.1.1 showed that new applications require the inclusion of energy storage units to complement the operation of the DC-AC power conversion. Therefore, this section presents a review of different power conversion systems aiming to operate with the hybrid DC-AC applications with energy storage, which in this case also operate in DC (either battery, supercapacitor or fuel cell depending on the power and energy needs). Then, it covers power conversion systems connecting two DC ports with one AC port. These systems can be categorised into three main groups depending on the Power Conversion Stages (PCS) used to perform the connection of the three elements. Fig. 1.6 summarises the proposed classification, showing that three major groups exist depending on whether they use three, two or a single PCS. The following subsections present a description of each category addressing the way they work with their advantages and disadvantages.

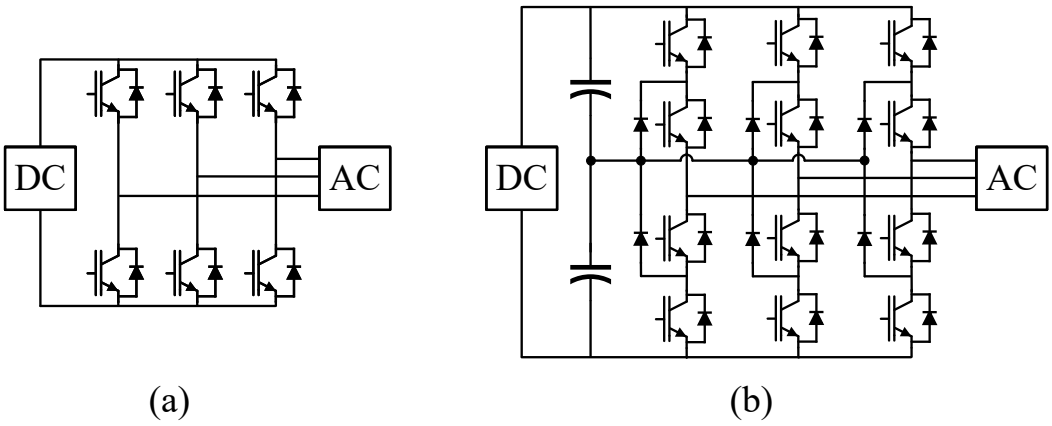


FIGURE 1.5. DC-AC Voltage source converters. (a) Two-levels topology. (b) Three-levels topology.

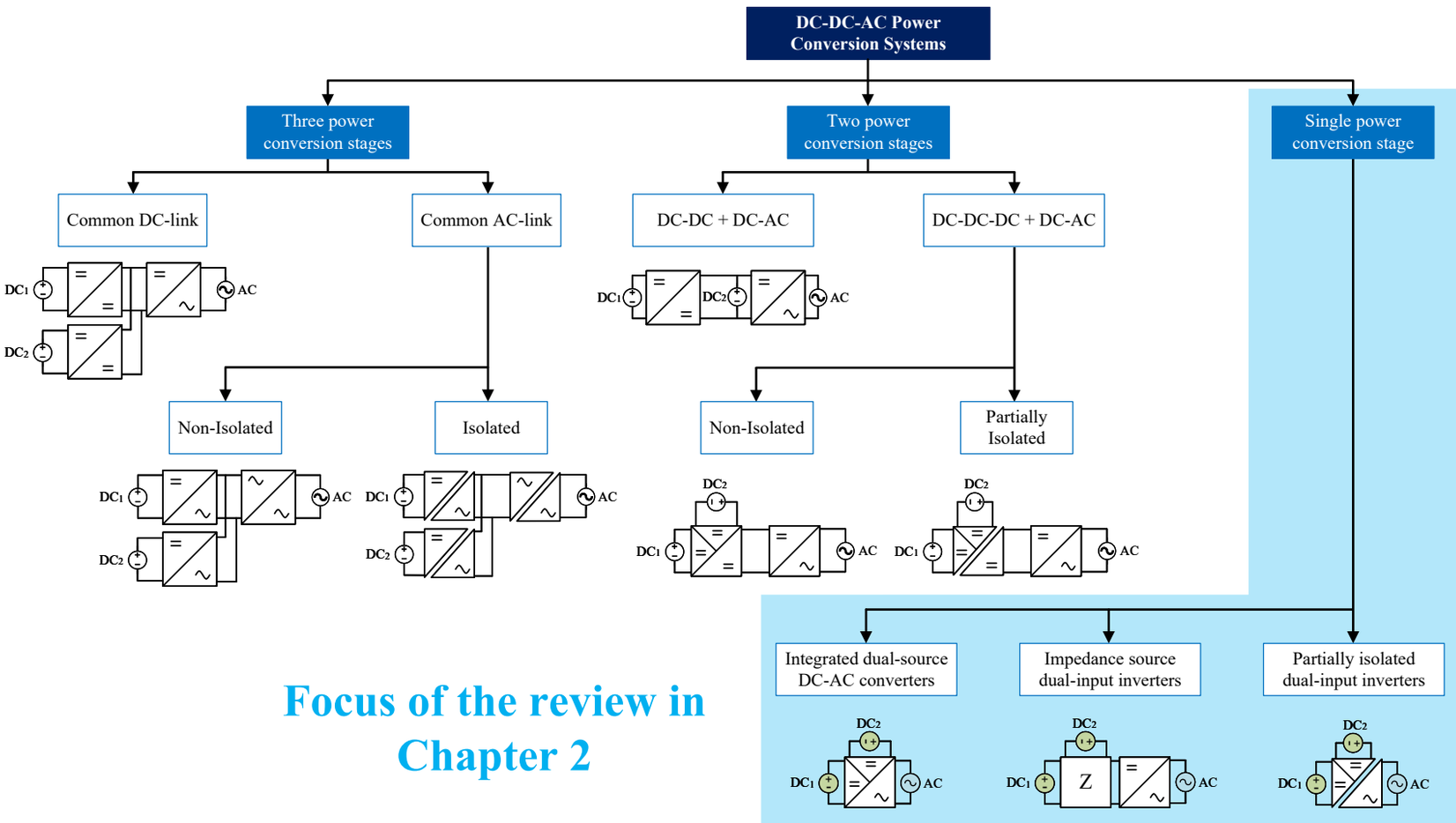


FIGURE 1.6. Classification of DC-DC-AC Power Conversion Systems.

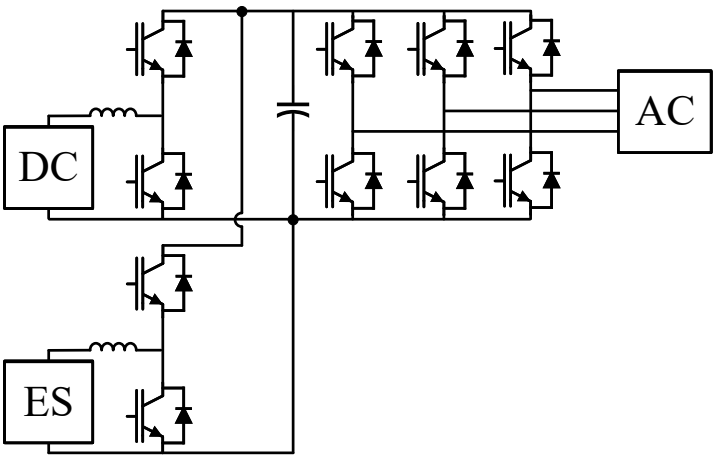


FIGURE 1.7. Example of a three power conversion stages system with common DC-link.

A. Three power conversion stages: Common DC link

The most straightforward solution to connect the three elements is to use one power converter interfacing each element. These solutions are used today in commercially available systems as they are based on well-known DC-AC and DC-DC topologies. Then, this category covers solutions using three power converters connected in a common DC link, therefore they contain two DC-DC converters plus a DC-AC one (F. Liu et al., 2014; Locment et al., 2012; Moré et al., 2015; Saxena et al., 2018; K. Sun et al., 2011; Thang et al., 2015; Thounthong et al., 2009). Fig. 1.7 shows an example of this approach, using two bidirectional buck-boost converters connecting the DC ports to the DC link where a classical two-levels DC-AC converter is attached. Depending on the application, DC-DC converters can be simplified to be unidirectional and DC-AC converters can be extended to a three-levels implementation.

The solution with three PCS allows controlling independently the currents flowing through each port, always considering the overall power balance of the system. Therefore, each converter is regulated by a separate single-variable control loop, which simplifies the implementation as it enables the use of classical control schemes. The main drawback of this solution is that connecting converters in cascade generates cumulative losses that reduce the overall efficiency of the system (A. K. Bhattacharjee et al., 2019). Furthermore,

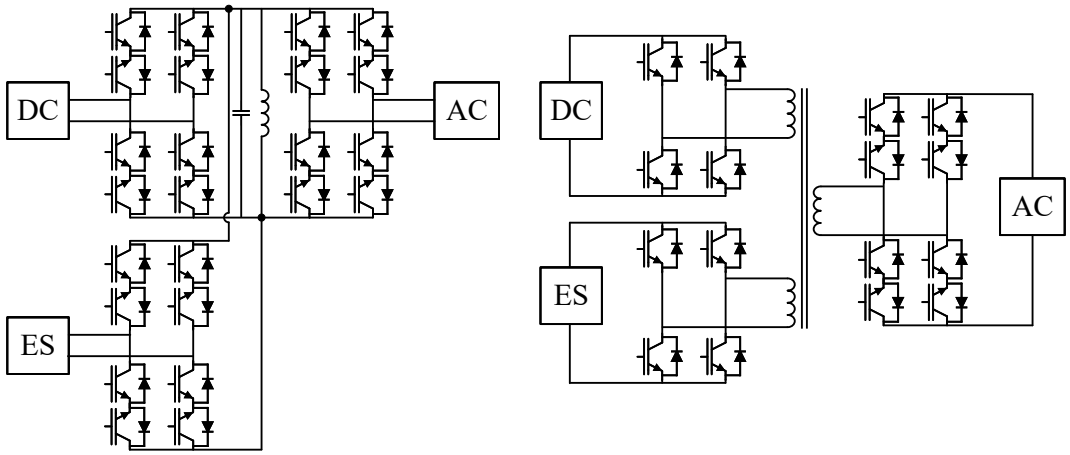


FIGURE 1.8. Examples of a three power conversion stages system with common AC-link. (a) Non-Isolated. (b) Isolated.

the use of multiple converters increases the components count and consequently the overall cost and failure probability grow.

B. Three power conversion stages: Common AC link

The common DC link is the dominant group in the category of solutions using three PCS, however, the need for a bulky electrolytic capacitor at the point of connection has motivated the research on using an AC link instead. Electrolytic capacitors can reduce the reliability of the solution, as they are very sensitive to temperature changes that can highly reduce their lifetime (Amirabadi et al., 2014). Thus, the use of an AC link appears as an alternative solution for eliminating the need for capacitors, aiming to improve the reliability of the system. The AC link requires the use of Current Source Converters (CSC) instead of VSC, as the element storing energy in the link is now an inductor replacing the capacitor. Consequently, the solutions in this category include two DC-AC converters plus an AC-AC converter (Amirabadi et al., 2013; Bilakanti et al., 2017; Haque et al., 2017).

Fig. 1.8 shows examples of the implementation of common AC link solutions for both non-isolated and isolated cases. The non-isolated case uses three CSC and it regulates the power flow by changing the time that every port charges or discharges the inductor.

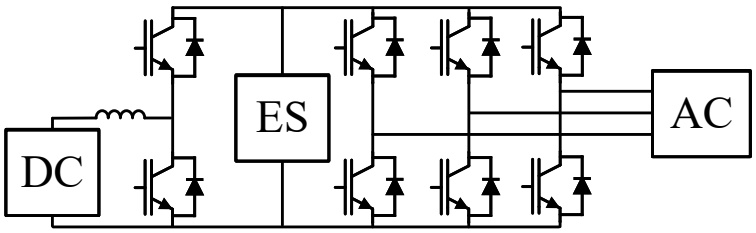


FIGURE 1.9. Example of a two power conversion stages system with DC-DC + DC-AC converters.

The frequency of charging/discharging is several orders higher than the one at the AC port. Additionally, a small capacitor is included in the link to allow resonance periods that enable the zero voltage turn-on of the switches. The isolated case replaces the inductor with a high-frequency three-winding transformer and operates in a similar manner to the non-isolated alternative. The main advantage of these solutions is a reduction in size and possible increment in efficiency by using a high-frequency AC link with soft-switching techniques. However, the control becomes more complex, as the soft-switching techniques impose restrictions to be met the same time of regulating the power through each port. Additionally, the number of active semiconductors escalates as bidirectional switches are needed for implementing the CSC.

C. Two power conversion stages: DC-DC + DC-AC

There are applications where the accurate control of the current at one of the DC ports is not highly relevant, for example when capacitors or super-capacitors are used o interface a DC source with the DC-AC converter. Relevant applications include ripple mitigation for PV systems and using of supercapacitors or batteries as secondary energy sources. Then, one of the DC-DC converters in the three PCS common DC-link implementations can be avoided, leading to a topology as the one shown in Fig. 1.9 (Dong, Cvetkovic, et al., 2013; Dong, Luo, et al., 2013; Gautam et al., 2020; Gautam et al., 2018; B. Liu et al., 2018; L. Zhang et al., 2015).

This group presents the same advantages as the common DC-link category, as it also allows using well-known topologies for the connection of the three ports. Moreover, the elimination of one DC-DC converter leads to a reduction in the required components, thus

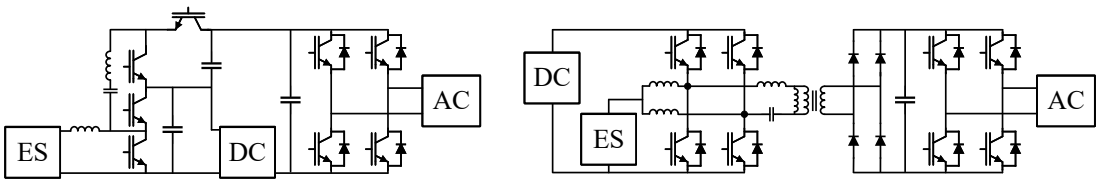


FIGURE 1.10. Examples of a two power conversion stages system with DC-DC-DC + DC-AC converters. (a) Non-Isolated. (b) Partially-Isolated.

improving the efficiency and overall cost of the solution. The control is implemented with two independent loops regulating the currents at the AC side and one of the DC ports connecting an element that could be affected by transient and oscillatory behaviours as a fuel cell or a PV array. The second DC element (namely ES in the Figures) is regulated by the overall power balance of the system, but the current can contain harmonics and/or transient spikes. Therefore, usually this element would be a capacitive element or a battery able to withstand this performance.

D. Two power conversion stages: DC-DC-DC + DC-AC

Multi-port converters have emerged as an attractive alternative to replace multiple PCS and therefore improve the efficiency and power density of the power electronics needed to integrate different renewable energy technologies. In this context, three-port DC-DC-DC converters appear as a suitable solution to connect elements such as PV arrays, batteries and fuel cells with loads in a compact manner. N. Zhang et al. (2016) and A. K. Bhattacharjee et al. (2019) present throughout studies, indicating how these converters can optimise the integration of ESS with variable renewable resources or the operation of Hybrid ESS. Therefore, these DC-DC-DC converters also represent a viable solution when complemented with DC-AC converters to connect two DC elements with the grid or an AC load.

Fig. 1.10 illustrate two examples of topologies in this group for non-isolated and partially-isolated sub-categories. Non-isolated solutions implement the DC-DC-DC converter using a combination of Buck/Buck-Boost/Boost cells in series, cascaded or stacked

configurations to perform the power flow between the three ports (Chien et al., 2014; Moradisizkoohi, Elsayad, & Mohammed, 2019; Moradisizkoohi, Elsayad, Shojaie, et al., 2019). Then, a conventional DC-AC converter interfaces the AC port, controlling the power flow from the DC sources. Partially-isolated configurations use a high-frequency link to connect with the load, similar to the AC-link isolated solutions. However, in this group, the two DC ports are connected through a single stage to the load side by merging a boost converter with a phase-shifted full-bridge (Deng et al., 2019; Lu et al., 2019; X. Sun et al., 2015; K. Wang et al., 2019; J. Zhang et al., 2015). The secondary side considers a rectifier interfacing with the DC-AC converter at the DC link.

Both sub-categories present a similar control scheme with two specific loops regulating the operation of each PCS. The first controller regulates the currents in the three-port DC-DC converter, using the duty cycle and the phase-shift variables to set the currents of the two DC sources. Then, the second controller regulates the DC-AC converter to achieve the power balance of the entire system. Analysis from A. K. Bhattacharjee et al. (2019) indicates that non-isolated solutions work better for lower power ($\leq$ 600 W), while isolated topologies are more suitable for powers above 600 W.

E. Single power conversion stage: DC-DC-AC converters

Following the same motivation behind the development of multi-port DC-DC-DC converters, single-stage DC-DC-AC power converters have been proposed by researchers during the last decade, looking to further optimise the PCS interfacing the three ports. These topologies perform the tasks of two or three separated converters, allowing the power flow control between three sources/loads with an optimised single power processing stage. The motivation behind these topologies is to reduce the required components, thus improving the efficiency and reliability of the power conversion system (Wu et al., 2017). Additionally, they can provide extra features such as embedded boost capabilities, continuous current at the dc elements or galvanic isolation with the ac port (A. K. Bhattacharjee & Batarseh, 2021; Ribeiro et al., 2010). However, they also present some limitations, such

as restricted power regulation capabilities and the need for advanced control and modulation techniques. Nevertheless, better-suited topologies for different applications can be determined, considering the mentioned limitations at the design stage. Thus, a comparative analysis of these single-stage three-port topologies is fundamental to classify them according to their features and possible applications.

The proposed converter described and analysed in Chapters 3 and 4 belongs to this group, as it allows connecting two DC ports with an AC one using the minimum amount of active semiconductors. Thus, it is especially suited for applications where energy storage needs to be embedded into the power electronics operating hybrid DC-AC systems. This group will be described in depth in Chapter 2 to further analyse the closest solutions, in terms of power density, to the proposed topology in the first part of this thesis.

1.2.2. High Power Topologies

HVDC technology using semiconductor devices has been implemented for more than 50 years, when thyristors started replacing the mercury-arc valves (Barnes et al., 2017). These devices require the existence of an AC grid to commutate and change the conduction state, therefore the HVDC converters based on thyristors are called Line-Commutated Converters (LCC). Fig. 1.11 shows a typical implementation of an LCC based on the first benchmark HVDC system defined by CIGRE (Szechtman et al., 1991). The converter operates by regulating the firing angle of the thyristors against the AC voltage. This technology is mature, covering the majority of commissioned HVDC projects around the world because of its reliability and high-power capability. However, LCCs present several disadvantages that limit their use for modern hybrid DC-AC systems: The active and reactive powers are coupled; they require a strong AC grid to operate, thus they are unable to provide grid forming capabilities; they require a large amount of filtering and reactive power compensation; and the operation difficult the implementation of multi-terminal systems, as reversing power flow requires to change the polarity of the DC voltage. Therefore, VSCs have risen as an adequate alternative to operate in high-voltage high-power systems too, as they address the limitations of LCCs. The first HVDC projects based on VSCs considered

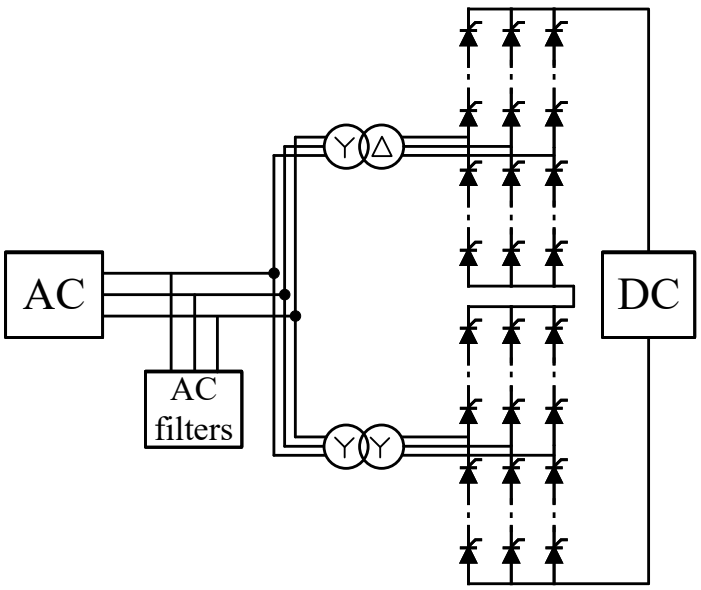


FIGURE 1.11. Example of a HVDC 12-pulse Line-Commutated Converter.

the use of conventional topologies as the ones shown in Fig. 1.5, replacing each device for large arrays of series connected devices to address the high-voltage levels. Then, the Modular Multilevel Converter (MMC) was implemented for the first time in an HVDC project in 2010 by Siemens in the Trans-Bay Cable project for a 400 MW, $\pm$ 200 kV, 85 km long HVDC line (Judge, 2016).

MMC stands out for High-Voltage Direct-Current (HVDC) applications because of its modularity, efficiency and reliability (Lesnicar & Marquardt, 2003; Saeedifard & Iravani, 2010; Tu et al., 2011). Fig. 1.12 presents the MMC circuit, consisting of six stacks of series connected half-bridge Sub-Modules (SM) together with an inductor to control the current through them. Each stack with the respective inductor conform an arm, and two arms compose a phase. The topology has been widely studied for applications described in Section 1.1.2, such as multi-terminals DC grids, off- and on-shore wind farms applications and AC grids interconnection (Debnath et al., 2015; Guan & Xu, 2012; Leon, 2018; Peralta et al., 2012; Saad et al., 2013; P. Wang et al., 2016). Furthermore, the use of MMC has enabled the increase in the power ratings of HVDC substations, with current projects built to operate above 1 GW. Thus, it is projected that the new capacity to be installed of these

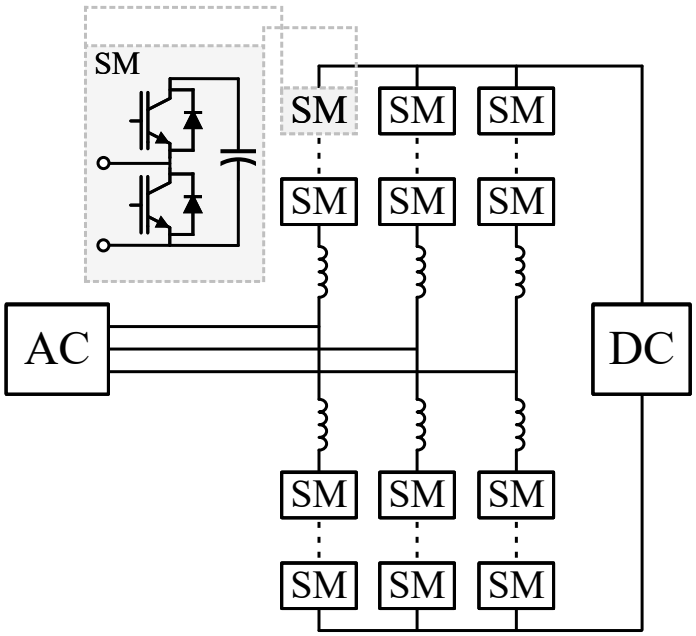


FIGURE 1.12. Modular Multilevel Converter.

systems between 2020-2028 doubles the capacity added during 2010-2019 (Nishioka et al., 2020). The latter is driving a modernisation on the requirements that the system operators ask to the MMC developers to agree with, such as the capability to provide frequency regulation and other ancillary services to strengthen the system response to contingencies.

The ability to provide additional grid services of the MMC partially depends on the amount of energy that it can use for transferring extra power to the side requiring additional regulation. The topology inherently includes energy storage as each SM contains a capacitor that holds the voltage to get to the HVDC levels. However, the average energy of an MMC falls into the range of 30-40 kJ/MVA, thus the services to provide from this source are very limited (Spallarossa et al., 2016). Therefore, integration of ESSs into MMC substations has been proposed as a feasible alternative to enable the provision of ancillary services to the grid (Errigo, Morel, et al., 2022). Accordingly, different ways to integrate ESS within the MMC have been published in the last years, considering different approaches based on the voltage, power and energy requirements. Fig. 1.13 shows the different approaches to integrate ESS into MMC substations published in the last years,

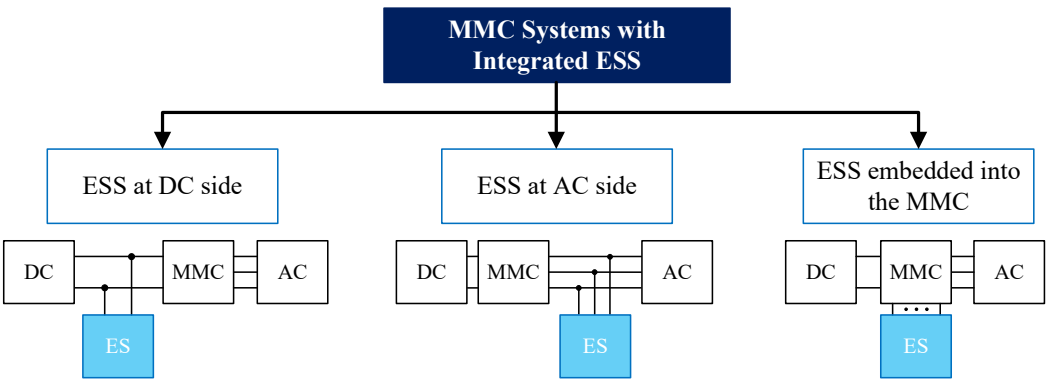


FIGURE 1.13. Classification of configurations to integrate ESS into MMC substations.

showing that three main groups can be defined based on the location of the energy storage elements.

A. ESS on DC side

The first approach is to connect the ESS on the DC side of the substation using a shunt configuration to inject or absorb current in a controlled way on that side (Díaz-González et al., 2020; Ma et al., 2021; Mukherjee & Strickland, 2015; S. Wang et al., 2022). This is the simplest approach from the controlling point of view, as it allows to regulate directly the power exchanged between the ESS with the substation. The connection is performed using a cascaded array of sub-modules including energy storage units (ES-SM), following the same principle behind the MMC topology to address the high-voltage levels. Fig. 1.14 shows the topology for this configuration, showing that the ESS is an independent converter from the MMC and has to connect to full DC voltage. The ES-SMs consist of a DC-DC converter connected to the regular SM to interface the energy storage units, thus allowing the decoupling of the ES units voltage to the HVDC level. S. Wang et al. (2022) concludes that this implementation shows the most cost-effective solution for integrating ESS into MMC substations. However, this implementation only ensures the provision of grid services to the DC side of the substation, as the MMC should be overrated if the extra power from the ESS has to be transferred on top of the nominal power to the AC side.

B. ESS on AC side

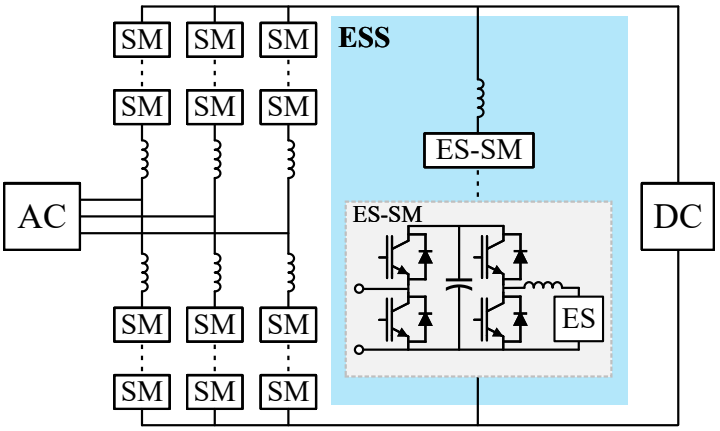


FIGURE 1.14. MMC substation with ESS on the DC side.

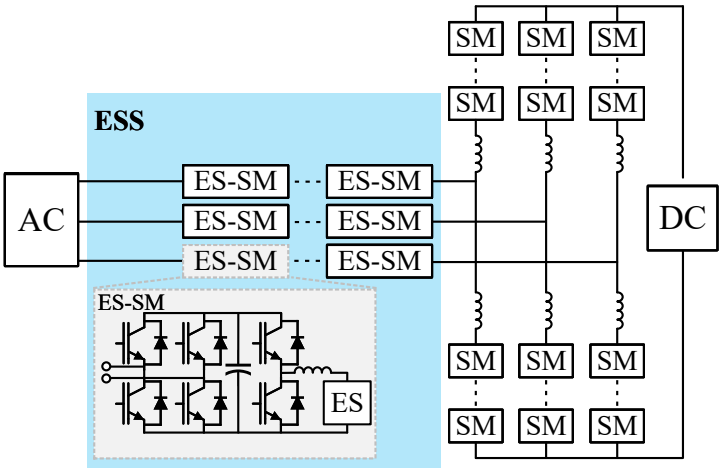


FIGURE 1.15. MMC substation with ESS on the AC side.

The second group also connects the ESS outside the MMC, but on the AC side using a series connection to sink or source power on that side when required (S. Wang et al., 2020; S. Wang et al., 2021). The ESS consists of a series connected array of full-bridge SM including energy storage units interfaced through a DC-DC conversion stage, as shown in Fig. 1.15. The ESS converter generates an AC voltage to control the amount of power to be exchanged with the grid, and it could be controlled separately from the MMC in the same way as the DC-side connected version. Additionally, the topology includes a set of anti-parallel connected thyristors in parallel to the ES-SMs, allowing to bypass the ESS converter when not in use. This configuration is proposed to block grid faults, and

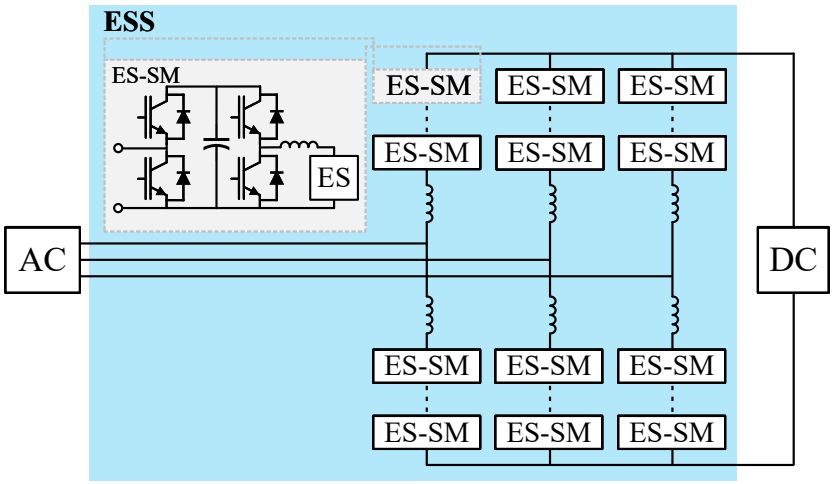


FIGURE 1.16. MMC substation with embedded ESS.

therefore the ESS converter should be able to withstand the full AC voltage. Consequently, the implementation on the AC side uses more devices than the one on the DC side, as the ESS is implemented in the three phases and it requires full-bridge SM instead of half-bridge ones.

C. ESS embedded into the MMC

The first two groups implement the ESS separated from the MMC complementing its operation, but without taking advantage of the topology itself. A different approach is to embed the ES units locally into the MMC SMs, exploiting the modularity and scalability of the topology instead of adding additional modular converters either on the DC or AC sides. This configuration considers the replacement of the MMC SMs by ES-SMs (see Fig. 1.16), using either supercapacitors or batteries depending on the energy and power requirements (Chaudhary et al., 2020; Errigo, Morel, et al., 2022; Hillers et al., 2015; Novakovic & Nasiri, 2017; Pinto et al., 2021; Soong & Lehn, 2014; Vasiladiotis & Rufer, 2015; Xu et al., 2022; Zeng et al., 2022; L. Zhang et al., 2019). This solution allows to enhance the DC-AC conversion by decoupling the two sides using the ESS to exchange power according to the system needs. The management of the ESS is integrated with the MMC controller using new loops to regulate the current flowing from or to the ES units, Vasiladiotis and Rufer (2015) provides an example of the controller structure needed.

The MMC-ESS configuration is the most flexible, as it allows power exchange directly from the substation to both DC and AC sides. Nevertheless, ESS-related services often only require a small amount of extra power from the converter, making partially-rated ESS more suitable (Soong & Lehn, 2016). Thus, the inclusion of partially rated ES into HVDC MMC substations appear as a feasible solution to extend the system capabilities with a limited impact on the operational ratings (Blatsi et al., 2021; Errigo et al., 2019; Errigo, De Oliveira Porto, et al., 2022; Henke & Bakran, 2016; Judge & Green, 2019; Neira et al., 2021; Zeng et al., 2019). A promising approach is the partial insertion of ES units into a subset of SMs, leading to an hybrid topology with both SMs and ES-SMs (Errigo et al., 2019; Errigo, De Oliveira Porto, et al., 2022; Henke & Bakran, 2016; Judge & Green, 2019; Zeng et al., 2019). This allows for reducing the number of DC-DC interfaces required and therefore the overall costs and power losses can be reduced. The ES-SMs can be unevenly distributed in the converter and the energy balance is performed using circulating currents. The number of required ES-SM depends on the additional service to be provided, results from (Judge & Green, 2019) indicate that a 0.1 p.u. increase in the MMC power is achieved using only 4% of ES-SM over all SMs. Therefore, this solution can enhance the operation of MMC substations, enabling the delivery of services from frequency regulation to load levelling and fault ride-through.

The main drawback of the implementation of ESS into MMC SMs (either full or partially-rated cases) is that the topology of the classic SM is modified. Thus, the stacks are modified and then current substations designs need to be modified to implement this solution. Therefore, an alternative configuration to include partially rated ESS into MMC substations is presented and analysed in Chapters 6-8.

1.3. Original Contributions and Layout of the Thesis

The main contribution of this thesis is the development and analysis of power converters topologies to integrate energy storage into AC-DC systems at different power rating levels. The project was developed at the Pontificia Universidad Católica de Chile (PUC) and The University of Edinburgh (UoE), following a dual-degree agreement between the

two universities. The thesis is organised in two parts: the first one describes the work developed for integrating ESS in a topology for low- and medium-power applications and; the second one presents the proposal for ESS integration in an MMC topology for high-power applications.

1.3.1. Original Contributions

The first part of the thesis (Chapters 2-5) was performed during the first half of the program at the Power and Energy Conversion Laboratory (PECLAB) of the PUC. The contribution of this first half is the proposal and development of a three-port dc-dc-ac converter using a single power processing stage. The state-of-the-art analysis presented in Chapter 2 was carried out by the author considering the available publications on three-port single-stage topologies developed to operate with ESS. The topology operation and control scheme to minimise the power conversion stages required to control the power flow between three ports (Chapter 3) are solely the work of the author. The idea of using coupled inductors to reduce the current load of the devices in the three-port converter (Chapter 4) is based on similar applications in the literature, which are cited in the relevant sections. The work supporting these chapters was performed under the supervision and advice of Dr. Javier Pereda.

The second part of the thesis (Chapter 6-8) was carried out within the Power Electronics Group at UoE. The main contribution of these sections is the development of a new MMC topology integrating partially rated ESS to extend the capabilities of providing additional services in the dc-ac power conversion. The topology and control scheme definition defined in Chapter 5 were performed collaboratively with Zoe Blatsi, Dr. Michael Merlin and Dr. Paul Judge. The power capability study, together with the losses analysis shown in Chapter 7 are solely work of the author under the supervision and advice of Dr. Michael Merlin. Finally, the experimental prototype used to test the proposal at laboratory scale described in Chapter 8 was developed jointly with Zoe Blatsi, with valuable advice from Dr. Michael Merlin, Dr. Paul Judge and Prof. Stephen Finney.

1.3.2. Thesis Objectives

The principal objective of this thesis is to design power converter topologies with the capability of integrating energy storage units into hybrid dc-ac systems. The proposed topologies consider the inclusion of energy storage in the design stage, aiming to minimise the required power processing stages and to improve overall operation.

The specific objectives are:

- To examine the existent single-stage three-port DC-DC-AC topologies in order to group them based on their operating principle to minimise power processing stages.
- To analyse the performance of the proposed single-stage three-port DC-DC-AC topology for low- and medium-power applications based on simulations and experimental results.
- To analyse the performance of the proposed MMC topology with integrated partially-rated energy storage for high-power applications.
- To design multi-variable modelling and control methods to regulate in an optimal manner the operation of the proposed topologies.

1.3.3. Hypotheses

The hypotheses formulation is in relation to the inclusion of ESS in the design of power converters. Thus, three main research hypotheses are defined:

- Multi-variable modelling and control algorithms exploit all the degrees of freedom of certain topologies, minimizing the power conversion stages of DC-AC systems with integrated energy storage.
- The proposed single-stage three-port DC-DC-AC converter with embedded energy storage manages the power flow between ports in a similar or better way than multi-stage solutions, in terms of efficiency, number of components and power density.

- The proposed design for an MMC topology with integrated energy storage extends the capabilities of the converter, keeping the ratings of the components in the original design.

1.3.4. Thesis Structure

The thesis is structured in two parts defined by the topologies developed to integrate ESS into power converters. The first part focuses on a proposed power converter for integrating ESS into low- and medium-power systems, while the second part is related to a developed MMC variant topology embedding ESS into HVDC substations. Thus, the first part is structured as follows:

Chapter 2 presents a comprehensive analysis of three-port single-stage DC-DC-AC solutions to contextualize the features of the proposed converter for low- and medium-power applications presented in the following chapters.

Chapter 3 introduces a proposed three-port dc-dc-ac converter with a single power processing stage to integrate ESS into DC-AC systems. The topology minimises the active components required to control the power flow between the three ports. A mathematical model is described to analyse the operation and control requirements of the proposal. Finally, the operation is validated with simulation and experimental results.

Chapter 4 investigates the use of coupled inductors as the interface for the second dc port of the three-port converter presented in the previous chapter. This variant allows for reducing the circulating currents of the converter, and therefore it aims to improve efficiency. Mathematical analysis is displayed to describe the advantages of the use of coupled inductors for the proposed converter.

Then, Chapter 5 presents simulation and experimental results for the proposed three-port topology to validate its operation under different scenarios. Additionally, an assessment of the results is included to provide a comparative analysis to the state-of-the-art three-port single-stage solutions presented in Chapter 2.

The second part is organised as follows:

Chapter 6 introduces the topology of an MMC with integrated partially-rated energy storage, enabling the provision of additional services to the dc-ac power conversion. The operation principle is explained, including the mathematical modelling and a comprehensive description of the requirements for the different parts of the topology.

Chapter 7 presents a design study for the presented topology including the proposal of a control method maximising the extra power to be delivered by the ESS while keeping the devices of the original MMC design. Moreover, an analysis of the power capability and power losses associated with the inclusion of extra ESS power is described to assess the operation of the proposed topology. Finally, simulation results for a conventional 1 GW MMC substation are displayed to validate the performance of the proposal.

Chapter 8 presents an experimental validation for the proposed topology, using a laboratory-scale prototype developed during the PhD project. The sections describe the converter specifications and structure to perform the tests. Finally, results are shown to validate the implementation of the topology and the control algorithm to manage the operation of the dc-ac system with augmented ESS capabilities.

PART I: CONVERTER PROPOSAL FOR INTEGRATING ESS INTO LOW- AND MEDIUM-VOLTAGE SYSTEMS

2. REVIEW OF SINGLE-STAGE THREE-PORT DC-DC-AC CONVERTERS

Hybrid power systems integrating renewable energy sources (RES), energy storage systems (ESS) and ac grids/loads have risen rapidly in the later years. In this context, systems with two dc elements connected to an ac port have become relevant because of their multiple applications, such as photovoltaic systems with integrated ES and hybrid EV powertrains (Batarseh & Alluhaybi, 2020; Ehsani et al., 2021). Therefore, there is a growing interest in developing multi-functional three-port power conversion systems with high-power density and efficiency (A. K. Bhattacharjee et al., 2019). Thus, single-stage three-port topologies have been proposed due to their reduction of power processing stages and required components. These topologies perform the tasks of two or three separate converters, allowing the power flow control between three sources/loads with an optimised power processing stage.

This chapter will present a technical review of the single-stage three-port dc-dc-ac converters proposed for emerging hybrid power systems. The objective is to introduce a comparative analysis between the different converters based on the topology characteristics, features, limitations and applications. The study also classifies the different topologies based on the operating principle used to minimise the power processing stages. The latter looks for standardising the existing solutions to facilitate state-of-art analysis for future proposals. The following sections present the proposed classification for the single-stage three-port dc-dc-ac converters, the relevant application cases and a comparative study considering the features of the analysed topologies.

2.1. Topologies Classification

Fig. 2.1 presents the proposed classification for the single-stage three-port dc-dc-ac topologies published in the last decade. Three major groups are defined based on the topology feature allowing the connection of the two dc ports with the ac side. This section will present a description of the proposed categories, with a focus on the topologies and operation principles.

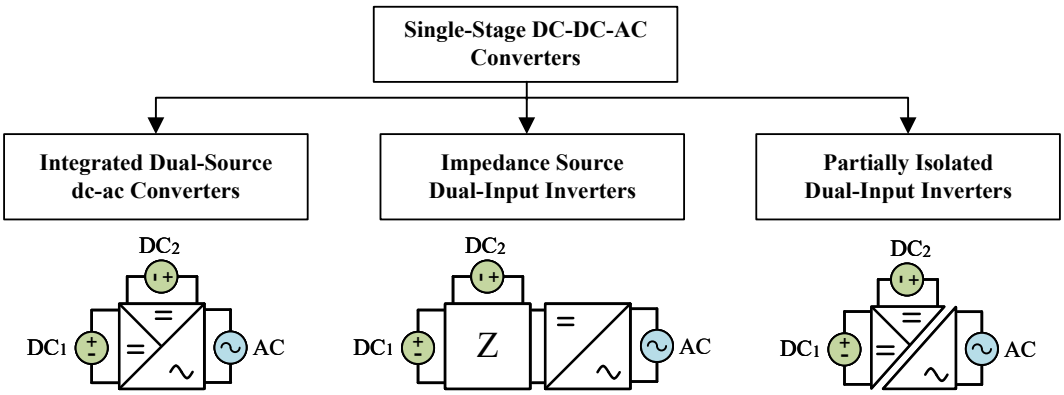


FIGURE 2.1. Classification of single-stage three-port DC-DC-AC converters.

2.1.1. Integrated dual-source dc-ac converters

The first category is called integrated dual-source dc-ac converters, it contains three-port topologies that use as a basis for a conventional DC-AC converter. Fig. 2.2 shows two example topologies for these solutions considering a single-phase case, although they also work in three-phase systems. The topologies in this category integrate a dc-dc conversion within one or more legs of the conventional dc-ac converter, thus enabling the power flow with the second dc port. The interface connecting the second dc port allows defining of the two major groups within this category: Split-source Inverters and Dual-source asymmetrical converters.

The first subcategory (Fig. 2.2(a)) corresponds to the Split-Source Inverters (SSI) (Abdelhakim et al., 2018; Abdelhakim, Mattavelli, & Spiazzi, 2017; An et al., 2019; Elthokaby et al., 2020; Hassan et al., 2020, 2021; Kan et al., 2015; Lee & Heng, 2017; Lee et al., 2019; Ribeiro et al., 2010; Yin et al., 2021), which embed a boost stage on one or more legs of the dc-ac converter. These topologies allow transferring power from a low voltage dc source DC_2 to both DC_1 and AC ports, using the legs of the converter to control two currents at the same time (L_{dc2}, L_{ac}). This is possible due to a degree of freedom (DoF) given by the switching states of the converter, as the zero states for the ac side (both upper or lower switches activated) create a different path for the current of L_{dc2}. The minimum additional components to generate this topology are one dc inductor and one diode per leg to be used

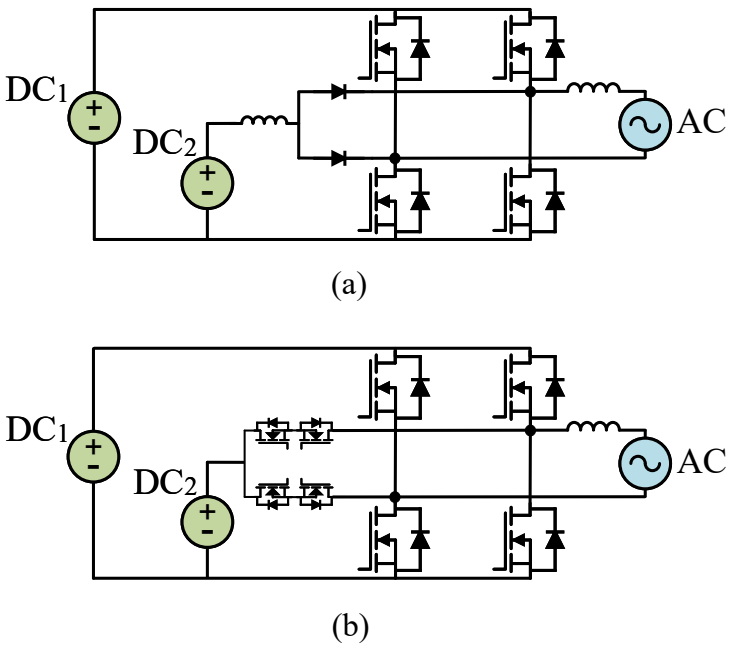


FIGURE 2.2. Integrated dual-source dc-ac converter examples. (a) Split-source inverter. (b) Dual-port asymmetrical converter.

as a DC-DC converter, thus the components count is reduced compared to a classical two-stage implementation. The use of diodes limits the power flow to be unidirectional from port DC_2, and also exposes these diodes to the fast switching of the converter legs.

Following the first publication of this topology (Ribeiro et al., 2010), several modified versions have been proposed in recent years aiming to optimise the operation of the split-source converter. Fig. 2.3 summarises the main proposals for the SSI that have been proposed for hybrid DC-AC systems. The conventional SSI (Fig. 2.3(a)) allows to connect a low voltage source at port DC_2 providing inherited boost capabilities and its operation follows the description in the previous paragraph. The voltage at $DC1$ must follow $v_{dc1}^{min} = v_{ac}^{peak} + v_{dc2}$, thus requiring a high over-dimension of the element connected on this port. The topology in Fig. 2.3(b) follows the same operational principles with reduced components and power capabilities if the active devices maintain the same current capabilities. Configuration in Fig. 2.3(c) enables the use of common-cathode diodes which are enclosed in the same package, thus reducing the parasitic inductance in the switching path

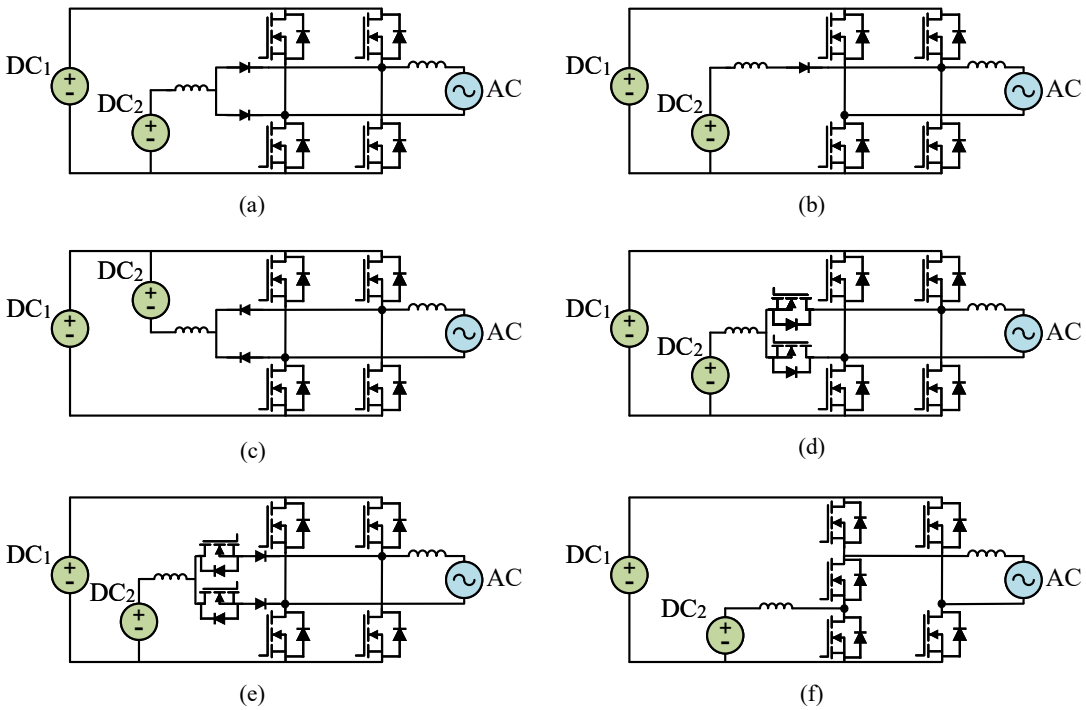


FIGURE 2.3. Split-source inverter variations. (a) Original Split-source inverter. (b) Reduced Split-source inverter. (c) Split-source inverter with common-cathode diodes. (d) Improved split-source inverter. (e) Active split-source inverter (f) Simplified split-source inverter.

where the diodes are placed. However, it requires to use a floating ground for the voltage source on DC_2, which adds complexity to the gate driver design of the active devices in the converter. The variant in Fig. 2.3(d) replaces the diodes for active devices, enabling bidirectional power flow and addressing the problem of high-frequency commutation of the diodes. Then, Fig. 2.3(e) shows a further extension that allows improving the use of the DC_1 voltage, as it reduces the minimum voltage to the level of a conventional DC-AC converter (i.e. $v_{dc1}^{min} = v_{ac}^{peak}$). This voltage reduction reduces the overall switching losses of the active devices, thus improving the efficiency of the power conversion. However, the active devices connecting DC_2 need to provide reverse blocking capabilities to avoid shoot-through of DC_1. Then, power conversion is again unidirectional for this topology. Finally, Fig. 2.3(f) shows a simplified split-source converter, reducing the extra semiconductor devices to just one and allowing the bidirectional power flow with the element on

DC_2. This version also improves the boost capabilities between the two DC ports but at expense of modifying the classic DC-AC converter configuration as it needs one phase with three switching devices instead of two.

The control of any SSI variation includes the regulation of at least two currents (DC_2 and AC ports) and optionally the voltage on DC_1 in case there is a capacitor or a PV array requiring power control on that port. Thus, the required controller for this topology needs to be designed as a multi-variable system. Two main approaches can be found in the literature: A system with linear single-variable controllers, decoupling terms and modified PWM schemes and; A system with a multi-variable controller acting directly on the switching states of the converter. The first approach (Abdelhakim, Mattavelli, Boscaino, et al., 2017) allows decoupling the control of DC and AC variables, resembling the control of conventional two-stages topologies. The second approach (Guler & Komurcugil, 2022) uses a full-state modelling to control multiple variables in a coupled way using techniques such as Model Predictive Control (MPC).

The second subcategory (Fig. 2.2(b)) consists on the Dual-Port Asymmetrical Multilevel Converters (DP-AMC) (Dorn-Gomba et al., 2018; C. Liu et al., 2019; J. Wang et al., 2020; J. Wang et al., 2021; J. Wang et al., 2019; Wu et al., 2018; Wu et al., 2017), which use modified three-level converters connecting the second dc port to the neutral point. Thus, these converters (Variants displayed in Fig. 2.4) replace the connection to the mid-point of DC_1 port with a connection to the new DC_2 element. This group also uses the DoF given by the switching states of the topologies to perform bidirectional power flow between the three ports. Furthermore, the operation is more flexible due to the increased number of states given by the additional semiconductor devices. These topologies use at least twice the number of switching devices compared to the first subcategory, but there is no need for extra passive components. The main limitation of this group is the limited power regulation capability for port DC_2, which leads to the use of an auxiliary DC-DC converter to extend this operation range. This limitation is generated by the unbalanced operation of the three-level converters and it varies with the voltage ratio between both DC ports. Literature review shows that variants of this topology require to comply with the relation

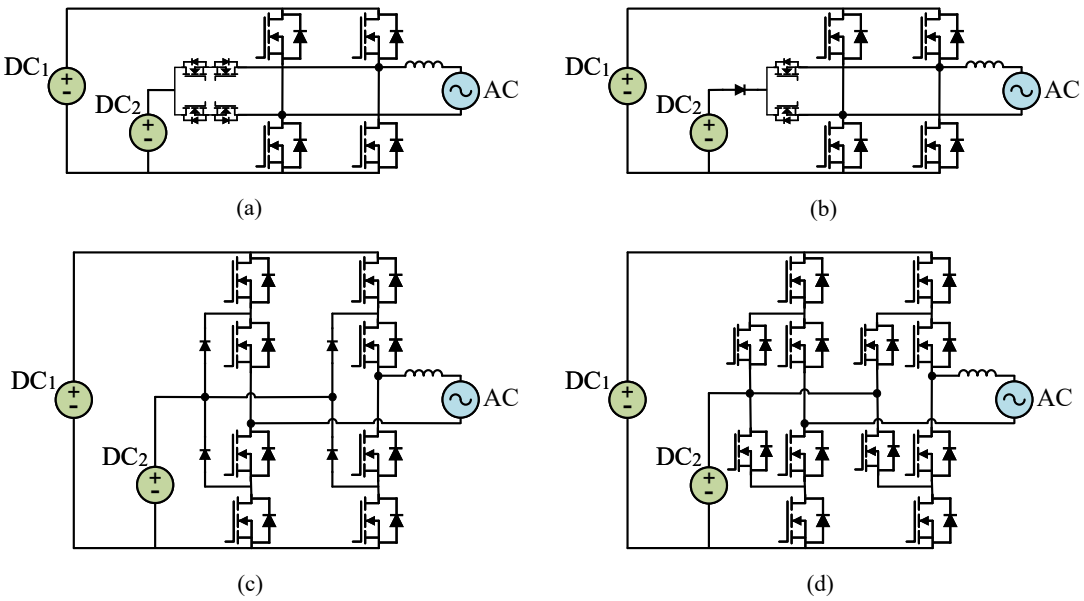


FIGURE 2.4. Dual-port asymmetrical converter variations. (a) T-Type DP-AMC. (b) Simplified T-Type DP-AMC. (c) NPC-Type DP-AMC. (d) ANPC Type DP-AMC.

$v_{dc2}^{min} = v_{ac}^{peak}$ to enable full power transfer capabilities among all three ports. Thus, the use of an auxiliary DC-DC converter between ports DC_2 and DC_1 is preferred as it allows for reducing the voltage of the second DC element improving the overall efficiency of the converter.

The reported controllers for DP-AMC variations consider the use of decoupled controllers to regulate each current (DC_2 and AC ports), considering the extended number of DoF compared to the two-level topologies used by SSI. The proposed controllers use a similar structure compared to conventional three-level DC-AC converters but include a modified PWM stage to account for the unbalance generated by the connection of DC_2. The modified PWM stage defines different operation stages depending on the relation of the voltages on the three ports, enabling the power transfer from DC_2 to the AC side just during the periods of time when $v_{dc2} \geq v_{ac}$. The latter explains the limitations on the power transfer capabilities of these converters that lead to the need for the mentioned DC-DC converter to improve the range of operation.

Table 2.1 shows the comparison of the components for different examples of the subcategories described in the present subsection. The split-source inverter shows the higher voltage boost capability for port DC_2, reaching maximum gain values of 4 to 5 (Abdelhakim et al., 2018). However, the modulation scheme should be carefully selected to minimise low-frequency ac ripple at the current of this second dc port that can be detrimental for batteries or fuel cells. Then, the DP-AMI shows the best power quality on the AC side, due to the increased number of available switching states. Additionally, the volume is reduced as there is no need for extra passive components. However, the power regulation capability is reduced at port DC_2, complicating its use with elements that require wide bidirectional power flow capabilities as batteries or supercapacitors.

TABLE 2.1. Summary for single-phase implementations of integrated dual-source dc-ac converters.

Topology	Transistors	Diodes	Inductors	Power flow
Original SSI (Ribeiro et al., 2010)	4	2	1	Unidirectional
Reduced SSI (Kan et al., 2015)	4	1	1	Unidirectional
Improved SSI (Lee & Heng, 2017)	6	0	1	Bidirectional
Active SSI (Yin et al., 2021)	6	2	1	Unidirectional
Simplified SSI (Lee et al., 2019)	5	0	1	Bidirectional
T-Type DP-AMI (J. Wang et al., 2021)	8	0	0	Bidirectional
Simplified T-Type DP-AMI (Wu et al., 2017)	6	1	0	Unidirectional
NPC DP-AMI (Dorn-Gomba et al., 2018)	8	4	0	Bidirectional

2.1.2. Impedance source dual-input inverters

The second category includes the impedance source converters modified to incorporate a second DC input on the impedance network. These topologies use one of the available capacitors in the Z- or qZ-source network to connect a DC element exchanging power with both DC input and AC output. Fig. 2.5 shows the overall structure of these converters for a single-phase configuration, which can be extended to a three-phase. These converters work by actuating on two control inputs: the modulation index of the DC-AC converter and the shoot-through ratio that allows for boosting the voltage of the dc ports. Therefore, these two DoF are used to regulate the currents at the AC and one of the DC ports, using the remaining one to address the power balance between the three elements.

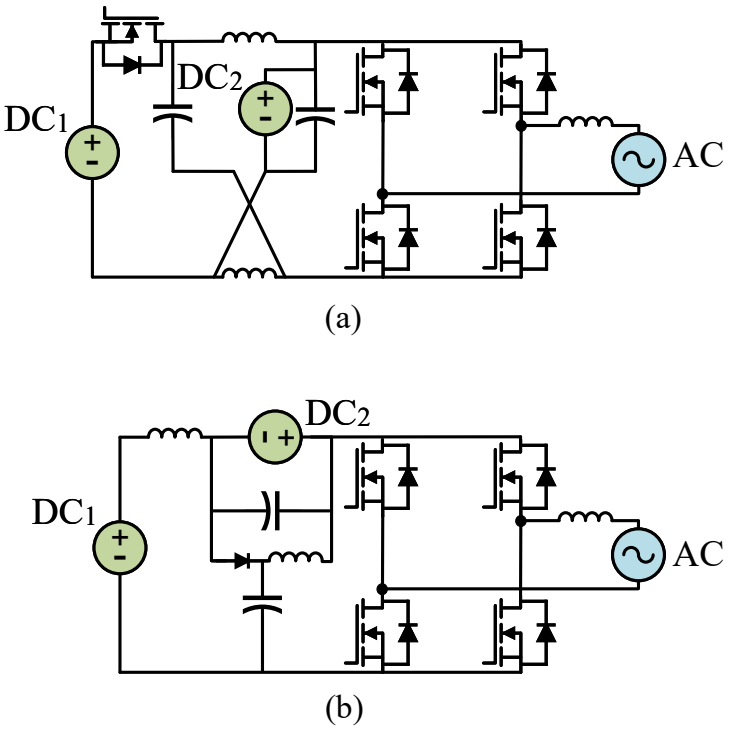


FIGURE 2.5. Impedance source dual-input inverter examples. (a) Z-source inverter. (b) qZ-source inverter.

The Z-source inverter (S. Hu et al., 2016) includes a second dc source in one of the capacitors of the impedance network, allowing bidirectional power flow between all three ports. Additionally, it can provide boost capabilities using the shoot-through state of the dc-ac converter. However, the boost ratio should be kept between 1 to 2 as higher values generate excessive losses. References (Varzaneh et al., 2021; Varzaneh et al., 2020) use two impedance networks and coupled inductors to enhance the boost capabilities, but at expense of doubling the amount of required passive elements. The main limitation of the Z-source inverters is the discontinuous current at the dc elements, which has to be addressed by large-size input capacitors.

The second type of converters in this category corresponds to the quasi-Z-source inverters, which use a modified impedance network creating a common dc rail between dc_1 and ac ports (Castiglia et al., 2020; Lashab et al., 2020; Liang et al., 2021; Liang et al.,

2018; Y. Liu et al., 2013). This topology follows the same operational principle of the Z-source, but features continuous dc currents at both ports and consequently reduces passive components sizing. The reported qZ-source converters provide limited voltage boost capabilities by using both dc ports with the impedance network to generate a higher voltage at the ac port.

Reported control systems for these converters consider the use of linear single-variable controllers regulating the currents on the DC_2 and AC ports. Each controller acts on one of the manipulated variables available, i.e. shoot-through ratio and modulation index respectively. Thus, the operation principle is similar as in the SSI controllers, as both look for using the zero-states of the DC-AC converter as the manipulated variable for regulating the current of the additional DC element.

Table 2.2 presents the comparison of the components for three examples of converters in this category. The switching devices count is kept low, as the needed DoF is given by the impedance network itself (with the shoot-through state). Voltage boost capability can be achieved with a dual impedance network, but the passive components count is significantly incremented. The qZ-source inverter shows the best operative conditions for the dc elements, and it is the most adequate choice when there is no requirement for a high-ratio voltage boost.

TABLE 2.2. Summary for three-phase implementations of impedance source dual-input dc-ac converters

Reference	Topology	Transistors	Diodes	Inductors	Capacitors
S. Hu et al., 2016	Z-source	7	0	2	2
Varzaneh et al., 2020	Z-source	7	4	2*	8
Y. Liu et al., 2013	qZ-source	6	1	2	2

**Inductors are replaced with three-winding transformers in this case.*

2.1.3. Partially isolated dual-input inverters

The last category consists of the partially isolated dual-input inverters, which feature galvanic isolation between the dc ports with the ac side (Fig. 2.6). These converters are based on microinverter topologies, as the Flyback (Alluhaybi et al., 2020; Hadi Zare et al.,

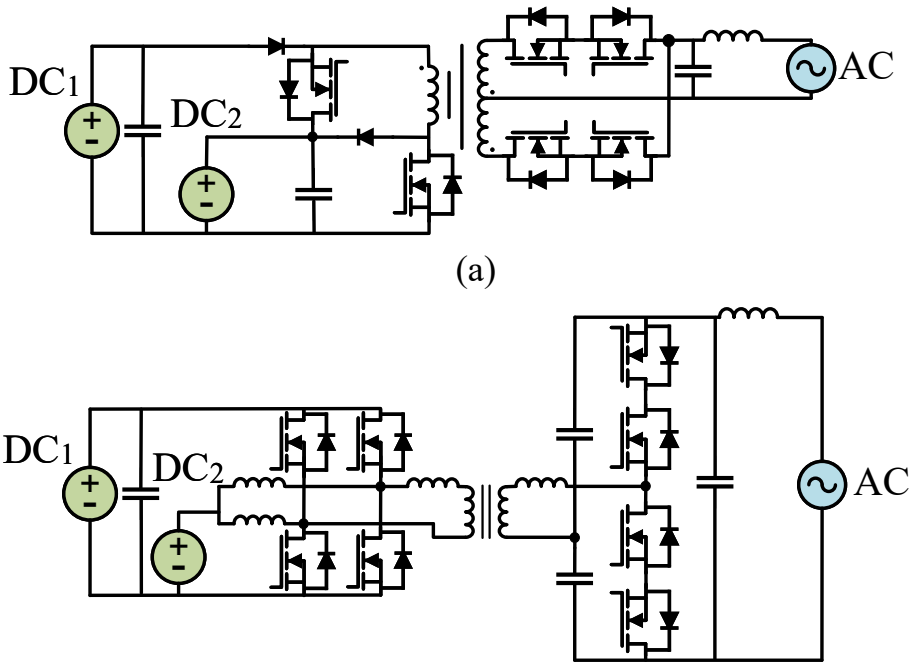


FIGURE 2.6. Partially isolated dual-input inverter examples. (a) Flyback-based TPC. (b) Dual-active Bridge-based TPC.

2017; Harb et al., 2014; H. Hu et al., 2011) and the dual active bridge (DAB) (A. K. Bhattacharjee and Batarseh, 2021; A. Bhattacharjee and Batarseh, 2020; X. Chen and Batarseh, 2021; Safayatullah et al., 2021), including an extra dc port on the primary side of the transformer. Additionally, they use a current source converter on the secondary to interface directly the high-frequency signals with the low-frequency grid. Therefore, these converters manage to connect the three ports without requiring extra unfolding or power conditioning stages. Modulation techniques as the dual-phase shift or triple-phase shift give the DOFs required to control the power flow between the elements. Furthermore, partially isolated dual-input converters have embedded voltage boost capabilities with the transformer. Also, some of them can work with soft-switching increasing the overall efficiency of the solution.

These converters have a reduced volume due to the use of a high-frequency link that decreases the sizing of the required passive components. Therefore, they are suitable for use as PV microinverters with energy storage support, enhancing the overall operation of

the system. The main limitation of this category is the elevated number of components and the complexity of the control and modulation techniques, compared to the previous categories.

2.2. Applications

Three-port dc-dc-ac converters present features that enable their use in different applications relevant for the present and future electrical system. Among these applications, the ones that can be highly benefited with single-stage conversion systems are:

- On- and off-grid hybrid PV-BES systems
- Hybrid EV powertrains
- On-grid low voltage PV or BES with embedded boost stage
- Hybrid fuel-cell BES systems
- PV green hydrogen generation

Hybrid PV-BES systems are already commercially available, and most of the solutions use power conversion systems with two or more power processing stages. Thus, the development of single-stage three-port converters can help to improve the efficiency and reliability of the system by reducing the number of components. The same principle applies to other commercially available systems, such as dual-PV systems. Additionally, single-stage three-port converters can also connect individual low-voltage elements (PVs or BES) to the grid, using the embedded boost capabilities present in some of the described topologies.

Hybrid EV powertrains are another application field that can be benefited by using single-stage three-port converters. These systems require to manage power interactions between the vehicle battery, an auxiliary dc source, such as supercapacitors or fuel cells, and the electrical machine performing the traction. Therefore, the reduction of power conversion stages can decrease the overall losses and volume of the solution, which are critical parameters in the design of such systems. Furthermore, single-stage three-port topologies

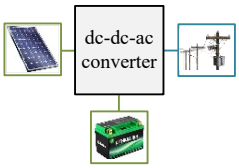
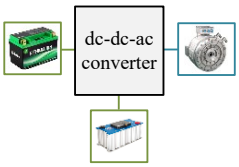
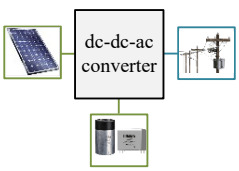
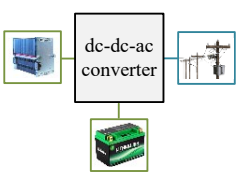
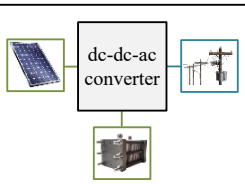
Application	Needed Features	Useful Features	Suitable Topologies
	- Bidirectional power flow at battery port. - Low-frequency ripple rejection at battery port.	- Extended power regulation capability to address variability of resource. - Boost capability to reduce serial connections PV or battery arrays.	- Bidirectional SSI & dual-port AMI. - qZ-source dual-input converter. - Partially isolated dual-input converters.
	- Bidirectional power flow for the three ports. - Low-frequency ripple rejection at battery port.	- Extended power regulation capability to address dynamic operation. - Reduced common-mode voltage variations to protect the motor.	- Z-source dual-input converter. - qZ-source dual-input converter.
	- High voltage gain.	- Extended power regulation capability to address variability of resource. - Reduced leakage currents.	- SSI. - Partially isolated dual-input converters.
	- Bidirectional power flow at battery port. - Low-frequency ripple rejection at dc ports.	- Continuous steady current at fuel-cell port. - Boost capability to connect to the ac grid.	- Bidirectional SSI & dual-port AMI. - qZ-source dual-input converter.
	- Continuous steady current at electrolyzer port. - Low-frequency ripple rejection at electrolyzer port.	- Extended power regulation capability to address variability of resource. - Boost capability to connect to the ac grid.	- Bidirectional SSI & dual-port AMI. - qZ-source dual-input converter.

FIGURE 2.7. Three-port converter applications and key features for their operation.

can also be beneficial for newer applications related to the use of hydrogen. For example, fuel-cell systems could enhance their operation by using a second dc energy storage element as a complement. Moreover, the generation of green hydrogen using PV energy is also an interesting field to explore the use of three-port topologies in an efficient and reliable manner.

Figure 2.7 showcase the listed applications that can enhance their operation using single-stage three-port topologies. The integrated dual-source converters present features,

such as bidirectional power flow and boost capabilities, that allow their use in several applications. Moreover, the reduced component count of these topologies can decrease the total volume and failure rate of the power conversion stage, generating a positive impact on applications such as hybrid PV-BES and new hydrogen applications. However, these topologies use the redundant switching states of the converter to regulate the power flow, generating oscillations in the common-mode voltage. Therefore, their use in hybrid EV powertrains should be further analysed, as these oscillations could be detrimental to electric motors. Impedance source dual-input converters also show bidirectional power flow and boost capabilities for the dc ports, with a reduced count of active devices. Additionally, common-mode voltage oscillations can be reduced through modulation techniques, enabling its use for hybrid EV powertrains. Finally, partially isolated dual-input inverters are best suited for low-power PV or hybrid PV-BES systems connected to the ac grid due to the use of high-frequency transformers. The transformer perform voltage boost and also provide galvanic isolation, maximising the impedance of the leakage current path. Furthermore, these topologies present high efficiencies as soft-switching techniques can be implemented for active devices.

2.3. Discussion

This section presents a comparative analysis based on the features of the three-port topologies previously described. The main parameters to perform the comparison are Operation principle and control system requirements, power ratings and power flow capabilities, voltage boost capabilities and quantity of active and passive components.

The operation principle of the single-stage three-port topologies is to use the available DoFs to perform the task that normally would be carried on by a second conversion stage. Thus, the three categories condense dc-dc and dc-ac conversion functionalities into an individual power converter. The first category (Integrated dual-source) uses the redundant states of a standard dc-ac converter to control a second current at a dc port in addition to the current at the ac port. Two main control schemes have been proposed in previous literature: The first scheme uses a nested loop with single-variable controllers for each current,

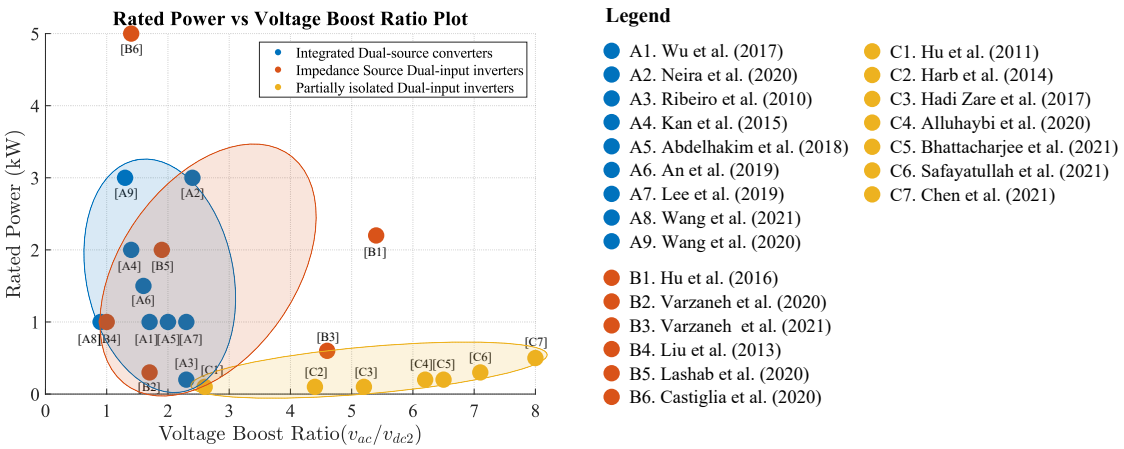


FIGURE 2.8. Rated power against voltage boost capability for DC-DC-AC converters.

together with a modified modulation scheme allowing to make use of the redundant switching states; And the second scheme uses a multi-variable controller acting directly on the switching states based on the required currents. The second category (Impedance source dual-input) uses the shoot-through state enabled by the impedance network to perform buck-boost functionality at the same time of the dc-ac conversion. Reported controllers for the topologies in this category include single-variable controllers acting on the shoot-through ratio to regulate the dc-dc conversion and on the modulation index to regulate the dc-ac power transfer. The last category (Partially isolated dual-input) uses a high-frequency link, working with the phase-shift angles to perform the dc-dc-ac power conversion. Publications for these topologies show that double- or triple-phase shift modulations can be used to regulate the power flow, using multi-variable controllers to obtain the duty cycles and phase shifts.

The power rating of the different categories is the main parameter to take into account for a comparative study, as it defines the possible applications for the different categories. Additionally, the voltage boost capability is also a key feature to analyse, as single-stage dc-dc-ac converters have been proposed to replace two-stage solutions to connect low-voltage dc sources to the ac grid. Figure 2.8 shows a plot that relates these two variables for topologies in the three defined categories. The integrated dual-source converters present a maximum boost ratio of 2.4, as for greater values the power range gets too reduced and

losses increase. The impedance source dual-input converters could reach higher voltage gains but at expense of increasing the passive components count. The plot shows that the first two categories cover a similar area of higher rated power but a limited voltage boost ratio. On the contrary, the third category presents very high voltage ratios but low power ratings due to the high-frequency isolation stage. Voltage gains up to 8.0 are reported in the literature for this category, with rated powers less than 0.5 kW.

Finally, Table 2.3 summarises the features and limitations of the defined categories using one topology as example for each of them.

TABLE 2.3. Single-stage three-port dc-dc-ac topologies comparison

Reference	Category	Topology	Features	Limitations
Ribeiro et al. (2010)	Integrated dual-source	SSI	Single-stage boost	Unidirectional power flow Low dc-link utilisation
Lee and Heng (2017)	Integrated dual-source	Improved SSI	Bidirectional power flow Reduced device count	Low dc-link utilisation
Wu et al. (2017)	Integrated dual-source	DP-AMI	Reduced passive components Reduced losses	Reduced power range
S. Hu et al. (2016)	Impedance source dual-input	Z-source	Bidirectional power flow	Reduced dc voltage range
Y. Liu et al. (2013)	Impedance source dual-input	Quasi-Z-source	Reduced active devices count Continuous dc currents	Unidirectional power flow Reduced power range
A. K. Bhattacharjee and Batarseh (2021)	Part. Isolated dual-source	DAB based	Soft-switching capabilities Galvanic isolation	Low power capability High active devices count

2.4. Chapter Conclusions

This chapter presents a categorisation for the emerging single-stage dc-dc-ac converters, defining three main groups based on the operation principle of the studied topologies. Each group uses different degrees of freedom to perform dc-dc and dc-ac power transfer simultaneously, without requiring additional power converters. The components count differs between the defined categories, as they include either passive or active components to enable the use of the required degrees of freedom. The reported converters have been proposed for low- and medium-power applications and for different voltage boost ratios between the dc ports and the ac one. Moreover, it is shown that each category covers a different range considering the rated power and voltage gain ratio. The first two categories (Integrated dual-source converters and Impedance source dual-input converters) are suitable for applications with higher power requirements and lower voltage boost needs. The remaining category (Partially isolated dual-input converters) is adequate for low-power applications with high-voltage boost requirements.

Hybrid dc-ac power systems have become an enabling technology for the integration of renewable energies and EVs to the electrical grid. Therefore, the optimisation of power conversion systems to interface multiple dc and ac elements has gained relevance in the last years. In this context, this article aims to help in the standardisation of three-port dc-dc-ac converters to facilitate the state-of-art study for new proposals. Three categories are defined and analysed considering the operation principle, rated power and components count. Firstly, Integrated dual-source converters perform the three-port power regulation by using dc-ac converter legs to perform a dc-dc conversion at the same time. These converters offer limited voltage boost capability (ratios up to 2.4) and present rated powers in the order of 1-5 kW. Thus, they are suitable for applications such as hybrid PV-BES or hydrogen fuel cells with BES systems. Secondly, Impedance source dual-input converters use a passive components network to enable the connection of the two dc ports with an ac grid or load. This category presents voltage gain ratios up to 5.4 between the dc and ac ports and it is also reported for a range of 1-5 kW in rated power. The main applications for these topologies

are hybrid energy storage systems, either connected to the grid or driving electric motors in EVs. Lastly, Partially isolated dual-input converters use a high-frequency isolated link with two dc sources at the primary and an ac port at the secondary. The converters in this category have the highest voltage gain ratios (up to 8.0), but the power is limited to less than 0.5 kW. Consequently, these converters are most suitable for PV micro-inverter operation with complementary BES.

A possible direction for future research in single-stage dc-dc-ac converters includes increasing the rated power of the topologies. Commercially available multi-stage solutions for applications such as hybrid EV powertrains, hybrid PV-BES or FC-BES systems are rated for powers from 10 to more than 100 kW. Therefore, studies should be performed to analyse the losses increment and the size of passive components required to extend the power capabilities of the single-stage three-port topologies to match the available multi-stage solutions.

3. THREE-PORT FULL-BRIDGE DC-DC-AC CONVERTER

The use of ESS in low- and medium-power DC-AC conversion systems has been widely developed in recent years due to the increasing use of applications such as grid-connected photovoltaic generation, hybrid electric vehicles, hydrogen-related energy projects and AC-DC micro-grids. Thus, different power converter topologies have been developed to manage the power flow between three ports (DC, AC and ESS) aiming to optimise the power density, efficiency and the components count. In this chapter, a fully bidirectional Three-Port Converter (TPC) connecting two DC ports with a single- or three-phase AC port is presented. The converter uses a single power processing stage as it accomplishes DC-DC and DC-AC conversions at the same time through the use of multi-variable control systems. Therefore, this converter uses the same number of semiconductors as conventional inverters and only adds a minimum amount of extra passive components to control power flow between three elements.

The chapter is organised as follows. Section 3.1 introduces the topology of the proposed converter and describes the operation to accomplish the three-port power regulation. Section 3.2 presents the multi-variable modelling method and the control scheme associated with fully exploiting the available degrees of freedom (DoF) of the topology. Then, Section 3.3 showcases design considerations for the converter based on the analysis of the previous sections. Finally, the main conclusions of the chapter are presented in Section 3.4.

3.1. Topology and Operation Principle

The proposed DC-DC-AC TPC is based on the full-bridge converter, where each leg is simultaneously used as a buck-boost converter. Therefore, this converter uses the same number of semiconductors as a conventional single- or three-phase DC-AC converter and only adds one inductor per leg to achieve an interleaved DC-DC converter, as it is shown in Fig. 3.1. Thus, the interaction between the AC port and the DC_1 port is like in a conventional full-bridge, and the interaction between the DC_2 port and the DC_1 port is like in a conventional buck-boost converter (see Fig. 3.2). The DC_2 port is decoupled from the

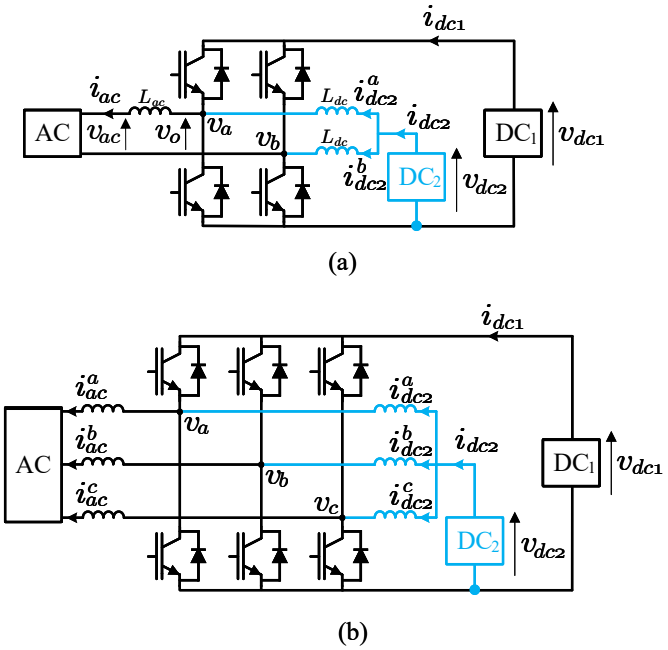


FIGURE 3.1. Topology of the proposed three-port converter. (a) Single-phase implementation. (b) Three-phase implementation.

AC side and can work with a lower voltage than the DC_1 port, which minimum value is limited by the peak AC voltage. Both DC ports could represent different types of sources or loads, such as PV modules, batteries, capacitors, fuel cells or DC micro-grids. And the AC systems could represent the grid, an AC motor or load, or an AC generator. However, the type of sources/loads will determine restrictions and specific control goals for the voltages and currents of the system.

The operation of the topology requires using an extra DoF compared to a conventional DC-AC converter, as it has to control the operation of the second DC port. Then, instead of using only the output voltage ($v_a - v_b$) as manipulated variable in a single-phase case, an internal voltage ($v_a + v_b$) is also manipulated to control the currents at all ports. Specifically, the change from one to two manipulated variables provides the capability to control i_{ac} and i_{dc2} at the same time, while i_{dc1} is used as slack to achieve power balance. The same analysis can be extended to the three-phase case, where there are two manipulated variables

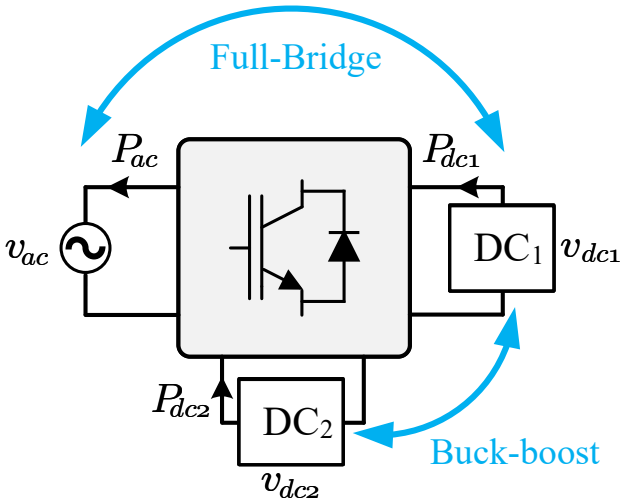


FIGURE 3.2. High-level operation of the proposed TPC.

to control the AC currents and one extra internal voltage to regulate the current of the dc_2 port.

The above-described operation principle agrees with the one for other single-stage DC-DC-AC topologies described in the previous chapter. In particular, the proposed topology fits into the Integrated Dual-Source DC-AC converters category as it embeds DC-DC capabilities in the phases of a conventional DC-AC converter.

3.2. Modelling and Control of the Converter

This section presents the dynamical modelling of the converter and a multi-variable control method to regulate the power flow between the three ports. The first part derives the expressions for the currents in the topology to be controlled with the respective voltages to be manipulated. Then the second part presents the developed control scheme to act on the available DoF simultaneously to regulate the operation of the topology.

3.2.1. Dynamical Modelling of the Topology

The currents to be controlled in the converter are defined by the inductors placed on the Ac port and the ones connecting the second DC element. Thus, (3.1) and (3.2) describe the behaviour of the regulated variables for the single-phase case considering the variables defined in Fig. 3.1.

$$\frac{di_{ac}}{dt} = \frac{1}{L_{ac}}(\overbrace{(v_a - v_b)}^{v_o} - r_{ac} \cdot i_{ac} - v_{ac}) \tag{3.1}$$

$$\frac{di_{dc2}}{dt} = \frac{1}{L_{dc}}(2v_{dc2} - (v_a + v_b) - r_{dc} \cdot i_{dc2}) \tag{3.2}$$

Expression (3.2) is obtained by adding the individual equations of the included DC inductors given in (3.3) and (3.4) and considering $i_{dc2} = i^a_{dc2} + i^b_{dc2}$.

$$\frac{di^a_{dc2}}{dt} = \frac{1}{L_{dc}}(v_{dc2} - v_a - r_{dc} \cdot i^a_{dc2}) \tag{3.3}$$

$$\frac{di^b_{dc2}}{dt} = \frac{1}{L_{dc}}(v_{dc2} - v_b - r_{dc} \cdot i^b_{dc2}) \tag{3.4}$$

Then, the dynamical equations for the three-phase implementation are obtained in the same way and shown in (3.5)-(3.8).

$$\frac{di^a_{ac}}{dt} = \frac{1}{L_{ac}}(v_a - r_{ac} \cdot i^a_{ac} - v^a_{ac}) \tag{3.5}$$

$$\frac{di^b_{ac}}{dt} = \frac{1}{L_{ac}}(v_a - r_{ac} \cdot i^b_{ac} - v^b_{ac}) \tag{3.6}$$

$$\frac{di^c_{ac}}{dt} = \frac{1}{L_{ac}}(v_a - r_{ac} \cdot i^c_{ac} - v^c_{ac}) \tag{3.7}$$

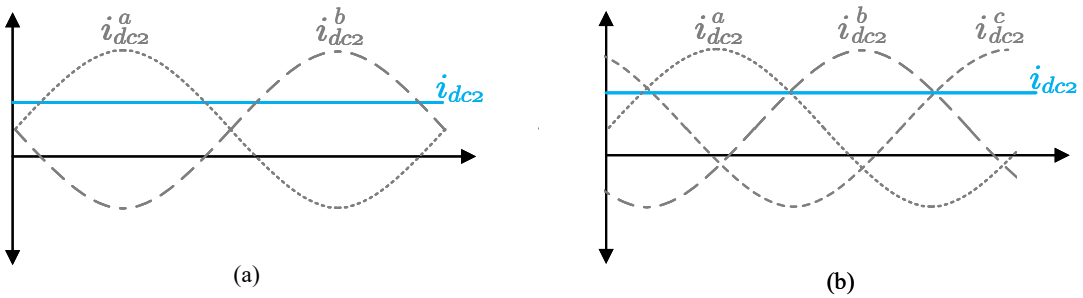


FIGURE 3.3. Current waveforms of the second DC port inductors. (a) Single-phase TPC. (b) Three-phase TPC.

$$\frac{di_{dc2}}{dt} = \frac{1}{L_{dc}}(3v_{dc2} - (v_a + v_b + v_c) - r_{dc} \cdot i_{dc2}) \tag{3.8}$$

The current i_{dc2} is generated by the sum of the currents of the DC interface inductors L_{dc}. These currents contain both DC and AC components defined by the voltage v_{dc2} and the output voltages from the converter legs. The oscillating component at the frequency of the AC port is cancelled at the dc_2 port by using $180°$ phase-shift between the inductor currents for the single-phase case and $120°$ for the three-phase, as it is shown in Fig. 3.3. Thus, each individual DC inductor faces a variable duty cycle at the fundamental AC frequency on top of the required DC component. However, the interleaved operation allows rejecting these AC components on the DC_2 port, protecting it from undesired low-frequency oscillations.

3.2.2. Multi-variable Control of the Converter

The design of the controller for the converter is based on the configuration of the elements connected on each port, this section will consider a single-phase configuration as the one shown in Fig. 3.4. Port DC_2 connects an energy storage unit, which has a lower voltage than the AC port due to the embedded boost capabilities of the converter. Then, port DC_1 can either connect a DC source as a PV array or contain just a capacitor to hold the needed voltage to connect the AC port, which can be a grid or a load as an AC motor.

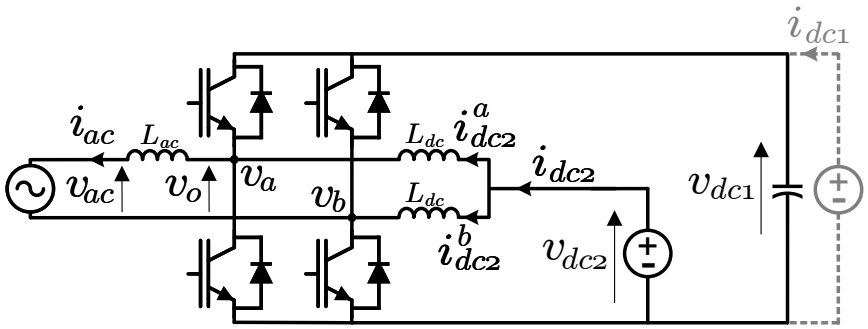


FIGURE 3.4. TPC configuration with energy storage unit on port DC_2.

Therefore, there are three variables to be controlled (i_{ac}, i_{dc2}, v_{dc1}) and two manipulated variables (v_a, v_b).

Following the review of control systems for single-stage three-port converters in Chapter 2, there are two main approaches to control a multi-variable system as the TPC in Fig. 3.4. A first approach considers the use of single-variable controllers for each current acting on individual manipulated variables to be defined. This method requires the use of decoupling terms and dynamic saturation blocks, as the maximum AC component is bounded by the voltage ratio between both DC ports. The second approach uses a full-state multi-variable controller to regulate both currents at the same time. This alternative calculates both control actions concurrently, thus allowing to take into account all restrictions in a direct manner. Hence, the second approach presents a direct way of controlling the required currents without needing of decoupling terms calculation. Consequently, a Multiple-Input Multiple-Output (MIMO) state-space approach is chosen to model and control the dynamics of the system.

The manipulated variables are defined by the output state of each leg of the converter and the voltage at DC_1 port. There are two approaches for the modelling of the legs: a switching-state model considering directly the state of the semiconductor devices; and an average model considering the use of a modulator stage. The selected modelling strategy defines the equations for the system and the appropriate control system to implement as described in the following subsections.

A. Switching-State Modelling of the Three-Port Converter

The first approach considers the switching states of the legs of the converter as the control actions to regulate the required currents. Then, this modelling approach defines the manipulated variables using the switching states of the legs of the converter (s_a, s_b) and the DC bus voltage v_{dc1} as $v_i = s_i \cdot v_{dc1}$ with $i \in \{a, b\}$. The value of the switching signals is either 1 or 0 depending on whether the upper or the lower device of the respective leg is conducting. Consequently, expressions (3.1) and (3.2) are rewritten considering the new definition for the converter voltages. This is expressed in (3.9) and (3.10).

$$\frac{di_{ac}}{dt} = \frac{1}{L_{ac}}(v_{dc1} \cdot (s_a - s_b) - r_{ac} \cdot i_{ac} - v_{ac}) \tag{3.9}$$

$$\frac{di_{dc2}}{dt} = \frac{1}{L_{dc}}(2v_{dc2} - v_{dc1} \cdot (s_a + s_b) - r_{dc} \cdot i_{dc2}) \tag{3.10}$$

Then, the dynamic behaviour of the capacitor in dc_1 is defined in (3.11) following the current directions in Fig. 3.4, where i_{dc1} is different from 0 just when there is an active power source connected to that port.

$$\frac{dv_{dc1}}{dt} = \frac{1}{C_{dc1}}(i_{dc1} + i_{ac} \cdot (s_b - s_a) + s_a \cdot i^a_{dc2} + s_b \cdot i^b_{dc2}) \tag{3.11}$$

Consequently, the model for the system is defined by (3.9)-(3.11), and it is non-linear as it presents multiplication between control inputs and state variables. This condition leads to consider the Finite Control Set Model Predictive Control (FCS-MPC) to perform the control of the converter, given its flexibility to operate systems with multi-variable and non-linear characteristics (Karamanakos and Geyer, 2020; Kouro et al., 2009; Rodriguez et al., 2013). This controller uses the model of the converter to predict the future value of the controlled variables, and then it determines the control actions using a cost function to minimise the error against defined references. Furthermore, it allows including the constraints for control actions on the optimisation problem, eliminating the need of external saturating blocks. In this case, the computation of the predicted variables is simplified

considering the reduced number of different switching states ($2^2 = 4$, as each leg has two possible states). In order to implement the controller, the model of the system needs to be converted to its discrete-time equivalent as that is the framework of the considered FCS-MPC. The discretization is performed using the forward Euler approximation in (3.12), where T_s corresponds to the sampling time period.

$$\frac{dx}{dt} \approx \frac{x(k+1) - x(k)}{T_s} \tag{3.12}$$

Then, subbing (3.12) in (3.9)-(3.11) gives the model of the converter to be used in the FCS-MPC algorithm, expressed in (3.13)-(3.15).

$$i_{ac}(k+1) = i_{ac}(k) + \frac{T_s}{L_{ac}}(v_{dc1}(k) \cdot (s_a(k) - s_b(k)) - r_{ac} \cdot i_{ac}(k) - v_{ac}(k)) \tag{3.13}$$

$$i_{dc2}(k+1) = i_{dc2}(k) + \frac{T_s}{L_{dc}}(2v_{dc2}(k) - v_{dc1}(k) \cdot (s_a(k) + s_b(k)) - r_{dc} \cdot i_{dc2}(k)) \tag{3.14}$$

$$v_{dc1}(k+1) = v_{dc1}(k) + \frac{T_s}{C_{dc1}}(i_{dc1}(k) + i_{ac}(k) \cdot (s_b(k) - s_a(k)) + s_a(k) \cdot i^a_{dc2}(k) + s_b(k) \cdot i^b_{dc2}(k)) \tag{3.15}$$

Thus, the controller generates the switching states of each leg by performing an minimization of the cost function in (3.16) with the error of the three controlled variables weighted by the factors λ_i.

$$J(k+1) = \lambda_1(i_{ac}(k+1) - i^*_{ac})^2 + \lambda_2(i_{dc2}(k+1) - i^*_{dc2})^2 + \lambda_3(v_{dc1}(k+1) - v^*_{dc1})^2 \tag{3.16}$$

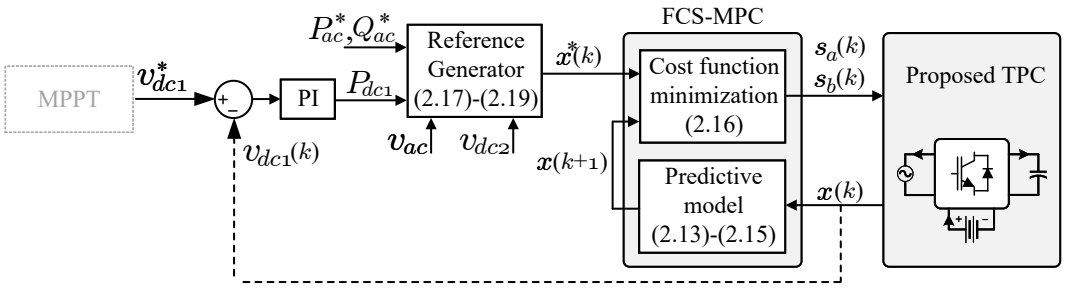


FIGURE 3.5. Control Scheme of FCS-MPC for the proposed TPC.

The overall control scheme, shown in Fig. 3.5, includes an outer PI controller and a reference generator besides the FCS-MPC. The PI controller addresses the capacitor voltage variations due to the inherent losses of the components of the converter and outputs the reference power for the port DC_1. Also, it can receive a reference from an outer block, as an MPPT if a PV array is connected at DC_1, to vary the voltage according to the energy resource conditions. The output of this outer controller is used, together with the power references at the AC side, to generate the current references for the grid and the battery ports following (3.17)-(3.19). Then, the MPC controller calculates the optimum signals s_i to drive the converter according to the calculated references. The power balance that led to (3.19) considers that the power required to keep the voltage of the capacitor (P_{dc1}) will be addressed by one of the bidirectional power sources (either the grid or the battery) when there is no active power source at DC_1.

$$i^*_{ac} = I^*_{ac} \sin(\omega t + \varphi) \tag{3.17}$$

$$I^*_{ac} = \frac{P^*_{ac}}{V_{ac} \cdot \cos(\varphi)} \quad with \quad \varphi = \arctan\left(\frac{Q^*_{ac}}{P^*_{ac}}\right) \tag{3.18}$$

$$i^*_{dc2} = \frac{P^*_{ac} - P_{dc1}}{v_{dc2}} \tag{3.19}$$

B. Average Modelling of the Three-Port Converter

This modelling technique considers the use of a modulator stage and defines the manipulated variables using an averaging approach. Therefore, the manipulated variables are defined as duty cycles for each leg (m_a, m_b), where $0 \leq m_i \leq 1$ with $i \in \{a, b\}$. Then, the corresponding duty cycles are used as input to a modulation stage that generates the switching signals (s_a, s_b) for each leg of the converter. Thus, (3.20) and (3.21) define the dynamical behaviour for the controlled variables in this case.

$$\frac{di_{ac}}{dt} = \frac{1}{L_{ac}}(v_{dc1} \cdot (m_a - m_b) - r_{ac} \cdot i_{ac} - v_{ac}) \tag{3.20}$$

$$\frac{di_{dc2}}{dt} = \frac{1}{L_{dc}}(2v_{dc2} - v_{dc1} \cdot (m_a + m_b) - r_{dc} \cdot i_{dc2}) \tag{3.21}$$

The second difference of this modelling is that the voltage on port dc_1 is considered to be regulated by the outer loop managing the power balance between the three ports. Therefore, the system can be controlled by a multi-variable linear regulator plus the inclusion of a Pulse Width Modulation (PWM) stage. This section considers the use of a Linear Quadratic Regulator (LQR) due to its dynamic response and robustness with multi-variable state-space modelled systems (Neacşu and Sîrbu, 2020). Then, (3.20) and (3.21) can be represented as a state-space model following expression (3.22).

$$\underbrace{\begin{bmatrix} \dot{i}_{ac} \\ \dot{i}_{dc2} \end{bmatrix}}_{\dot{x}} = \underbrace{\begin{bmatrix} \frac{-r_{ac}}{Lac} & 0 \\ 0 & \frac{-r_{dc}}{Ldc} \end{bmatrix}}_{A} \underbrace{\begin{bmatrix} i_{ac} \\ i_{dc2} \end{bmatrix}}_{x} + \underbrace{\begin{bmatrix} \frac{v_{dc1}}{Lac} & \frac{-v_{dc1}}{Lac} \\ \frac{-v_{dc1}}{Ldc} & \frac{-v_{dc1}}{Ldc} \end{bmatrix}}_{B} \underbrace{\begin{bmatrix} m_a \\ m_b \end{bmatrix}}_{u} + \underbrace{\begin{bmatrix} \frac{-1}{Lac} & 0 \\ 0 & \frac{2}{L_{dc}} \end{bmatrix}}_{E} \underbrace{\begin{bmatrix} v_{ac} \\ v_{dc2} \end{bmatrix}}_{u_{ext}} \tag{3.22}$$

The LQR is an optimal controller, as the FCS-MPC, however, it uses a constant feedback gain matrix K to calculate the control input as $u_{LQR} = K \cdot (x^* - x)$. This matrix is obtained by minimising the cost function in (3.23) with Q and R weighting matrices for the controlled variables and the manipulated variables change respectively.

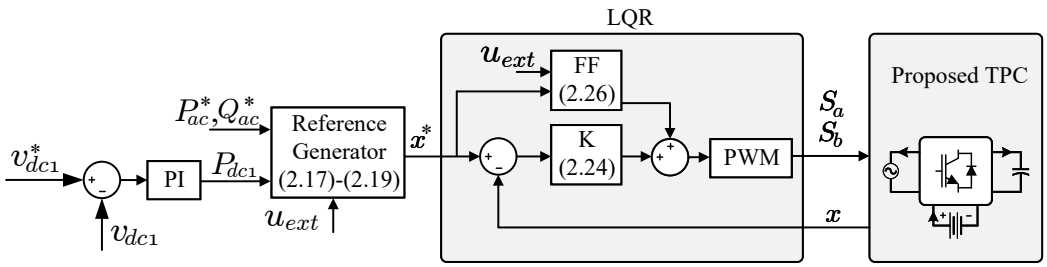


FIGURE 3.6. Control Scheme of LQR for the proposed TPC.

$$J = \int_0^\infty (x^T Q x + u^T R u) dt \tag{3.23}$$

Then, K is calculated using (3.24) where P represents the solution of the continuous Riccati equation in (3.25) (Kedjar and Al-Haddad, 2009).

$$K = R^{-1} B^T P \tag{3.24}$$

$$A^T P + PA - PBR^{-1} B^T P + Q = 0 \tag{3.25}$$

The described LQR controller works with small-signal models, then a feed-forward term must be used to address the effect of the references and the external disturbances. This is expressed in (3.26).

$$u_{ff} = B^{-1}(\dot{x^*} - A \cdot x^* - E \cdot u_{ext}) \tag{3.26}$$

Therefore the control action to modulate is calculated as in (3.27).

$$u^* = u_{LQR} + u_{ff} \tag{3.27}$$

Then, the overall control scheme (3.6) follows a similar structure to the one for the switching-state modelling, with an outer loop controlling the voltage of the dc_1 capacitor, and an inner loop regulating the currents following the same references in (3.17)-(3.19).

3.3. Design of the Converter

This section studies the voltage and current characteristics of the topology to obtain design guidelines for the three-port DC-DC-AC power conversion system. The first part analyses the voltage limits for the operation of the converter and its relation with the power flow capability between the three ports. Then, the second part investigates the current load of the devices based on the references for AC and DC ports.

3.3.1. Voltage and Power Characteristics

The design of the converter (component sizing and control scheme) depends on the systems to be connected at each port, as they could require voltage or current control and unidirectional or bidirectional power flow. Therefore, in order to characterize the topology, the rest of the subsection considers the configuration of Fig. 3.4, with a capacitor at DC_1, a battery at DC_2 and the single-phase grid at the AC side. This configuration allows to: connect a battery to the grid with a small capacitance at the DC-bus, as the battery is placed at the second DC-port which is free of low-frequency harmonics; and reduce the required series connected battery cells, as v_{dc2} can be lower than the peak voltage at the AC port. Furthermore, an additional source as a PV can be connected in parallel with the capacitor at DC_1 to use the converter in a hybrid PV-BESS application. Thus, the following analysis applies to grid-connected BESS with boost capability and hybrid PV-BESS also connected to the ac-grid.

In the proposed TPC, the voltage ratio between v_{dc2} and v_{dc1} defines the dc component of the voltages v_a and v_b generated by the legs of the converter. This bias is highly relevant as it determines the maximum peak voltage of v_o. In a regular h-bridge, the DC component for each leg is always $0.5v_{dc1}$, thus each voltage could use the entire linear range to generate the sinusoidal component. However, in the TPC topology, variations on the v_{dc2} voltage

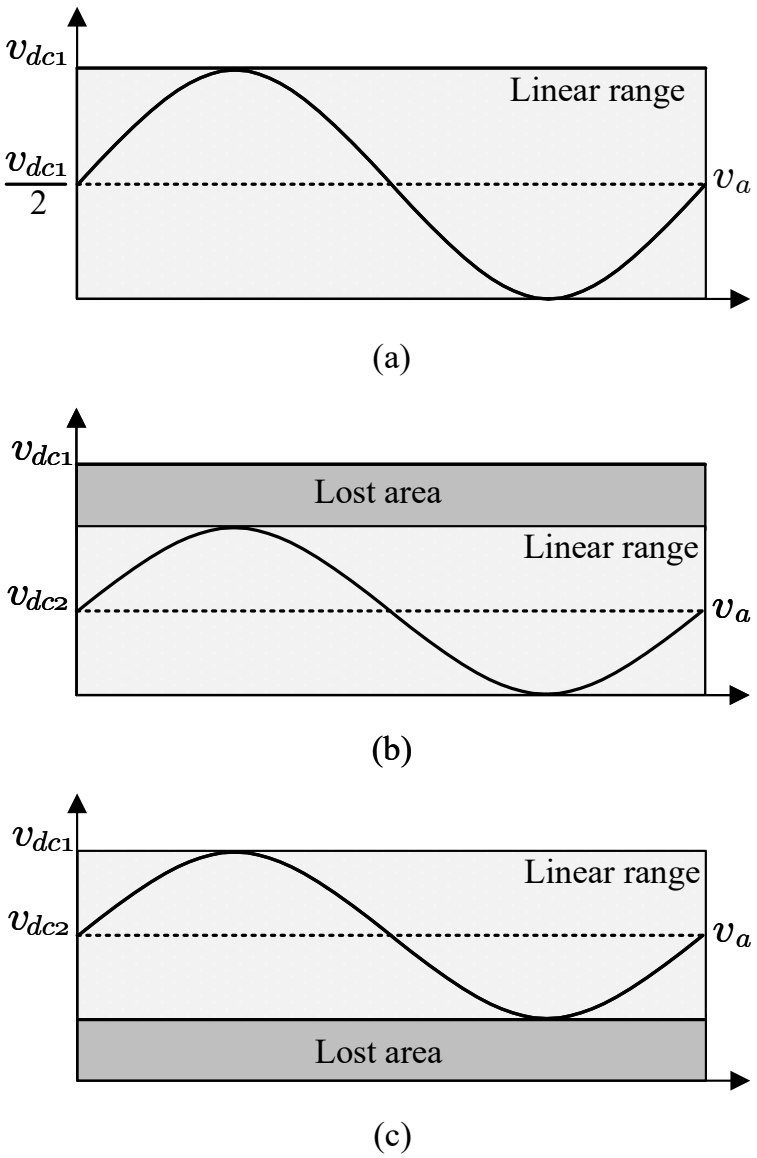


FIGURE 3.7. Operating range for leg voltages. (a) Regular h-bridge. (b) Proposed TPC with $v_{dc2} < 0.5 \cdot v_{dc1}$. (c) Proposed TPC with $v_{dc2} > 0.5 \cdot v_{dc1}$

reduce the useful linear range and hence limit the maximum output voltage, as it is shown in Fig. 3.7. Consequently, in order to use the full voltage range at the AC output, the relation between both DC voltages should be $v_{dc2} = 0.5v_{dc1}$. However, different voltage ratios and rated power can be selected according to the application. Considering the mentioned

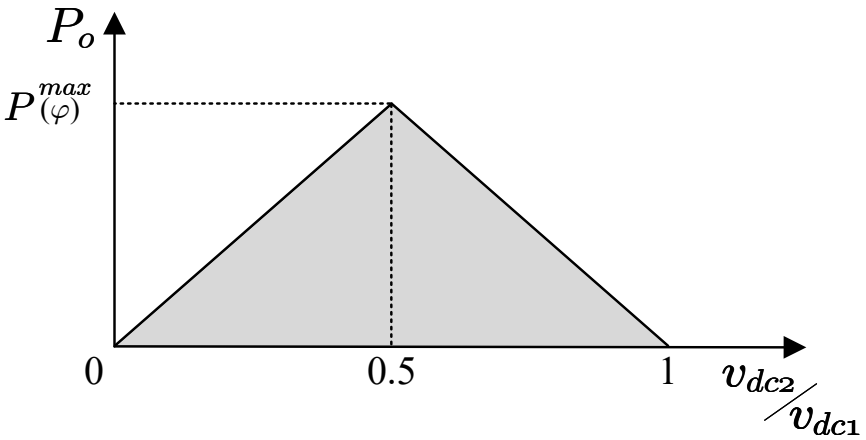


FIGURE 3.8. Output power range vs. v_{dc2}/v_{dc1} ratio

applications with a battery at dc_2, the variations on the voltage depending on the state of charge should be included in the design to determine the limits of the operating range.

The active power at the AC port is characterized by (3.28), where V_o and V_{ac} represent the magnitudes of the output and grid voltages respectively and φ is the phase angle between both voltages. The power equation is the same of a regular DC/AC converter, but the exposed limitation on the output voltage should be considered according to (3.29). Therefore, the power characteristic depends on the relation of the dc voltages and it is shown in Fig. 3.8, where φ is determined by the power factor delivered. The figure shows that the output power at the AC port is maximised when the ratio $v_{dc2}/v_{dc1} = 0.5$, which is the ratio that also allows the full utilisation of the DC_1 bus voltage.

$$P_o = \frac{V_o \cdot V_{ac}}{X_{Lac}} \sin(\varphi) \tag{3.28}$$

$$V_o^{max} = \begin{cases} 2 \cdot v_{dc2} & v_{dc2} \leq 0.5 \cdot v_{dc1} \\ 2 \cdot (v_{dc1} - v_{dc2}) & v_{dc2} > 0.5 \cdot v_{dc1} \end{cases} \tag{3.29}$$

The voltage analysis can be further extended to address the required operating conditions for a grid-connected TPC, where the AC voltage and the maximum power to be exchanged is fixed. Thus, the required voltage levels at both DC ports can be defined as a function of V_{ac} to analyse the needed dimension of these two elements. Two relations are defined in (3.30)-(3.31), following an analysis similar to the one performed for split-source inverters in (Yin et al., 2021). D_{dc} represents the DC level (ratio) and M_{ac} the amplitude of the AC component of each leg in a per unit basis.

$$V_{dc1} = \frac{V_{dc2}}{D_{dc}} \tag{3.30}$$

$$V_o = 2M_{ac}V_{dc1} = \frac{2M_{ac}}{D_{dc}}V_{dc2} \tag{3.31}$$

Then, considering Fig. 3.7 and (3.29) the maximum range for the AC component amplitude is defined in (3.32).

$$\begin{aligned} 0 \leq M_{ac} \leq D_{dc} \quad &, D_{dc} \leq 0.5 \\ 0 \leq M_{ac} \leq (1 - D_{dc}) \quad &, D_{dc} > 0.5 \end{aligned} \tag{3.32}$$

Thus, the minimum required voltages V_{dc1} and V_{dc2} for a given fixed V_o can be calculated by maximizing the modulation index M_{ac} for the entire operational range. Equation (3.32) indicate that $M_{ac}^{max} = D_{dc}$ when $D_{dc} \leq 0.5$, then replacing this maximum value in (3.31) leads to (3.33).

$$V_o = \frac{2M_{ac}^{max}}{D_{dc}}V_{dc2} = \frac{2D_{dc}}{D_{dc}}V_{dc2} = 2V_{dc2} \Rightarrow V_{dc2}^{min} = \frac{V_o}{2} \tag{3.33}$$

The last expression indicates that the minimum voltage magnitude for the source on DC_2 is half of the required voltage at the AC side V_o, considering both fixed grid voltage V_{ac} and rated power P_{rated} to deliver. It also indicates that $D_{dc} = 0.5$ leads to the best use of the DC bus voltage V_{dc1}, avoiding the over-dimension for this element.

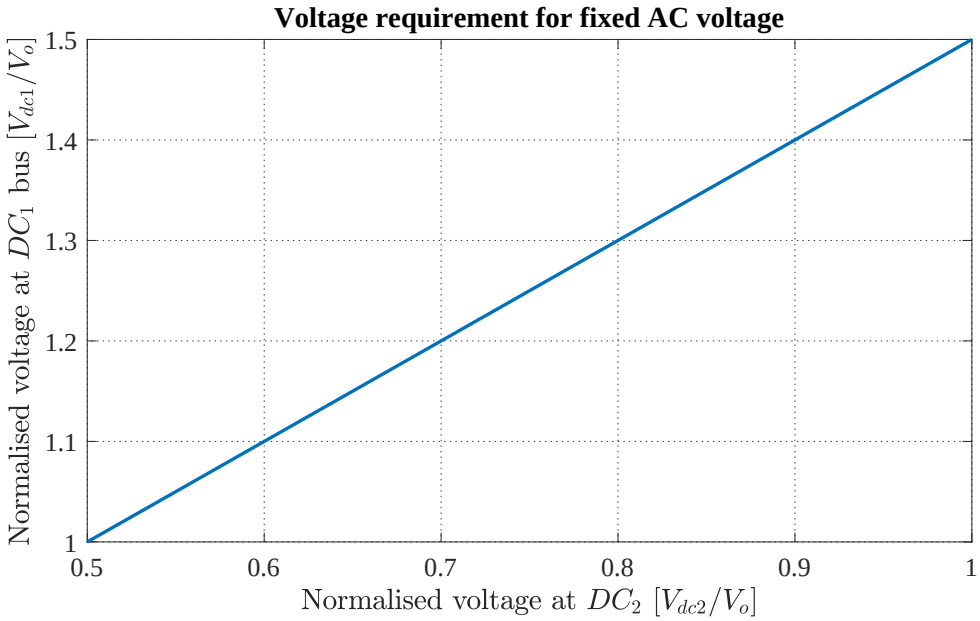


FIGURE 3.9. Voltage requirement at DC_1 bus for fixed AC voltage and varying DC_2 voltages.

Then, the maximum modulation index changes for DC ratios $D_{dc} > 0.5$, becoming $M_{ac}^{max} = (1 - D_{dc})$, which replacing again in in (3.31) leads to a different expression in (3.34).

$$V_o = \frac{2M_{ac}^{max}}{D_{dc}} V_{dc2} = \frac{2(1 - D_{dc})}{D_{dc}} V_{dc2} \Rightarrow V_{dc2} = \frac{D_{dc}}{2(1 - D_{dc})} V_o \tag{3.34}$$

Equation (3.34) can be used together with (3.30) to obtain the minimum voltage V_{dc1} needed for the converter to operate under the same conditions above described. The result is plotted in Fig. 3.9 normalised by the required output voltage V_o. The figure shows that the DC-link voltage at port DC_1 is fully used when $V_{dc2} = 0.5 \cdot Vo$, leading to the best operational conditions. Then, the requirement increases linearly with V_{dc2} to a maximum of $1.5 \cdot Vo$ when the voltage on DC_2 has the same magnitude as he required on the AC port.

3.3.2. Current Load Characteristics

The second relevant parameter for the design of the converter is the current load of the devices considering the power references for the three ports. The single-stage three-port configuration implies that the devices on the converter carry the current components for both DC-AC and DC-DC conversion stages. Then, each leg of the TPC carries a current component for the AC output, but also a component for the inductors interfacing the port DC_2. Therefore, the load characteristic of the switching devices differs from the one in a normal DC-AC converter. Thus, the currents flowing through each device are expressed in (3.35) considering the current directions in Fig. 3.4.

$$\begin{aligned} i^a_{upper} &= i_{ac} - i^a_{dc2} \qquad & i^a_{lower} &= i^a_{dc2} - i_{ac} \\ i^b_{upper} &= -i_{ac} - i^b_{dc2} \qquad & i^b_{lower} &= i^b_{dc2} + i_{ac} \end{aligned} \tag{3.35}$$

The reference for i_{ac} follows (3.17) and (3.18), while the references for i^a_{dc2} and i^b_{dc2} depends on (3.19) and the required voltages v_a and v_b to control the converter. The voltages are obtained by replacing the current references i^*_{ac} and i^*_{dc2} in (3.1) and (3.2) and neglecting the resistor losses terms of the inductors (r_{ac}, r_{dc}), leading to expressions (3.36) and (3.37).

$$(v_a - v_b)^* = V_{ac}\sin(\omega t) + \omega L_{ac} I_{ac}\cos(\omega t + \varphi) \tag{3.36}$$

$$(v_a + v_b)^* = 2v_{dc2} \tag{3.37}$$

Then, the leg voltages are displayed in (3.38), which is obtained by adding and subtracting the last equations.

$$\begin{aligned} v^*_a &= v_{dc2} + \tfrac{1}{2}(V_{ac}\sin(\omega t) + \omega L_{ac} I_{ac}\cos(\omega t + \varphi)) \\ v^*_b &= v_{dc2} - \tfrac{1}{2}(V_{ac}\sin(\omega t) + \omega L_{ac} I_{ac}\cos(\omega t + \varphi)) \end{aligned} \tag{3.38}$$

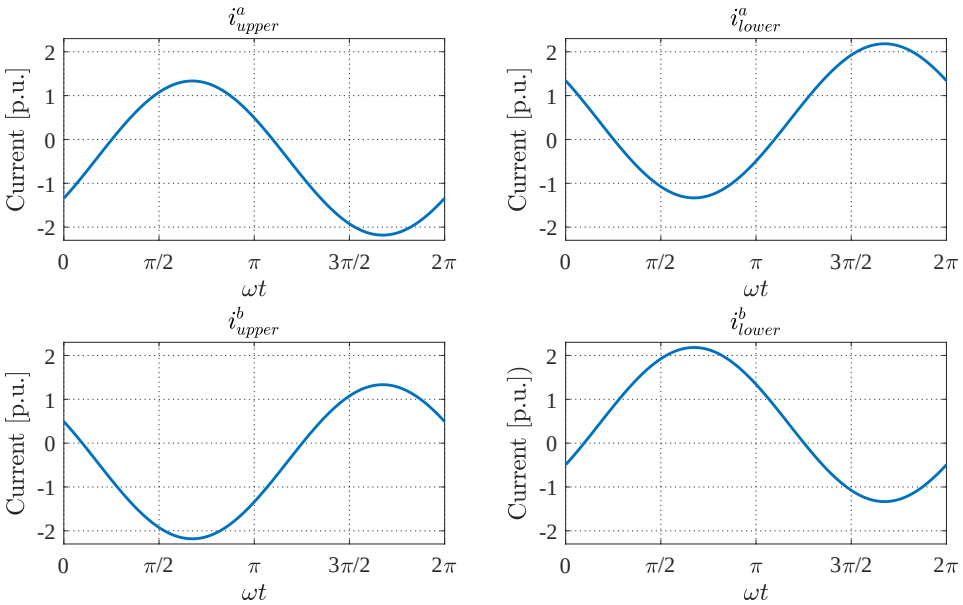


FIGURE 3.10. Current load of the TPC switching devices.

Substituting (3.38) into (3.3) and (3.4) gives (3.39) and (3.40).

$$\frac{di^{a^*}_{dc2}}{dt} = -\frac{1}{2L_{dc}}(V_{ac}\sin(\omega t) + \omega L_{ac} I_{ac}\cos(\omega t + \varphi)) \tag{3.39}$$

$$\frac{di^{b^*}_{dc2}}{dt} = \frac{1}{2L_{dc}}(V_{ac}\sin(\omega t) + \omega L_{ac} I_{ac}\cos(\omega t + \varphi)) \tag{3.40}$$

Thus, expressions for each inductor can be obtained in (3.41) and (3.42), considering an equal share of the DC component. These equations show that each inductor carries an AC current component, which magnitude is mainly determined by the voltage magnitude on the AC port V_{ac}, the angular frequency ω and the inductance value L_{dc}. These AC terms do not contribute to the power transfer and should be minimised to avoid extra losses.

Finally, Fig. 3.10 shows the current waveforms for the switching devices, following (3.35), depicting the different biases between the upper and lower devices in the same leg. The latter defines the conduction times for the transistors and anti-parallel diodes, and therefore it will define different power losses for the devices.

$$i_{dc2}^{a^*} = \frac{i_{dc2}^*}{2} + \frac{1}{2\omega L_{dc}}(V_{ac}\cos(\omega t) - \omega L_{ac} I_{ac}\sin(\omega t + \varphi)) \tag{3.41}$$

$$i_{dc2}^{b^*} = \frac{i_{dc2}^*}{2} - \frac{1}{2\omega L_{dc}}(V_{ac}\cos(\omega t) - \omega L_{ac} I_{ac}\sin(\omega t + \varphi)) \tag{3.42}$$

3.4. Chapter Conclusions

This chapter presented a fully bidirectional DC-DC-AC three-port converter to address the power control of hybrid systems with two DC and one AC port with a single power processing stage, reducing topology complexity and improving power density compared to multiple stages solutions. The topology is based on a conventional DC-AC converter and it generates a new DC port using each inverter leg as a buck-boost converter, so two or three inductors (single- or three-phase implementations) are incorporated to decouple the new DC port from the AC side. This new DC port presents two main advantages, it allows the power transfer to an AC side of higher voltage and; it is free of the low-frequency harmonics that could damage elements as batteries or be detrimental to the MPPT of PV panels, especially in single-phase power converters.

The converter operates by exploiting the degrees of freedom of the topology to concurrently control the currents (powers) on the three ports. Thus, multi-variable dynamical modelling was introduced to represent the behaviour of the converter. Furthermore, two possible control schemes were presented using a switching-state modelling approach and an average modelling including a modulation stage strategy. Both controller implementations work over the full-state representation of the system, calculating the control inputs in a coupled manner following the nature of the system.

Finally, a design study of the proposed converter was presented analysing the main variables to consider in terms of currents and voltages to support while operating. It was shown that the converter can work with variable ratios between the voltages v_{dc1} and v_{dc2}, but the maximum power output is accomplished when $v_{dc2}/v_{dc1} = 0.5$. Moreover, the converter should comply with $v_{dc2} \geq 0.5V_{ac}$ for grid-connected scenarios, to ensure the

maximum rated power at all times. Also, current load analysis for the converter showed that active devices face different currents due to new components related to the embedded DC-DC conversion. The following chapter will present a variation in the design allowing to reduce the new current components, thus improving the efficiency of the overall power conversion system.

4. COUPLED INDUCTOR THREE-PORT FULL-BRIDGE DC-DC-AC CONVERTER

The presented TPC in Chapter 3 enables the inclusion of an ES element into a DC-AC converter using a single power conversion stage. The interface to the second DC port, including an ES unit, is an array of inductors allowing the use of the DC-AC converter legs simultaneously as buck-boost converters. Although the current at port $DC2$ is purely DC, Section 3.3.2 showed that each inductor carries an AC component on top of the DC current due to the DC-AC conversion. These AC currents do not contribute to power exchange and just circulate inside the converter, increasing the current load of switching devices and inductors themselves (see Fig. 3.10). Consequently, the proposed TPC presents higher losses due to these circulating currents which increase with the AC voltage requirement. Therefore, a modified version of the topology is presented in this Section aiming to reduce the circulating currents of the converter and thus improve the overall efficiency.

The modified version of the TPC considers the use of coupled inductors in the interface of the second DC port, replacing the inductors of the base proposal. The latter allows exploiting the phase angle between the AC currents on the inductors to counteract on their magnitudes using the magnetic flux generated on each winding. Thus, the total impedance for the AC components increases, as each winding gets influenced by the current flowing on the winding (or windings) of the other (or others) phases. The rest of the chapter is organised as follows. Section 4.1 presents the topology and the theory supporting the use of coupled inductors for this application. Section 4.2 shows the mathematical modelling for the converter and the control scheme, describing its similitude with the one designed for the TPC. The design of the converter focused on the design of the coupled inductor is presented in Section 4.3. Section 4.4 concludes the chapter by stating the main findings for the presented topology.

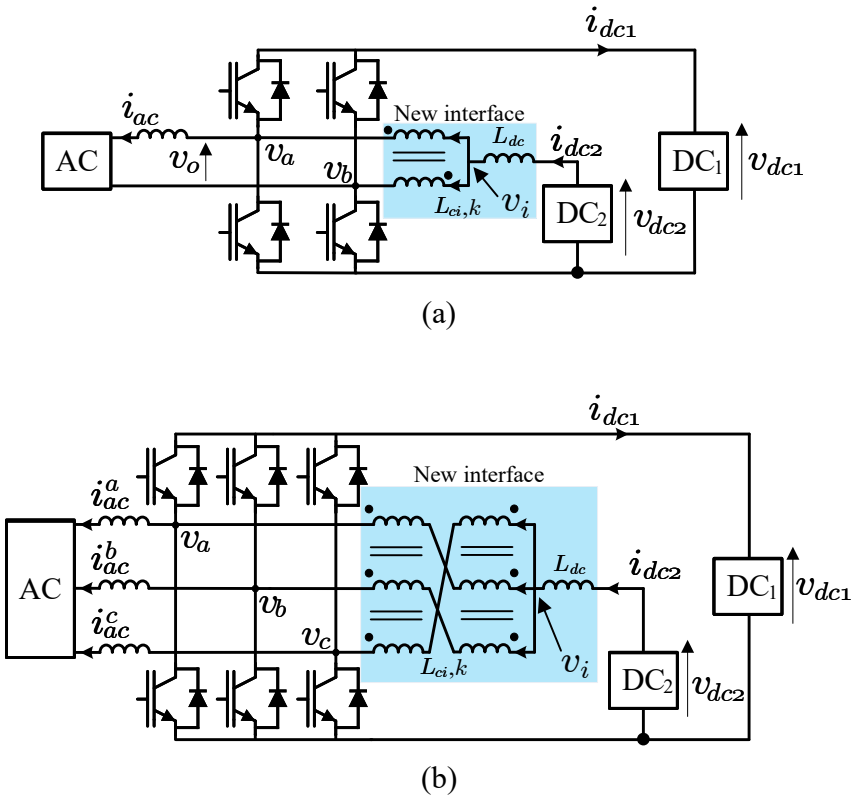


FIGURE 4.1. Topology of the modified three-port converter. (a) Single-phase implementation. (b) Three-phase implementation.

4.1. Topology and Operation Principle

The analysed converter is based on the DC-DC-AC TPC, modifying the interface to the port dc_2 to include coupled inductors instead of individual ones. Thus, the converter conserves the same features of the TPC: single power conversion stage, minimised number of switching devices and bidirectional power capabilities in all ports. Fig. 4.1 shows the proposed converter for the single- and three-phase implementations, highlighting the modification of the $DC2$ interface. The coupling of the inductors aims to use the inherited phase-shift of AC systems ($180°$ for single-phase scenario and $120°$ for three-phase) to

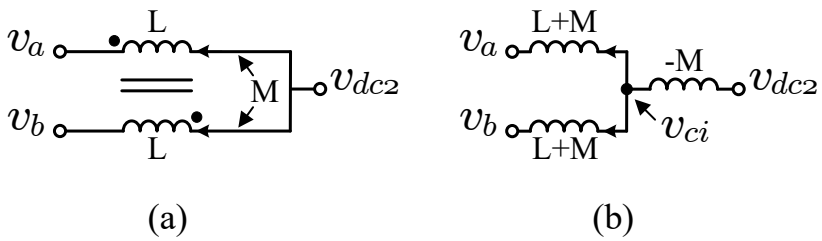


FIGURE 4.2. Coupled inductors analysis. (a) Single-phase circuit. (b) Single-phase equivalent circuit.

reduce the magnitude of the circulating low-frequency AC currents on the TPC. Additionally, an extra DC inductor should be included at the DC side of the interface to address the high-frequency components on the current, as explained later in the section.

The effect of the coupling is to modify the behaviour of each inductor (winding) by integrating them in the same core, so each current can modify the dynamics of the flowing on the complementary winding (Boillat & Kolar, 2012; Wong et al., 2000). Fig. 4.2 shows the coupled inductor circuit for the single-phase case and the equivalent circuit obtained when using a common core for the windings. The circuit in Fig. 4.2(a) is described by the expressions in (4.1), where L represents the self-inductance and M the mutual inductance between the windings. Then, the set in (4.1) is equivalent to (4.2), which characterises the equivalent circuit in Fig. 4.2(b). The equivalent circuit shows how the resulting inductance (and therefore the impedance) of each winding increases, thus reducing the consequent currents generated by the voltage applied to them. However, it also shows a negative effect on the inductance on the DC side, explaining the addition of an extra inductor on that side to account for this reduction.

$$\begin{aligned} v_{dc2} - v_a &= L\frac{di^a_{dc2}}{dt} - M\frac{di^b_{dc2}}{dt} \\ v_{dc2} - v_b &= L\frac{di^b_{dc2}}{dt} - M\frac{di^a_{dc2}}{dt} \end{aligned} \tag{4.1}$$

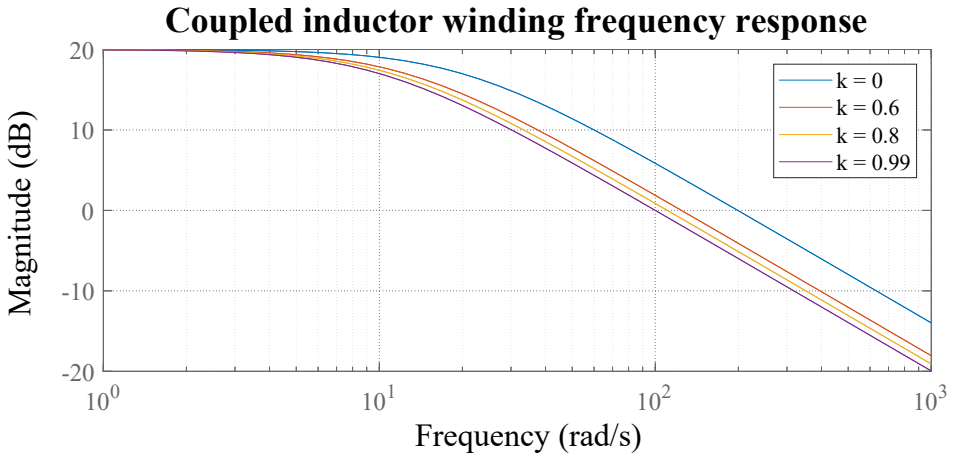


FIGURE 4.3. Coupled inductor winding frequency response for different coupling factors.

$$
\begin{aligned}
v_{ci} - v_a &= (L+M)\tfrac{di^a_{dc2}}{dt} \\
v_{ci} - v_b &= (L+M)\tfrac{di^b_{dc2}}{dt} \\
v_{dc2} - v_{ci} &= -M\tfrac{d(i^a_{dc2}+i^b_{dc2})}{dt}
\end{aligned}
\tag{4.2}
$$

The coupling degree between both windings defines how much the inductance seen at each of them increases. The transfer function for each winding is shown in (4.3), considering $M = k \cdot L$, with k defined as the coupling factor, and r_L representing the winding resistance.

$$
\frac{i_L}{v_L} = \frac{1}{sL \cdot (1+k) + r_L} \tag{4.3}
$$

Then, Fig. 4.3 shows how the magnitude of the current through the inductor decreases when the coupling factor between the windings increases. The analysis can be extended to a three-phase implementation, showing the same low-pass behaviour to filter the undesired circulating AC currents.

4.2. Modelling and Control of the Converter

The modelling of the converter follows the same format as the one for the presented TPC in the previous chapter, where the dynamic equations are defined by the inductors in the system. However, modifying the port DC_2 interface requires addressing the coupled inductors interface to include its effect on the dynamic relations of the converter.

The behaviour of the converter on the AC side remains unmodified, as the modification just affects the currents on the inductors connecting the second DC port. Thus, (4.4) defines the dynamic equation for the current on the AC port, considering the single-phase case.

$$\frac{di_{ac}}{dt} = \frac{1}{L_{ac}}(\overbrace{(v_a - v_b)}^{v_o} - r_{ac} \cdot i_{ac} - v_{ac}) \tag{4.4}$$

Then, the currents at each winding of the coupled inductor are defined in (4.5) and (4.6), following the variables defined in Figs. 4.1 and 4.2(a) and considering $M = k \cdot L_{ci}$.

$$L_{ci}\frac{di^a_{dc2}}{dt} - M\frac{di^b_{dc2}}{dt} = v_i - v_a - r_{ci} \cdot i^a_{dc2} \tag{4.5}$$

$$L_{ci}\frac{di^b_{dc2}}{dt} - M\frac{di^a_{dc2}}{dt} = v_i - v_b - r_{ci} \cdot i^b_{dc2} \tag{4.6}$$

Furthermore, the inclusion of the extra DC inductor defines a new equation to consider in the modelling shown in (4.7).

$$L_{dc}\frac{di_{dc2}}{dt} = v_{dc2} - v_i - r_{dc} \cdot i_{dc2} \tag{4.7}$$

Expression (4.8) is then obtained by adding (4.5) and (4.6), and considering $i_{dc2} = i^a_{dc2} + i^b_{dc2}$.

$$(L_{ci} - M)\frac{di_{dc2}}{dt} = 2v_i - (v_a + v_b) - r_{ci} \cdot i_{dc2} \tag{4.8}$$

Then, combining (4.7) and (4.8) leads to defining the dynamic relation for the current at the port dc_2 in (4.9).

$$(2L_{dc} + L_{ci}(1-k))\frac{di_{dc2}}{dt} = 2v_{dc2} - (v_a + v_b) - (r_{ci} + 2r_{dc}) \cdot i_{dc2} \tag{4.9}$$

Expression (4.9) shows that for coupling factors $k \approx 1$ the inductance of the CI gets cancelled at the DC port, explaining the need for using the extra L_{dc} inductor. The equivalent circuit in Fig. 4.2(b) with its respective set of equations in (4.2) can be used to get the dynamics of each winding. Then, (4.5) and (4.6) translate into (4.10)-(4.12), showing how the inductance approximately doubles its value for $k \approx 1$.

$$L_{ci}(1+k)\frac{di^a_{dc2}}{dt} = v_{ci} - v_a - r_{ci} \cdot i^a_{dc2} \tag{4.10}$$

$$L_{ci}(1+k)\frac{di^b_{dc2}}{dt} = v_{ci} - v_b - r_{ci} \cdot i^b_{dc2} \tag{4.11}$$

$$(L_{dc} - kL_{ci})\frac{di_{dc2}}{dt} = v_{dc2} - v_{ci} - r_{dc} \cdot i_{dc2} \tag{4.12}$$

The controller of the converter can be implemented in the same way as in the TPC, considering the change in the modelling above described. This section considers the use of an average modelling, aiming to achieve an ordered harmonic spectrum by using a modulating stage. The base equations for the model are (4.4) and (4.9) that can be rewritten as in (4.13) and (4.14), considering the modulation index of each leg (m_a, m_b) as the manipulated variables.

$$\frac{di_{ac}}{dt} = \frac{1}{L_{ac}}(v_{dc1} \cdot (m_a - m_b) - r_{ac} \cdot i_{ac} - v_{ac}) \tag{4.13}$$

$$(2L_{dc} + L_{ci}(1-k))\frac{di_{dc2}}{dt} = 2v_{dc2} - v_{dc1} \cdot (m_a + m_b) - (r_{ci} + 2r_{dc}) \cdot i_{dc2} \tag{4.14}$$

Then, the state-space model is obtained in (4.15) following the same procedure of section 3.2.2, part B. As stated previously, the terms regulating the AC current remain unchanged and the modifications just affect the lower row of the system matrices.

$$\begin{aligned}\underbrace{\begin{bmatrix}\dot{i}_{ac}\\ \dot{i}_{dc2}\end{bmatrix}}_{\dot{x}} &= \underbrace{\begin{bmatrix}\frac{-r_{ac}}{Lac} & 0\\ 0 & \frac{-(r_{ci}+2r_{dc})}{(L_{ci}(1-k)+2L_{dc})}\end{bmatrix}}_{A}\underbrace{\begin{bmatrix}i_{ac}\\ i_{dc2}\end{bmatrix}}_{x}\\ &+ \underbrace{\begin{bmatrix}\frac{v_{dc1}}{Lac} & \frac{-v_{dc1}}{Lac}\\ \frac{-v_{dc1}}{(L_{ci}(1-k)+2L_{dc})} & \frac{-v_{dc1}}{(L_{ci}(1-k)+2L_{dc})}\end{bmatrix}}_{B}\underbrace{\begin{bmatrix}m_a\\ m_b\end{bmatrix}}_{u}\\ &+ \underbrace{\begin{bmatrix}\frac{-1}{Lac} & 0\\ 0 & \frac{2}{(L_{ci}(1-k)+2L_{dc})}\end{bmatrix}}_{E}\underbrace{\begin{bmatrix}v_{ac}\\ v_{dc2}\end{bmatrix}}_{u_{ext}}\end{aligned} \tag{4.15}$$

The references for the controller are the same as defined for the TPC, and given again in (4.16)-(4.18) for readability purposes.

$$i^*_{ac} = I^*_{ac}\sin(\omega t + \varphi) \tag{4.16}$$

$$I^*_{ac} = \frac{P^*_{ac}}{V_{ac}\cdot\cos(\varphi)} \quad with \quad \varphi = \arctan\left(\frac{Q^*_{ac}}{P^*_{ac}}\right) \tag{4.17}$$

$$i^*_{dc2} = \frac{P^*_{ac} - P_{dc1}}{v_{dc2}} \tag{4.18}$$

Then, the overall control structure follows the scheme shown in Fig. 4.4, where the LQR gain is obtained as in section 3.2.2 part B., and the feed-forward term follows (4.19) with the matrices defined in (4.15).

$$u_{ff} = B^{-1}(\dot{x^*} - A\cdot x^* - E\cdot u_{ext}) \tag{4.19}$$

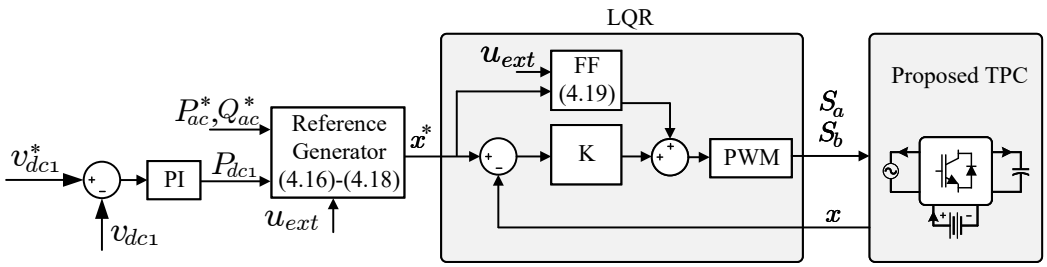


FIGURE 4.4. Control Scheme of LQR for the proposed TPC with coupled inductors.

4.3. Design of the Converter

The main motivation behind the content presented in this chapter is the reduction of the AC currents circulating in the converter without taking part in the power transfer process. These currents depend on the operation conditions of the AC port and increase the overall current load of the devices in the TPC. Thus, this section will analyse how the use of coupled inductors reduces the current load of the converter, following the study presented in section 3.3.2. Additionally, the design requirements for the new interface are also stated in this section, providing the guidelines for the construction of the required coupled inductor for a single-phase case.

4.3.1. Coupled Inductor Impact on the Current Load Characteristics

The first step in the analysis is to obtain the voltages to be generated by the legs under steady-state conditions, as these voltages will define the current flowing through the inductors. The calculation of these voltages considers the currents flowing through the converter according to the power references to be regulated on each port (Defined in (4.16)-(4.18)). Then, these references are replaced into the dynamic equations to get the voltages to be generated by the converter, considering the same approach of section 3.3.2. Expression (4.20) correspond to the dynamic equation for the AC port, considering the set-point in (4.16) and neglecting the resistor losses.

$$(v_a - v_b)^* = v_{ac} + \omega L_{ac} I_{ac} \cos(\omega t + \varphi) \tag{4.20}$$

The reference for the DC port i_{dc2} is assumed to be constant in steady-state, thus (4.21) reflects the result of replacing the constant value defined by (4.18) into (4.9).

$$(v_a + v_b)^* = 2v_{dc2} \tag{4.21}$$

Then, by adding and subtracting (4.20) and (4.21) the expressions for the voltages of each leg are obtained in (4.22)

$$\begin{aligned} v_a^* &= v_{dc2} + \tfrac{1}{2}(V_{ac}\sin(\omega t) + \omega L_{ac} I_{ac}\cos(\omega t + \varphi)) \\ v_b^* &= v_{dc2} - \tfrac{1}{2}(V_{ac}\sin(\omega t) + \omega L_{ac} I_{ac}\cos(\omega t + \varphi)) \end{aligned} \tag{4.22}$$

The voltages are then substituted into (4.10) and (4.11), to obtain the effect on the currents flowing through each winding of the coupled inductor. This is shown in (4.23) and (4.24) neglecting the resistor losses.

$$L_{ci}(1+k)\frac{di_{dc2}^a}{dt} = v_{ci} - (v_{dc2} + \frac{1}{2}(V_{ac}\sin(\omega t) + \omega L_{ac} I_{ac}\cos(\omega t + \varphi))) \tag{4.23}$$

$$L_{ci}(1+k)\frac{di_{dc2}^b}{dt} = v_{ci} - (v_{dc2} - \frac{1}{2}(V_{ac}\sin(\omega t) + \omega L_{ac} I_{ac}\cos(\omega t + \varphi))) \tag{4.24}$$

The expressions can be further reduced when the constant i_{dc2}^* reference is replaced in (4.12) resulting in $v_{ci} = v_{dc2}$. Thus, final expressions for the derivatives of the currents through the windings are obtained in (4.25) and (4.26).

$$\frac{di_{dc2}^{a^*}}{dt} = -\frac{1}{2L_{ci}(1+k)}(V_{ac}\sin(\omega t) + \omega L_{ac} I_{ac}\cos(\omega t + \varphi)) \tag{4.25}$$

$$\frac{di_{dc2}^{b^*}}{dt} = \frac{1}{2L_{ci}(1+k)}(V_{ac}\sin(\omega t) + \omega L_{ac} I_{ac}\cos(\omega t + \varphi)) \tag{4.26}$$

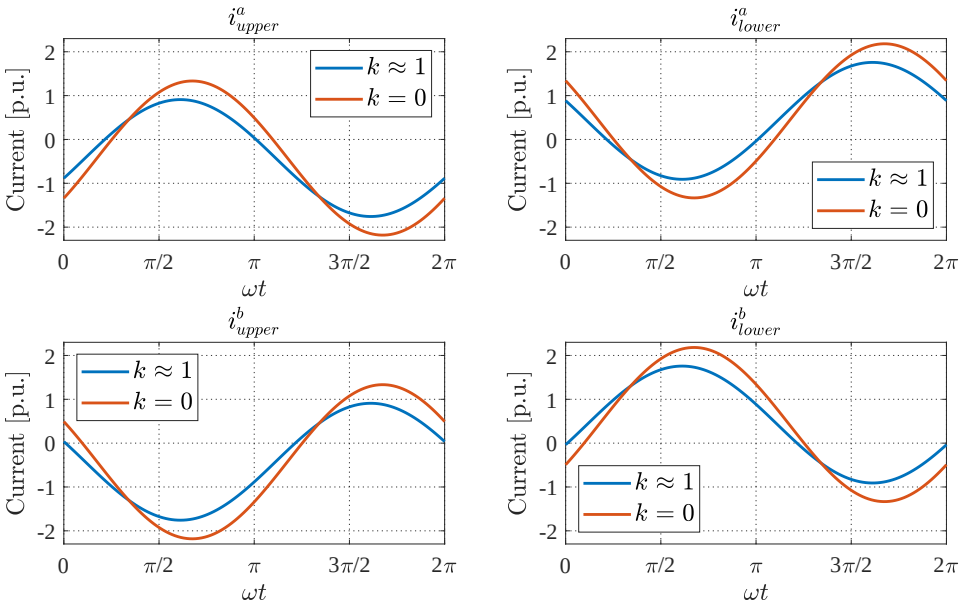


FIGURE 4.5. Comparison of current load of the TPC switching devices for cases with and without coupling.

Finally, the currents for each winding are expressed in (4.27) and (4.28) considering an equal share of the DC current. The expressions show that a coupling factor $k \approx 1$ doubles the inductance of each winding, thus reducing the AC circulating component to half of its original value. Thus, current waveforms for each device are obtained and shown in Fig. 4.5, depicting how the total load is reduced for the case with coupled inductors. Specifically, the absolute peak current through the devices gets reduced by 20% and the RMS value by 22% for the studied case.

$$i^{a^*}_{dc2} = \frac{i^*_{dc2}}{2} + \frac{1}{2\omega L_{ci}(1+k)}(V_{ac}\cos(\omega t) - \omega L_{ac} I_{ac}\sin(\omega t + \phi)) \tag{4.27}$$

$$i^{b^*}_{dc2} = \frac{i^*_{dc2}}{2} - \frac{1}{2\omega L_{ci}(1+k)}(V_{ac}\cos(\omega t) - \omega L_{ac} I_{ac}\sin(\omega t + \phi)) \tag{4.28}$$

4.3.2. Coupled Inductor Design

The magnetic analysis is a fundamental part of designing power electronics systems, with numerous research published in recent years analysing the design of inductors for

different applications (Gu et al., 2013; Salmon et al., 2009; H. Wang et al., 2019). Thus, this subsection will provide the guidelines for the design of the coupled inductor used to interface the second DC port of the TPC. The design procedure is mainly based on the geometrical constant method that can be found in Erickson and Maksimovic (2020) and McLyman (2004).

The main factors that determine the design of an inductor are:

- The desired inductance
- The voltage across its terminals
- The operating frequency
- The flux density

The desired inductance depends on the operating conditions of the TPC for the specific case. A value of 5 mH per winding is selected in this section, and the same value will be used for the implementation with individual inductors to perform a comparative analysis. Furthermore, this section considers a converter with the parameters specified in Table 4.1. The required inductor operates at a low frequency (50 Hz), then relatively large flux densities should be expected (McLyman, 2004). Consequently, iron laminations are selected as the material for the core of the inductor, as they can withstand flux densities up to 1.6 T. The voltage across the inductors is determined by subtracting v_{dc2} from (4.22) and given in (4.29). Then, the magnetic flux in volt-seconds applied to the inductor is expressed in (4.30) for the positive portion of the cycle.

TABLE 4.1. Parameters of the Analysed TPC for the Coupled Inductor Design.

Description	Parameter	Value
Desired inductance per winding	L_{ci}	5 mH
Nominal grid voltage	V_{ac}	120 V / 50 Hz
Power rating	P_o^{max}	3 kW
DC1 Voltage	v_{dc1}	200 V
DC2 Voltage	v_{dc2}	100 V
Maximum Flux Density	B_{max}	1.6 T

$$v_L(t) = \pm\frac{1}{2}(V_{ac}\sin(\omega t) + \omega L_{ac} I_{ac}\cos(\omega t + \phi)) \tag{4.29}$$

$$\lambda_L = \int_0^{T/2} v_L(t)dt \tag{4.30}$$

TABLE 4.2. Parameters used in the Inductor Design.

Description	Parameter	Unit
System Parameters		
Wire effective resistivity	ρ	$\Omega - cm$
Total RMS winding currents	I_{tot}	A
Applied volt-seconds	λ_L	$V - sec$
Allowed power dissipation	P_{tot}	W
Winding filling factor	K_u	
Core loss exponent	β	
Core loss coefficient	K_{fe}	W/cm^3T^β
Core Dimensions		
Core cross-sectional area	A_c	cm^2
Core window area	W_a	cm^2
Mean length per turn	MLT	cm
Magnetic path length	l_m	cm
Peak AC flux density	ΔB	T
Wire areas	A_w	cm^2

The required core size is determined by optimising the AC flux density to minimise the total power losses, which consist of the addition of the core losses and the conduction losses. The procedure can be found in Section 12 of Erickson and Maksimovic (2020), and it leads to the expression in (4.31). The right side of the expression is determined by the operating conditions of the system, while the term k_{gfe} is defined as the core geometrical constant and it is defined as in (4.32). Thus, (4.31) determines the required core size able to withstand the operation condition of the TPC in terms of voltages and currents applied to the coupled inductor. Then, (4.32) is used to check whether the selected core is large enough to satisfy the design requirements. Table 4.2 showcase all the variables with their description and units to calculate the presented values.

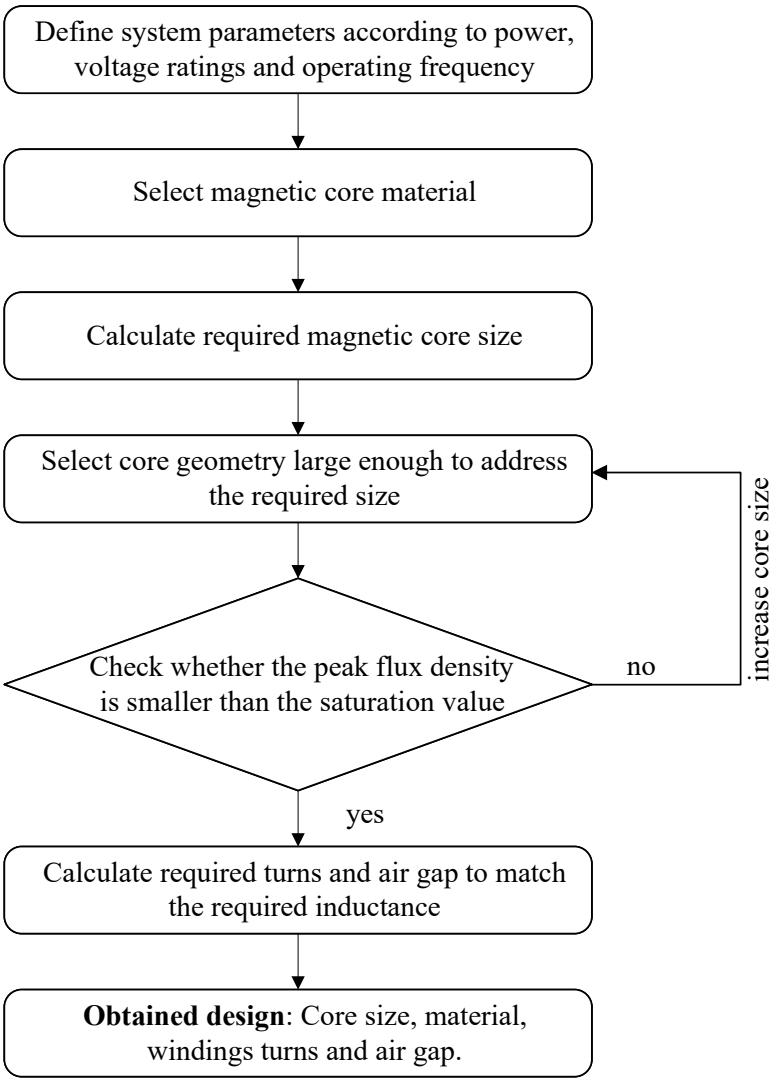


FIGURE 4.6. Flowchart illustrating the coupled inductor magnetic design.

$$K_{gfe} \geq \frac{\rho \lambda_L^2 I_{tot}^2 K_{fe}^{(2/\beta)}}{4 K_u (P_{tot})^{((\beta+2)/\beta)}} \tag{4.31}$$

$$K_{gfe} = \frac{W_a (A_c)^{(2(\beta-1)/\beta)}}{(MLT) l_m^{(2/\beta)}} \left[\left(\frac{\beta}{2} \right)^{-\left(\frac{\beta}{\beta+2}\right)} + \left(\frac{\beta}{2} \right)^{\left(\frac{\beta}{\beta+2}\right)} \right]^{-\left(\frac{\beta+2}{\beta}\right)} \tag{4.32}$$

TABLE 4.3. Obtained Coupled Inductor Design.

Description	Value
Core material	Silicon steel laminations
Core geometry	UI180
Turns per winding	97
Air gap length	2.35 mm

Summarising, the procedure to design the coupled inductor is summarised in Fig. 4.6. It starts by calculating the required magnetic core size according to the configuration for the TPC; followed by an iterative process to find the adequate core size able to withstand the peak flux density; to finalise with the calculation of the air gap and windings turns to achieve the expected inductance value. The main parameters for the obtained design are then displayed in Table 4.3, which considers the values in Table 4.1 and expressions (4.27)-(4.30) for the operative conditions of the converter.

4.4. Chapter Conclusions

This chapter investigated a modification of the three-port DC-DC-AC topology proposed in chapter 3 to reduce the circulating currents that increase the losses of the original proposal. The modification consists of replacing the inductors connecting port DC_2 to the middle points of the converter phases with an array of coupled inductors instead. The magnetic coupling aims to increase the overall impedance on this interface to the low-frequency components generated by the voltage on the AC port. Analysis shows that inversely coupled inductors on a single-phase case allow for doubling the impedance of the interface to the AC components, effectively reducing the circulating currents that do not participate in the power transfer.

The modelling of the modified converter follows the same structure as the one presented in Chapter 3 for the original topology. Thus, a multi-variable approach allows analysing of the variables of the TPC to obtain a dynamic model of the system, enabling the design of the appropriate controller. Additionally, the modelling allows for studying the steady-state behaviour to quantify the effect of the modified coupled-inductors interface on

the overall current load of the devices in the converter. Analysis shows that the AC components in the currents through the DC_2 interface inductors can be reduced to 50%, which leads to a reduction of 38% in the overall current load through the switching devices for a converter with specified parameters.

Finally, a procedure for designing the coupled inductors interface was also presented, based on the modelling and operation parameters defined for the TPC. The procedure shows how to calculate the minimum core size, based on the peak magnetic flux to withstand while operating under steady-state conditions. The procedure outputs a design including silicon steel laminations in a UI180 geometry, which enables the reduction of the circulating currents in a grid-connected scenario.

5. RESULTS AND ASSESSMENT OF THE THREE-PORT FULL-BRIDGE DC-DC-AC CONVERTER

A single-stage three-port DC-DC-AC converter has been proposed in the previous chapters using the minimum quantity of devices to regulate the power flow between the three ports. Chapter 2 presented the topology, modelling and design analysis of the investigated TPC, while chapter 3 studied a modification to optimise the operation in terms of current load reduction. Thus, this chapter presents the simulation and experimental results of the proposed TPC to validate the design and control developed in the previous chapters. The converter is simulated in Matlab/Simulink for different DC-DC-AC systems, to validate its use for integrating ESS into hybrid DC-AC applications. The magnetic design of chapter 3 is implemented using the PLECS library to assess the impact of using a coupled inductor interface in the TPC. Then, an experimental setup is used to verify the TPC operation at a reduced power scale level. Finally, an assessment of the proposed converter against the state-of-the-art single-stage three-port converters is presented to compare its features.

5.1. Simulation Results

This section presents simulation results for the single-phase and three-phase TPC presented and analysed in the previous chapters. The single-phase case considers both configurations described in section 3.2: a grid-connected BESS exploiting the boost capability of the TPC and; a hybrid PV-BESS system delivering constant power to the grid, using the battery as an energy buffer. On the other hand, the three-phase case considers a hybrid system with two DC sources feeding an ac-load. The converters and control systems were implemented using Matlab/Simulink, as the platform provides a widely used toolbox for power electronics.

5.1.1. Single-phase TPC

The single-phase TPC proposed in chapter 3 and reprised in Fig. 5.1 was simulated in a low-power application with the parameters presented in Table 5.1. The configuration considers a battery on the low voltage port DC_2 and a capacitor to hold the voltage on port

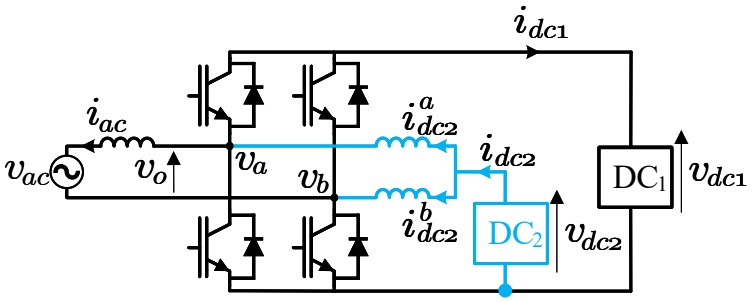


FIGURE 5.1. Single-phase implementation of the TPC.

TABLE 5.1. Parameters of the simulated single-phase converter

Description	Parameter	Value
Nominal grid voltage	V_{ac}	120 V / 50 Hz
Power rating	P_o^{max}	3 kW
AC Inductor	L_{ac}	5 mH
DC1 Capacitor	C	2.2 mF
DC1 Capacitor Voltage	v_{dc1}	200 V
DC2 Inductors	L_{dc}	5 mH / 25 mΩ
DC2 Battery Voltage	v_{dc2}	72 V
MOSFETs C3M0010090K	V/I	900 V / 197A
Sampling Frequency	f_s^{max}	20 kHz
FCS-MPC weighting factors	λ_1,λ_2,λ_3	8, 3, 0.3

DC_1. The parameters were selected in order to obtain a maximum output active power of 3 kW with a voltage variation of $\pm 10\%$ at the capacitor bus at steady-state conditions. The proposed TPC shows the capability to boost the battery voltage, enabling the power transfer to the grid from a low-voltage source, and deflecting all the double-frequency oscillations of the single-phase power to the capacitor. The system is regulated using the control scheme in Fig.3.5 that considers an FCS-MPC regulator to generate the switching signals for the active devices on the TPC. The cost function weighting factors were obtained in a heuristic manner aiming to minimise the tracking error of the controller currents.

The converter operates correctly in the defined power range, Fig. 5.2 shows the response of the variables of the system for an output power increasing from 0.4 to 3 kW. The battery current in Fig. 5.2(a) is free of low-frequency harmonics and follows the reference with little overshoots at the step changes. The voltage of the DC bus is kept at the

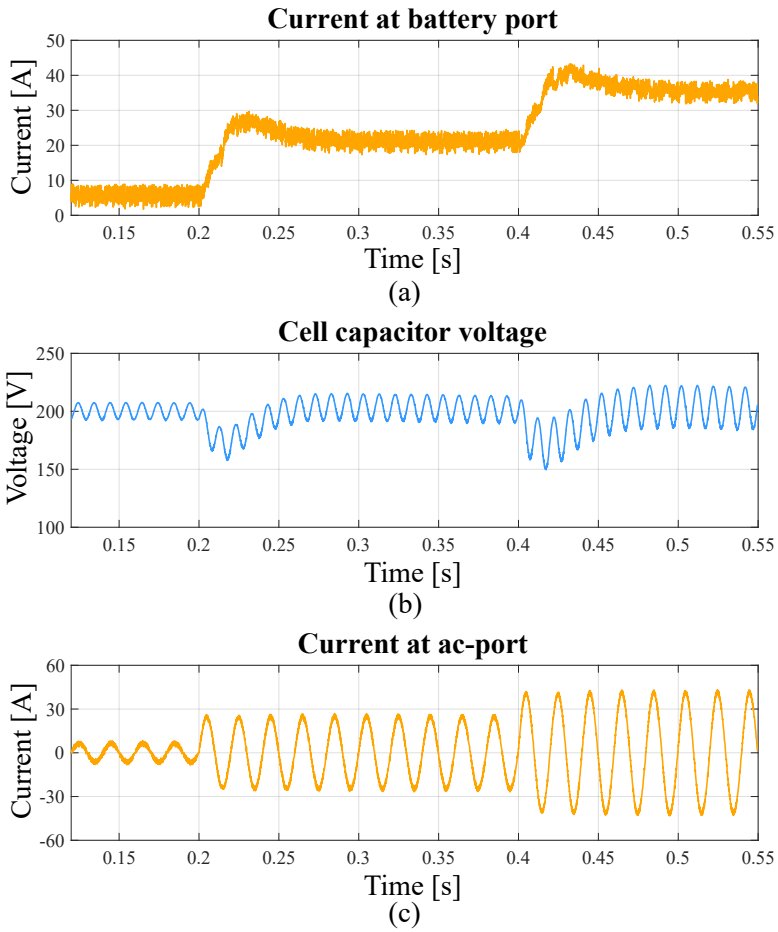


FIGURE 5.2. Simulation results for the single-phase TPC used as a boost inverter. (a) Battery current. (b) Capacitor voltage. (c) Grid current.

desired value with a maximum ripple of $\pm 10\%$ at the maximum power requirement (Fig. 5.2(b)). The last port, corresponding to the AC side, shows a correct current response with fast-tracking of the sinusoidal reference as it is shown in Fig. 5.2(c). The variables at the AC side are analysed at maximum power (3 kW) to obtain the harmonic components on the voltage and current injected to the grid. Fig. 5.3 shows the output voltage with its respective harmonic content plus the harmonic components of the current after filtering. The voltage waveform is similar to a unipolar modulation, but at the zero-crossings, it becomes similar to a bipolar modulator as the FCS-MPC does not include an external modulator.

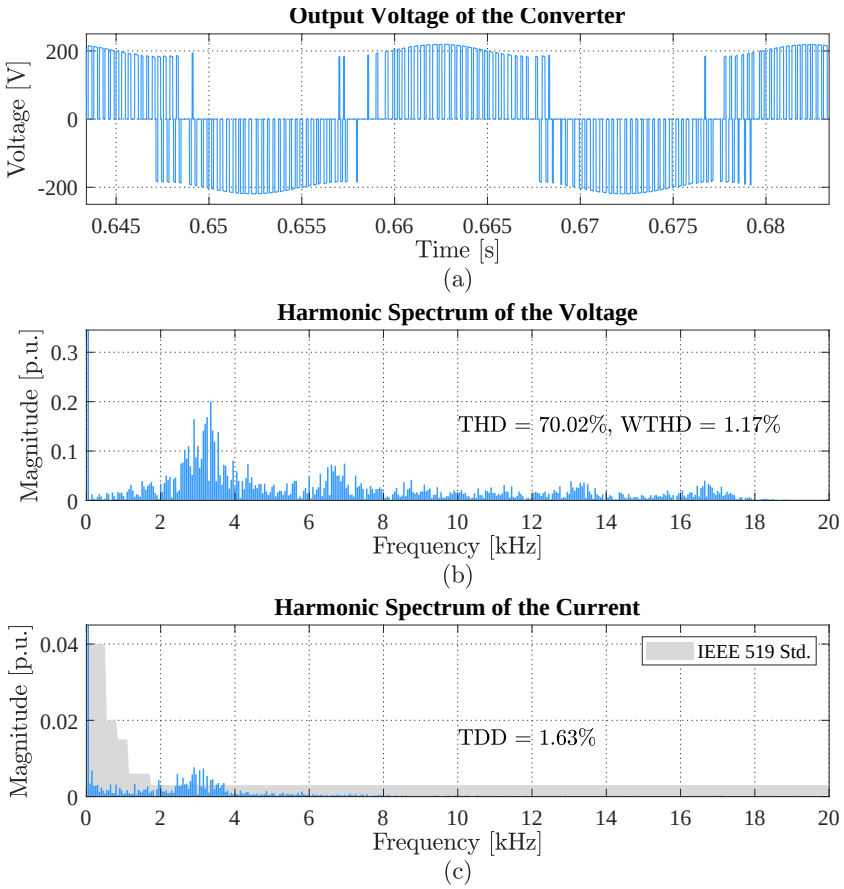


FIGURE 5.3. Simulation results at 3kW. (a) Output voltage. (b) Harmonic spectrum of the output voltage. (c) Harmonic spectrum of the output current.

Thus, the control sets the switching state that ensures the minimisation of the cost function using all positive, negative and zero states. The lack of modulation stage leads to the spread voltage harmonic spectrum shown in Fig. 5.3, which shows a dominant switching frequency at around 3.3 kHz. However, despite this spread spectrum characteristic of the FCS-MPC algorithm, the distortion indicators are suitable for a DC/AC converter, achieving a WTHD=1.17% for the output AC voltage before filtering. Finally, Fig. 5.3(c) depicts the magnitude for the current harmonic components in a per unit base, showing very small magnitudes at low-frequency harmonics, agreeing with the unpolluted waveform shown in Fig. 5.2(c). The Total Demand Distortion (TDD) is 1.63% staying below the required 5% set by the standard IEEE 519 for current distortion limits (“IEEE Standard for Harmonic

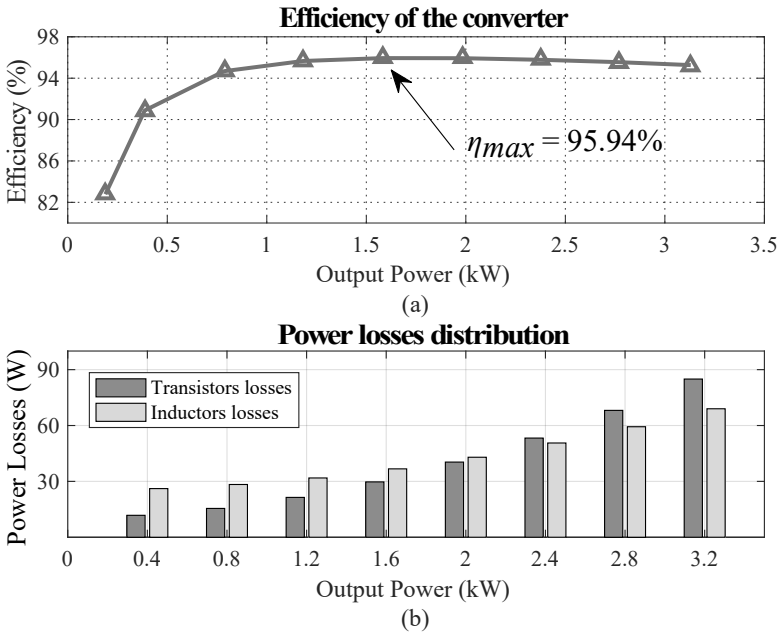


FIGURE 5.4. (a) Simulated power efficiency for the converter. (b) Distribution of power losses.

Control in Electric Power Systems", 2022). The current harmonics remain under the grid code limit for most of the spectrum, showing slight violations for harmonic frequencies above $h = 40$.

The simulated efficiency is similar to other similar converters based on the h-bridge as the H5 (Li et al., 2019). Fig. 5.4 (a) shows the efficiency for the entire output power range, considering transistor losses and the losses associated with the inductors interface (Conduction losses, as core losses represent less than 5% comparatively). The power losses can be separated in two main groups, the first associated to the transistors (conduction and switching losses) and the second related to the conduction losses in the new decoupling inductors. The losses at the transistors are mainly related to conduction losses and can be unequal depending on the power transfer between the different ports (following the analysis in section 3.3.2). Fig. 5.4 (b) shows that the conduction losses at the inductors are the most relevant at low power, until 2 kW, then the semiconductor losses are the highest. The latter is because the decoupling inductors present a constant AC current independent of the output power. Therefore, the inductors present a fixed loss proportion for all the power ranges and

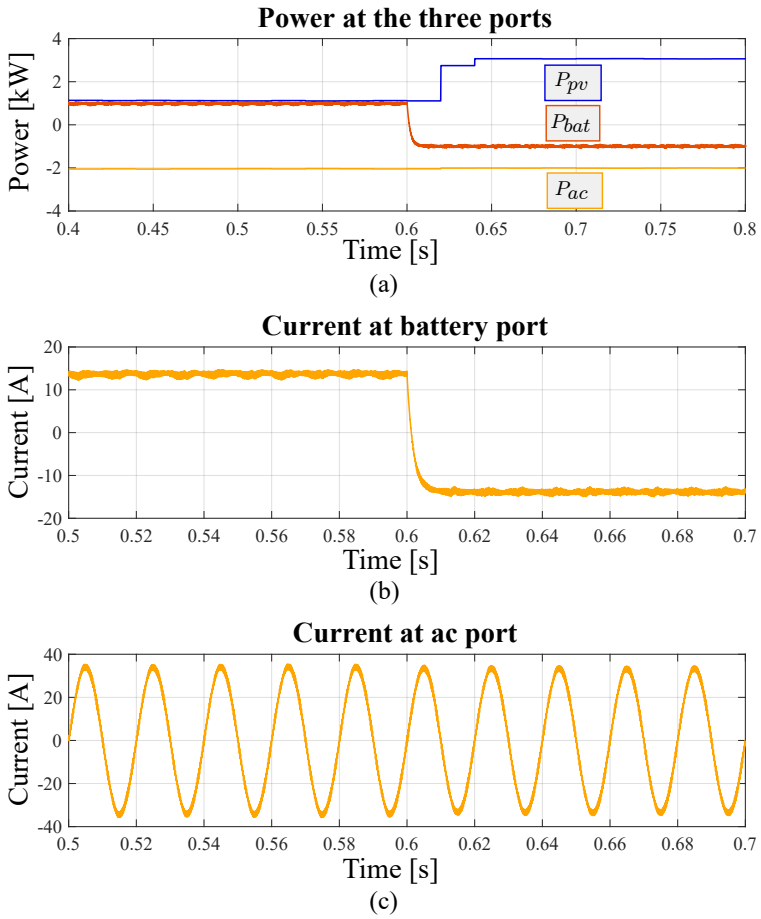


FIGURE 5.5. Simulation results for the single-phase TPC used in a hybrid PV-BESS configuration. (a) Power at the three ports. (b) Current at the battery port. (c) Grid current.

a varying proportion related to the power transfer. Thus, the constant value of the inductors losses is the major component at low power, but after 2 kW it is surpassed by the transistors losses.

Moreover, when an active power source as a PV is connected at DC_1 port, the control of the battery current previously shown can be used to deliver a constant power output to the AC grid. This is the second configuration for the single-phase case, which considers the port DC_1 as a unidirectional active power source and DC_2 as a bidirectional energy buffer. Fig. 5.5(a) shows the power response of the system to a change in the PV generation, where

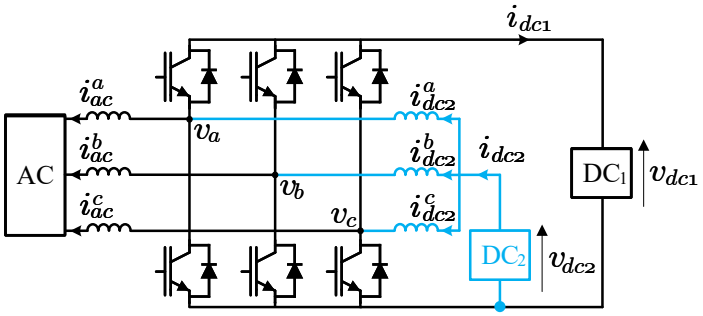


FIGURE 5.6. Three-phase implementation of the TPC.

TABLE 5.2. Parameters of the simulated three-phase converter

Description	Parameter	Value
DC1 source voltage	v_{dc1}	150 V
DC2 source voltage	v_{dc2}	300 V
AC load inductor	L_{ac}	13.9 mH
AC load resistor	R_{ac}	6 Ω
AC load power factor	$cos(\phi)$	0.813
DC2 Inductors	L_{dc}	5 mH / 25 mΩ
Sampling Frequency	f_s^{max}	20 kHz

the battery delivers or absorbs power to address the balance of the three ports. The bidirectional performance of the battery port is shown in Fig. 5.5(b), where the controlled current change accordingly to keep the AC current constant (Fig. 5.5(c)) despite the variations on the power delivered at DC_1.

5.1.2. Three-phase TPC

The three-phase TPC in Fig. 5.6 was simulated with the parameters enlisted in Table 5.2, using a primary current-controlled power source at DC_2 port and a complementary bidirectional power source at DC_1 feeding an AC RL load, similar to a hybrid vehicle powertrain. The modelling resembles the one for the single-phase case, as detailed in chapter 3, with the addition of an additional switching state given by the third phase. Thus, FCS-MPC is used for this implementation too to regulate the multiple variables in the converter.

TABLE 5.3. Operation modes for the three-phase converter

Mode	Main reference I	Main Reference II	Power Balance
I	P_{ac}	$P_{dc2} = 0$	$P_{dc1} = P_{ac}$
II	P_{ac}	$0 < P_{dc2} < P_{ac}$	$P_{dc1} = P_{ac} - P_{dc2}$
III	P_{ac}	$P_{dc2} > P_{ac}$	$P_{dc1} = P_{ac} - P_{dc2}$
IV	$P_{ac} = 0$	$P_{dc2} > 0$	$P_{dc1} = -P_{dc2}$

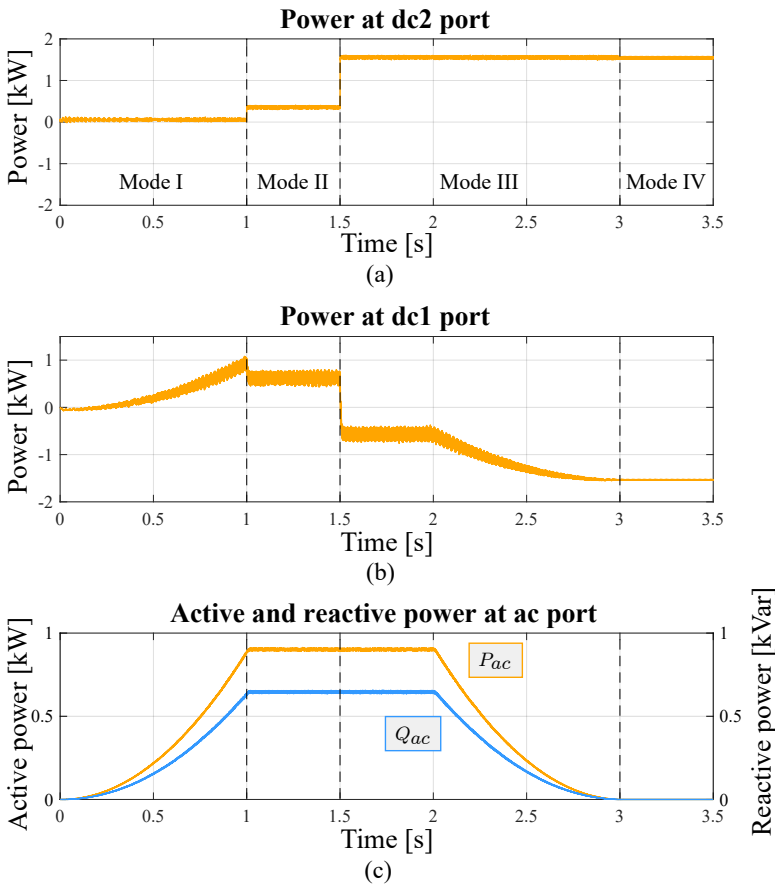


FIGURE 5.7. Simulation results for the three-phase TPC at 50 Hz. (a) Power at dc_2 port. (b) Power at dc_1 port. (c) Power at AC port.

As the TPC has three ports and each one can generate or absorb energy, the converter can operate in several modes, but is always restricted to the power balance $P_{ac} = P_{dc1} + P_{dc2}$. Therefore, the converter can control the power of two ports directly, and the third power just follows the power balance restriction. In this simulation, the powers of the AC and DC_2 ports were chosen as main references, and the power of DC_1 follow the

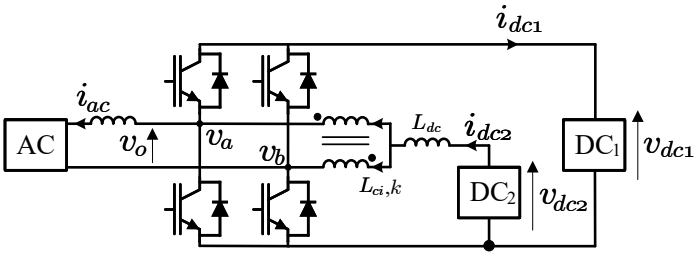


FIGURE 5.8. Single-phase implementation of the TPC with coupled inductors interface.

power balance, as is summarized in Table 5.3. Then, four operational modes are defined depending on the configuration of the ports for delivering and absorbing power.

Fig. 5.7 shows the power response of the three ports for the different operation modes defined in Table 5.3. Both DC sources are able to deliver the active power required by the load independently and in conjunction. Additionally, DC_2 source could inject power to DC_1, verifying the bidirectional feature of the converter.

5.1.3. Single-phase TPC with coupled inductors

This section presents simulation results of the TPC implemented with the coupled inductors interface studied in chapter 4 to validate the described advantages in terms of the current load. The studied case is a single-phase implementation of a grid-connected BESS using the boost capability of the TPC, as shown in Fig. 5.8. The implemented converter considers the design of the coupled inductor and the control method defined in the previous chapter. Table 5.4 summarises the parameters of the system, which correspond to the parameters in Table 5.1 with the changes corresponding to the new interface.

The converter is modelled using the average approach presented in section 4.2, thus allowing the use of an LQR controller together with a modulation stage. Thus, the presented results allow to compare the reduction in the circulating currents due to the magnetic coupling of the DC_2 interface and also show the difference in the control system implemented.

Fig. 5.9 shows the response of the converter to changes in the reference power to be delivered at the AC side. It depicts that the operation of the TPC with coupled inductors operates similarly to the case with singular inductors studied in chapter 3. The first row in

TABLE 5.4. Parameters of the simulated single-phase converter with coupled inductors

Description	Parameter	Value
Nominal grid voltage	V_{ac}	120 V / 50 Hz
Power rating	P_o^{max}	3 kW
AC Inductor	L_{ac}	5 mH
DC1 Capacitor	C	2.2 mF
DC1 Capacitor Voltage	v_{dc1}	200 V
DC2 Coupled Inductor	L_{ci}	5 mH per winding
DC2 Coupling factor	k	0.99
DC2 DC Inductor	L_{dc}	1 mH
DC2 Battery Voltage	v_{dc2}	72 V
PWM Switching Frequency	f_s	10 kHz
MOSFETs C3M0010090K	V/I	900 V / 197A

both columns shows how the current at port DC_2 is free of low-frequency harmonics for the two cases. However, the high-frequency filtering is reduced for the case with coupled inductors, as shown in section 4.1. The filtering can be increased by elevating the value of L_{dc} to match the ripple magnitude of the case in column (b). The second row depicts the effect of coupling the inductors in reducing the magnitude of the AC circulating components. The magnitude is reduced in 50% by integrating the windings in a common core, considering the same inductance per winding in both cases. The latter validates the analysis presented in previous sections. Finally, the third row shows that the operation at the AC side remains unchanged after the inclusion of coupled inductors. Then, Fig. 5.10 shows how the flux density is kept under the defined maximum magnitude for the maximum power operating point. The latter validates the magnetic design exposed in the previous section 4.3.2.

Then, Fig. 5.11 depicts the variables at the AC port to show the difference of using an LQR controller with a PWM scheme generating the switching signals for the semiconductor devices. The overall control system follows the scheme presented in Fig. 4.4, where the LQR generates the two modulation signals that generate the switching signals using a PWM block with two triangular carriers with a phase-shift of 180◦. The voltage output, in this case, is similar to the one generated by a bipolar modulation, although the zero state is also used for brief times due to the operational needs of the TPC. The use of the modulation stage fixes the major component of the frequency spectrum to the switching frequency

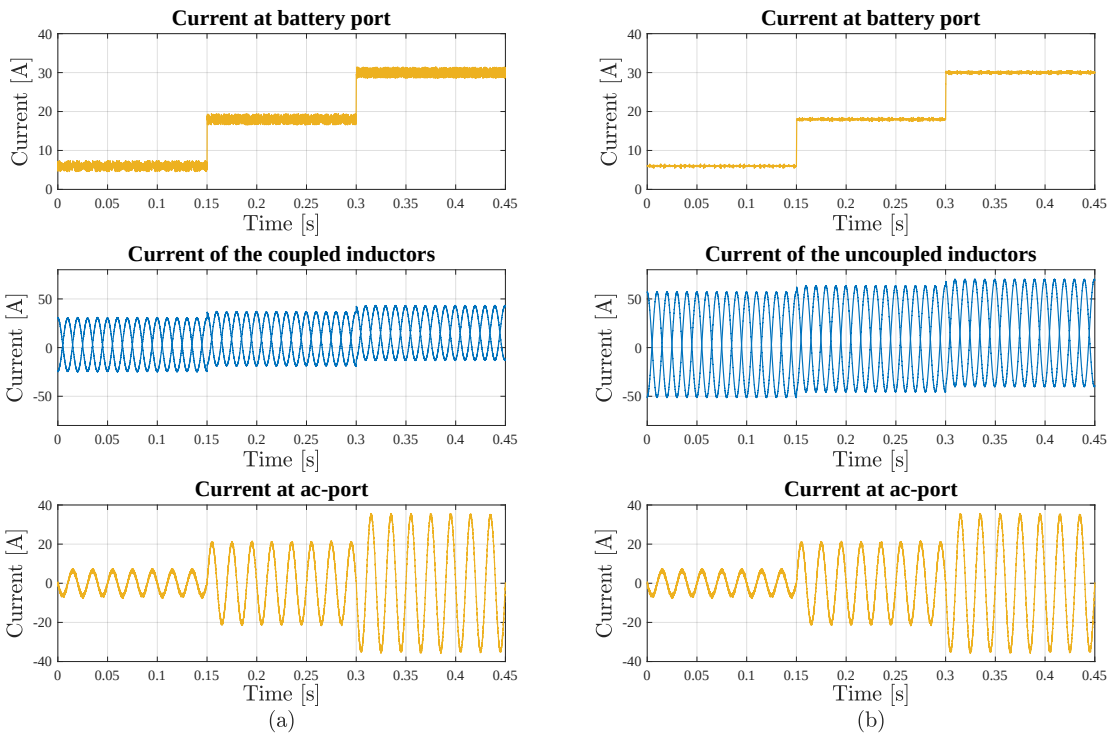


FIGURE 5.9. Simulation results for the single-phase TPC used as a boost inverter. (a) Results with coupled inductors. (b) Results without coupled inductors.

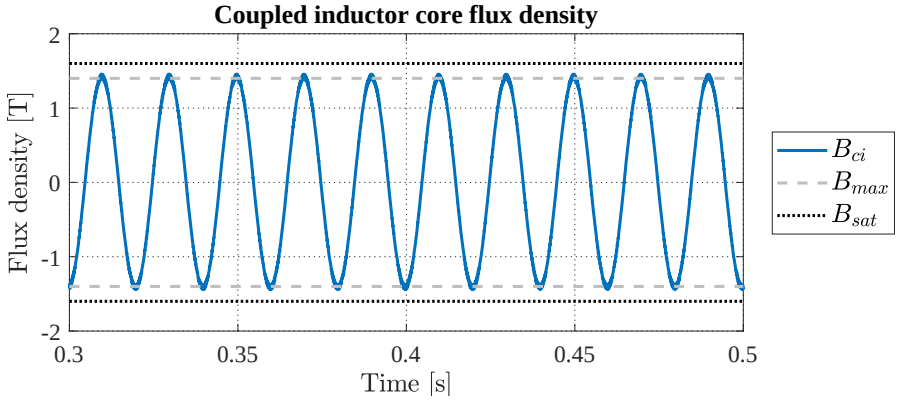


FIGURE 5.10. Simulation results for the flux density of the designed coupled inductor.

(10 kHz), reducing the WTHD to 0.74% before filtering. Then, Fig. 5.11(c) illustrates the harmonic spectrum for the AC current, showing that the harmonics at all frequencies but the switching one are easily filtered by the AC inductance. The latter can be filtered by

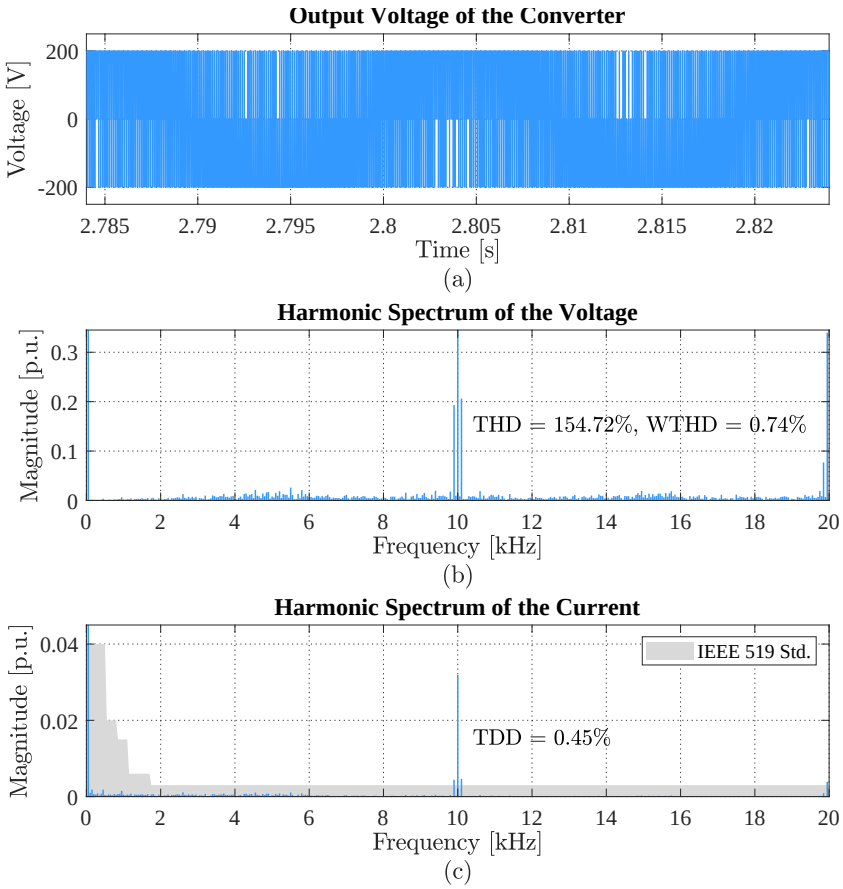


FIGURE 5.11. Simulation results at 3kW. (a) Output voltage. (b) Harmonic spectrum of the output voltage. (c) Harmonic spectrum of the output current.

enhancing the AC filter to an LC configuration, although just with an L type the TDD still is reduced to a 0.45% because of the modulation stage.

5.2. Experimental Results

The simulated results of the past section were validated in a scaled-down single-phase prototype in order to check the topology features previously described. The configuration follows the same structure shown in Fig. 5.1 with the parameters shown in Table 5.5. The experimental setup is configured to deliver a maximum power of 100 W to a low-voltage AC side which connects to the grid through a transformer. The controller implemented uses an FCS-MPC algorithm to calculate the required switching states for the TPC. This

TABLE 5.5. Parameters of the Experimental Setup

Description	Parameter	Value
Nominal grid voltage	V_{ac}	25 V / 50 Hz
Power rating	P_o^{max}	100 W
AC Inductor	L_{ac}	5 mH
DC1 Capacitance	C	3.3 mF
DC1 Capacitor Voltage	v_{dc1}	50 V
DC2 Inductors	L_{dc}	5 mH / 25 mΩ
DC2 Battery Voltage	v_{dc2}	15 V
Sampling Frequency	f_s^{max}	20 kHz
MOSFETs CCS020M12CM2	V/I	1.2 kV / 20A

TABLE 5.6. Specifications of the OPAL OP4510 Unit

Description	Value
Real-time processor	Intel Xeon E3 v5, 4-core, 3.5GHz
FPGA	Kintex-7 XC7K325T
Analog Inputs	32x 16-bit channels, 2Msps, differential, -20 ... 20 V
Digital Outputs	64x push-pull channels, 50 ns resolution, 5 ... 30 V
Programming platform	Matlab Simulink / RT-Lab

controller is implemented in an OPAL-RT platform OP4510 operating at a sampling frequency of 20 kHz. The OPAL platform is a real-time system including a processing system complemented with an FPGA and I/O cards interfacing digital and analog signals. The main specifications of the OPAL system are displayed in Table 5.6.

Fig. 5.12 shows the implementation of the TPC using a commercially available full-bridge module, considering that the topology uses the same configuration. The converter receives digital signals from the real-time controller commanding the switching state of each leg. The signals are calculated using the FCS-MPC controller that takes as inputs the currents through the inductors of the system and the voltage of the capacitor on port DC_1.

Thus, Fig. 5.13 illustrates the obtained results for the battery current, the capacitor voltage and the AC current during a power reversal operation. These are the same variables shown for the single-phase simulations in Fig. 5.2, but under a step change at the required power to show the bidirectional feature of the converter and the fast dynamic behaviour. The decoupling of the DC side from the oscillating power component of the single-phase

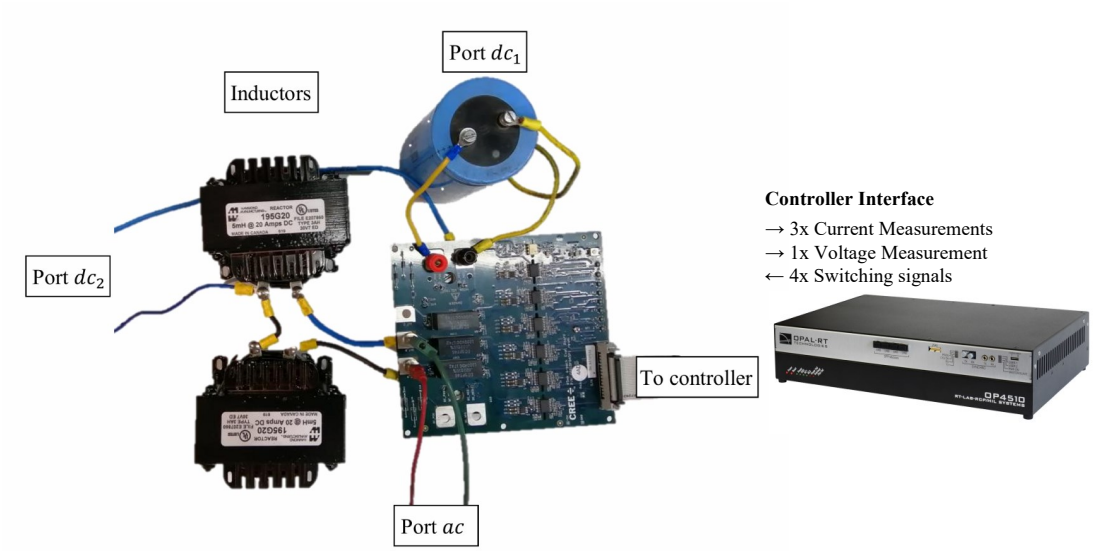


FIGURE 5.12. Experimental TPC cell using CREE CMF20102D.

grid is shown in the capacitor voltage, which is oscillating at twice the fundamental frequency, and in the battery current, which is free of low-frequency oscillations. In the beginning, the battery is draining power from the grid, and at the power reversal step, it starts delivering power to the AC grid. Fig. 5.13(b) shows the capacitor behaviour increasing the ripple but maintaining the reference value at the power reversal. The sinusoidal current shows excellent dynamic response, as it is shown in Fig. 5.13(c). Finally, the generated output voltage and its harmonic spectrum are shown in Fig. 5.14. The voltage waveform and harmonic spectrum are coincident with the simulated results, which validates the proposed theoretical analysis, topology and control scheme.

5.3. Assessment of the proposed converter

The proposed DC-DC-AC three-port converter enables the connection of two DC elements with an AC port minimising the number of active devices required. The topology follows the recent trend of proposals for single-stage three-port converters, aiming to reduce the overall components count and complexity of multi-stage solutions. Following the review presented in chapter 2, the proposed topology fits into the category of Integrated

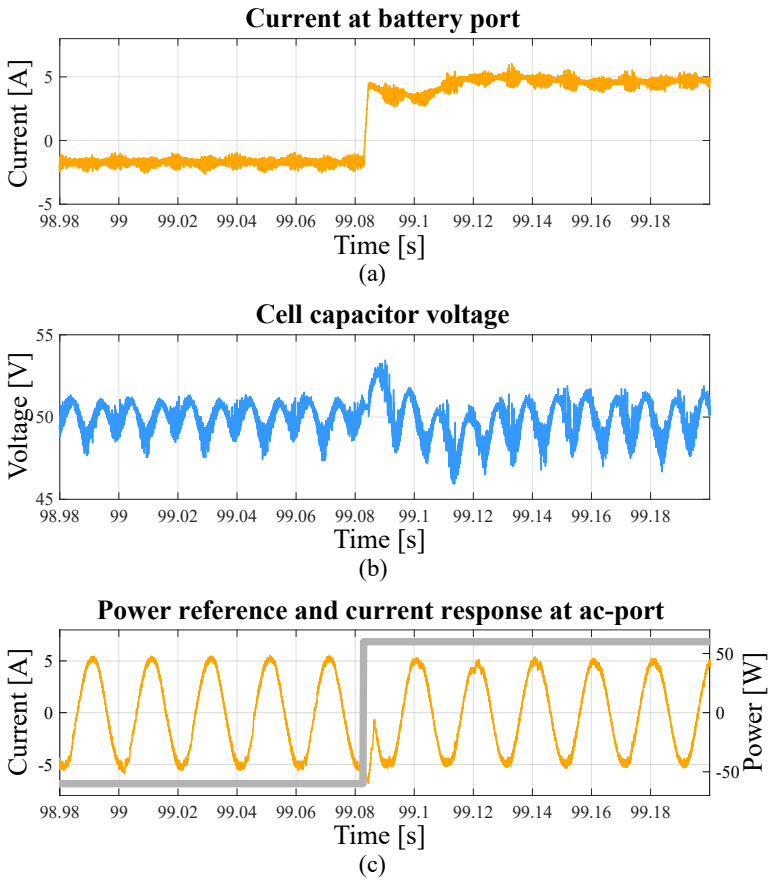


FIGURE 5.13. Experimental results. (a) Current at battery port. (b) Voltage at capacitor port. (c) Power and current at grid port.

Dual-source DC-AC converters, as it is based on a conventional DC-AC topology integrating a buck-boost stage on each phase. Thus, a comparative analysis is performed in this section to present a trade-off study between the different single-stage topologies.

Table 5.7 reprises the summary shown in chapter 2 including the proposed TPC in the comparison. The topology enables bidirectional power flow capabilities among all three ports, as validated in the previous sections. Thus, it has an increased power range compared to the majority of SSI topologies and the simplified T-Type. The TPC minimises the used active devices compared to the topologies with bidirectional capabilities, as it uses at least one less transistor. However, it requires two inductors (individual ones, or coupled), thus

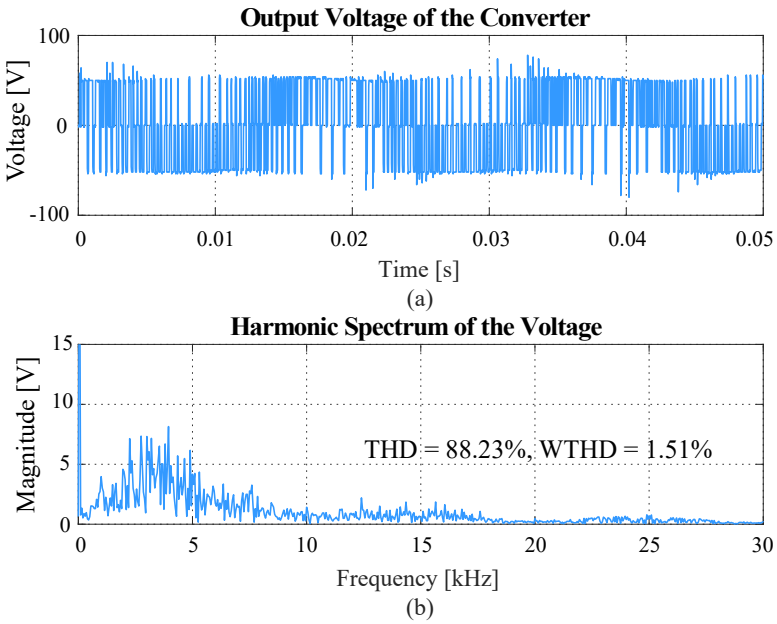


FIGURE 5.14. Experimental results at 60 W. (a) Output voltage. (b) Harmonic spectrum of the output voltage.

TABLE 5.7. Comparison of single-phase integrated dual-source DC-AC converters including the proposed TPC.

Topology	Transistors	Diodes	Inductors	Power flow
Original SSI (Ribeiro et al., 2010)	4	2	1	Unidirectional
Reduced SSI (Kan et al., 2015)	4	1	1	Unidirectional
Improved SSI (Lee & Heng, 2017)	6	0	1	Bidirectional
Active SSI (Yin et al., 2021)	6	2	1	Unidirectional
Simplified SSI (Lee et al., 2019)	5	0	1	Bidirectional
T-Type DP-AMI (J. Wang et al., 2021)	8	0	0	Bidirectional
Simplified T-Type DP-AMI (Wu et al., 2017)	6	1	0	Unidirectional
NPC DP-AMI (Dorn-Gomba et al., 2018)	8	4	0	Bidirectional
Proposed TPC	**4**	**0**	**2**	**Bidirectional**

increasing the overall volume of the solution compared to the topologies displayed in the table.

The operational capabilities of the single-stage DC-DC-AC converters depend on the voltage levels present in each of the three ports. Thus, the different topologies present

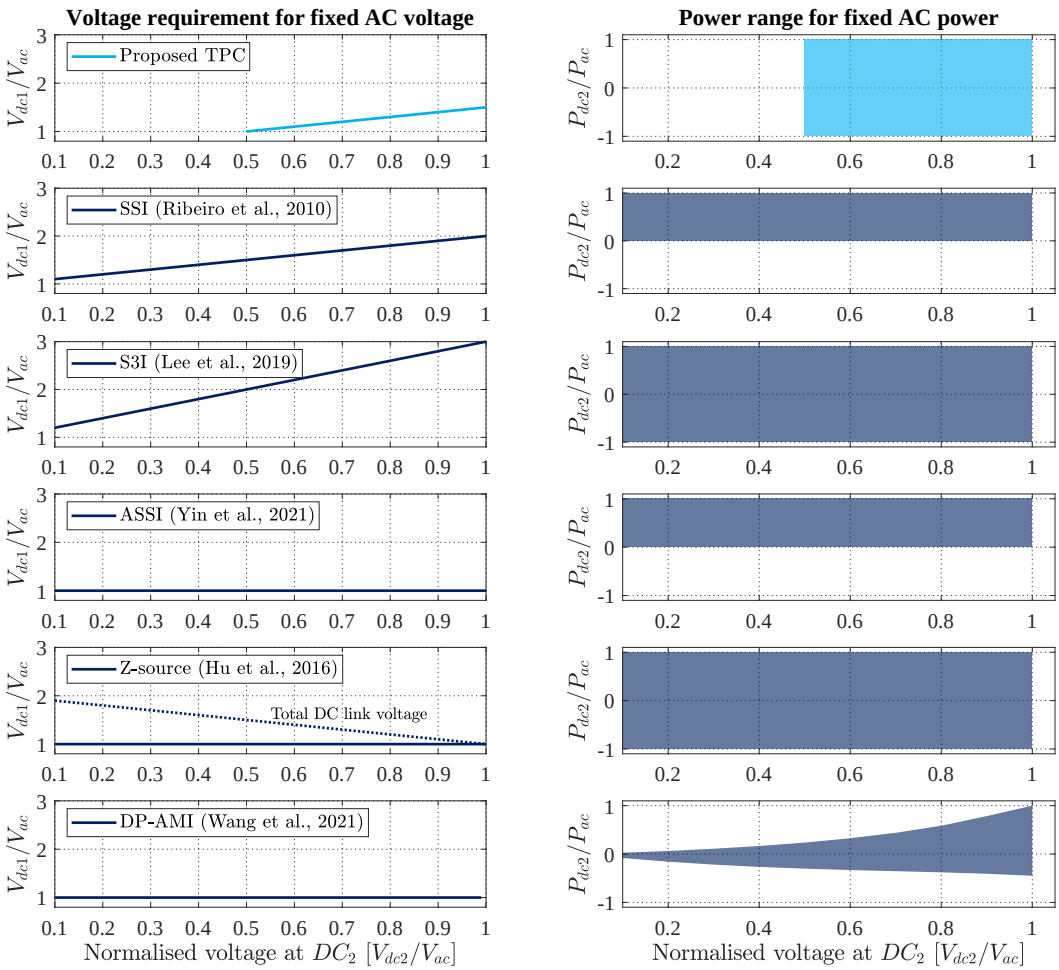


FIGURE 5.15. Characterisation of different single-stage three-port DC-DC-AC topologies. Left column: Voltage requirement on port DC_1 for different boost characteristics. Right column: Power capability of port DC_2 for different boost characteristics.

specific requirements in terms of the minimum voltages to define the power range that can be covered using a single power processing stage. Then, a comparative evaluation of the integrated dual-source DC-AC converters is performed considering a single-phase grid-connected scenario. The analysis defines a fixed base voltage for the AC port V_{ac} to then derive the required voltages at ports DC_1 and DC_2 to enable the operation and moreover, how the power range changes with these ratios.

Fig. 5.15 shows the voltage and power capabilities for the main topologies displayed in Table 5.7. The first row shows the proposed TPC, which presents boost capabilities for the port DC_2 limited by the required output voltage. Thus, the minimum voltage required at DC_2 is $0.5V_{ac}$, from there onward, the voltage at DC_1 increases linearly until $V_{dc1} = 1.5V_{ac}$ when $V_{dc2} = V_{ac}$. The converter shows fully bidirectional capabilities for its voltage range, allowing transferring of the total rated power on each port. The second row shows the split-source inverter, which shows boost capabilities for the entire range increasing the voltage on DC_2 linearly with DC_1. The power range is limited at the low voltage port, as the diodes limit the current to be unidirectional. Then, the simplified split-source converter is shown, illustrating the same boost capabilities as the SSI but with a higher requirement for DC_1. The power range for the S3I is fully bidirectional for the entire range, as the extra active device enables bidirectional current on DC_2. The active split-source inverter presents full-range boost capabilities without needing of increase the voltage on DC_1, thus reducing the voltage stress compared to previous solutions. Its power range is also unidirectional on port DC_2, limiting its use to photovoltaic PV arrays or fuel cells. The Z-source converter allows keeping $V_{dc1} = 1$p.u. for the entire boosting range, however the total voltage stress for switching devices varies following the dashed line. It presents bidirectional capabilities for all ports depending on the configuration for the impedance network. Finally, the dual-port asymmetrical multilevel inverter is presented, showing that voltage on DC_1 can be kept at 1p.u. for the entire range. This converter can provide power from DC_2 just at the instants where $V_{dc2} > V_{ac}$, as it does not include a boost interface. Thus, its power range is very limited compared to the previously shown three-port converters. The latter leads to the use of an auxiliary DC-DC converter complementing the operation of the converter on this category.

5.4. Chapter Conclusions

The proposed TPC in chapter 3 and the variation presented in chapter 4 were validated using simulation and experimental results to study its operation. The results show that the converter provides bidirectional power transfer capabilities for all its ports using

a single-power processing stage. Simulation models were used to validate its operation on grid-connected hybrid energy storage with solar generation capabilities and on a three-phase system feeding an inductive load from hybrid sources. The obtained results show consistency with the analysis presented in previous chapters, showing boost capabilities and low-frequency ripple-free current on the new DC port. Furthermore, the proposed modification of the topology including coupled inductors was also simulated to validate the enhanced operation reducing the circulating currents on the interface of port DC_2.

An experimental scaled-down prototype was used to check the topology operation and the features previously described. The results show a correct operation during a power reversal operation, validating the bidirectional capabilities of the converter. Additionally, the overall voltage and current waveforms agree with the results obtained with the simulation models.

The converter was modelled as a MIMO non-linear system in order to obtain the capability to control the power flow between the three ports simultaneously. The FCS-MPC shows an adequate response for the simulated and experimental tests allowing to follow of different power configuration references with good dynamic responses. Additionally, the computational burden is low given the simplicity of the topology, which simplifies the optimization algorithm execution. Also, the LQR plus modulation stage was proven in simulation displaying an improvement in the harmonic distortion of the AC output, which is fundamental for grid-connected scenarios.

Summarising, an assessment of the converter and the obtained results were performed to analyse its features compared against different single-stage DC-DC-AC converters. Analysis shows that the proposed topology minimised the number of active devices required for the three-port power transfer. However, it requires the inductors interface to connect port DC_2, which increases the overall volume and losses of the solution. The TPC shows to be competitive in terms of voltage requirements and power capabilities compared to the main topologies presented in chapter 2, given its voltage boost and bidirectional power transfer capabilities.

PART II: CONVERTER PROPOSAL FOR INTEGRATING ESS INTO HIGH-VOLTAGE SYSTEMS

6. MODULAR MULTILEVEL CONVERTER WITH INTEGRATED ENERGY STORAGE

The inclusion of ESS at the utility-scale appears as a fundamental development to support modern grid operation in terms of stability and resilience in the context of the rising inclusion of renewable sources and HVDC links, which do not contribute to the overall inertia of the system. Consequently, the capability to provide frequency regulation and other ancillary services to strengthen the system response to contingencies is becoming a requirement for high-power converters. In this regard, different approaches (described in chapter 1) to integrate ESS into MMC substations have been proposed to enable a partial decoupling of the power on the AC and DC sides, thus allowing the delivery of the mentioned ancillary services. The partial inclusion of ESS into the Sub-Modules (SMs) of the MMC shows a promising approach to minimise the number of extra devices required, considering the energy requirements for these services. Results from (Judge & Green, 2019) indicate that the replacement of 4% of all the SMs for Energy Storage Sub-Modules (ES-SMs) enables the injection of an extra 0.1 p.u. power from the ESS to either the DC or AC sides of the substation. Furthermore, (Errigo et al., 2019) shows that the inclusion of these ES-SMs could be performed at the phase level, but also at the stack level, using the circulating currents to perform the overall energy balance of the topology.

This chapter presents a different approach for integrating partially rated ESS into HVDC MMC substations, enabling the power flow to both DC and AC sides of the converter. The inclusion of the ESS is done with new branches connected in parallel with the inductors of each phase of the converter. The studied topology keeps the design of the original MMC unmodified, as it just adds partially rated ESS with electrical connections outside the valve hall. Therefore, this solution is suitable for retrofitting existing MMC substations to add services such as fast frequency response, load levelling or black start support.

The configuration and working principle of the studied topology is introduced in section 6.1, describing the main variables defining the system. The mathematical modelling of the topology is given in section 6.2. Section 6.3 provides an analysis of the operation of

the MMC stacks, considering the effect of the different parameters available to configure. Then, Section 6.4 describes the configuration of the partially rated ESS stacks to be connected to the MMC substation. Section 6.5 concludes the chapter with the main remarks of the presented topology.

6.1. Topology and Operation Principle

This section presents the proposed MMC topology with integrated ES connected in parallel branches with each phase. The topology adds partially rated ESS to the MMC, keeping the original infrastructure unmodified. Thus, the proposal aims to upgrade MMC substations, enabling the provision of ancillary services with minimum impacts on the original design. The inclusion of the partially rated ESS is performed using parallel branches to a portion of the phases of the MMC converter. The parallel branches consist of a partially rated dc-ac conversion stage connecting the ES units with the main MMC stacks formed by half-bridge SMs. This configuration allows placing the ESS in a separate allocation from the main valve hall and performing the connection at the existing busbars for the converter reactors, as shown in Fig. 6.1. The characterisation of these ES branches varies according to the original placement of the arm inductors in the MMC (either at the AC middle points of the SM stacks or at the DC terminals). These branches need to operate with the same insulation level as the MMC, considering that they connect to the same busbars. However, the voltage of operation is reduced as the ESS just provides a small fraction of the rated power for the substation.

Fig. 6.2 shows the proposed topologies for the two possible ESS-MMC substation layouts. The ES branches are connected to each phase of the converter in both cases, allowing energy exchange with the MMC stacks. The energy exchange is performed by a new circulating current operating at a different frequency from the ac and dc sides of the substation. This operation is possible due to the degree of freedom associated to the circulating currents of the MMC, which can be used for transferring power between the different stacks of the converter. Thus, the ES branches need to provide an ac voltage operating at the required frequency in both cases that consequently will drive the new current component.

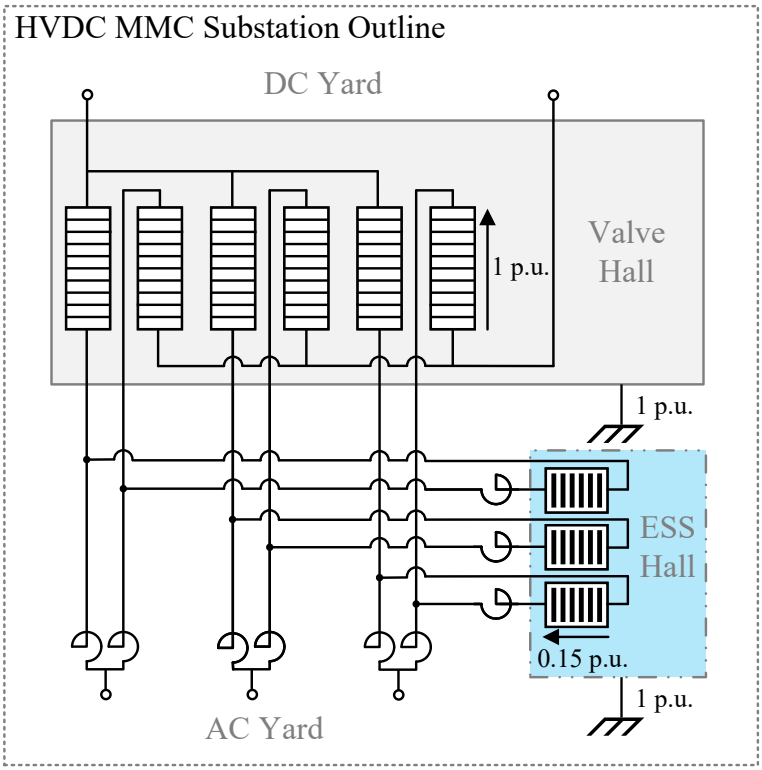
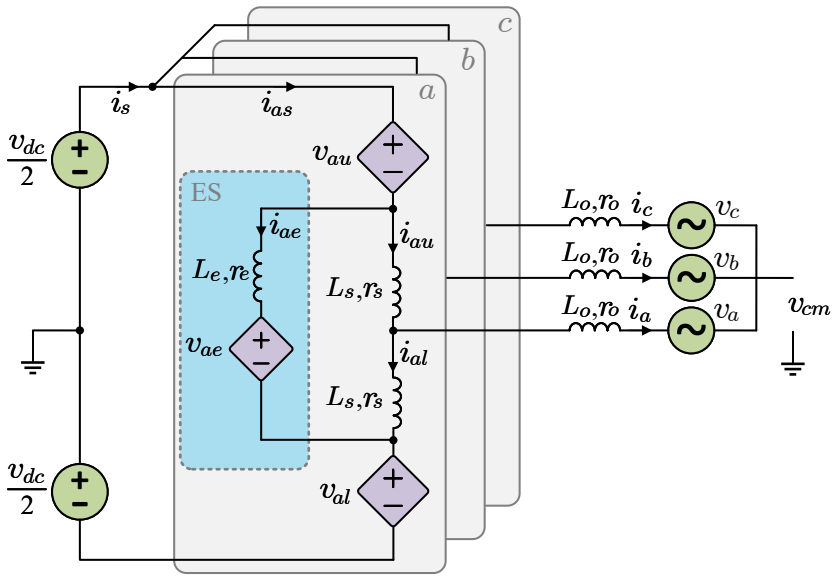
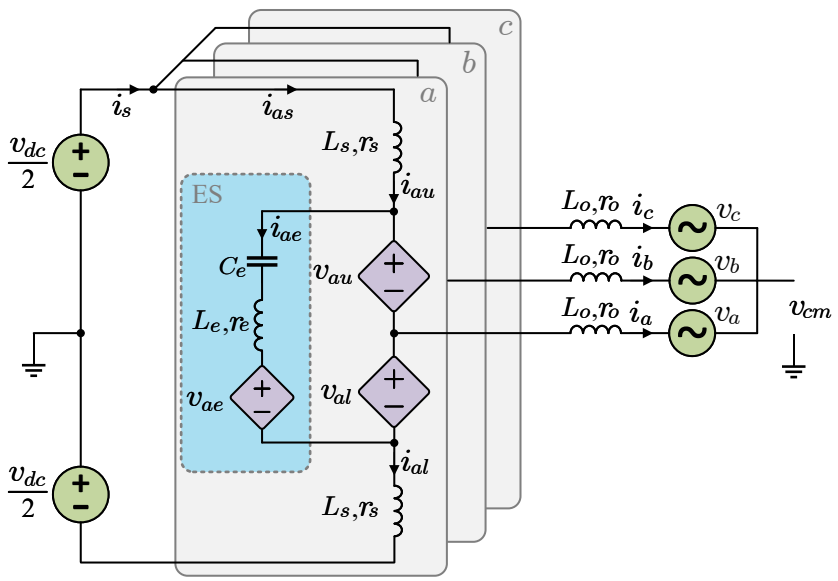


FIGURE 6.1. Example of the proposed outline for the upgraded MMC substation with ES.

Fig. 6.2(a) displays the configuration where the arm inductors are on the AC side of the converter. In this case, the ES branch connects in parallel with both arm inductors for each phase. The voltage across those inductors has a DC component close to zero in nominal MMC operation. Therefore, the output voltage of the ES converter is directly applied to them when there is a power transfer from the ESS. Otherwise, Fig. 6.2(b) shows the configuration where the inductors are placed on the DC side of the arms (Friedrich, 2010; Rohner et al., 2010). In this scenario, the ES branches get connected in parallel with the stacks of each phase. Consequently, the ES arm needs to support an additional dc component equal to v_{dc}. To avoid overrating the ES stack, Configuration (b) uses a capacitor in series with the ES stacks to provide the DC component while allowing the AC circulating current to pass through.



(a)



(b)

FIGURE 6.2. Proposed MMC with Parallel ES Branches. (a) Configuration with inductors at the ac side. (b) Configuration with the inductors at the dc side.

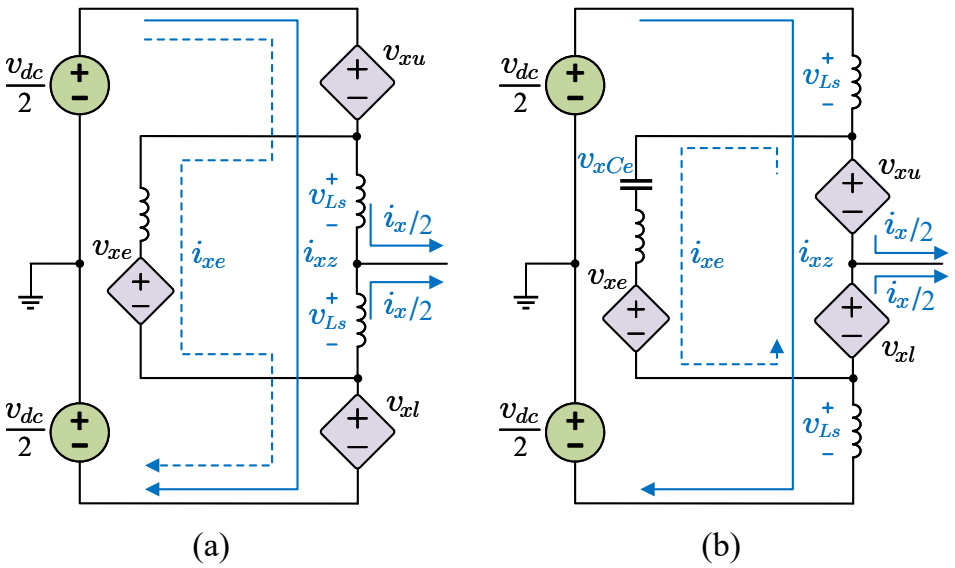


FIGURE 6.3. Currents through one phase of the converter. (a) Configuration with inductors at the ac side. (b) Configuration with the inductors at the dc side.

The proposed topologies operate using a third frequency component performing the energy transfer between the ESS and the MMC stacks. The extra frequency component provides a decoupling degree between the powers on the DC and AC sides, following the power transfer orthogonality principle (Chitransh et al., 2021; Ferreira, 2013). The new AC component is included in the circulating current of the converter to generate a limited ac voltage at the terminals of the ES branches. Then, a new current i_{xe} (with $x = \{a, b, c\}$) flows between the stacks and the ES branch to exchange power between them. The path for this new current changes depending on the configuration of the MMC substation. Fig. 6.3 illustrates the different paths for i_{xe}, together with the circulating and AC currents (i_{xz} and i_x respectively) for one phase of the topology. These currents are defined in the same manner as in a regular MMC, following expressions given in (6.1) and (6.2) with i_{xu} and i_{xl} representing the currents for the upper and lower stacks of each phase.

$$i_{xz} = \frac{i_{xu} + i_{xl}}{2} \tag{6.1}$$

$$i_x = i_{xu} - i_{xl} \tag{6.2}$$

6.2. Modelling of the converter

The dynamical model of the topology is based on a conventional MMC with the inclusion of equations for the ES branches. For the MMC, evaluating any of the configurations in Fig. 6.2 lead to expressions in (6.3) and (6.4), when considering the upper and lower paths from the ground on middle-point of the DC bus to the ground on the AC side.

$$\frac{v_{dc}}{2} - v_{xu} - L_s\frac{di_{xu}}{dt} - r_s i_{xu} - L_o\frac{di_x}{dt} - r_o i_x - v_x - v_{cm} = 0 \tag{6.3}$$

$$-\frac{v_{dc}}{2} + v_{xl} + L_s\frac{di_{xl}}{dt} + r_s i_{xl} - L_o\frac{di_x}{dt} - r_o i_x - v_x - v_{cm} = 0 \tag{6.4}$$

Then, (6.5) and (6.6) define the dynamics of the ac and circulating currents. These expressions are obtained by adding and subtracting (6.3) and (6.4) and considering the current relations in (6.1) and (6.2). Parameters r_s and r_o represent the parasitic resistances of the corresponding inductors and v_{cm} address the common-mode voltage if existing. These equations remain unmodified from the conventional MMC, as the topology of the main stacks is not changed.

$$(L_s + 2L_o)\frac{di_x}{dt} = (v_{xl} - v_{xu}) - (r_s + 2r_o)i_x - 2v_x - 2v_{cm} \tag{6.5}$$

$$2L_s\frac{di_{xz}}{dt} = v_{dc} - (v_{xl} + v_{xu}) - 2r_s i_{xz} \tag{6.6}$$

Then, the dynamics of the ES branches will be defined by different equations depending on the used configuration. Equation (6.7) regulate the dynamics of the ES currents for the topology with the inductors at the ac side (Fig. 6.3(a)). This equation also depends on

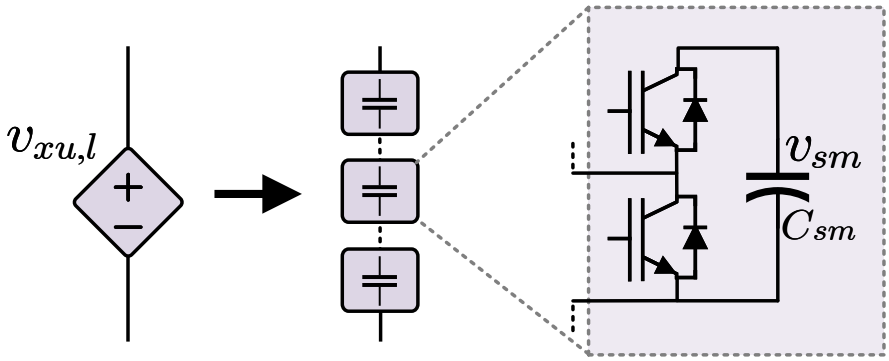


FIGURE 6.4. Stack equivalent model (left) and SM topology (right) for the MMC branches.

the common-mode term $(v_{xl}+v_{xu})$, showing a coupling degree between the circulating and the ES currents.

$$L_e\frac{di_{xe}}{dt} = v_{dc} - v_{xe} - (v_{xl} + v_{xu}) - r_e i_{xe} \tag{6.7}$$

The configuration with the inductors at the dc side (Fig. 6.3(b)) has a dynamical model containing one additional equation because of the included capacitor. Equations (6.8)-(6.9) describe the dynamics in this case for the ES currents and ES capacitors voltages.

$$L_e\frac{di_{xe}}{dt} = -v_{xe} + (v_{xl} + v_{xu}) - r_e i_{xe} - v_{xCe} \tag{6.8}$$

$$C_e\frac{dv_{xCe}}{dt} = i_{xe} \tag{6.9}$$

Therefore, both configurations can be represented by multi-variable dynamical models to regulate the power flow between the AC, DC and ES sides.

6.3. MMC Stack Analysis

The MMC stacks are the same as in a conventional MMC (shown in Fig. 6.4), as the idea is to keep the original electrical circuit unmodified. The proposed topology exploits the DoF associated with including an extra harmonic component in the total circulating current

in addition to the DC component essential for DC-to-AC power conversion, as in (6.10). Thus, the current through the stacks will contain the three different frequency components, following the outer power references P_{ac}, P_{dc} and P_{es}. The magnitudes of the DC and AC components of each phase are defined in the same way as in a conventional MMC and given in (6.11)-(6.13). The harmonic component related to the ESS depends on the parameters h and φ_z, which determine the harmonic order of the frequency and the phase angle of the component used for the power transfer between the ESS and the MMC stacks. The harmonic component should just interact with the ESS stack and the MMC stacks, but not with the AC and DC sides. Thus, there are two main restrictions for the proposal to operate correctly:

- Harmonic frequency should not be zero-sequence, as there would be harmonic pollution to the DC in this case.
- Operation of the ESS in the three phases must be coordinated to ensure the addition of the three harmonic currents is cancelled on the DC side of the MMC.

$$i^*_{xz} = I^*_{dc} + \underbrace{I^*_z \sin\left(h(\omega t + \theta_x) + \varphi_z\right)}_{extraDoF} \tag{6.10}$$

$$I^*_{dc} = \frac{P^*_{dc}}{3v_{dc}} \tag{6.11}$$

$$I^*_{ac} = \frac{P^*_{ac}}{3v_{ac} \cdot \cos\left(\varphi_{ac}\right)} \quad with \quad \varphi_{ac} = \arctan\left(\frac{Q^*_{ac}}{P^*_{ac}}\right) \tag{6.12}$$

$$i^*_x = I^*_{ac} \sin\left(\omega t + \theta_x - \varphi_g\right) \tag{6.13}$$

Then, the reference for the currents of the ES branches is shown in (6.14). The magnitude I^*_e depends on the power requirement $P_{es} = P_{ac} - P_{dc}$ and the voltage induced at the stack inductors by the circulating current. This voltage is defined in (6.15), considering the variables shown in Fig. 6.3.

$$i_{xe}^{*} = I_{e}^{*} \sin\left(h(\omega t + \theta_x) + \varphi_e\right) \tag{6.14}$$

$$v_{Ls}^{tot} = 2 \cdot v_{Ls} = 2 \cdot L_s \frac{di_{xz}^{*}}{dt} = 2h\omega L_s I_z^{*} \cos\left(h(\omega t + \theta_x) + \varphi_z\right) \tag{6.15}$$

Then, the expression for the ESS current magnitude is obtained in (6.16) by combining (6.14) and (6.15). The selection of $\varphi_e - \varphi_z = \pi/2$ ensures the minimum current magnitude for the required power. Additionally, it can be seen that the magnitude decreases when the selected harmonic frequency is higher.

$$I_{e}^{*} = \frac{P_{es}/3}{h\omega L_s I_z^{*} \sin\left(\varphi_e - \varphi_z\right)} \tag{6.16}$$

Therefore, the arm currents can be defined considering the three frequency components expressed in the above-described equations. Thus, (6.17) defines the arm current, where there are two fixed components given by the power references and two variable components which can be used to optimise the operation of the ES branch. The variable terms in (6.17) depend on four degrees of freedom:

- Harmonic frequency h
- Circulating current magnitude I_z^{*}
- Circulating current phase-angle φ_z
- Phase-shift between harmonic terms $\varphi_z - \varphi_e$

$$i_{xs}^{*} = \underbrace{I_{dc}^{*} \pm \frac{I_{ac}^{*}}{2} \sin\left(\omega t + \theta_x - \varphi_g\right)}_{DC-AC:fixed} + \underbrace{I_z^{*} \sin\left(h(\omega t + \theta_x) + \varphi_z\right) + I_e^{*} \sin\left(h(\omega t + \theta_x) + \varphi_e\right)}_{ESS:tunable} \tag{6.17}$$

The arm current and all other operation variables of the converter will vary depending on the configuration of the latter DoF. Fig. 6.5 shows the effect of the circulating current magnitude, for different harmonic selections, on the most relevant operation variables of

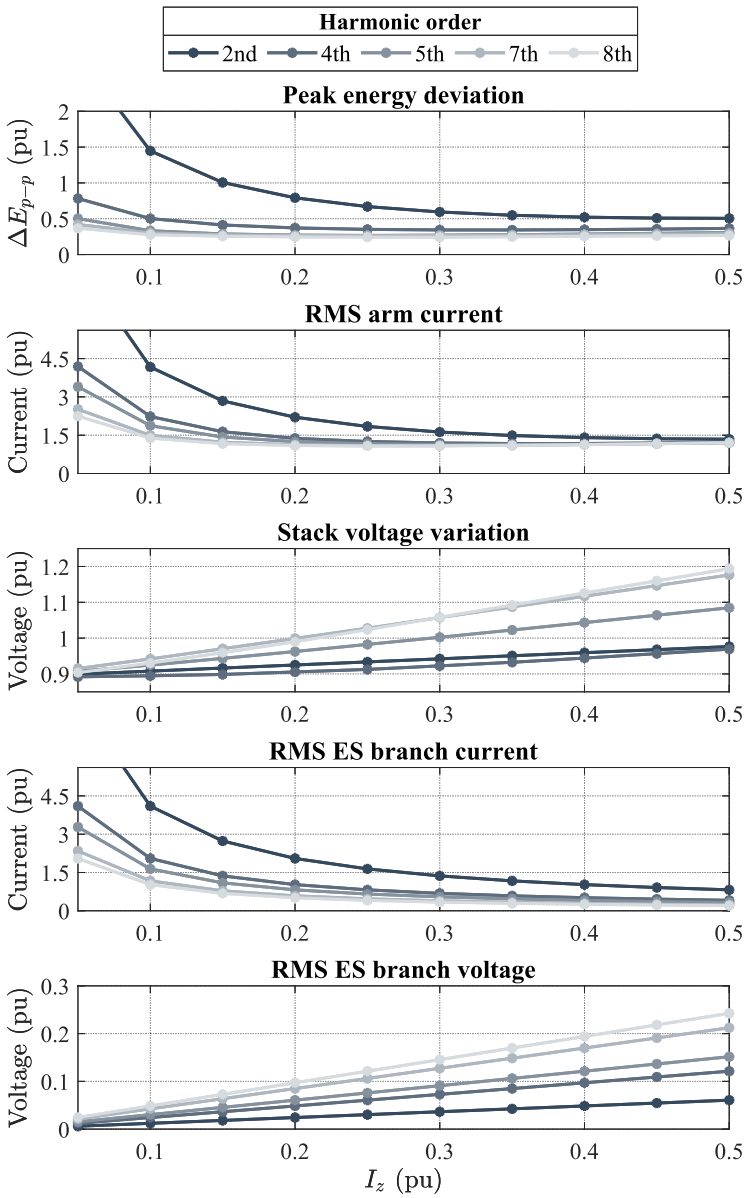


FIGURE 6.5. Effect of the circulating current magnitude on the converter variables for different frequencies.

the converter. An additional power delivery of 0.1 p.u. is considered from the ES, increasing the injected power to the ac side up to 1.1 p.u. As it is evident, higher frequencies provide the best operational conditions in terms of energy deviation and arm current peaks.

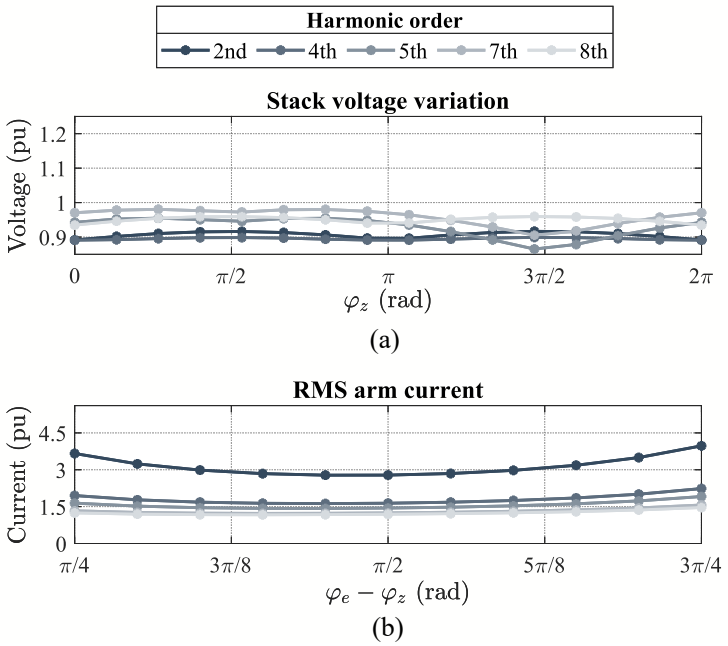
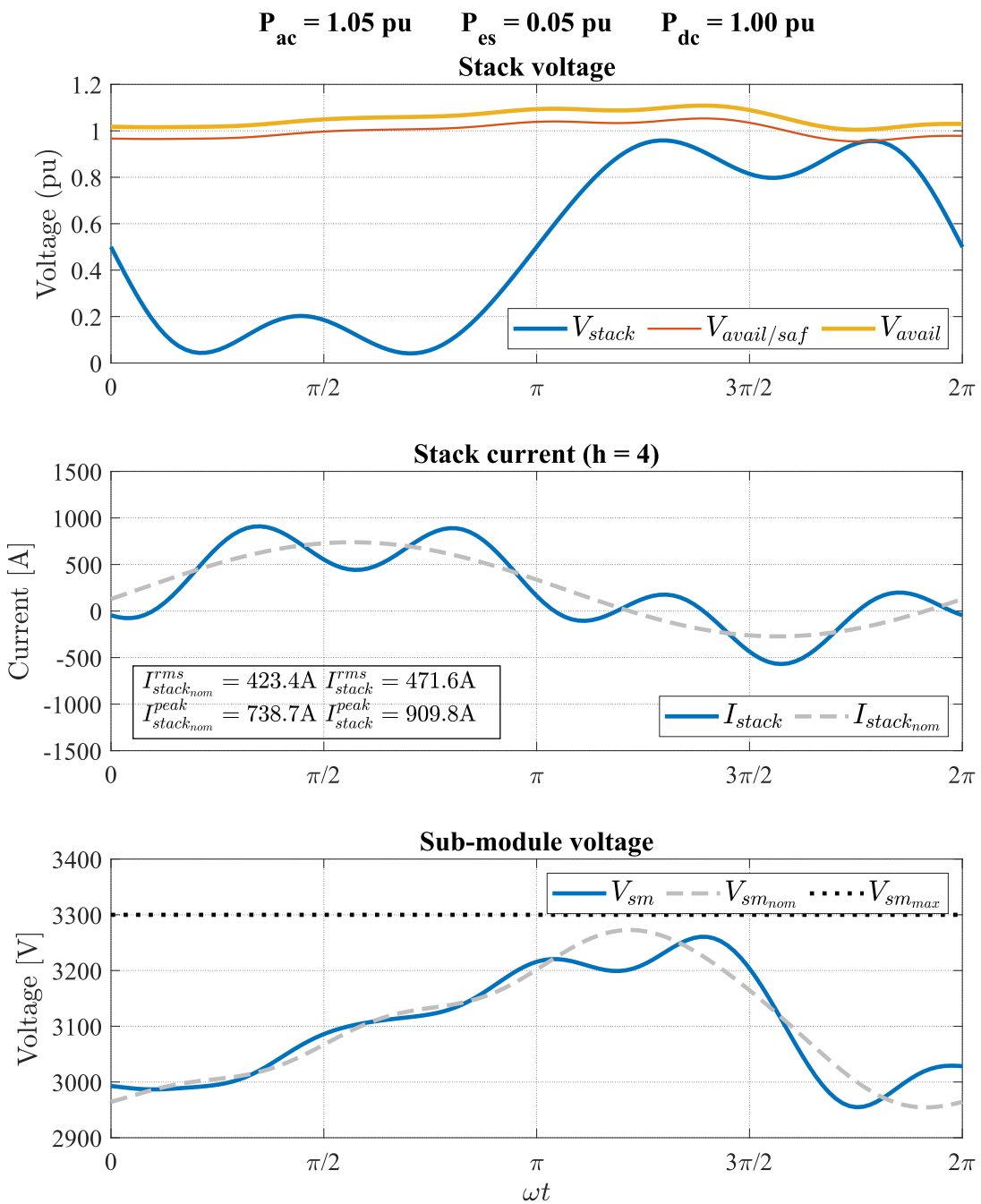


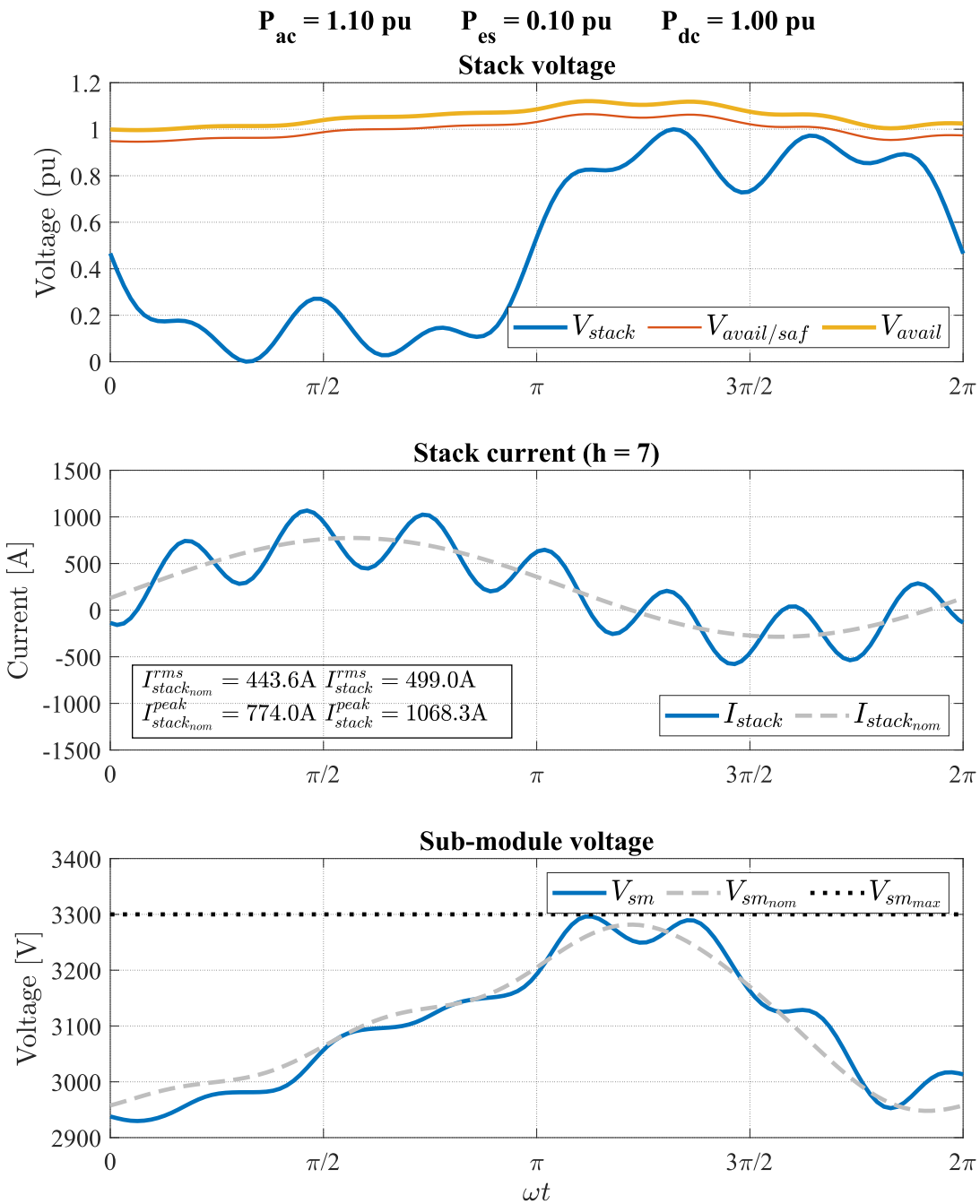
FIGURE 6.6. Effect of the harmonic phase angles for different frequencies. (a) Stack voltage variation for different circulating current phase angles. (b) Arm current variation for different phase-shift angles.

Furthermore, a circulating current magnitude between 0.1 and 0.2 achieve the minimum current stress within the voltage limits for the stacks.

The angles φ_z and φ_e have little impact on the main operative conditions of the converter. However, they can be used to optimise the operation of the system by reducing the stack voltage requirements and the arm currents magnitude for a given power reference. Fig. 6.6(a) illustrates the variation on the stack voltage required to deliver 0.1 p.u. power from the ES for a fixed circulating current magnitude. The voltage amplitude varies up to a 0.1 p.u. depending on the selected harmonic frequency and the phase-angle φ_z. Additionally, the phase angle between the circulating and ES currents ($\varphi_z - \varphi_e$) allows to move the peak position of the high-frequency term in the arm currents. Thus, it could be used to further reduce the maximum value by opposing it to the fundamental current peak (Fig. 6.6(b)). Nevertheless, this implies an increment of the reactive power processed by the ES converter.


P ac = 1.05 pu
P es = 0.05 pu
P dc = 1.00 pu
Stack voltage
Voltage (pu)
1.2
1
0.8
0.6
0.4
0.2
0
0
π/2
π
3π/2
2π
V_{stack}
$V_{avail/saf}$
V_{avail}
Stack current (h = 4)
Current [A]
1500
1000
500
0
-500
-1000
-1500
$I^{rms}_{stack_{nom}} = 423.4\text{A}$ $I^{rms}_{stack} = 471.6\text{A}$
$I^{peak}_{stack_{nom}} = 738.7\text{A}$ $I^{peak}_{stack} = 909.8\text{A}$
I_{stack}
$I_{stack_{nom}}$
Sub-module voltage
Voltage [V]
3400
3300
3200
3100
3000
2900
V_{sm}
$V_{sm_{nom}}$
$V_{sm_{max}}$
ωt

(a)



(b)

FIGURE 6.7. Operation of one arm of the proposed converter compared to a conventional MMC. (a) MMC-IPB with $P_{es} = 0.05$ p.u. and $h = 4$. (b) MMC-IPB with $P_{es} = 0.1$ p.u. and $h = 7$.

Finally, Fig. 6.7 exemplifies voltage and current waveforms during a partial power delivery from the ES branches for different harmonic frequencies and power references.

6.4. ES Stack Analysis

The topology integrates the ESS into the MMC using parallel branches to the converter phases. These branches consist of single-phase partially rated dc-ac converters generating an ac voltage at the defined harmonic frequency to exchange power with the main stacks of the MMC. The power rating of these converters depends on the ancillary service to provide. For example, the power reserve capacity of a 1 GW substation should be in the order of 10 to 50 MW for frequency regulation and black start support (ENTSO-E, 2021; Errigo, Morel, et al., 2022; National Grid, 2016; Stynski et al., 2020), ultimately representing a small fraction of the rated power for a classical MMC substation, e.g. 1% - 5%. Therefore, this work considers that the dc-ac converter integrating the ESS into the MMC should be capable of exchanging at least 5% of the substation rated power in both charging and discharging directions. The latter power requirement can be covered by considering a voltage rating of 0.15 p.u. for this DC-AC converter.

A multilevel cascaded topology is used to implement the partially rated converters connecting the ESS with the MMC phases, as shown in Fig. 6.8. The topology follows the modular approach of the MMC, distributing the ES units into a string of full-bridge SMs. Each ES-SM includes a bidirectional dc-dc converter interfacing the ES unit with the SM capacitor. The dimensioning of the ES-SMs depends on the operational parameters as the rated power and the rated voltage for the ES units. The size of the passive components of the ES-SMs is obtained following guidelines from (Pinto et al., 2021).

The cascaded ESS converter is connected to the MMC phases through a L or an LC interface depending on the original configuration of the substation (Fig. 6.3). The inductor for both cases is calculated following (6.18), where X_e is the required reactance, V_e represents the magnitude of the ES branch voltage, S_e is the power rating of the ESS and $\omega_e = h\omega$ is the frequency for the ES branch.

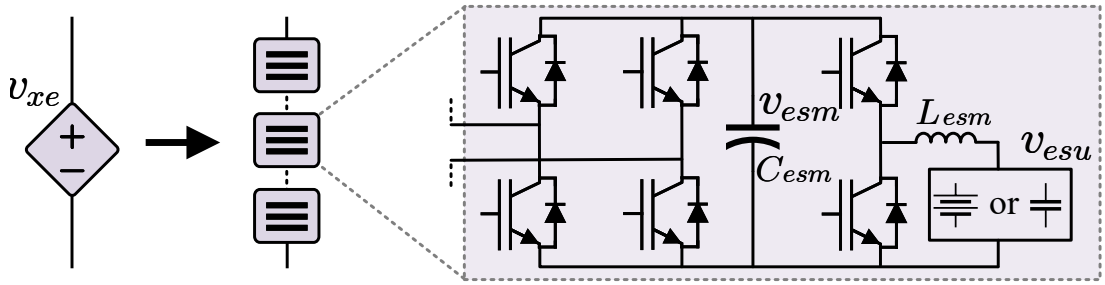


FIGURE 6.8. Stack equivalent model (left) and SM topology (right) for the ES branch.

$$L_e = X_{e(pu)} \frac{V_e^2}{\omega_e S_{es}} \tag{6.18}$$

Equation (6.19) describes the steady-state voltage of the branch capacitors for the configuration with the MMC inductors at the DC side. The latter is obtained by combining (6.9) and (6.14). The voltage includes a fixed component withstanding the voltage of the DC side and a variable oscillation depending on the current flowing between the ESS branches and the MMC stacks.

$$v_{xCe}^* = v_{dc} + \underbrace{\frac{I_e^* \cos\left(h(\omega t + \theta_x) + \varphi_e\right)}{C_e \omega_e}}_{\Delta v_{Ce}(t)} \tag{6.19}$$

Then, the ES branch capacitor is calculated by (6.20), which depends on the acceptable voltage variation Δv_{Ce} that the capacitor will have during the operation of the ESS at maximum current I_e^*.

$$C_e = \frac{I_e^*}{\Delta v_{Ce} \omega_e} \tag{6.20}$$

Finally, it is important to remark that the ESS branches need to be bypassed during DC or internal fault conditions, following the partially-rated voltage for these stacks (v_{xe} = 0.15 p.u.). Thus, the MMC substation should follow the same isolation procedure with the addition of bypassing the new ESS branches under the mentioned fault conditions.

6.5. Chapter Conclusions

This chapter analysed an original way to integrate Energy Storage into an MMC substation, where the ES units are connected in parallel to the arm inductors instead of inside the Sub-Modules or stand-alone on the AC or DC sides. This investigated topology enables the then-augmented MMC to deliver ES-related services while at the same time allowing the MMC to operate conventionally. The exchange of energy is achieved through an harmonic circulating current in the arms, trading off additional losses and higher energy deviation on the stacks with the convenience of keeping the original MMC station mostly unchanged. By acting on the harmonic order, phase angle, and magnitude of this circulating arm current, it is possible to achieve operating conditions where the maximum arm currents remain at the same level as in the conventional operation of the MMC; therefore, no upgrade of the semiconductors would be needed. An analytical study reveals a trade-off between the power rating exchanged between the AC, DC sides and ES, depending on the harmonic frequency of the circulating current, maximum arm current magnitude, SM voltage deviation, and stack voltage constraints. The proposed topology appears to be an efficient alternative to other ES systems found in the literature, thanks to its minimal required design changes and ability to deliver ES-related service during low power operating points.

7. DESIGN STUDY FOR THE MODULAR MULTILEVEL CONVERTER WITH INTEGRATED ENERGY STORAGE

The previous chapter presented the topology for an MMC with integrated partially-rated ESS using parallel branches to the converter phases. The analysis showed that there are different DoF to define the operation of the system, varying the power capability to deliver from the ESS and the losses of the converter. Thus, the control system plays a fundamental role, as it determines how the converter will operate depending on the used algorithms. Therefore, this chapter analyses how the design is tackled to exploit the DoF and optimise the additional power flow from the ESS.

The overall control scheme with the blocks regulating the new ESS current components is presented in section 7.1. Then, section 7.2 presents a case study design to illustrate the operational characteristics of the topology operated with the presented control system. Section 7.3 displays simulation results for the operation of the presented substation showing steady-state and dynamical response for the main waveforms of the topology. Finally, section 7.4 presents the main conclusions regarding the displayed results.

7.1. Control Scheme

The control scheme for the topology follows the same structure as a conventional MMC controller, as shown in Fig. 7.1. The main difference is the inclusion of the two highlighted blocks regulating the power flow of the ES branches. The present section details each block of the control scheme grouped by their main function (Conventional MMC or ESS integration related).

7.1.1. MMC operation related blocks

The main operational blocks for the proposed topology are the same ones as in a conventional MMC, as the configuration of the stacks in the converter remains unchanged. The first block calculates the references for the grid currents following the power requirements defined by the operator of the substation. The calculation follows (6.12) and (6.13), calculating the magnitude and phase-angle required based on the active and reactive power

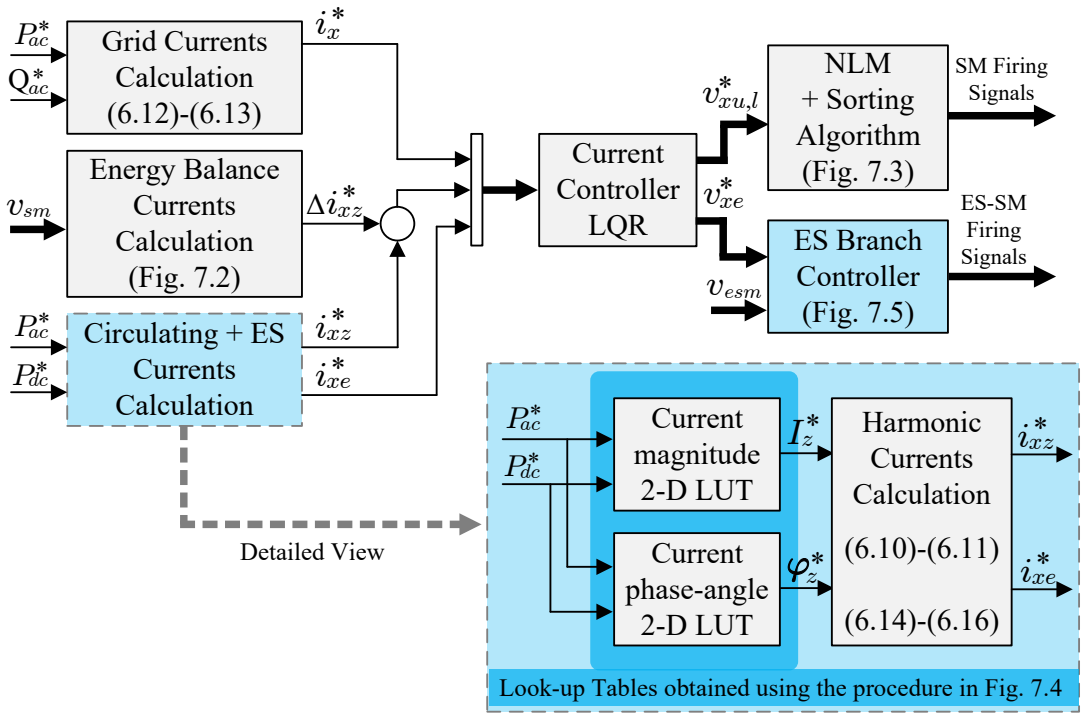


FIGURE 7.1. Overall control scheme.

to be exchanged on the AC side. The second block in this category is the overall energy controller that keeps the voltage of the MMC stack SMs on the required voltage level. The structure of this controller is shown in Fig. 7.2, illustrating three main components: The energy calculator; a horizontal balance to exchange energy between the phases of the converter and; a vertical balance to exchange energy between the upper and lower stack in each phase.

The energy calculator receives the measurement from the SMs of each stack and outputs a per-unit energy value to be used in the following controllers. This block includes a moving average filter to eliminate the second-harmonic (and higher frequencies) oscillations present in the SM that do not affect the mean value of the voltage. Then, the per-unit energy is calculated following (7.1) which uses the energy in (7.2) normalised by the nominal arm energy value in (7.3). All the definitions consider $x = a, b, c$ and $y = u, l$.

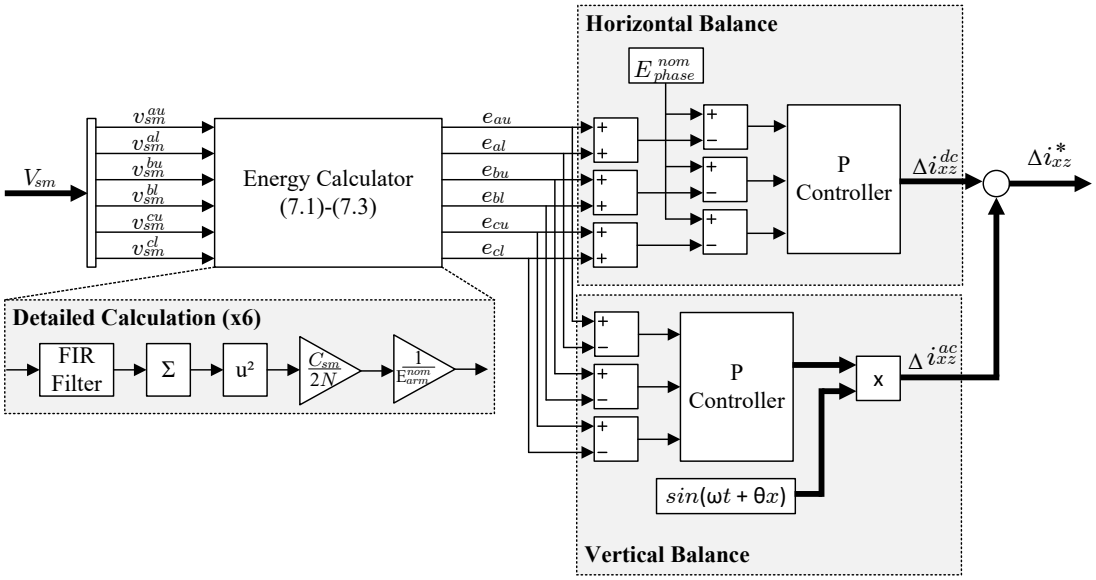


FIGURE 7.2. Detailed Energy Balance Block.

$$e_{xy} = \frac{E_{xy}}{E_{arm}^{nom}} \tag{7.1}$$

$$E_{xy} = \frac{C_{sm}}{2N}\left(\sum_{i=1}^{N} v_{smi}^{xy}\right)^2 \tag{7.2}$$

$$E_{arm}^{nom} = 0.5NC_{sm}\left(v_{sm}^{nom}\right)^2 \tag{7.3}$$

Then, the horizontal balance calculates a DC component to be included in the circulating current to regulate the phase energy to its nominal value $E_{phase}^{nom} = 2E_{arm}^{nom}$. This operation is done using a proportional controller, which can be complemented with an integral loop if needed. Finally, the vertical balance considers the anti-parallel fundamental AC voltages on the upper and lower arms of each phase to generate an AC current transferring energy between both arms. Both DC and AC balance components are then added to the overall circulating current to be regulated by the current regulator.

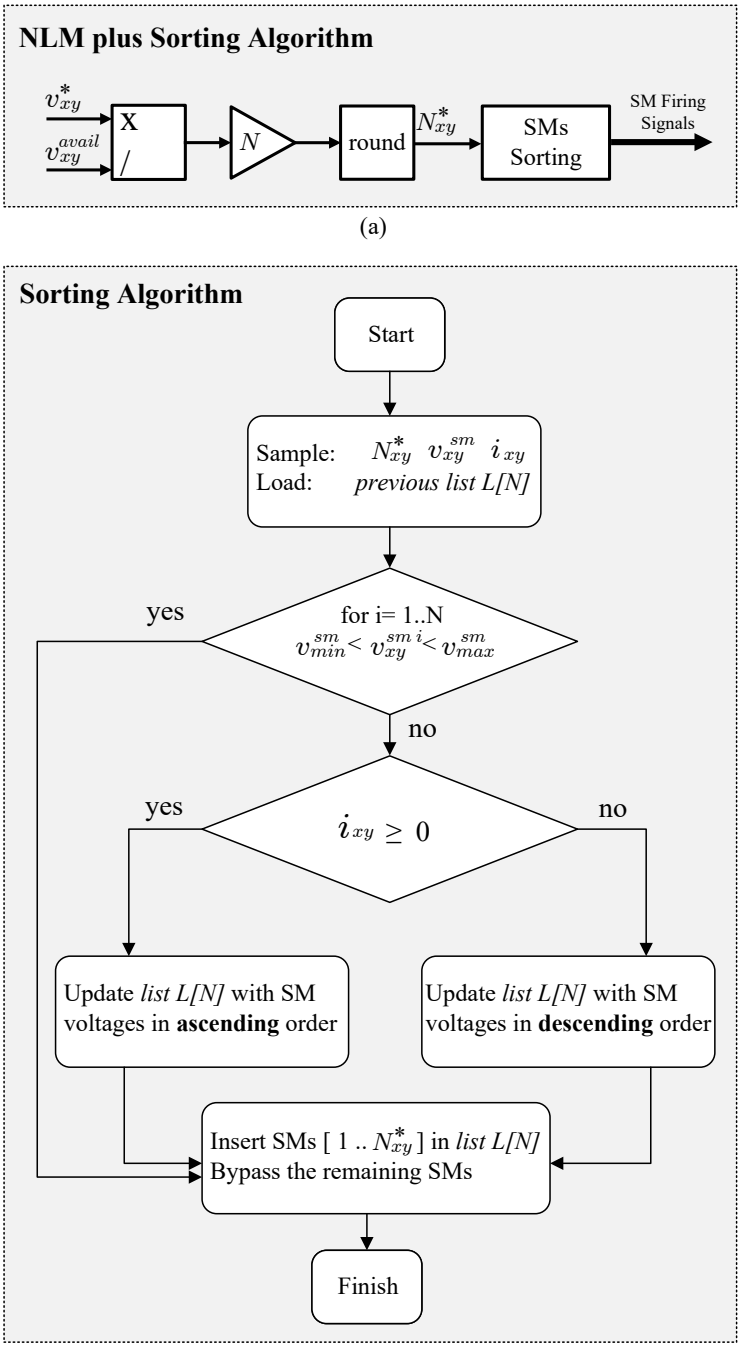


FIGURE 7.3. Nearest Level Modulation plus Sorting Scheme. (a) Overall scheme. (b) Sorting algorithm flowchart.

The third block in this category is the multi-variable current controller, which computes the required stack voltages to regulate all currents to the described references. An LQR controller is selected, considering the linear average model described by the dynamic equations (6.5)-(6.9). The output of this controller is then separated into two sets of variables, the voltages to be generated by the MMC stacks; and the ones for the ESS stacks. The MMC voltages use a standard Nearest Level Modulation together with a sorting algorithm to keep the energy balance of the SMs within each stack, which defines the last block of this subsection.

Fig 7.3(a) shows the overall modulation stage, where the number of SMs to be inserted is calculated with the reference voltage from the current controller v_{xy}^{*} and the total stack voltage v_{xy}^{avail}. Then, Fig 7.3(b) details the sorting algorithm used to select which SMs are inserted or bypassed. The algorithm uses a defined tolerance band for the SM voltages and updates the sorting list when any of them exceeds the limits. The list sorting depends on the direction of the stack current, which determines either ascending or descending order accordingly. Then, the required number of SMs is inserted using the most updated list, with the rest of them being bypassed. The procedure is standard for MMC topologies, with details available in Sharifabadi et al. (2016).

7.1.2. ESS branches operation related blocks

This subsection describes the two highlighted blocks in Fig. 7.1 related to the extra variables to control the ESS integrated into the MMC. The first block is on the outer layer of the controller and it calculates the harmonic components to be part of the circulating and ES branches currents. This block receives the references for the powers to be met at both DC and AC sides of the MMC and assign the ESS power accordingly to achieve the power balance for the converter. Then, the harmonic components can be assigned to optimise the magnitude of the total stack current following (6.17). Thus, these components are determined to minimise the current load of the stacks, while maximising the extra power capability to exchange between the ES branches and the MMC stacks. The latter

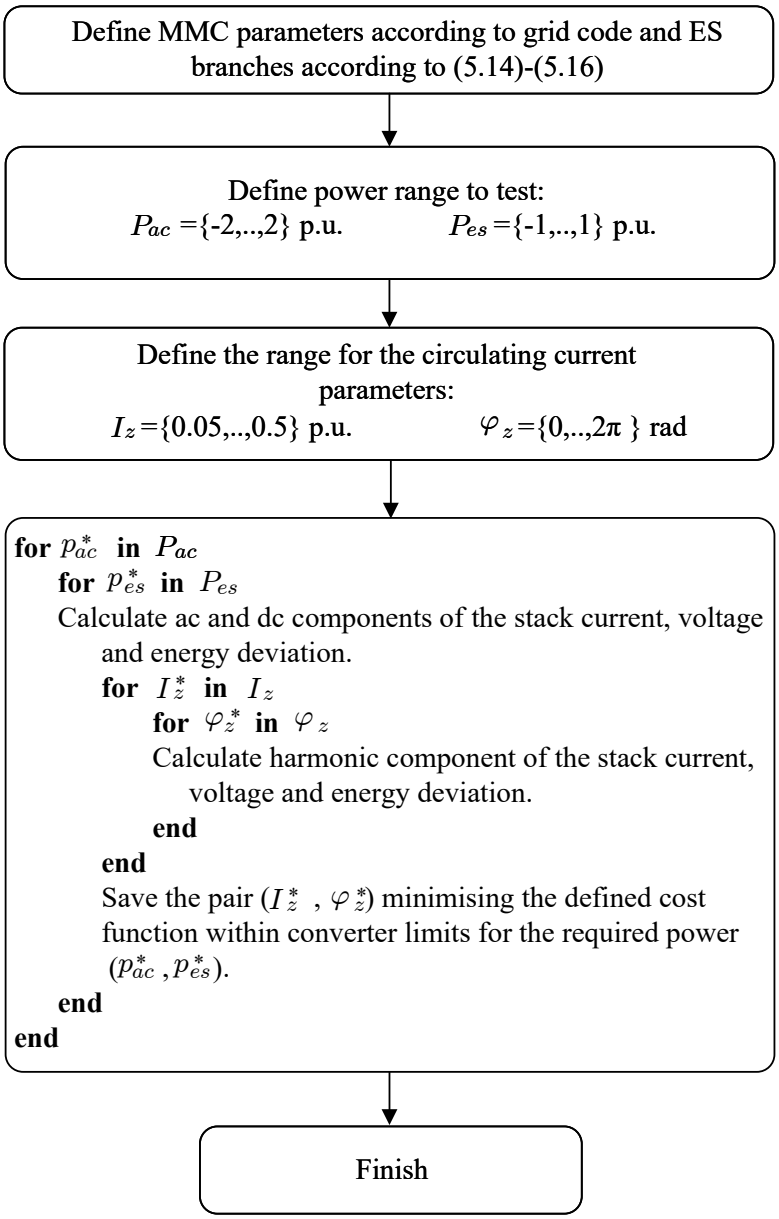


FIGURE 7.4. Flowchart illustrating the method to generate the circulating current parameters lookup tables.

is done through an offline optimisation process calculating the amplitude (I_z^*) and phase-angle (φ_z), for a matrix of (P_{ac}^*, P_{es}^*) points, that minimise the amplitude of the mentioned current. The process is detailed in Fig. 7.4 and results in the two look-up tables shown in

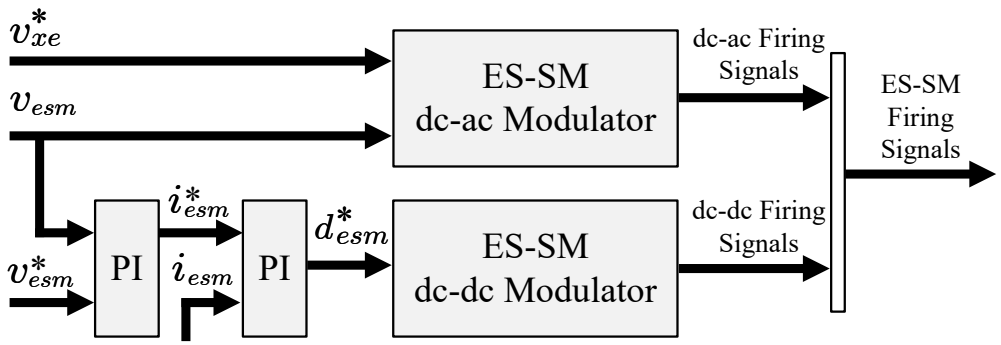


FIGURE 7.5. ES branches control scheme.

Fig. 7.1. Section 6.3 provides a further explanation of how these variables affect the total stack current (Figures 6.5 and 6.6). Furthermore, section 7.2 will present an analysis of how this optimisation process impacts the capability and the performance of the converter. Finally, the outputs of this block are used together with the grid currents calculation block and the energy balance block to define the references for all the regulated currents to be controlled with the described LQR controller.

The second block regulating the operation of the ESS receives the voltage reference to be generated from the multi-variable controller and computes the firing signals for the ES-SMs. This controller is presented in Fig. 7.5 and consists of two main loops regulating the switching of the DC-AC and the DC-DC converters in the ES-SMs. The upper block in Fig. 7.5 is a PWM stage generating the firing signals for the full-bridges of the ES-SMs to follow the voltage reference v^*_{xe}. Then, the lower part contains a cascaded control loop regulating the voltage of the capacitors of these SMs by acting on the current to be delivered by each ES unit. Next, this current is regulated with an inner controller that computes the duty cycle to be modulated in the second PWM block generating the firing signals for the DC-DC converter interfacing the ES units with the ES-SM capacitors. Altogether, this control section regulates the ESS branches to deliver the required power to the MMC stacks for achieving the commanded power decoupling between the DC and AC sides.

7.2. Case Study Design and Analysis

This section presents the operative conditions of the substation and the requirements to implement the additional partially rated energy storage capabilities. The base case is a standard 1 GW MMC substation with the parameters specified in the first section of Table 7.1. The design considers nominal energy of 40 kJ/MVA, an arm reactance of 0.1 p.u. and a number of 277 half-bridge SMs.

Then, the ESS converter follows the design outlined in the previous chapter. It is rated to operate at a maximum voltage of 0.15 p.u. and it should be capable of exchanging at least 5% of the substation rated power. The parameters for the branches are shown in the second section of Table 7.1. The design of the ES-SMs considers operative voltage of 1.5 kV and a maximum current ripple of 20% for the energy storage units. Both configurations share the same parameters, and the only difference is the inclusion of the series-connected capacitor in the case with the MMC inductors connected at the dc side.

The following subsections show a study on the operative conditions of the system, based on simulation results considering the indicated parameters.

7.2.1. Power Capability Analysis

This subsection explores the power capability of the converter to process the extra power from the ESS while keeping the operational limits of the base MMC substation. The limits to be considered are the ones that define the design of a MMC converter:

- Maximum current of the semiconductor devices: This value is set according to a 4.5kV/2000A IGBT device for the SMs.
- Maximum voltage of the SM capacitors: This voltage is set to 3 kV considering the aforementioned device.
- Maximum attainable voltage of the stacks: This limit is set to v_{dc} plus the ripple according to the operation point.
- Minimum attainable voltage of the stacks: This limit is set to 0, as half-bridge SMs are used.

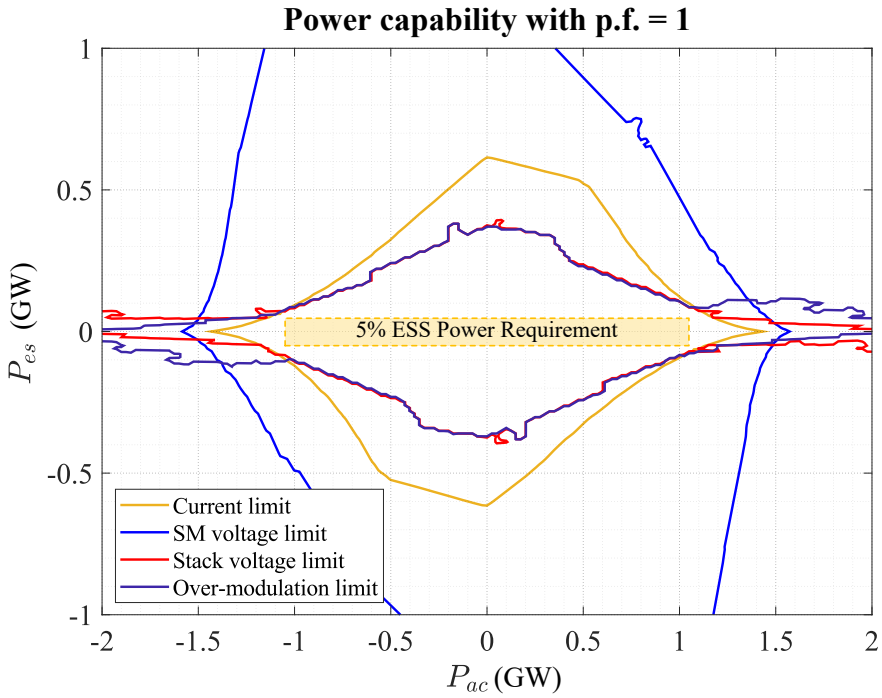
TABLE 7.1. Parameters of the Simulated Converter

Description	Parameter	Value
MMC Parameters		
DC voltage	v_{dc}	750 kV
Modulation index	m	0.94
Rated power	P_{rated}	1 GW
Transformer reactance	X_o	0.15 p.u.
Arm inductor	L_s	59.8 mH
		(0.1 p.u.)
Nominal SM voltage	v_{sm}	2.8 kV
SM capacitor	C_{sm}	6.6 mF
Number of SMs	N	277
ESS Parameters		
AC Voltage	v_{xe}	0.15 p.u.
AC harmonic frequency	h	8
Minimum rated power	P_{es}^{min}	50 MW
Branch inductor	L_e	19.9 mH
		(0.1 p.u.*)
Branch capacitor**	C_e	3.2 μF
Nominal ES-SM voltage	v_{esm}	2.25 kV
ES unit voltage	v_{esu}	1.5 kV
ES-SM capacitor	C_{esm}	3.3 mF
ES-SM dc-dc inductor	L_{esm}	3.2 mH
Number of ES-SMs	N_{es}	50
Switching frequency of ES-SMs dc-ac stage	f_{sw}^{dc-ac}	800 Hz
Switching frequency of ES-SMs dc-dc stage	f_{sw}^{dc-dc}	1.8 kHz

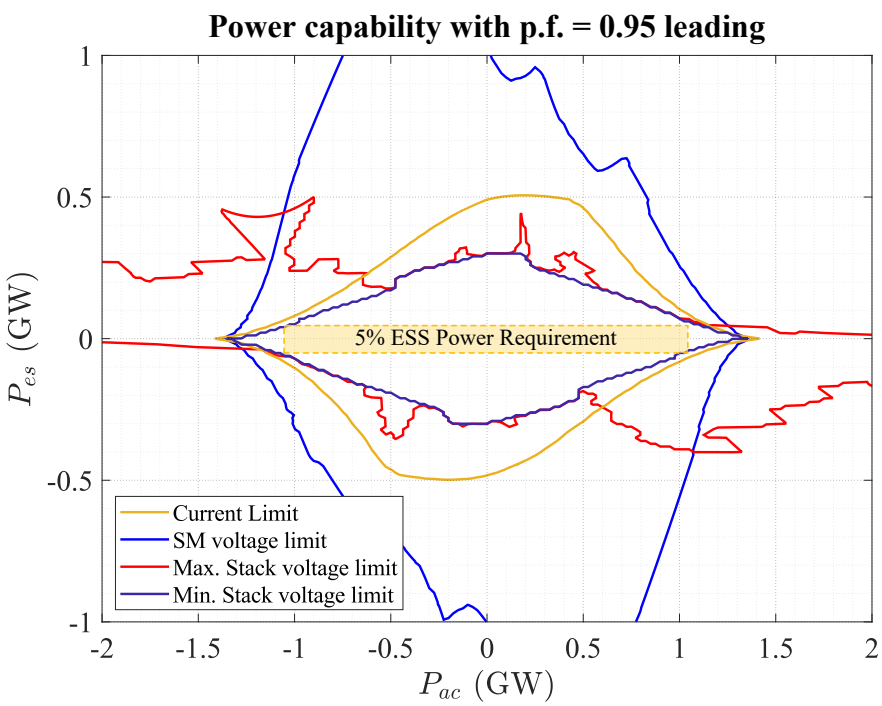
**Respect to the ratings of the ESS converter.*
***Configuration with inductors on the dc side.*

Then, a feasible area of operation is obtained by simulating the system operation for different power references (P_{ac}, P_{es}) and checking where the limits are reached.

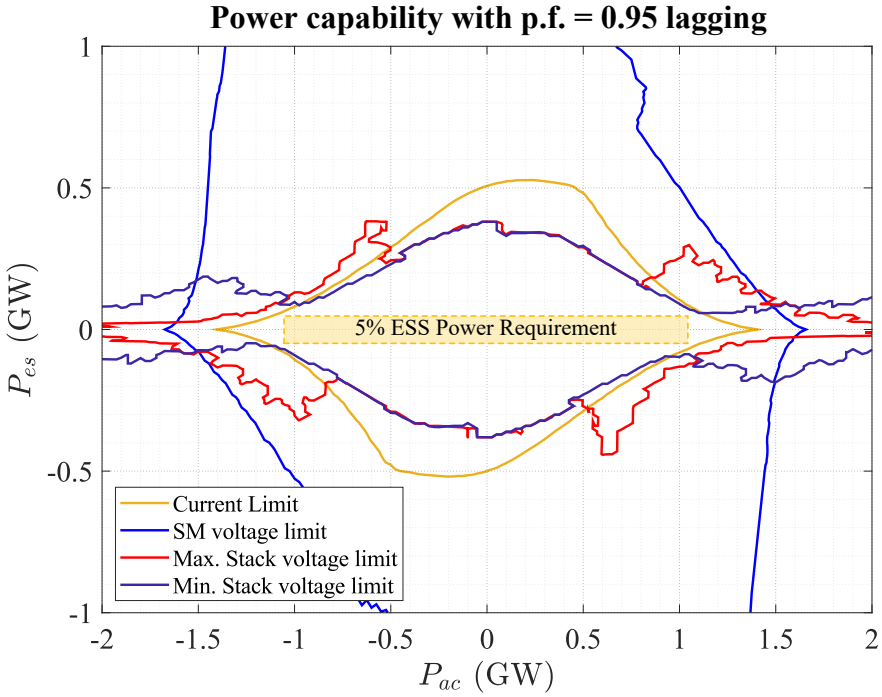
Fig. 7.6 shows how the feasible operation area of the proposal overcomes the minimum required for exchanging 5% of power from the ESS. Furthermore, the topology allows to exchange up to 37% of extra power from the ESS under partial load conditions without requiring any upgrade on the original MMC topology. The latter is relevant for substations interfacing wind turbine farms to the grid, as they could work at partial load conditions depending on the availability of the resource. Furthermore, plots (b) and (c) illustrate that the capability still complies with the 5% ESS power requirement for lagging and leading


Power capability with p.f. = 1
1
0.5
0
-0.5
-1
P_{es} (GW)
5% ESS Power Requirement
Current limit
SM voltage limit
Stack voltage limit
Over-modulation limit
-2
-1.5
-1
-0.5
0
0.5
1
1.5
2
P_{ac} (GW)

(a)


Power capability with p.f. = 0.95 leading
1
0.5
0
-0.5
-1
P_{es} (GW)
5% ESS Power Requirement
Current Limit
SM voltage limit
Max. Stack voltage limit
Min. Stack voltage limit
-2
-1.5
-1
-0.5
0
0.5
1
1.5
2
P_{ac} (GW)

(b)



(c)

FIGURE 7.6. Power capability plot of the converter for $h = 8$ with different power factors ($P_{dc} = P_{ac} - P_{es}$). (a) Operation with $\cos(\varphi_{ac}) = 0$. (b) Operation with $\cos(\varphi_{ac}) = 0.95$. (c) Operation with $\cos(\varphi_{ac}) = -0.95$.

power factors, which is an operational requirement for grid-connected converters. The capability plot shows that the stack voltage limits are the most restrictive because of the third frequency component required to exchange power with the ESS. Inversely, the SM voltage limit is the most permissive, as the higher frequency component has little impact on the energy variation of the SM capacitors. Simulations show that the feasible area is the same for both configurations, as the extra capacitor in the ES branch does not affect the variables in the MMC stacks. Also, the symmetry of the area indicates that the proposal can be used in both inverting and rectifying MMC substations.

The capability plot shown in Fig. 7.6 was obtained by using a cost function minimising the current peaks in the MMC and ESS stacks of the converter. Therefore, the feasible area within the current limits is maximised by selecting I_z^* and φ_z according to Fig. 7.4 using

the cost function defined in (7.4). This optimisation is performed offline using an iterative approach for obtaining the magnitude and phase-angle that minimise the current load for each pair (P_{ac}, P_{es}). Thus, the process optimise the operational area within the limits of the original MMC converter.

$$J = \lambda_1 \hat{i_{xs}} + \lambda_2 \hat{i_{xe}} \tag{7.4}$$

7.2.2. Power Losses Analysis

This subsection presents a study to quantify the extra losses generated by the semiconductor devices of the topology due to the additional power flow from the ESS. The study considers the use of a 4.5kV 2000A IGBT from ABB Semiconductors (ABB 5SNA2000K 450300), which specifications can be found in ABB (2018). The selection is based on the power and SM voltage for both MMC and ES stacks shown in Table 7.1. Therefore, every switching device in the simulated model is implemented using the selected device. Then, the associated loss data are obtained by simulating the converter to operate under different power references until reaching steady-state conditions.

The losses considered for the analysis include switching and conduction losses for all the devices in the MMC and ESS valves. The MMC stacks operate using a Nearest Level Modulation (NLM) plus a sorting algorithm to keep the voltage balance of the SMs. Thus, the average switching frequency will vary for different operational points, depending on whether there is a power exchange with the ESS. The ESS stacks use PWM blocks with different frequencies for the DC-AC and DC-DC stages, as shown in Fig. 7.5 and specified in Table 7.1. The losses are calculated using the data from the manufacturer for the specified device, which include the switching energies related to turn-on and turn-off events and the voltage drop while conducting current. Then, a time-domain simulation is used to obtain the total losses for the different power operation points defined, following a procedure as the one in Rohner et al., 2010.

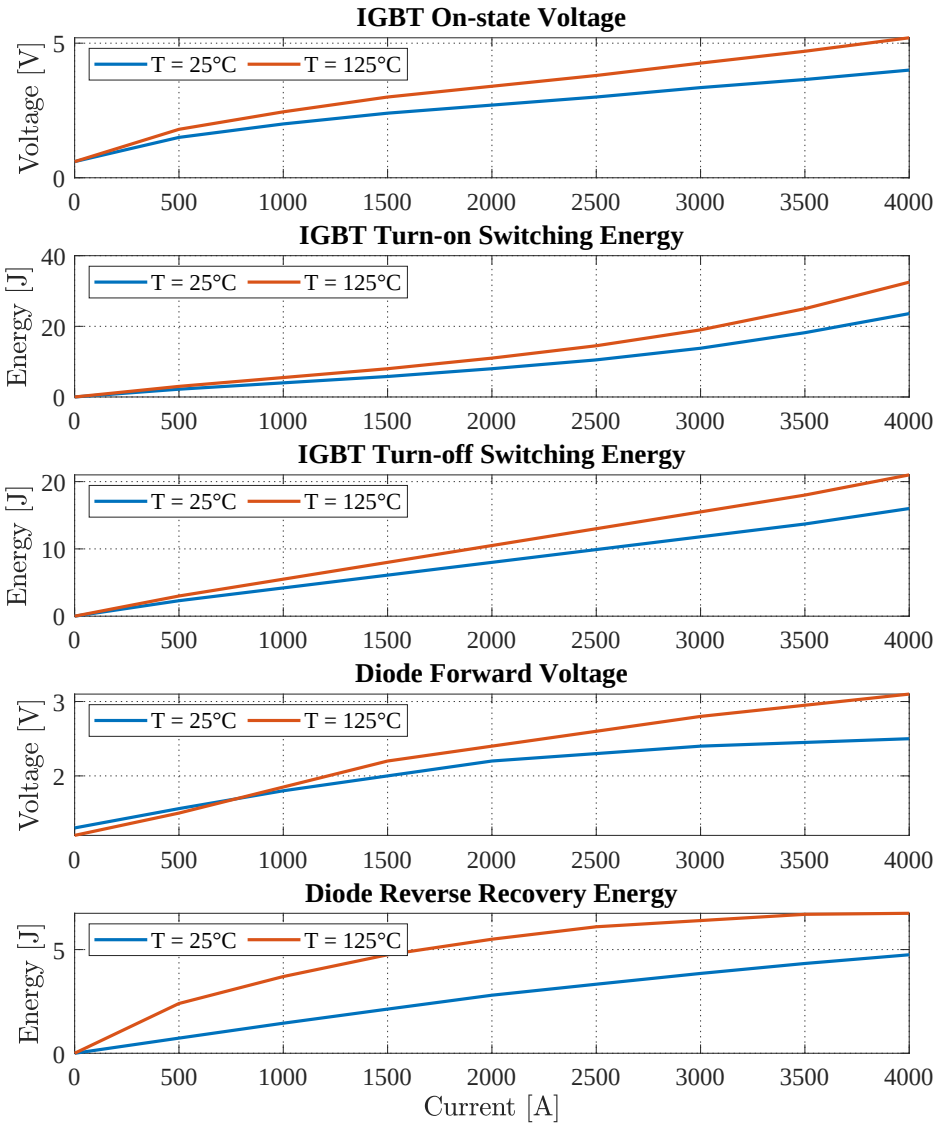
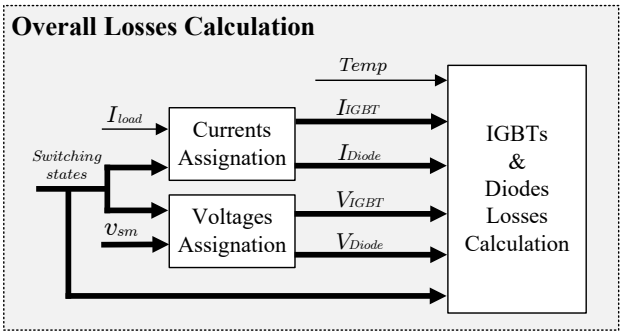
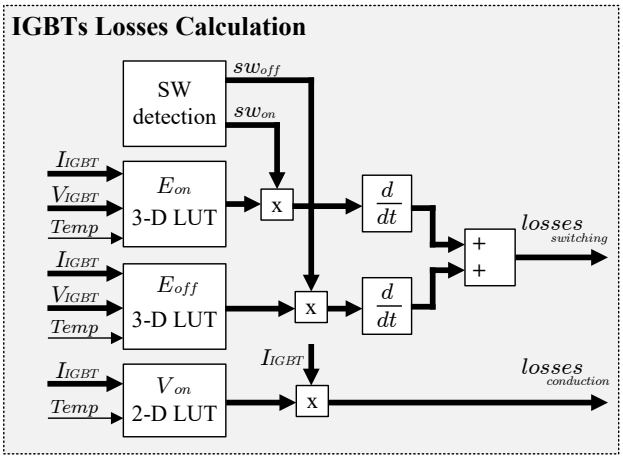


FIGURE 7.7. Conduction and switching losses characteristic for the selected device ABB 5SNA2000K450300 working at a reference voltage $V_{CE} = 2.8\ kV$.

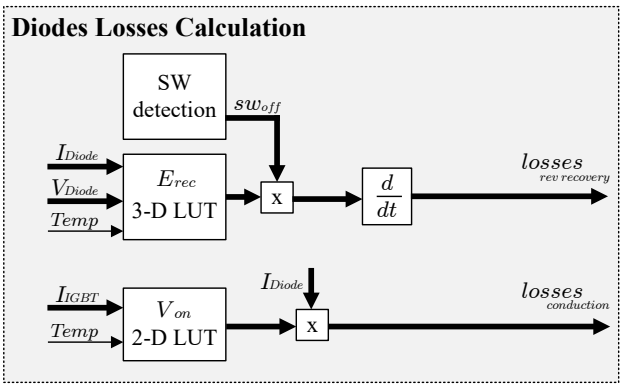
The included losses for each device are separated into IGBT-associated and Diode-associated, following (7.5) and (7.6). Thus, Fig. 7.7 shows the loss characteristics for the selected device considering two different operational temperatures. The data is plotted for a $V_{CE} = 2.8\ kV$ which matches with the operational SM voltage defined in Table 7.1. The data is used in the simulation models to obtain an average value for the losses for



(a)



(b)



(c)

FIGURE 7.8. Losses calculation diagram. (a) Overall losses calculation scheme. (b) IGBT-associated losses calculation. (c) Diodes-associated losses calculation.

every device and then added to obtain the power losses associated with every stack in the proposed topology. The overall procedure for calculating the losses of each stack follows the same structure, and it is shown in Fig. 7.8.

Fig. 7.8(a) displays the high-level blocks for calculating the losses of MMC and ESS stacks. The first blocks take the current load of the analysed stack, together with the voltage of each SM (or ES-SM) and assign the currents and voltages to every IGBT and diode included in the SMs based on the switching states. Then, the variables are used as inputs to the main block calculating the losses of the IGBTs and diodes for a fixed operating temperature set to 70°C in this study. Fig. 7.8(b) illustrate the calculation for the IGBTs losses using the data for the turn-on and turn-off energy characteristics and the conduction voltage drop across the device. Finally, Fig. 7.8(c) shows the procedure for the diodes of the SMs using the reverse recovery energy values and the forward voltage when the current is flowing through the diode.

$$P_{loss}^{IGBT} = P_{cond}^{IGBT} + P_{Ton}^{IGBT} + P_{Toff}^{IGBT} \tag{7.5}$$

$$P_{loss}^{Diode} = P_{cond}^{Diode} + P_{Rec}^{Diode} \tag{7.6}$$

Thus, Fig. 7.9 illustrates the overall semiconductor devices losses for a P_{ac} range of $\pm$1.1 p.u. and P_{es} varying between $\pm$0.1 p.u. The losses are kept under 1% of the substation rated power for the complete studied range. In this regard, the losses behave similarly to a conventional MMC in the horizontal axis because the current magnitude is the main losses generator in this direction (Conduction losses). However, the losses magnitude increases quicker in the vertical axis due to the inclusion of the harmonic component to exchange power with the ESS (Higher switching losses). Furthermore, the converter is less efficient when the ESS is delivering power ($P_{es} > 0$) than when it is absorbing power.

Fig. 7.10 shows the impact of including the harmonic component to exchange power with the ESS on the switching frequency of the MMC SMs. It shows that the resulting

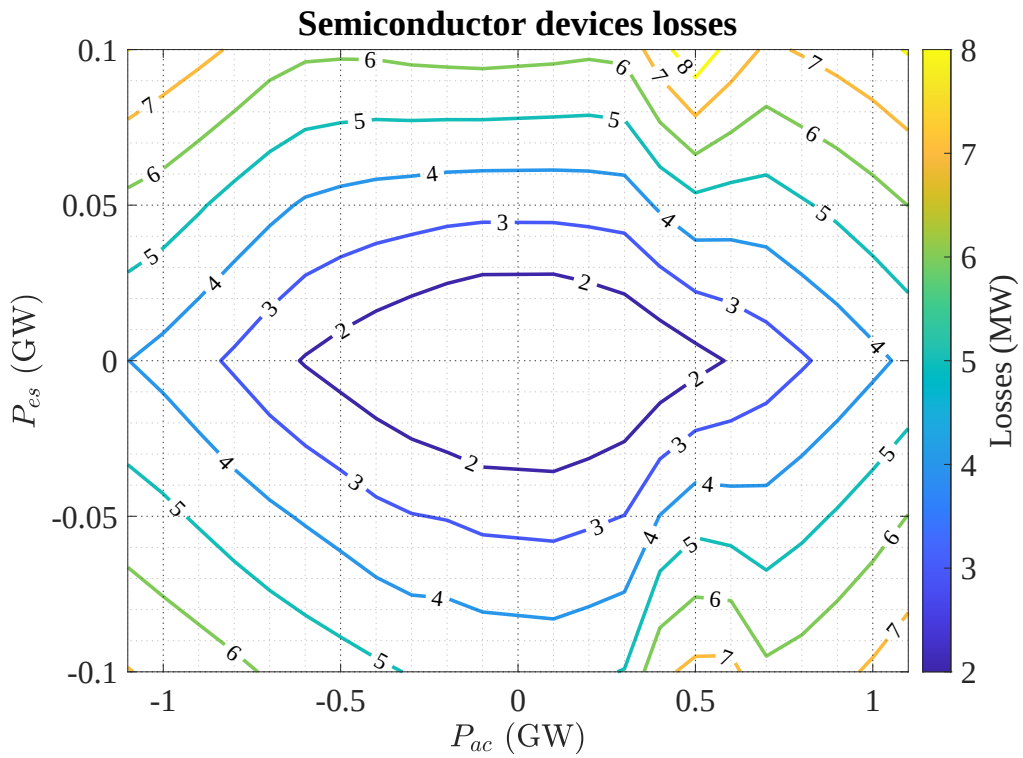


FIGURE 7.9. Losses associated to the switching devices for different power scenarios, where $P_{dc} = P_{ac} - P_{es}$.

switching frequency of the sorting algorithm for the nominal MMC operation ($P_{es} = 0$) is close to 120 Hz, matching the conventional frequency of these converters. Then, the switching frequency increases with the magnitude of P_{es}, as the stacks need to generate the new harmonic component ($h = 8$ in this case). However, the maximum reported switching frequency is less than 240 Hz, which keeps the losses under 1%, as shown in Fig. 7.9.

Therefore, the proposed system with the parameters in Table 7.1 can exchange $\pm 5\%$ of extra power on top of the original ratings of the substation without requiring upgrades on the main circuit. The losses at the semiconductors devices increase with the magnitude of the ESS power. However, the system gains the ability to provide some decoupling between dc and ac sides that is useful for services such as fast frequency response. Furthermore, the capability plot shows that the ESS can exchange up to 37% of extra power under partial load conditions if the ES branch converters are rated accordingly.

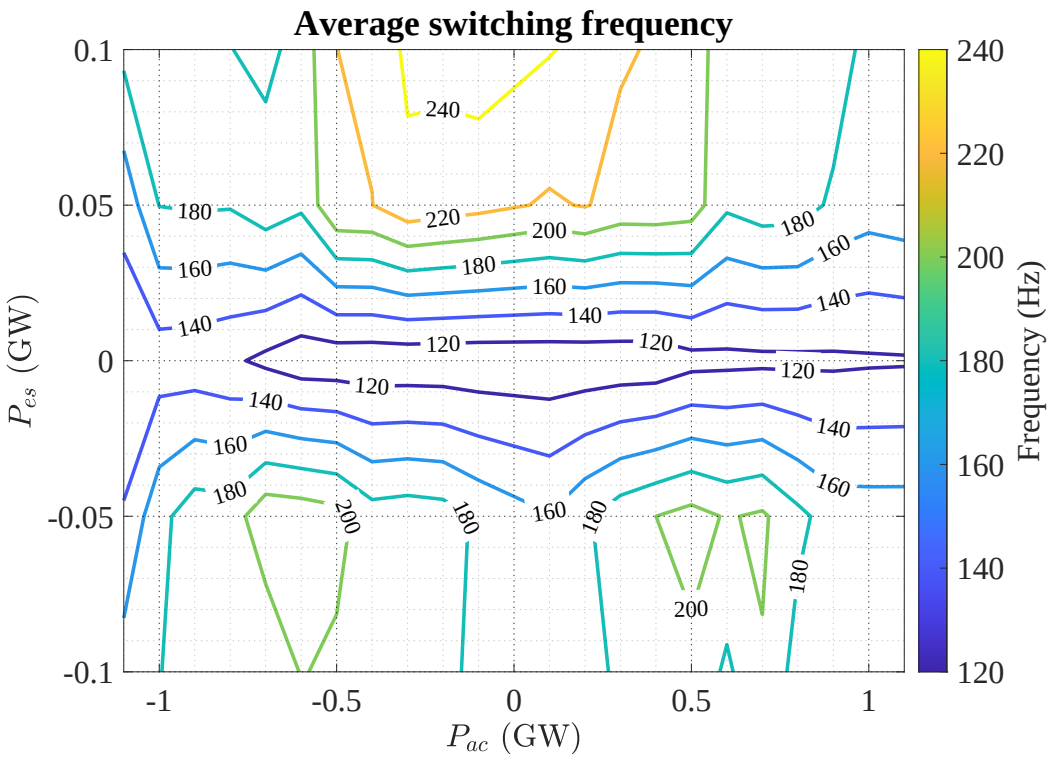


FIGURE 7.10. Resulting switching frequency of the MMC SMs for different power scenarios, where $P_{dc} = P_{ac} - P_{es}$.

7.3. Simulation Results

The proposed topology in chapter 6 with the control scheme presented in the previous sections was implemented in Matlab/Simulink to validate the operation for the analysed design case with parameters in Table 7.1. The implementation of the converter considers a vectorised approach to emulate the switching of every device in the SMs and ES-SMs, while keeping the computational time under reasonable limits. Thus, the following sub-sections describe the operation of the proposed system showing the relevant current and voltage waveforms involved.

7.3.1. General Waveforms for Both Configurations

This subsection presents steady-state results to illustrate general operational waveforms for the main variables of the proposed topology. The analysis considers both configurations presented in Fig. 6.2 representing a 1 GW MMC substation with extended capabilities due to the included ESS branches.

The location of the phase inductors in the MMC defines the configuration of the ESS branch to be used, as stated previously in chapter 6. Nevertheless, the only change between the two configurations is the inclusion of a series capacitor in the ES branch to address the dc voltage in the configuration with the inductors at the dc side. Therefore, the waveforms of the currents and voltages of the MMC stacks behaves in the same way for both configurations. Fig. 7.11 illustrate the MMC stack and ES branch waveforms for the system injecting 5% of extra power from the ESS. It shows how the stack voltage and current include a third frequency component at the defined harmonic frequency to perform the power exchange. Furthermore, the lower two plots depict the ESS converter current and voltage working at 400 Hz ($h = 8$).

Fig. 7.12 shows the voltage oscillation of the capacitor for the configuration in Fig. 6.3(b). The value of the capacitor C_e is chosen to limit the voltage ripple to $\pm 5\%$, which is verified in the plot. These capacitors represent in total 6.7% of the MMC stored energy considering that they withstand the value of v_{dc}.

7.3.2. Dynamic Response

This subsection presents the dynamic response of the system to changes in the power reference levels. The analysis is based on the topology in Fig. 6.2(a) as it has been shown that both topologies behave in a similar manner. The first half of the simulation shows the converter operating partial-load conditions to increase up to nominal power at both AC and DC sides at $t = 0.65$. Then, during the simulated period different degrees of decoupling are achievd by changing the power P_{es} exchanged by the ESS branches with the MMC stacks.

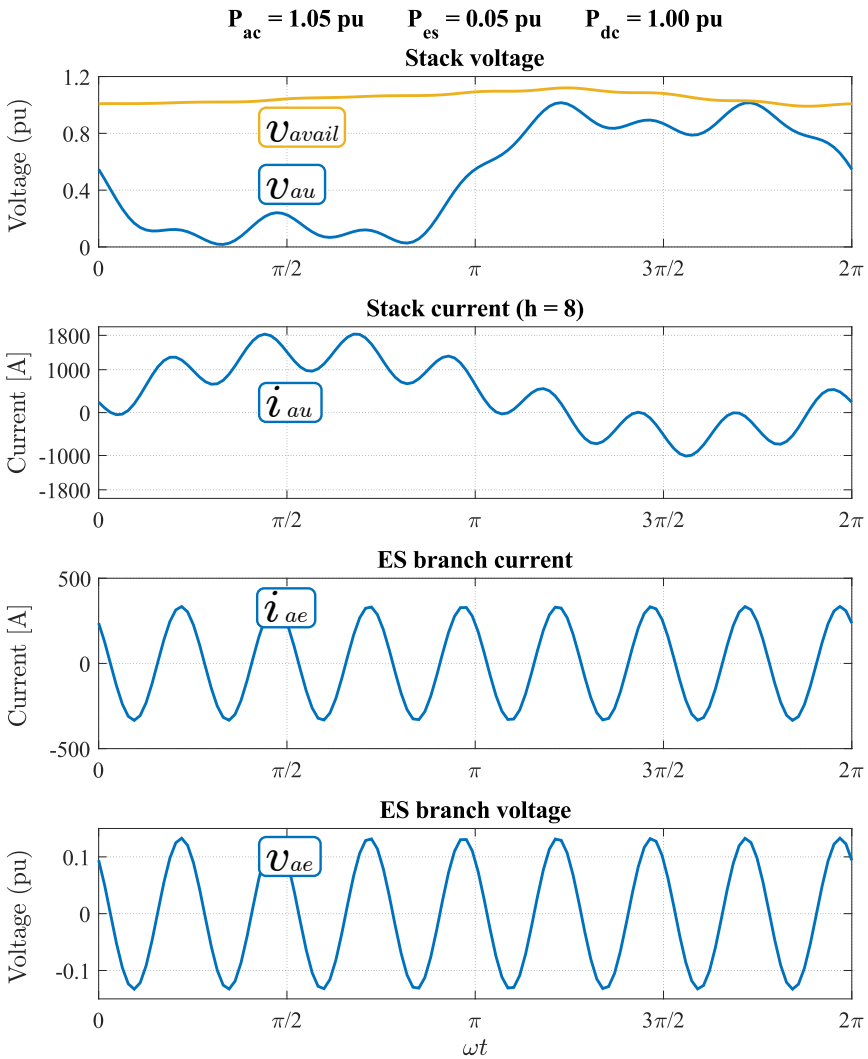


FIGURE 7.11. Steady-state waveforms for the converter injecting 5% of extra power from the ESS.

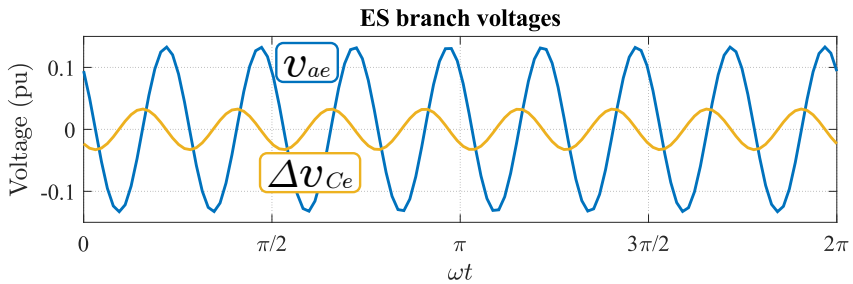


FIGURE 7.12. ES branch voltages for an injection of 5% extra power from the ESS with a branch type b (inductors at the dc side).

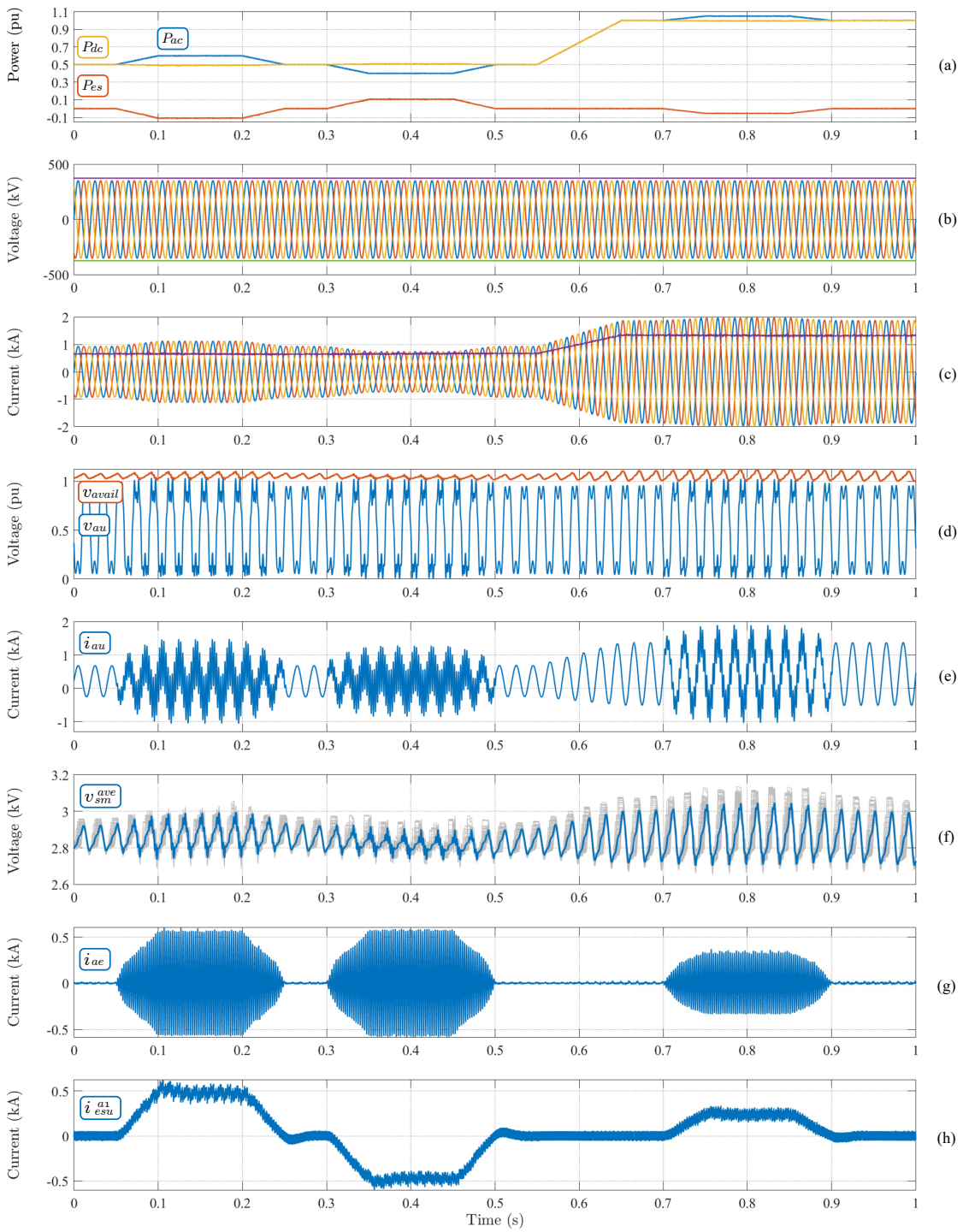


FIGURE 7.13. Dynamic response of the converter for different power reference levels. (a) Power requirements at ac, dc and ES sides. (b) ac and dc voltages. (c) ac and dc currents. (d) Stack voltages. (e) Stack current. (f) SMs voltages and average. (g) ES branch current. (h) ES-SM dc current.

Fig. 7.13 illustrates the operation of the system for different power references at the dc and ac sides. The ESS provides the required power to maintain the energy balance of the converter at all times, as shown in the plot (a) of the figure. Furthermore, it is shown that the system can provide $\pm 10\%$ of extra power from the ESS under partial load conditions and 5% at full load operation. Plots (b) and (c) display the ac and dc voltages and currents respectively, showing that the harmonic component is not present outside the converter. Plot (d) shows that the stack voltage requires a limited variation in terms of magnitude to generate the new harmonic component. The latter explains why the switching frequency and losses are kept within bounds, as they do not increase linearly with the harmonic frequency. Furthermore, the plot shows that the inclusion of the harmonic component in the MMC stacks do not affect the total available voltage, consisting of the sum of all the SM voltages in the stack. Then, plot (e) illustrates how the stack current includes the harmonic component only when there is power exchange with the ESS. The SM voltages are kept balanced using a regular sorting algorithm, plot (f) shows the variation of the average value with the inclusion of the harmonic frequency. The ES branch current operates at the selected frequency and it tracks the reference rapidly to start the power exchange with the main circuit, as shown in (g). Finally, plot (h) shows the current at the inductor of the dc-dc converter in the first ES-SM in the ES branch in phase a.

7.4. Chapter Conclusions

The proposed topology enables the inclusion of partially-rated ESS into MMC substations without requiring an upgrade on the ratings of the original SM-stack design. The added ESS is connected in parallel with the arm inductors and exchanges power through the use of specially developed, higher-harmonic, circulating currents. The maximum power which can be extracted from this ESS is limited by a combination of the maximum current magnitudes through the SM stacks, the lower and upper limits for the stack voltages, and the SMs voltage deviation. Thus, control algorithms have been developed to maximise the feasible power area within the operational limits of the original MMC. Results show that

the proposed system can provide up to 37% of extra power from the integrated ESS at partial load conditions in a simulated 1 GW substation. When the AC/DC power conversion is higher (e.g. over 0.4 pu), the ESS can still provide a minimum of 5% of power to the AC side for the entire range. The extra power capability agrees with the requirements for modern services from the HVDC substation, such as fast frequency response, load levelling, or total black start support.

The ESS is integrated into the substation using partially rated dc-ac cascaded converters connected in parallel with the phases of the MMC. Two variants of the topology are presented based on the electrical location of the arm inductors (either at the AC middle points of the SM stacks or at the DC terminals). Specific modifications to the ESS consider the inclusion of a capacitor for the case where the arm inductors are on DC terminal sides. Simulation results show that both variants work in the same manner, extending the results to both ESS configurations. The included ESS only contributes to the MMC substation losses in proportion to the amount of power processed by the ESS itself. The power losses for the entire MMC station increase by an additional 1% of the rated power for a power flow of $\pm 10\%$ from the ESS.

8. EXPERIMENTAL PROTOTYPE FOR THE MODULAR MULTILEVEL CONVERTER WITH INTEGRATED ENERGY STORAGE

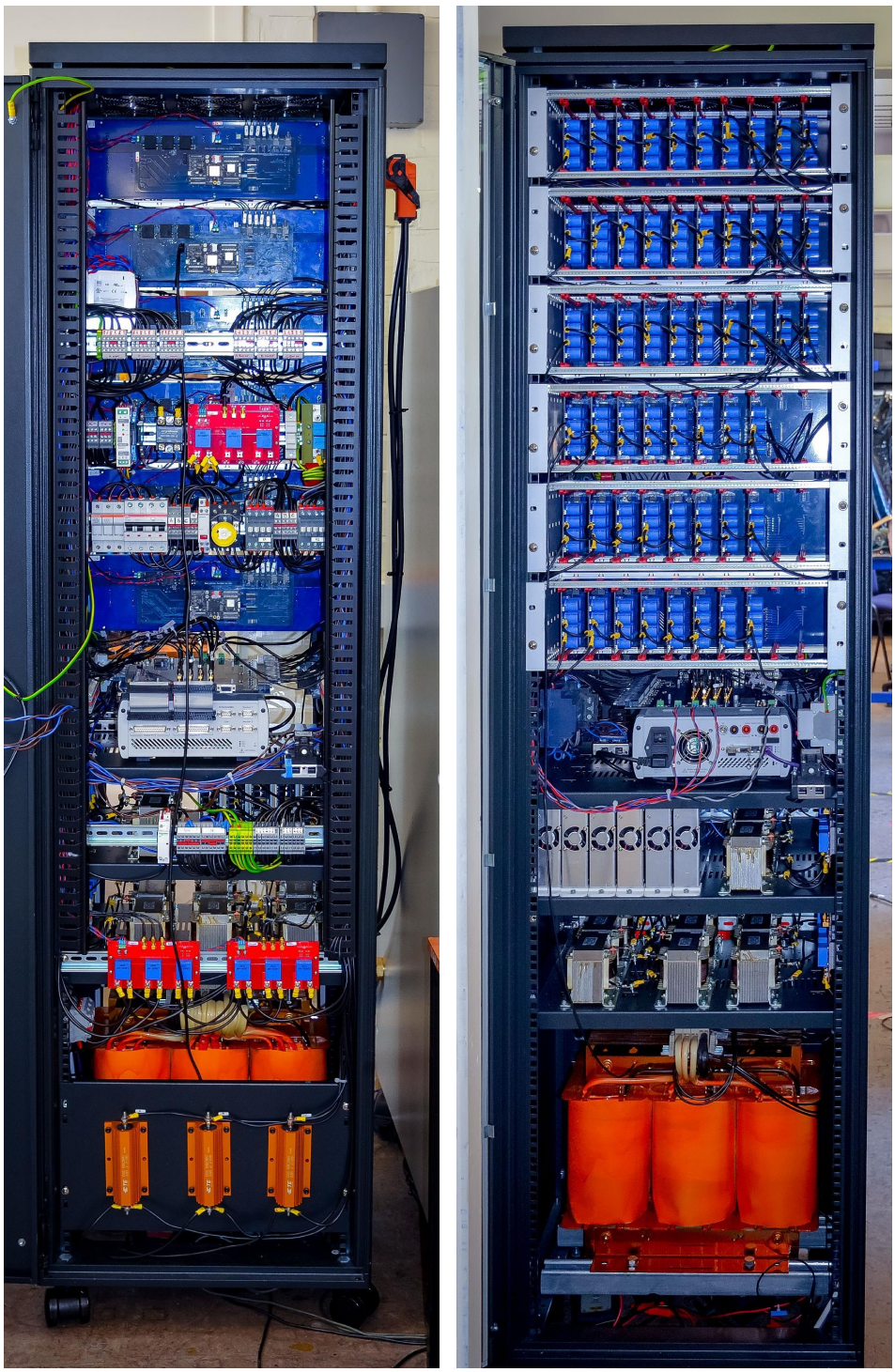
This chapter describes the development of a experimental setup to test the studied MMC with energy storage integrated into parallel branches. The hardware setup was designed, built and commissioned at the University of Edinburgh in a collaborative work with fellow PhD student Zoe Blatsi. The converter was developed to work primarily as a conventional MMC, with capabilities of testing different approaches for integrating energy storage units. The following sections will describe the converter specifications, the implementation of the hardware, the controller and the results obtained during operation.

8.1. Converter Specification

The objective of the converter is to be able of operating as a MMC with half- or full-bridge SMs, and also to allow the testing of different configurations to integrate ES units into the topology. Fig. 8.1 shows the built converter inside its cabinet. The grid interface transformer is mounted at the base, with pre-charge resistors attached on the back side; then, the inductors for the arms and the AC side follows in the next level; the third level upwards contain DC power supplies to emulate ES units; the central controller consist of a dSPACE MicroLabBox installed on the fourth level; and finally, the SM stacks including their local control units occupy the top half of the cabinet. The nominal operating parameters for the converter are displayed in Table 8.1.

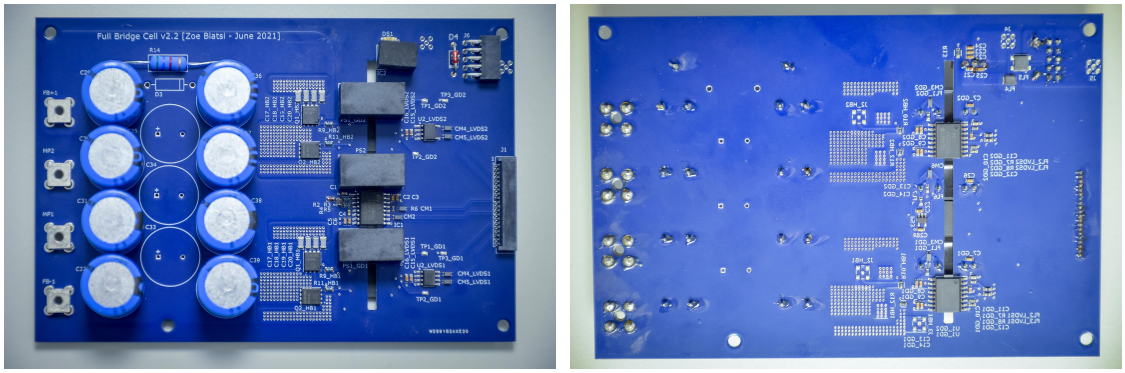
TABLE 8.1. Specifications of the MMC Setup

Description	Value
DC voltage	± 200 V
Power rating	4 kW
Number of SMs per stack	8
Type of SM	half/full bridge
Stack inductors	4.8 mH
SM capacitors	2.64 mF
Transformer arrangement	Star-Star
Transformer turns-ratio	1.21



(a) (b)

FIGURE 8.1. MMC Experimental Setup. (a) Rear View. (b) Front View.



(a) (b)

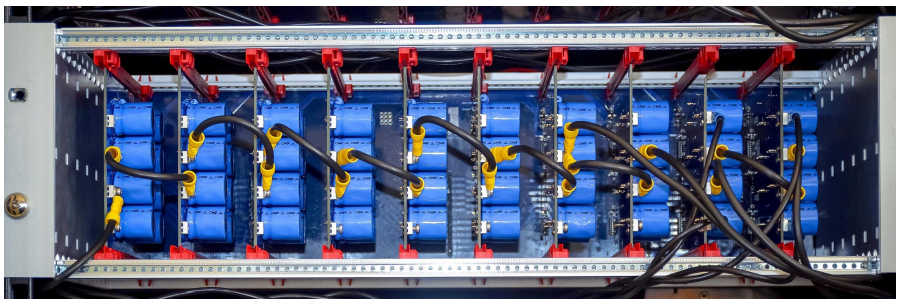
FIGURE 8.2. Sub-module board. (a) Top View. (b) Bottom View.

8.2. Overall Hardware Setup

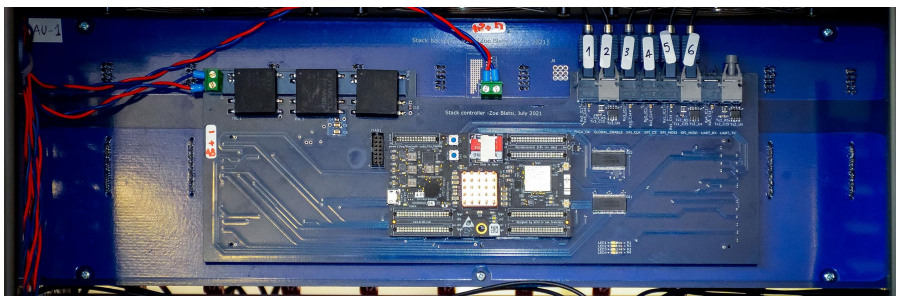
The converter is comprised of six stacks with capacity of connect ten SMs, but using eight for the main MMC circuit. The remaining positions are used to connect ES-SMs for the test of topologies with partially-rated ES, as explained later in the section. The SMs are flexible to operate as full- and half-bridge depending on the wiring of the prototype. Fig. 8.2 shows the implemented SM board used to build the MMC. The board includes a connector receiving the gate signals and sending the voltage of the DC bus, a MOSFET implemented full-bridge with the respective gate driver circuits, the SM capacitors with an isolated ADC device measuring the voltage, and power connectors to chain with the other SMs in the stack. The board implements the power stage isolated from the control side by using different power planes and isolated power supplies. The main design parameters of the SM boards are shown in Table 8.2. The SMs are mounted on a back-plane board routing all the LVDS signals and power supply for the control side of the SMs. The back-plane board also connects to the local control units, implemented using System-on-Chip (SoC) ICs mounted on the rear side of the board. The stack back-plane configuration is displayed in Fig. 8.3, showing the SMs side and the local controller side. AMD/Xilinx Zynq-7020 system is used as local control unit, connecting with all SMs of the stack through LVDS signals. The connection with the central control unit is performed through an optically isolated Serial Peripheral Interface (SPI) bus shown on the top right corner of Fig. 8.3(b).

TABLE 8.2. Specifications of the Sub-Module

Description	Value
Semiconductor devices	4x MOSFET Infineon BSC600N25NS3
SM capacitance	2.64 mF
Gate drivers IC	2x Texas Instruments UCC20520DW
Power supplies	3x Murata MEJIS2412SC 12V
Isolated voltage measurement IC	ST-Microelectronics ISOSD61L ADC
Communication bus	LVDS



(a)



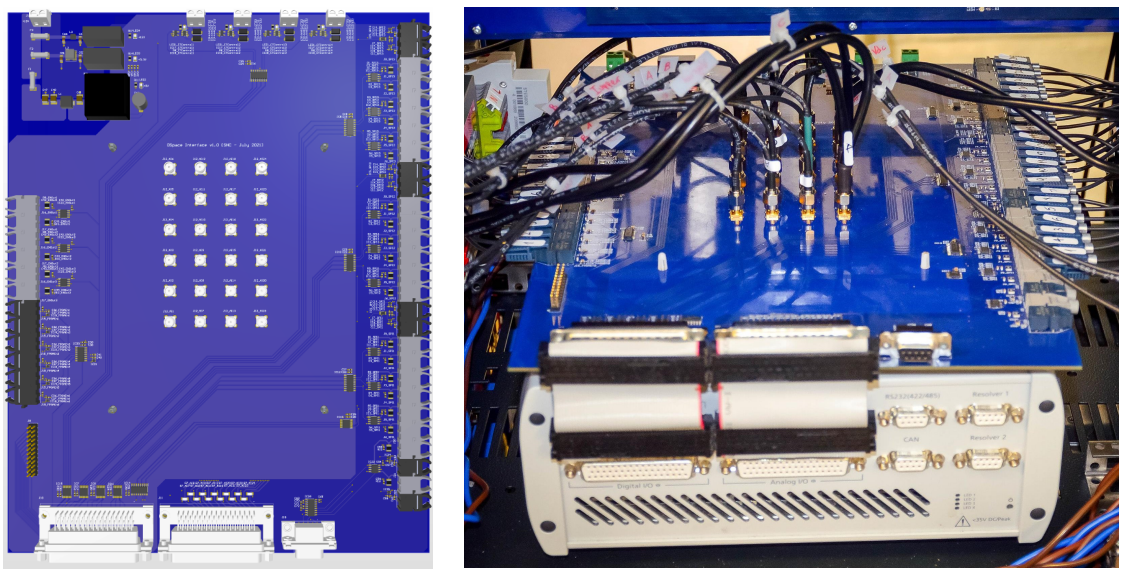
(b)

FIGURE 8.3. Stack back-plane board with 10 SMs. (a) Front View. (b) Rear View.

The central control unit is implemented on a dSPACE MicroLabBox real-time control system, which consists on a real-time processor complemented with a FPGA and I/O cards for connecting analog and digital signals. The dSPACE controller is connected to a host computer through a Ethernet interface, allowing its programming and monitoring in real-time. The main specifications of the control system are shown in Table 8.3. Then, an interface board was designed for connecting the MicroLabBox with the rest of the systems in the converter. The board includes: circuits for adapting digital I/O to fiber-optic

TABLE 8.3. Specifications of the dSPACE MicroLabBox Unit

Description	Value
Real-time processor	NXP (Freescale) QorlQ P5020, dual-core, 2 GHz
FPGA	Kintex-7 XC7K325T
Analog Inputs	24x 16-bit channels, 1Msps, differential, -10 ... 10 V
Digital I/O	48x bidirectional channels, 10 ns resolution, 2.5/3.3/5 V
Programming platform	Matlab Simulink / ControlDesk



(a) (b)

FIGURE 8.4. dSPACE Interface Board. (a) Altium Designer 3D model. (b) Manufactured Board.

signals connecting with the local control boards; SMA connectors for receiving the analog measurements through shielded cables; driving circuits for managing contactors of the converter; and connectors interfacing the board with the central control unit. Fig. 8.4 showcases the board on the used design program (Altium Designer) and the final implementation with all the connections in place.

Finally, the measurements for the currents and voltages of the experimental rig are done with developed boards using galvanic isolated transducers. The used transducers are the LEM LV 25-P and LA 25-NP, which output a current signal proportional to the measured variable. The signals are sent to the central control unit using coaxial cable to

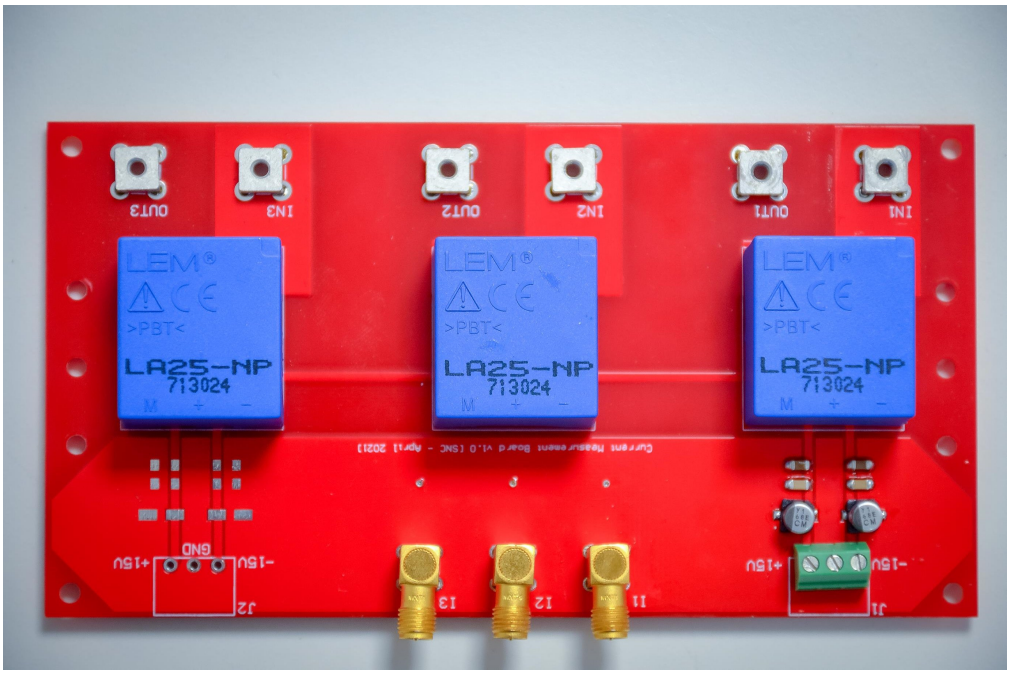


FIGURE 8.5. Designed Current Measurement Board.

withstand the noise inside the cabinet. Fig. 8.5 illustrates the implementation of a current measurement board.

8.3. Controller Structure

The control of the power converter is implemented in a two-layer scheme with a central unit, performing the high-level tasks, connected to local units regulating the operation of the stacks of the MMC. The central control unit takes care of the analog measurements of the system and executes the energy and current controllers for the MMC. Then, it communicates with each stack to send the voltage reference to be generated and it receives the local voltage measurements to be used in the control. The local control units perform the SMs voltage measuring and execute the switching algorithm to generate the commanded output while keeping the balance of the SMs. The overall control references and feedback gains are set in a user interface running on a host computer. Fig. 8.6 shows the overall control scheme considering the hardware description of the previous section.

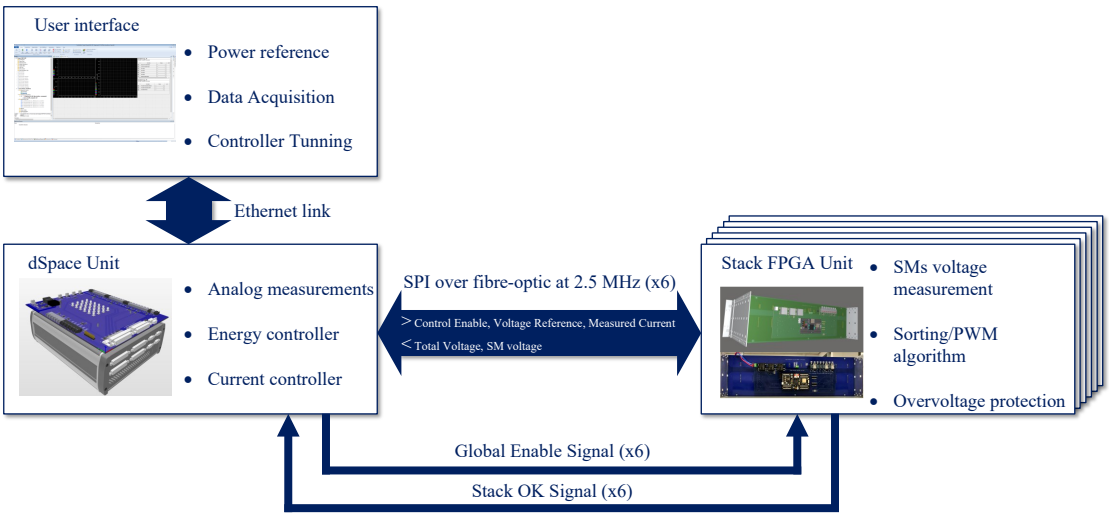


FIGURE 8.6. Overall Hardware Control Scheme.

The central control unit implements the high-level control to follow the power references received from the user interface over a Ethernet link. The control at this level contains two main control loops, an energy controller keeping the voltage of the MMC capacitors at the required level; and a current controller generating the voltage references to be modulated by the stacks. Fig. 8.7 showcases these controllers, indicating the origin and destination of the signals. The dSPACE unit is configured to have a sampling time of 100 μs, which is enough to perform the required calculations between samples.

The communication between the central unit and the local controllers is done through SPI lines over fiber-optic links working at 2.5 MHz. There are three SPI lines on the dSPACE interface board, with capacity for connecting two local units each. Therefore, each SPI line connects to a different phase, exchanging information in a full-duplex mode with each stack controller of the respective phase. The variables sent to the local controllers are the voltage reference, the measurement of the stack current and an enable signal for the controller. Then, the variables received from the local units are the total available voltage (addition of all capacitor voltages) and the individual voltage of one capacitor for acquisition purposes.

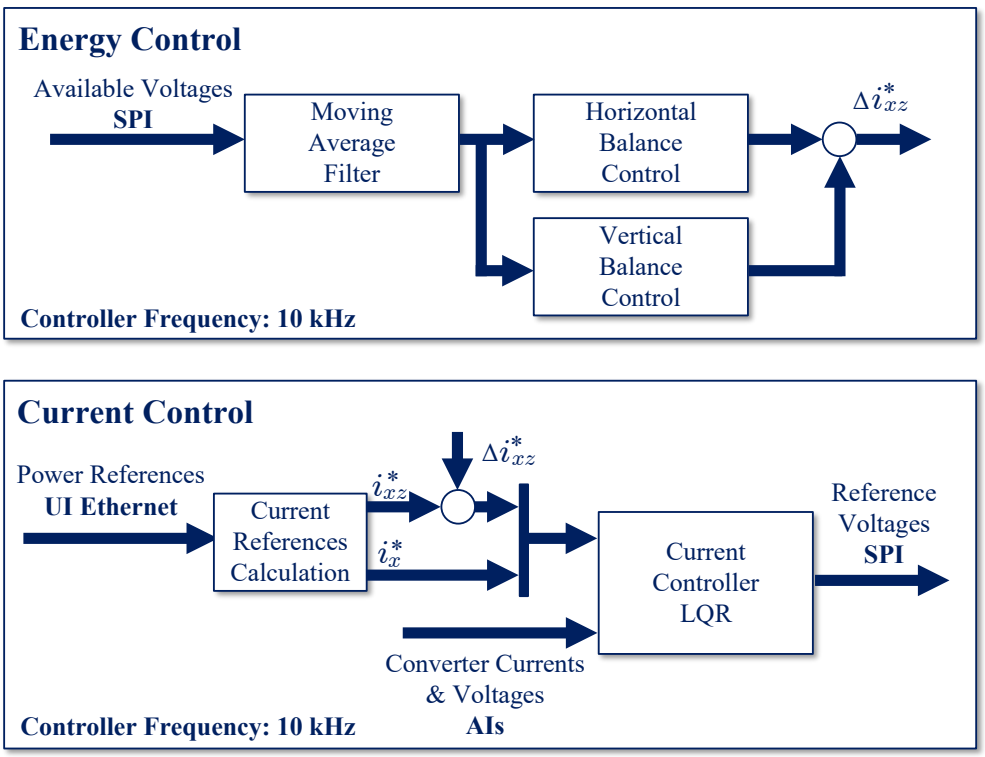


FIGURE 8.7. Central Controller Functional Blocks.

The local controllers implement the low-level control of the stacks based on the references received from the central unit and the voltage measurements from the isolated ADCs. The main blocks of this controller are shown in Fig. 8.8, with a detailed view of the algorithm generating the switching signals. The implementation complements the classical sorting algorithm based on Nearest Level Control (NLC) by adding a PWM stage to implement the last level. Then, the overall switching frequency is increased, but just one SM of the stack switches at high frequency at any given time. The latter is necessary due to the reduced amount of SMs compared to industry implementations, where the sorting algorithm based on NLC generates a smooth output by itself.

Lastly, there is a health monitoring and protection scheme coordinated between a closed loop between the central and local controllers. The loop is implemented with a bidirectional optical-fibre link, where each control unit sends a signal indicating whether the operation is under normal conditions. The central control unit checks two main variables

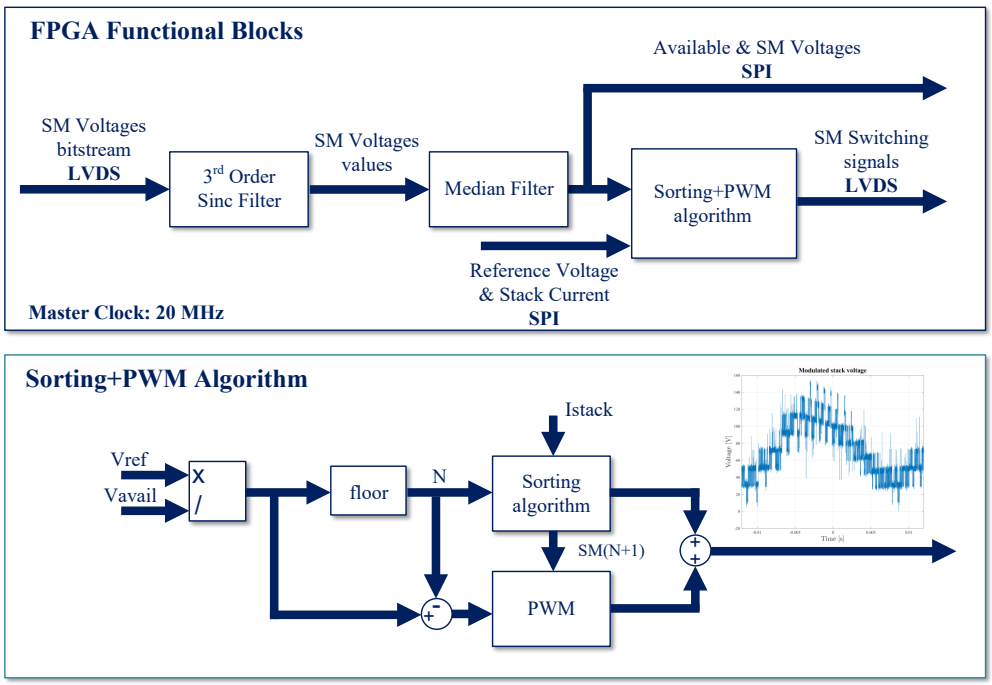


FIGURE 8.8. Local Controller Functional Blocks.

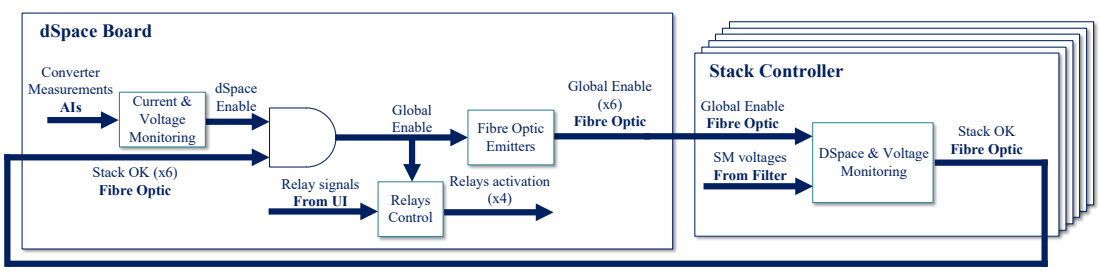


FIGURE 8.9. Closed-loop Health Monitoring.

to emit a global enable signal to the local units and permit the closure of the contactors of the converter. The signals driving the global enable generation are: the current and voltage measurements from the analog inputs; and the signals from each stack indicating normal operation of the respective SMs. The local controllers work in a similar way, setting a healthy stack signal, based on the voltages of the SMs and the global enable reception from the dSPACE unit. Fig. 8.9 displays the monitoring loop, where the driving of healthy signals is done using fast logic gates to ensure appropriate time response under abnormal conditions.

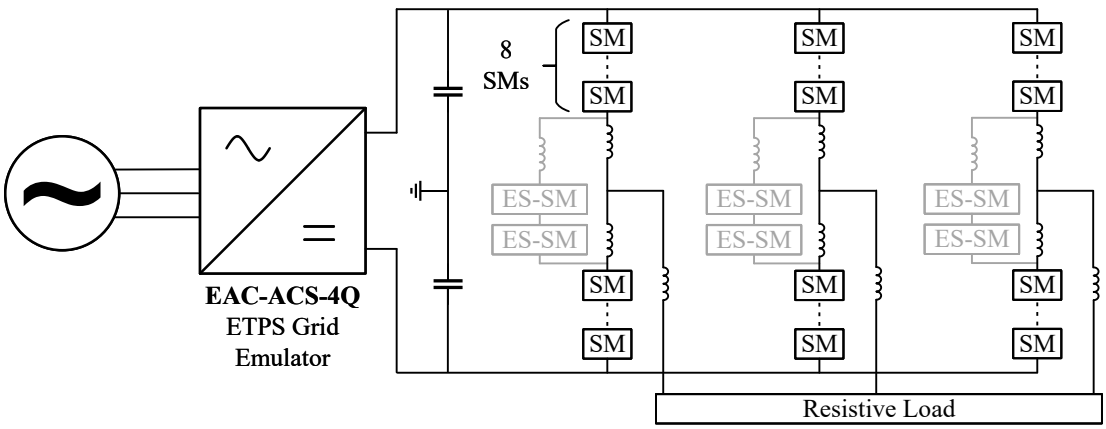


FIGURE 8.10. Experimental setup configuration including ES branches optionally connected.

8.4. Experimental Results

The setup described in previous sections is used to validate the operation of the MMC topology with integrated partially-rated energy storage. The overall configuration of the power system is shown in Fig. 8.10, where the MMC is connected to a DC power supply and a resistive load on the AC side. The DC power supply is the 30 kVA grid emulator EAC-ACS-4Q, which is set to deliver a steady voltage of 400 V. Then, the MMC consists of six stacks with eight half-bridge SMs each with he details described in the previous sections. Finally, the ES branches are implemented in branches of two full-bridge ES-SMs serially-connected with an inductor interfacing the phases of the MMC. The ES units are emulated with 500 W DC power supplies Mean Well RSP-500-48. Thus, several tests were performed to check the correct operation of the built converter and the control system associated. The tests are divided into two main groups: A first set of tests to validate the MMC operation; and a second set of tests to check the operation with integrated energy storage.

8.4.1. Operation as MMC

This subsection presents the obtained results for the converter operating as a conventional MMC feeding a resistive load on the AC side with the main electrical parameters

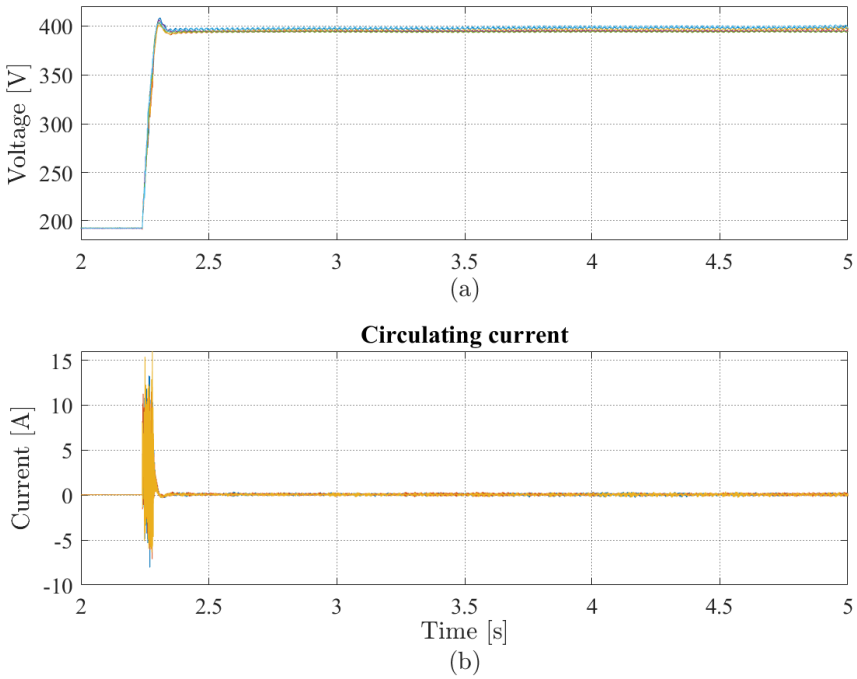


FIGURE 8.11. Initial charge of the MMC capacitors. (a) Total available voltage charging up to 400 V. (b) Circulating currents charging the stacks.

of the converter displayed in Table 8.1. The first set of results is presented in Fig 8.11, which displays the charging procedure of the stacks from the start value close to 200 V to the set value of 400 V. The initial value is given by the connection of the MMC to the DC power supply with all the SMs in blocked state, which charges them up to half of the nominal voltage as the current flows through the diodes to pre-charge the capacitors of each phase. Then, Fig 8.11(a) shows the instant when the controller is enabled taking the total available voltage of every stack to the nominal value in approximately 60 ms. Furthermore, Fig 8.11(b) displays the dynamic of the circulating current that presents a high current transient to then decay to a steady-ste value close to zero for maintain the voltages at the set-point.

Fig. 8.12 displays the main variables of the converter while operating at 3.8 kW transferred from the DC side to the AC load. The first plot shows the AC side currents, showing the balance operation at the required 50 Hz frequency. Then, following two plots show the

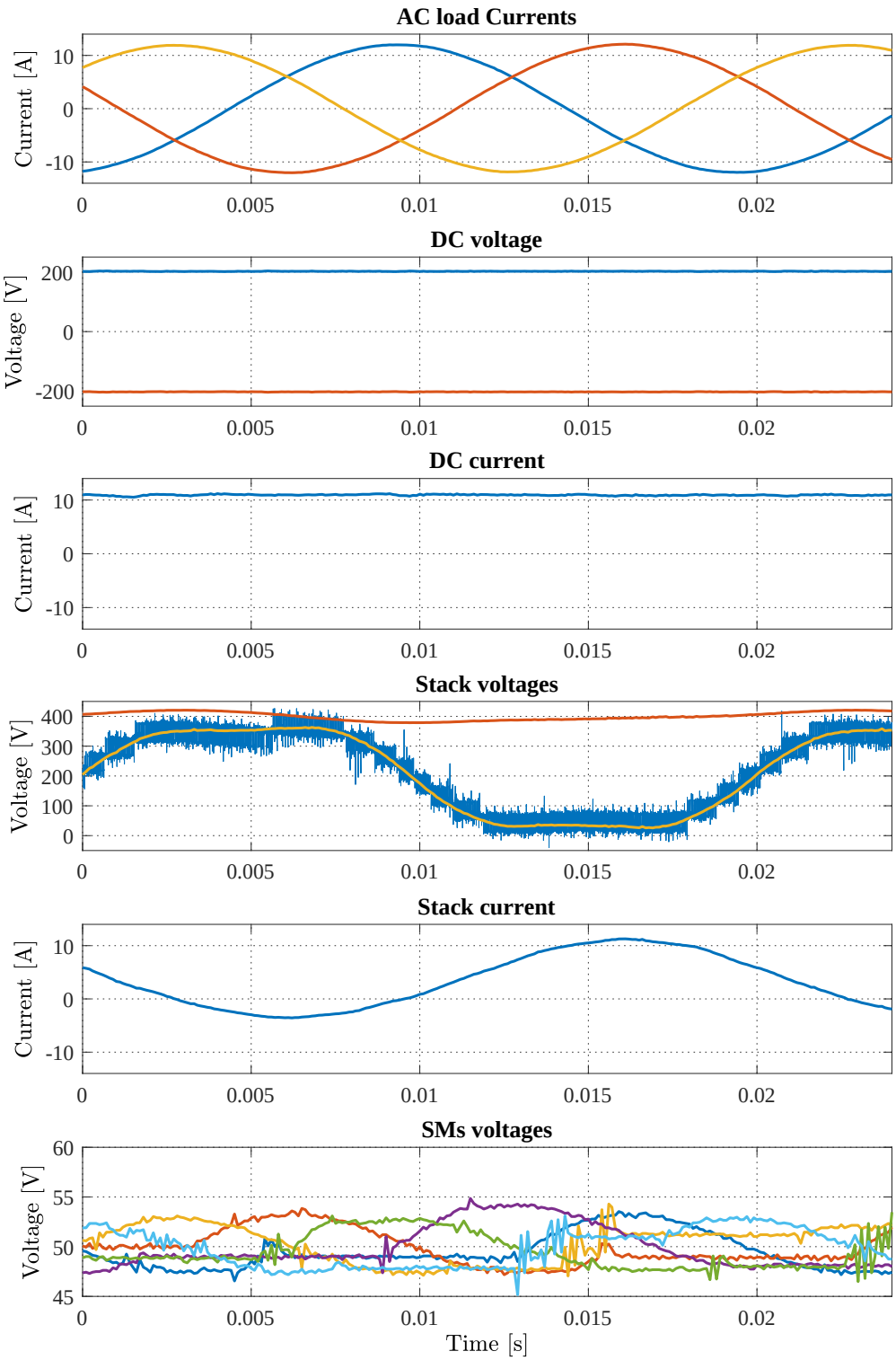


FIGURE 8.12. Steady-state results for the MMC operating at 3.8 kW.

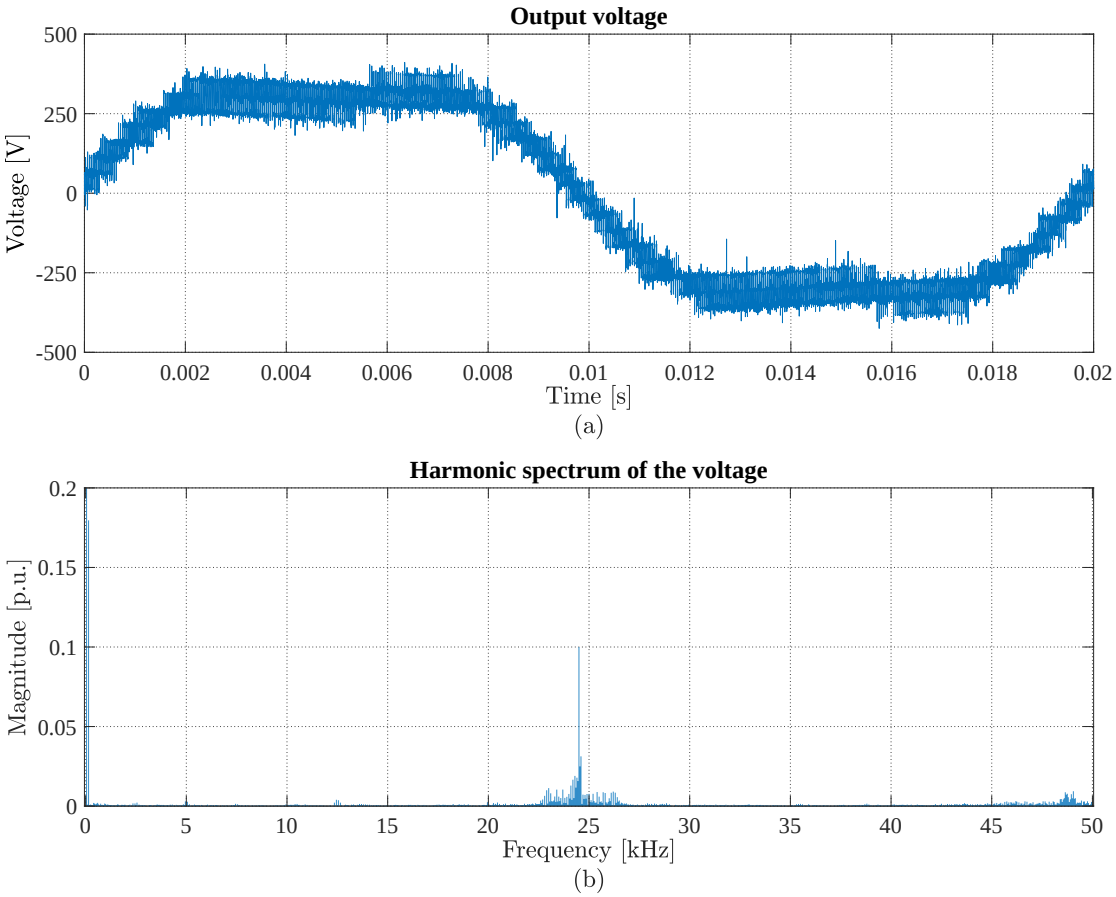


FIGURE 8.13. Output voltage of one phase of the MMC. (a) Output voltage of the converter. (b) Harmonic spectrum of the output voltage.

DC voltage and current respectively, illustrating a steady current regulated to keep the energy of the converter while feeding the AC load. The fourth plot presents the main variables for one of the stacks, showing how the reference voltage is correctly modulated by the local controller. Additionally, it shows the available voltage kept at 400 V, which represents the nominal value for each stack set at the energy controller. Then, following plot shows the corresponding stack current containing both DC and AC components used for the power transfer. Finally, last plot illustrates the voltage of one SM for each stack kept at the right value of $v_{sm} = v_{dc}/N = 50$ V.

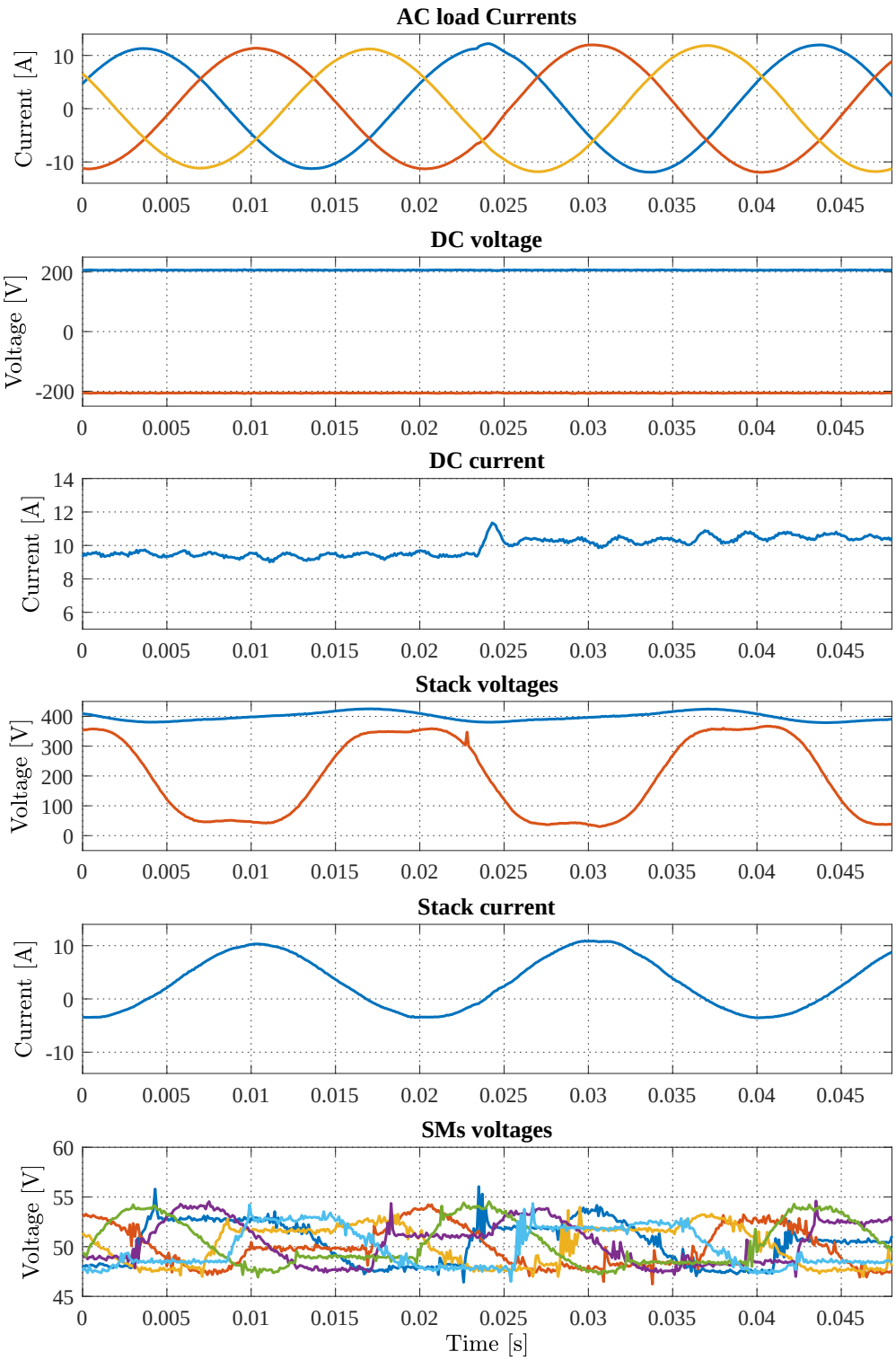


FIGURE 8.14. Dynamical response results for the MMC for a step on the AC power from 3.4 kW to 3.8 kW.

The total output voltage of one phase of the MMC contains 17 levels, considering 8 SMs per stack and the 0 V level. Fig. 8.13(a) shows this voltage oscillating from 400 V to -400 V to feed the AC load with the required power. Then, Fig. 8.13(b) displays the frequency spectrum for this voltage, illustrating the inclusion of the third harmonic used to extend the voltage capabilities at the fundamental frequency. Also, it shows that the the modulation scheme together with the number of SMs used results in a switching frequency close to 25 kHz. The overall spectrum validates the feature of the MMC to generate high resolution voltages with minimum harmonic content.

The transient response to a step on the power reference from 3.4 kW to 3.8 kW is shown in Fig 8.14. The plots display the step performed at $t = 0.024$ with instant changes on the currents on the AC and DC sides. Furthermore, the fourth plot shows the total available voltage kept at the nominal value, validating the operation of the outer energy controller. Also, it shows the change in the commanded stack voltage to address the new current reference. The last two plots illustrate the stack current for one phase and the voltages for one SM of each phase respectively. The SMs are balanced during the entire time because of the included sorting algorithm which govern the energy of each SM to follow the nominal value.

8.4.2. Operation as MMC with Energy Storage

This subsection shows the operation of the second configuration for the converter, including the ES branches to validate the proposed topology in chapters 6 and 7. The ESS branches consist of two full-bridge SMs with DC power supplies, emulating the ES units, connected directly to the capacitor of the SMs. Thus, the experimental setup is used to test a unidirectional power injection from the ESS to the AC load as complement of the DC power supply. The main parameters of the ES branches are displayed in Table8.4. The maximum amplitude for the AC voltage of the ES branches is 100V, representing a 0.25 p.u. of the DC voltage of the MMC. Additionally, the frequency selected is 200 Hz, corresponding to the fourth harmonic of the voltage on the AC side.

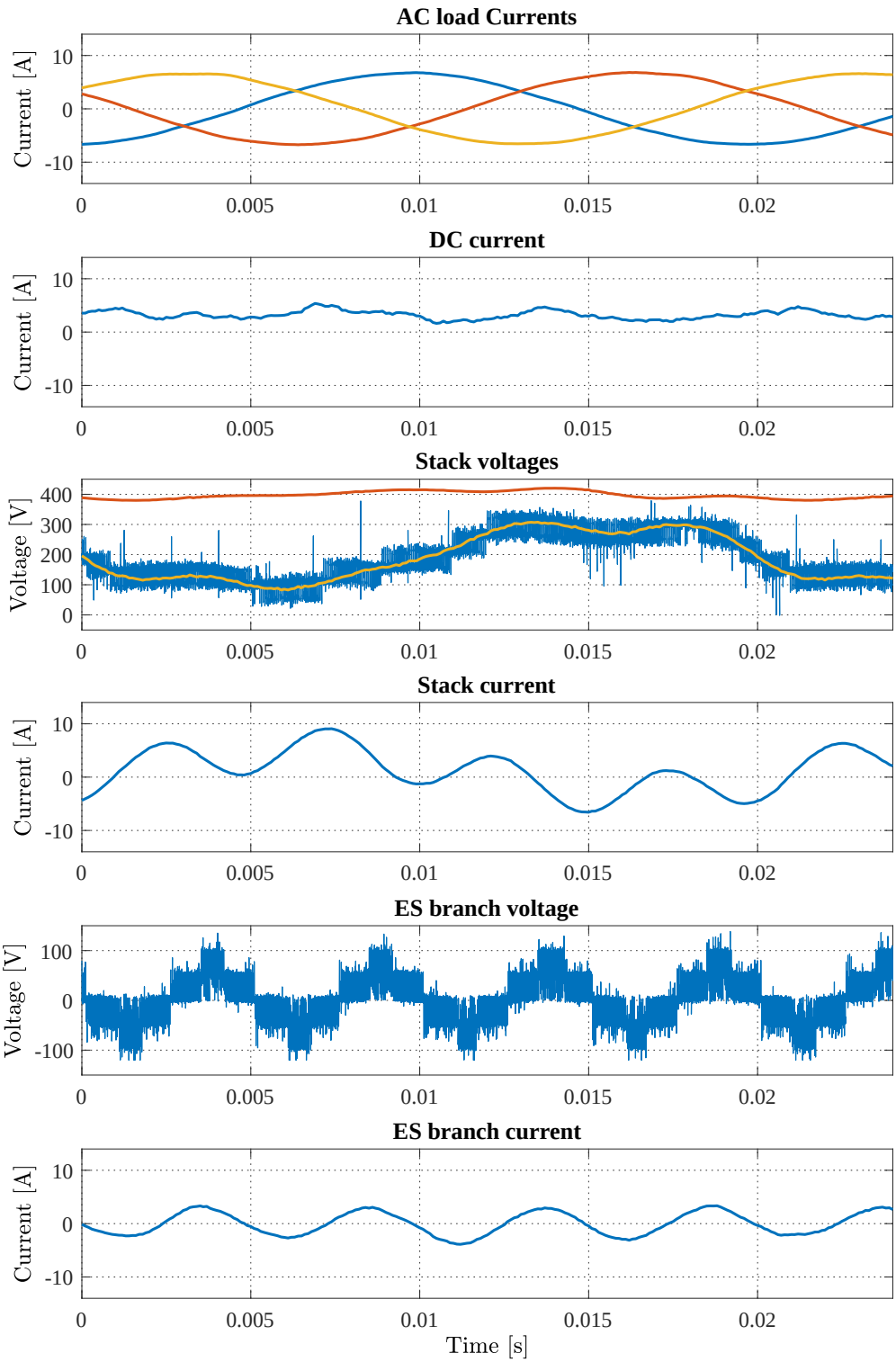


FIGURE 8.15. Steady-state results for the MMC with ESS operating at $P_{ac} = 1.2$kW and $P_{es} = 0.2$kW.

TABLE 8.4. Specifications of the ES branches of the MMC Setup

Description	Value
AC voltage	0.25 p.u.
Harmonic frequency	200 Hz (4^{th} harmonic)
Number of ES-SMs per branch	2
Type of SM	full bridge
Branch inductors	4.8 mH

Fig. 8.15 displays the operation of the experimental MMC with integrated ES units for a partial-load scenario, where 1.2 kW are being delivered to the AC load while the included ESS provides 0.2 kW. The first two plots illustrate the currents at the AC and DC side, showing a similar waveform to the ones for the conventional MMC tests. Thus, it is shown that the inclusion of the harmonic currents enabling the power transfer from the ESS just circulate within the stacks and do not flow to the AC or DC sides of the converter. Then, the third plot displays the stack reference and modulated voltages together with the total available voltage. The modulation stage is able to generate a correct voltage including the required 4^{th} harmonic component, given the limited magnitude of this component. Also, the available voltage is kept within bounds, oscillating around the reference voltage in the same way as the conventional MMC operation. The following plot presents the stack current for the same stack, showing the presence of the three frequency components (DC, AC fundamental and AC harmonic). Finally, the last two plots illustrate the ES branch voltage and current for the phase where the analysed stack is installed. The voltage shows the five available levels to generate the 200 Hz sinusoidal waveform required for exchanging power with the MMC stacks. This voltage is generated with a PWM modulator, following the structure presented in chapter 6. Then, the ES current shows the required sinusoidal waveform at the harmonic frequency, validating the control of this variable to provide the set-point power for the ES branch.

8.5. Chapter Conclusions

This chapter presented the design and built of a lab-scale MMC demonstrator for testing the operation of a conventional MMC and the proposed configuration with integrated

energy storage. The converter enables performing tests of up to 4 kW power transfer from the DC to the AC side, using 8 SMs per stack operating as half-bridges. Additionally, it includes 2 SMs per phase to integrate ES units and validate different approaches of including ESS into the MMC topology. The overall setup includes a two-layer control system, considering a central control unit performing the energy and current regulation; and local stack control units generating the firing signals for the SMs using a sorting algorithm plus a PWM scheme.

Experimental results validate the operation of the developed converter as a conventional MMC, managing the power flow from the DC to an AC load while keeping the energy balance of the stacks. Steady-state and transient response results verify the operation of the selected control system, which governs the converter with the described distributed approach. Furthermore, the experimental setup is also tested with the proposed configuration in chapters 6 and 7 for enabling power transfer from ES branches using a new frequency component. The frequency selected was 200 Hz (4^{th} harmonic of the AC frequency), considering the sampling rate and the bandwidth of the hardware control unit. Thus, the converter is capable of injecting power from ES units complementing the power delivered from the DC side power supply. The presented results emulate the simulated results in low-power scale showing a similar behaviour in the currents of the systems with the reduced number of SMs.

9. CONCLUSION AND FUTURE RESEARCH

9.1. General Conclusions

The work presented in this thesis focuses on the design of power electronics converters for hybrid DC-AC systems with capability of embedding energy storage units to complement their operation. The research is organised in two broad topics, the first one related to power converters for low- and medium-power applications; and the second one for high-power high-voltage applications. The project describes the development of two different power converters, including the design, modelling and validation of the topologies and control methods associated. Both converters aim to address some of the challenges of the future power grids, which have to face the increasing demands of electrification and the inclusion of renewable energies to achieve the sustainability goals for the world.

The first part of the dissertation concerns the study of a single-stage three-port DC-DC-AC converter developed to operate in hybrid systems with reduced topology complexity compared to state-of-the-art multi-stage solutions. The converter follows the same topology of a conventional two-level DC-AC converter, enabling the connection of a second DC port through the inclusion of an array of inductors connecting the middle point of the legs. Thus, it allows the simultaneous operation as a DC-AC converter and as an interleaved buck-boost DC-DC converter to regulate bidirectional power flows among the three ports. The incorporated DC ports can be used to connect an energy storage element, providing two main operating features: Embedded boost capability to exchange energy with an AC port working at higher voltage; and smooth DC current control filtering low-frequency harmonics that could be detrimental to the operation of the energy storage unit.

The operation of the converter exploits the available degree of freedom, given by the redundant switching states of the conventional DC-AC converter, to regulate a second current without requiring extra semiconductor devices. Thus, the solution minimises the required components to interface two DC elements with one AC port, regulating the power flow between the three sides. Therefore, the proposed converter is especially suitable for hybrid

systems where two DC units must connect to an AC port (e.g. Grid connected PV-Battery Systems or Hybrid Fuel-Cell/Battery EV Powertrains). The control of the converter uses a multi-variable approach to regulate the required currents at the same time in a coordinated manner. Two different control schemes are analysed, showing that the system can be governed using direct switching strategies, as the Finite Control Set Model Predictive Control; or modulated schemes, using linear controllers as the Linear Quadratic Regulator.

Analysis shows that the three-port operation of the converter modifies the voltage and current characteristics compared to the base DC-AC converter. The voltage of the added DC port adjusts the maximum range for the AC output voltage, and consequently the power capability for that port. The full range for the output is reached when the relation between the voltages of the two DC elements is 2:1. Furthermore, the inclusion of the interface for the second DC port changes the current load of the converter devices, as the leg voltages set new currents through the added inductors. Specifically, there is a new DC component performing the power transfer with the new DC port, but also an extra AC component circulating through the inductors that generates an unbalance on the load of the semiconductor devices and create further losses to be addressed at the design stage. Simulation analysis show that efficiencies up to 95.94% can be reached for a 3 kW design, which compares to efficiencies of similar state-of-the-art topologies.

Moreover, a modified version of the proposed topology including coupled inductors on the interface for the second DC port was presented to reduce the overall current load of the devices in the converter. The new interface takes advantage of the AC voltages of each leg (two or three, depending if single- or three-phase is selected) to generate magnetic flux on the coupled leg (or legs), elevating the impedance to the circulating AC current. Thus, the magnitude of these circulating currents can be reduce to half of its value when no magnetic coupling is considered. Both versions of the DC-DC-AC TPC were validated with simulation results to show their operation with the developed controllers. Furthermore, the TPC was also implemented in a reduced-scale prototype showing the bidirectional power flow capability with embedded boosting operation for the second DC port.

The second part of the dissertation focus on the proposal of an HVDC MMC converter topology integrating partially-rated ESS to enhance the operation of the power transfer between the DC and AC sides. The proposal embeds the ESS into new branches connected in parallel to the arm inductors of the MMC, keeping the original configuration of the stack unmodified. Thus, the proposal differs from the previously proposed integration of ES units into the MMC sub-modules or in stand-alone implementations on the AC or DC side. The operation of the proposed topology considers the use of a harmonic current component to transfer power between the ESS and the MMC stacks, complementing the conventional DC-AC power interaction. This operational feature is based on the available degree-of-freedom on the circulating current, allowing to define a third power transfer frequency, which does not interact directly with the DC and AC loops. Thus, it enables delivering extra power to either the DC or AC sides, trading off additional losses and higher energy deviation on the stacks with the convenience of keeping the MMC substation mostly unchanged.

The ESS is integrated into the substation using partially rated dc-ac cascaded converters connected in parallel with the phases of the MMC. Two variants of the topology are presented based on the electrical location of the arm inductors (either at the AC middle points of the SM stacks or at the DC terminals). Specific modifications to the ESS consider the inclusion of a capacitor for the case where the arm inductors are on DC terminal sides. Simulation results show that both variants work in the same manner, extending the results to both ESS configurations.

The presented analysis shows that the proposal allows the injection of an additional 37% of power from the ESS under partial-load conditions for the substation while keeping the original ratings for the components of the converter. The maximum power was obtained considering an optimisation process on the included harmonic components, considering the limits on the maximum stack currents, the limits for the stack voltages and the maximum deviation of the voltage of the SMs. Furthermore, the ESS can still provide 5% of power to the AC or side of the converter when the substation is operating close to the nominal power rating. This extra capacity agrees with the requirements for modern ancillary services from

the HVDC substation, such as frequency response or load levelling. Moreover, the losses for the entire converter vary in proportion to the amount of power processed by the ESS itself. Thus, the power losses for the entire MMC station increase by an additional 1% of the rated power for a power flow range of $\pm 10\%$ from the ESS.

The operation of the topology was validated using full-scale simulation models and a reduced-scale experimental prototype. Simulation results validate the injection of power to both AC and DC sides of the converter operating as an interface between an HVDC line and an HVAC side. The displayed results show that the ESS branches operate with a reduced voltage rating, complementing the MMC operation without affecting the behaviour of the currents outside the converter. A laboratory-scale prototype was built to test the real-time operation of the proposed topology and the control system. Thus, experimental results show agreement with the simulated results, validating the capacity of the converter to exchange power between the DC, AC and ES sides using the defined three frequency components.

9.2. Publications arising from this thesis

The PhD project has lead to the publication of the below-listed articles and patent:

- **Journal Papers**
  - *Three-Port Full-Bridge Bidirectional Converter for Hybrid DC/DC/AC Systems*. S. Neira, J. Pereda and F. Rojas. IEEE Transactions on Power Electronics, 2020.
  - *Modular Multilevel Converter with Parallel Branch Providing Integrated Partially Rated Energy Storage*. S. Neira, Z. Blatsi, P.D. Judge, M.M.C. Merlin and J. Pereda. IEEE Transactions on Power Delivery, 2023.
- **Conference Papers**
  - *Three-Port Full-Bridge Cell for Multilevel Converters with Battery Energy Storage*. S. Neira, J. Pereda, M.M.C. Merlin and F. Rojas. IEEE Energy Conversion Congress and Exposition (ECCE), 2019.

- *A Novel Three-Port NPC Converter for Grid-Tied Photovoltaic Systems with Integrated Battery Energy Storage*. S. Neira, A. Lizana and J. Pereda. IEEE 11th International Symposium on Power Electronics for Distributed Generation Systems (PEDG), 2020.
- *Sequential Phase-Shifted Model Predictive Control for a Multilevel Converter with Integrated Battery Energy Storage*. S. Neira, P. Poblete, R. Cuzmar, J. Pereda and R. Aguilera. IEEE 11th International Symposium on Power Electronics for Distributed Generation Systems (PEDG), 2020.
- *Consensus-Based Distributed Control of a Multilevel Battery Energy Storage System*. S. Neira, P. Poblete, J. Pereda and F. Nuñez. IEEE 21th Workshop on Control and Modelling for Power Electronics (COMPEL), 2020.
- *Modular Multilevel Converter with Inductor Parallel Branch Providing Integrated Partially Rated Energy Storage*. S. Neira, Z. Blatsi, P.D. Judge, M.M.C. Merlin and J. Pereda. IEEE 12th Energy Conversion Congress and Exposition – Asia (ECCE-Asia), 2021.
- *A technical overview of single-stage three-port dc-dc-ac converters*. S. Neira, Z. Blatsi, M.M.C. Merlin and J. Pereda. 24nd European Conference on Power Electronics and Applications (EPE'22 ECCE Europe), 2022.

- **Patents**
  - *Conversor de Potencia Multi-Puerto y sistema y Uso Asociados*. J. Pereda and S. Neira. WO 2022/226669 A1, Published Nov. 2022.

9.3. Future research topics

Following the research results presented in this thesis, there are some topics that appear as relevant to be developed in the future:

- The increasing of the rated power for single-stage three-port DC-DC-AC converters represents an interesting problem to be analysed in the following years. Trends for these converters show rated power below 5 kW, while multiple-stage

solutions cover ranges up to 100 kW. Considering the proposed topology, the development of the coupled-inductors interface appears as fundamental to enable increasing the power transfer while keeping the overall current load within acceptable range. This represents a possible topic to develop based on the design and simulation results presented in the first part of the dissertation.

- The inclusion of partially-rated ESS into MMC substations using configurations such as the one proposed in the second part of this thesis is receiving interest from the research community, as they enable the provision of additional services compared to currently installed substations. Considering the novelty of this topic, a future study analysing the different proposals and performing a comparative study in terms of hardware requirements, added losses and power capabilities, seems to be useful when the number of published solutions reaches a relevant quantity.

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