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Research on low frequency ripple suppression technology of inverter based on model prediction

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Abstract: The low frequency ripple of the input side current of the single-phase inverter will reduce the efficiency of the power generation system and affect the overall performance of the system. Aiming at this problem, this paper proposes a two-modal modulation method and its MPC multi-loop composite control strategy on the circuit topology of a single-stage boost inverter with a buffer unit. The control strategy achieves the balance of active power on both sides of AC and DC by controlling the stable average value of the buffer capacitor voltage, and provides a current reference for inductance current of the DC input side. At the same time, the MPC controller uses the minimum inductor current error as the cost function to control inductor current to track its reference to achieve low frequency ripple suppression of the input current. In principle, it is expounded that the inverter using the proposed control strategy has better low frequency ripple suppression effect than the multi-loop PI control strategy, and the conclusion is proved by the simulation data. Finally, an experimental device of a single-stage boost inverter using MPC multi-loop composite control strategy is designed and fabricated, and the experimental results show that the proposed research scheme has good low frequency ripple suppression effect and strong adaptability to different types of loads.

Key words: boost type, low frequency ripple suppression, model predictive control, single stage inverter

1. Introduction

With the continuous improvement of human society's demand for sustainable energy, new energy power generation technologies such as photovoltaics and wind power have attracted more and more attention [1–7], and inverter technology is a key technology in new energy power generation systems [8–12]. Single-phase inverters are usually used in small and medium power applications such as energy storage systems and power distribution systems (such as photovoltaic systems) [13]. However, the low frequency ripple on the input side of single-phase inverters greatly affects many performances of the inverter. For example, in inverters using fuel cells, low frequency ripple in the input current will increase battery losses, reducing efficiency and dynamic performance [14]. In the photovoltaic inverter, the low frequency ripple of the input current will affect the MPPT of the photovoltaic cells, reducing the power generation efficiency of the system and the energy utilization rate of the photovoltaic cells [15, 16]. In addition, in the field of electric vehicles, which has developed rapidly in recent years, the existence of low frequency ripple will cause damage to the power battery of electric vehicles [17]. Therefore, the research and application of input current low frequency ripple suppression technology have important engineering significance.

The input current low frequency ripple suppression technology usually adopts methods such as adding a buffer circuit in the main circuit and improving the control strategy to transfer the low frequency pulsating reactive power in the circuit to other components. Low frequency ripple suppression technology can be divided into passive filter technology and active filter technology. In traditional passive filtering technology, a large electrolytic capacitor is usually connected in parallel with the input source of the inverter. This capacitor and the internal resistance of the input source form a first-order low-pass filter to filter the secondary ripple component [18]. However, the low frequency ripple suppression effect of the input current obtained by passive filtering technology is poor, and the passive components in the filtering circuit are bulky and short-lived.

In order to achieve better ripple suppression and power density, some researchers use existing circuit hardware as an auxiliary circuit to suppress DC side low frequency ripple. References [19] and [20] proposed capacitive active filter circuits based on an auxiliary battery charging module, and reference [21] used an existing charging system to act as an active filter for auxiliary battery charging or as a power battery charger. By time-sharing multiplexing, high frequency current and low frequency current ripples in the driving charging mode can be suppressed separately. Although these methods have good low frequency ripple suppression of the DC side input current, they all require the addition of passive energy storage devices and relays with low integration. Reference [22] have proposed a circuit that achieves a high power factor with a wide output voltage range, as well as ripple power decoupling without using electrolytic capacitors, but the additional inductors and switching devices add to the size and manufacturing costs of the circuit system. Subsequently, in order to reduce the size of the circuit and reduce the cost of the circuit hardware, many articles proposed integrating the active filter circuit with the original circuit and diverting low frequency ripple to the buffer capacitor. Reference [23] improved the traditional boost circuit to propose a new single-stage inverter circuit topology, reference [24] proposed a new active filter single-stage boost inverter topology based on the buck-boost circuit, and reference [25] proposed a four-switch single-phase common-ground photovoltaic inverter with power decoupling capability. The power decoupling circuit in these circuits partially or even

completely shares switches with the original converter, integrating the power decoupling circuit with the original converter without the need for additional power electronics. The researchers have also made improvements in the control strategy for the low frequency ripple suppression technique. Reference [26] proposed a controller based on automatic power decoupling concept for a dependent power decoupling circuit with no extra switches. Reference [27] proposed a DC bus capacitor decoupling control strategy for a full-bridge inverter, but the proposed circuit topology uses input filter capacitors and buffer capacitors with a large capacitance, and the proposed control strategy is complicated. Reference [28] proposed a multi-loop PI control strategy based on three-modal modulation for a single-stage boost inverter with a buffer unit. Input current low frequency ripple suppression effect of this scheme is good, but the single-stage boost circuit used in reference [28] can only operate at a unit power factor and cannot be adapted to other loads.

Based on the research of these above related papers, this paper proposed an MPC multi-loop composite control strategy based on two-modal modulation for a single-stage boost inverter with a buffer unit. The control strategy has good low frequency ripple suppression effect and strong load adaptability.

2. Circuit topology and input current low frequency ripple suppression mechanism

The circuit topology of single-stage boost inverter with a buffer unit is shown in Fig. 1. The circuit is composed of the cascading of the input source V_{in}, the input filter C_{in}, an energy storage inductor L, the buffer unit, a single-phase inverter full-bridge and a C output filter. The buffer unit is located on the DC side of the inverter, and is composed of a switch S_0, two diodes D_{s1}, D_{s2} and a buffer capacitor C_b. Four blocking diodes are connected in series with the power switches $S_1 \sim S_4$ on the bridge arm of the single-phase inverter, and constituting two-quadrant power switches that can withstand bidirectional voltage stress and unidirectional current stress, at the same time, the inverter is capable of operating with a power factor of 0 to 1 in any case. The buffer unit and the single-phase inverter full-bridge jointly realize the suppression of low frequency pulsating power and the boost inversion of the circuit.

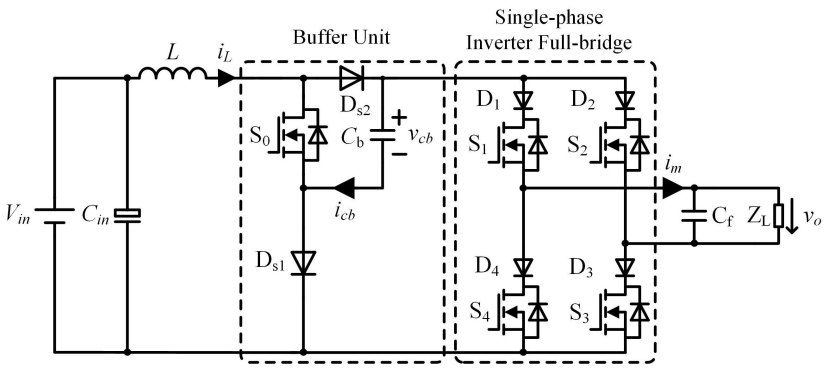


Fig. 1. Single-stage boost inverter with a buffer unit circuit topology

The single-stage boost inverter with buffer unit has four circuit modes:

1. Mode I-inductor magnetization mode: only the switch S_0 is turned on, V_{in} magnetizes L through S_0 and D_{s1}, the output filter supplies power to the load;
2. Mode II-capacitor charging mode: the switches S_0~S_4 are all turned off, the diodes D_{s1} and D_{s2} are naturally turned on, V_{in} and L jointly charge C_b, and the output filter supplies power to the load;
3. Mode III(IV)-capacitor discharge energy feeding mode: the switches S_0, S_1, S_3 (or S_0, S_2, S_4) are turned on, the capacitor C_b is discharged, the inductor L is magnetized, and i_L rises. V_{in} outputs positive (negative) modulation current i_m through L, C_b and S_1, S_3 (or S_2, S_4), and supplies power to C_{f} and Z_{L}, respectively;
4. Mode V(VI)-energy feeding mode: the switches S_1, S_3 (or S_2, S_4) is turned on, V_{in} outputs positive (negative) modulation current i_m through L and S_1, S_3 (or S_2, S_4), and supplies power to C_{f} and Z_{L}, respectively.

Among them, Mode I and Mode II are non-energy feeding modes, and Modes III–VI are energy feeding modes. Modes I, III, and IV are the modes in which the energy storage inductor is magnetized and the inductor current increases; Mode II is the mode in which the energy storage inductor is demagnetized and the inductor current decreases; and for Modes V and VI, when $V_{\text{in}} > |v_o|$, the inductance is magnetized and the inductor current increases, and when $V_{\text{in}} < |v_o|$, the inductance is demagnetized and the inductor current decreases.

This proposed circuit topology not only ensures the inverter function of the circuit, but also suppresses the low frequency ripple of the input current (inductor current).

Set the fundamental components of the output voltage and output current as:

$$V_o(t) = \sqrt{2V_o}\sin(\omega_o t)\,, \tag{1}$$

$$i_o(t) = \sqrt{2I_o}\sin(\omega_o t - \varphi)\,, \tag{2}$$

among them, V_o and I_o are the effective values of the inverter output voltage and current, ω_o is the power frequency sinusoidal voltage angular velocity, and φ is the inverter power factor angle.

Without considering the high frequency ripple of the energy storage inductor current $i_L(t)$ and the buffer capacitor voltage $v_{cb}(t)$, if the input current (inductor current) low frequency ripple can be suppressed during normal operation, and neglecting the device losses, from power conservation, we can get:

$$i_{\text{in}}(t) = \frac{P_{dc}}{V_{\text{in}}} = \frac{V_o I_o \cos\varphi}{V_{\text{in}}}\,. \tag{3}$$

At this time, the buffer capacitor voltage is:

$$\begin{aligned} & v_{cb}(t)\cdot C_b \cdot \frac{\mathrm{d}v_{cb}(t)}{\mathrm{d}t} = V_o I_o \cos(2\omega_o t - \varphi) \\ \Longrightarrow\quad & v_{cb}(t) = \sqrt{\frac{V_o I_o}{\omega_o C_b}}\cdot\sin(2\omega_o t - \varphi) + V_x \end{aligned}\,. \tag{4}$$

V_x is the integral constant term.

In order to suppress the low frequency ripple of the inverter input current, combined with the inverter circuit topology, power decoupling can be achieved by flexibly combining circuit

modes and reasonably adjusting the duty cycle. The specific idea is, when the average value of buffer capacitor voltage reference is reasonably set to $V^*_{cb\,\mathrm{ave}}$, the input and output active power can realize the balance by controlling the average value of the buffer capacitor voltage $V_{cb\,\mathrm{ave}}$ to be equal to $V^*_{cb\,\mathrm{ave}}$. That is, when the output power is constant, if the average value of the buffer capacitor voltage is higher than $V^*_{cb\,\mathrm{ave}}$, it indicates that the input active power is too large, and the reference value of the input current needs to be reduced, otherwise the reference value of the input current needs to be increased. Therefore, the voltage average value error of the buffer capacitor can be used as the reference for the energy storage inductor current, and the current can be controlled to track its reference value by configuring a suitable circuit mode to achieve a stable average value of the buffer capacitor voltage. When the load active power is constant, the energy storage inductor current reference obtained from the buffer capacitor voltage average error is also constant, and if the energy storage inductor current can track its reference, the purpose of low frequency ripple suppression of the input current can be achieved.

3. Mode modulation and control strategy

3.1. Multi-loop PI control strategy based on three-modal modulation

The multi-loop PI control strategy adopts three-modal modulation as shown in Fig. 2. Under this modulation strategy, there are three circuit modes corresponding to two operating modes in each switching cycle, namely the capacitor charging mode and the capacitor discharging mode. Among them, the capacitor charging mode includes the inductor magnetizing mode, the capacitor charging mode and the energy feeding mode, namely Modes I, II, V(VI); the capacitor discharging mode includes the inductor magnetizing mode, the capacitor discharging energy feeding mode and energy feeding mode, namely Modes I, III(IV), V(VI).

When $|m| + d < 1$, the inverter works in the capacitor charging mode, as shown in the k_1-th switching cycle in Fig. 2. In the interval $[k_1T_s,\ (k_1 + |m|)T_s]$, $[(k_1 + |m|)T_s,\ (k_1 + 1 - d)T_s]$ and $[(k_1 + 1 - d)T_s,\ (k_1 + 1)T_s]$, the inverter works in Modes V, II and I, respectively; when $|m| + d > 1$, the inverter works in the capacitor discharge mode, as shown in the k_2-th switching cycle in Fig. 2. In the interval $[k_2T_s,\ (k_2 + 1 - d)T_s]$, $[(k_2 + 1 - d)T_s,\ (k_2 + |m|)T_s]$ and $[(k_2 + |m|)T_s,\ (k_2 + 1)T_s]$, the inverter works in Modes VI, IV and I, respectively.

The multi-loop PI control strategy consists of a ripple suppression double loop and an output voltage loop, as shown in Fig. 3. The double-loop ripple suppression is composed of an outer loop of capacitor voltage average value and an inner loop of energy storage inductor current. The capacitor voltage v_{cb} obtains the average value of the capacitor voltage $V_{cb\mathrm{ave}}$ through the moving average filtering algorithm, and the error formed by $V_{cb\mathrm{ave}}$ and its reference value $V^*_{cb\mathrm{ave}}$ is passed through the PI controller to obtain the reference value i^*_L of the energy storage inductor current, then the inductor current error formed by i_L and i^*_L obtains the magnetization duty ratio d through the PI controller. The error between the reference value v^*_o of the output voltage and the output voltage v_o is passed through the PI controller to obtain the energy feeding duty ratio m. In each high frequency switching period T_s, d is compared with the monotonically decreasing sawtooth wave v_{c1} to generate the driving signal of the switch S_0. And m is compared with zero level to generate the positive and negative half cycle judgment signal v_v of the inverter. After taking the absolute value of m, it is compared with the monotonically increasing sawtooth

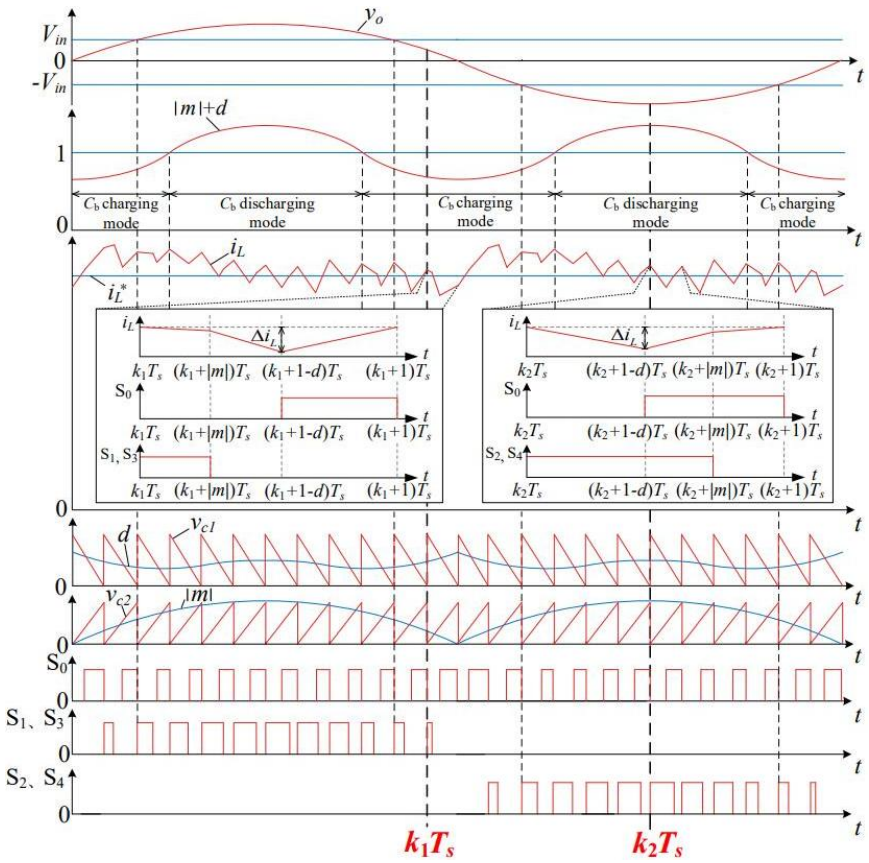


Fig. 2. Three-modal modulation control principle waveform

wave v_{c2} to generate the inverter energy feeding pulse width modulation signal v_d, and the driving signals of the inverter full-bridge switches S_1~S_4 are obtained by v_v and v_d through the logic circuit.

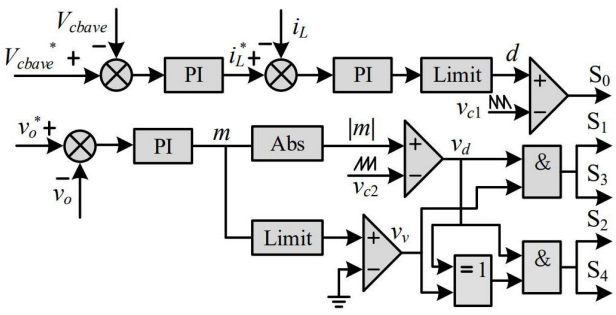


Fig. 3. Multi-loop PI control strategy block diagram

3.2. MPC multi-loop composite control strategy based on two-modal modulation

The proposed MPC multi-loop composite control strategy adopts two-modal modulation as shown in Fig. 4. In order to realize real-time control of the output voltage, each T_s under the two-modal modulation strategy contains the non-energy feeding mode (Modes I, II) and the energy feeding mode (Modes III, VI); and in order to ensure that the input current fastly tracks its DC reference without low frequency ripple components, the model prediction result is used to determine the state of switch S_0 in each T_s. When $S_0 = 0$, the non-energy feeding and energy feeding modes of each switching cycle correspond to Modes II and V(VI) respectively, and the inverter works in the inductance demagnetization mode, and i_L decreases throughout T_s; when $S_0 = 1$, the non-energy feeding and energy feeding modes of each switching cycle correspond to Modes I and III(IV), respectively, and the inverter works in the inductor magnetization mode, and i_L rises throughout T_s.

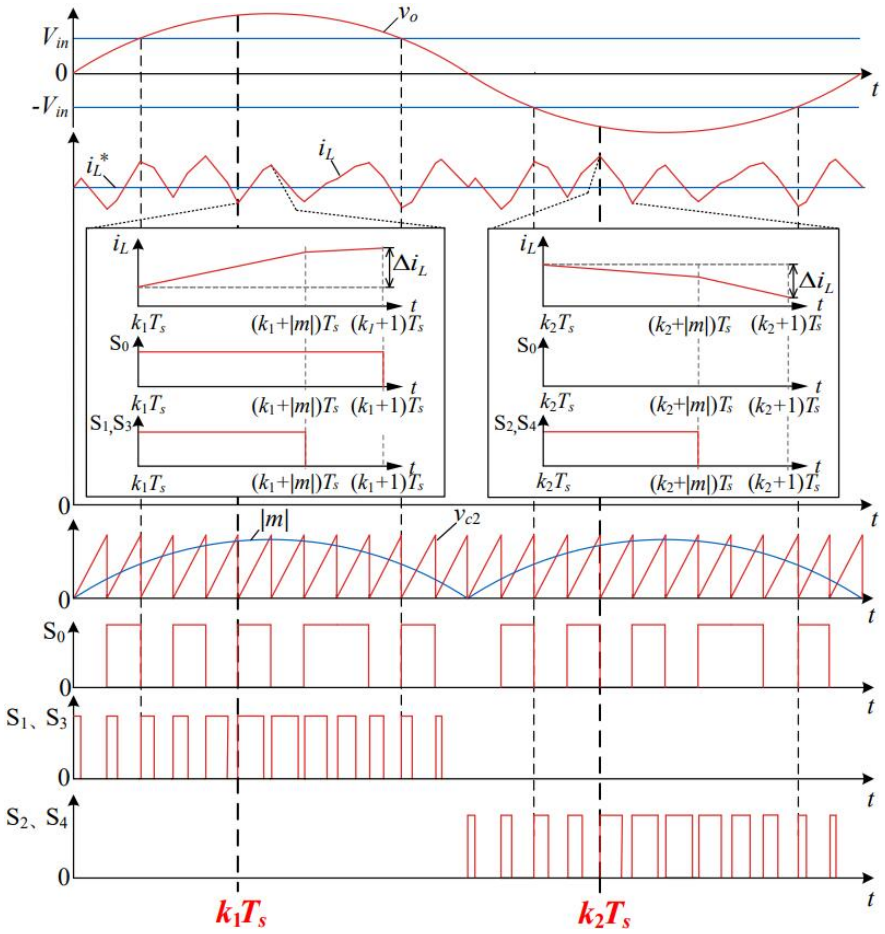


Fig. 4. Two-modal modulation control principle waveform

As shown in the k_1-th switching cycle in Fig. 4, the circuit works in the inductor magnetization mode. In the interval $[k_1T_s,\ (k_1+|m|T_s]$, circuit works in Mode III, the energy storage inductor is magnetized, and i_L rises; in the interval $[(k_1+|m|)T_s,\ (k_1+1)T_s]$, circuit works in Mode I, the energy storage inductor is still magnetized, and i_L continues to rise. As shown in the k_2-th switching cycle in Fig. 4, the circuit works in the inductor demagnetization mode. In the interval $[k_2T_s,\ (k_2+|m|)T_s]$, the circuit works in Mode VI, and the change of the storage inductor current i_L depends on the voltage across the inductor in the present mode; in the interval $[(k_2+|m|)T_s,\ (k_2+1)T_s]$, the circuit works in Mode II, the energy storage inductor is demagnetized, and i_L decreases.

It can be seen from Fig. 4 that the inductor magnetization mode will inevitably cause i_L to increase, and the inductor demagnetization mode will inevitably cause i_L to decrease. Therefore, the operating mode of each T_s period can be determined by setting the cost function of the model predictive controller, which can minimize the error of the inductor current i_L.

In order to realize the prediction of the current i_L in the cost function, the discrete prediction expression of the energy storage inductor current is obtained by combining the inductance volt-ampere relationship with the forward Euler method:

$$\hat{i}_L(k)=i_L(k)+\frac{v_L(k)}{L}t. \tag{5}$$

In e.g. (5), $i_L(k)$ and $v_L(k)$ are the current and voltage of the energy storage inductor at the initial moment of the k-th T_s, respectively.

When the inverter works in the inductor magnetization mode, the predicted value of the energy storage inductor current at the end of the k-th T_s is:

$$\hat{i}_L(k)=i_L(k)+\frac{V_{\text{in}}+v_{cb}-\text{sgn}\,(m)v_o}{L}|m|T_s+\frac{V_{\text{in}}}{L}(1-|m|)T_s\,. \tag{6}$$

When the inverter is in the inductor demagnetization mode, the predicted value of the energy storage inductor current at the end of the k-th T_s is:

$$\hat{i}_L(k)=i_L(k)+\frac{V_{\text{in}}-\text{sgn}\,(m)v_o}{L}|m|T_s+\frac{V_{\text{in}}-v_{cb}}{L}(1-|m|)T_s\,. \tag{7}$$

So, the cost function is:

$$g(k)=i_L^*(k)-\hat{i}_L(k). \tag{8}$$

According to the $g(k)_{\min}$ calculated by each T_s, the model predictive controller selects the circuit operating mode where $g(k)_{\min}$ is located, and determines the S_0 state.

Combining the above the two-modal modulation and the model prediction cost function, the proposed MPC multi-loop composite control strategy is shown in Fig. 5. This control strategy is composed of a ripple suppression double loop and an output voltage loop. The ripple suppression double loop is composed of an outer loop of the buffer capacitor voltage average value and an input current model prediction inner loop. In the outer loop, the error formed by the average value of the capacitor voltage $V_{cb\,\text{ave}}$ and its reference value $V^*_{cb\,\text{ave}}$ is passed through the PI controller to obtain the reference value i_L^* of the inductor current in the inner loop, and finally the inner loop model prediction controller will directly provides the drive signal of S_0. In the output voltage

loop, the output voltage reference value v_o^* and the output voltage v_o form an error, and then the error passes through the PI controller to obtain the energy feeding duty ratio m, and m is compared with zero level to generate the positive and negative half cycle judgment signal v_v of the inverter. After taking the absolute value of m, it is compared with the monotonically increasing sawtooth wave v_{c2} to generate the inverter energy feeding pulse width modulation signal v_d, and the driving signals of the inverter full-bridge switches S_1~S_4 are obtained by v_v and v_d through the logic circuit.

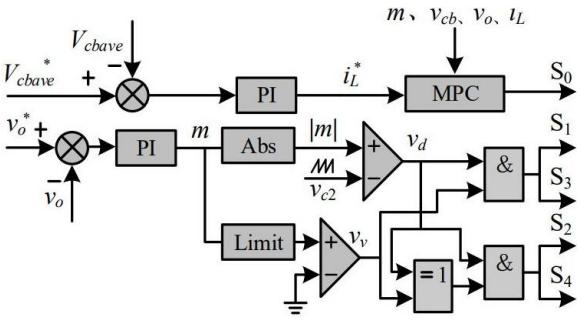


Fig. 5. MPC multi-loop composite control strategy block diagram

4. Comparison of low frequency ripple suppression effects under two control strategies

As shown by the inductor current i_L waveforms in Fig. 2 and Fig. 4, there are differences in the low frequency ripple suppression effects of the energy storage inductor current under two different control strategies.

For multi-loop PI control method based on three-modal modulation, the voltage reduction phase of the inverter, namely $|v_o| < V_{\text{in}}$, the energy storage inductance remains magnetized in the energy feeding mode during each T_s period, and this leads to the fact that the actual magnetization time in the step-down phase is greater than dT_s, and i_L will continue rising. Since the three-modal modulation method cannot completely suppress the rise of i_L in real time, the rise of i_L has a cumulative effect, which is equivalent to the existence of a double-frequency interference in i_L, that is, i_L must contain a certain double-frequency ripple.

Under the model predictive control, the circuit operating mode obtained from the cost function determines the on-off of S_0 in the whole T_s, and thus can effectively control the current i_L in real time, that is, S_0 is on, i_L must rise; when S_0 is turned off, i_L will inevitably decline, and thus ensuring that i_L can track its benchmark quickly.

In the inductor magnetization mode, the variation of the energy storage inductor current in one T_s is:

$$\Delta i_{L\text{on}} = \frac{V_{\text{in}} + v_{cb} - \text{sgn}\,(m) v_o}{L} |m| T_s + \frac{V_{\text{in}}}{L} (1 - |m|) T_s \,. \tag{9}$$

In the inductor demagnetization mode, the variation of the energy storage inductor current in one T_s is:

$$\Delta i_{L\text{off}} = \frac{V_{\text{in}} - \text{sgn}\,(m)v_o}{L}|m|T_s - \frac{V_{\text{in}} - v_{cb}}{L}(1-|m|)T_s\,. \tag{10}$$

According to e.g. (10), in demagnetization mode, when $V_{\text{in}} < \text{sgn}\,(m)v_o$, there is always $\Delta i_{L\text{off}} > 0$; when $V_{\text{in}} > \text{sgn}\,(m)v_o$, and if the value of $V_{cb\,\text{ave}}$ is large enough, $\Delta i_{L\text{off}} > 0$ can also be achieved. Therefore, the demagnetization mode can ensure that i_L always decreases.

According to e.g. (9) and e.g. (10):

$$\Delta i_{L\text{on}} - \Delta i_{L\text{off}} = \frac{2V_{\text{in}} + (2|m|-1)\,v_{cb}}{L}T_s - \frac{2\text{sgn}(m)|m|v_o}{L}T_s = f(t)\frac{T_s}{L}\,. \tag{11}$$

Taking resistive full-load as an example, since m and v_o are approximately in phase, and the positive and negative half cycles of v_o are symmetrical, so only the positive half cycle of v_o needs to be calculated. Taking the derivative of $f(t)$ to get:

$$\acute{f}(t) = 2\omega_o M\cos\omega_o t\left(\frac{V_oI_o}{\omega_oC_b}\sin 2\omega_o t + V_x\right)^{\frac{1}{2}} + \frac{(2M\sin\omega_o t - 1)V_oI_o\cos 2\omega_o t}{C_b\left(\frac{V_oI_o}{\omega_oC_b}\sin 2\omega_o t + V_x\right)^{\frac{1}{2}}} - 2\sqrt{2}\omega_o MV_o\sin 2\omega_o t, \tag{12}$$

where M is the maximum value of the energy feeding duty cycle $m(t)$. Additionally, according to e.g. (12), the extreme point can be obtained as $t = \dfrac{\pi}{4\omega_o}$, and there is a maximum value $f\left(\dfrac{\pi}{4\omega_o}\right) < 0$, which means that there is always $\Delta i_{L\text{on}} < \Delta i_{L\text{off}}$ under resistive load. It can be seen that under the MPC control, the energy storage inductor current i_L changes once corresponding to the inductor demagnetization mode of one T_s and the inductor magnetization mode of NT_s, that is, the change period T_{s0} is $(N+1)T_s$, as shown in Fig. 6.

According to Fig. 6, it can be obtained:

$$N = \frac{\Delta i_{L\text{off}}}{\Delta i_{L\text{on}}} = \frac{v_{cb}}{V_{\text{in}} + mv_{cb} - mv_o} - 1. \tag{13}$$

According to the value range of m, it can be known from e.g. (13) that when $m = 0$, N approximately obtains the maximum value:

$$N_{\max} \approx \frac{V_{cb\,\text{ave}} - V_{\text{in}}}{V_{\text{in}}}\,. \tag{14}$$

From Fig. 6, the maximum value of T_{s0} can be obtained as:

$$T_{s0\,\max} = (1+N_{\max})\,T_s = \frac{V_{cb\,\text{ave}}}{V_{\text{in}}}T_s\,. \tag{15}$$

It can be seen from e.g. (15) that $T_{s0\,\max}$ is much smaller than the power frequency period T_o, so i_L can quickly track i_L^*, and there is almost no low frequency pulsation, that is, i_L only has high frequency pulsation. Therefore, in principle, compared with the multi-loop PI control strategy, the proposed MPC multi-loop composite control strategy has stronger low frequency ripple suppression ability.

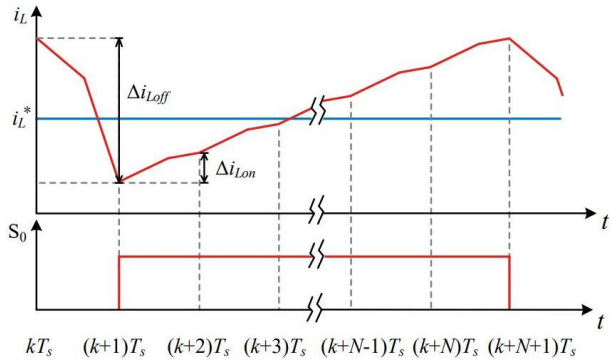


Fig. 6. Inductor current change waveform

5. Simulation and experiment

5.1. Simulation analysis

Under the parameters in Table 1, the simulation results of the inverter working under resistive full-load using the multi-loop PI control strategy are shown in Fig. 7. Among them, it can be seen from Figs. 7(a)–(c) that the inverter input 100 V DC voltage, the output waveforms of v_o and i_o are good, and the low frequency pulsation of i_{in} and i_L is small, and v_{cb} presents approximately double-frequency pulsation near its reference value. The FFT of input current i_{in} is shown in Fig. 7(d), the THD value of the input current i_{in} is 1.61% and its harmonic content is maximum at 200 Hz frequency, which is about 1.1%, indicating it has a good low frequency ripple suppression of the input current.

Table 1. Key parameters of circuit

Parameter name	Symbol	Value	Unit
Rated power	S	1 000	VA
Rated output voltage rms value	V_o	220	V
Input voltage	V_{in}	100	V
Energy storage inductor	L	2.85	mH
Buffer capacitor	C_b	100	μF
Input filter capacitance	C_{in}	330	μF
Output filter capacitance	C_{f}	10	μF
Switching frequency	f	50	kHz
Buffer capacitor voltage reference	$V^*_{cb\,\text{ave}}$	380	V
Load resistance	R	48.4	Ω

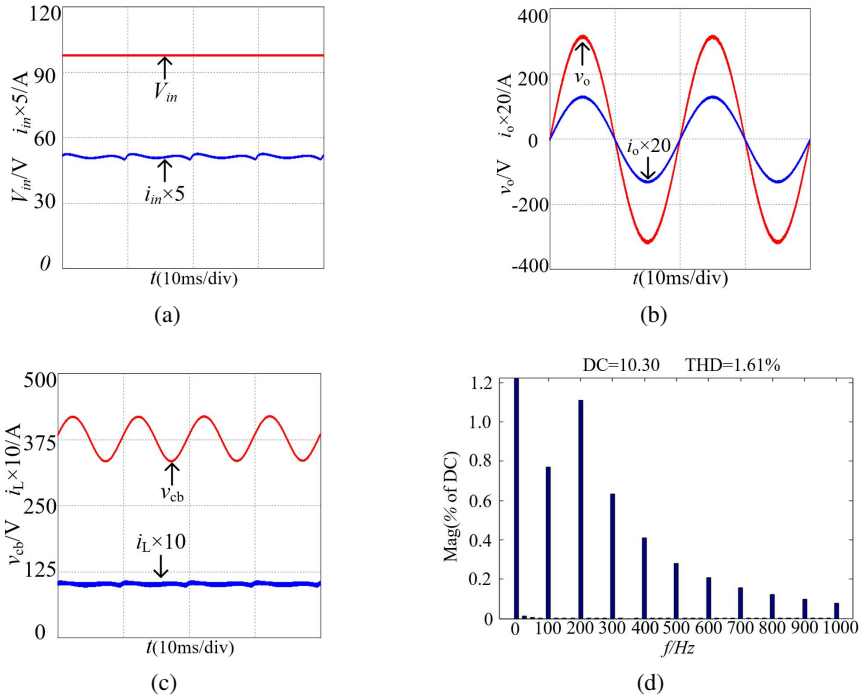


Fig. 7. Steady-state simulation waveform of resistive full-load with multi-loop PI control strategy: input voltage V_{in}, input current i_{in} (a); V_{in} = 100 V output voltage v_o, output current i_o (b); buffer capacitor voltage v_{cb}, energy storage inductor current i_L (c); FFT of input current i_{in} (d)

With the same circuit parameters, the simulation results of the inverters using MPC multi-loop control strategy are shown in Fig. 8. Figures 8(a)–(c) shows that the inverter can still output v_o and i_o with high quality when it inputs 100 V DC voltage. And compared with the results of multi-loop PI control, it can be noticed that compared to the inductor current i_L in Fig. 7(c), the inductor current i_L in Fig. 8(c) has increased high frequency pulsation, but compared to the input current i_{in} in Fig. 7(a), the input current i_{in} in Fig. 8(a) has no significant low frequency pulsation, which is similar to the DC current. It can be seen from Fig. 8(d) that the THD value of the input current i_{in} is 0.88% and the low frequency harmonic content of i_{in} is maximum at 100 Hz frequency, which is about 0.5%, and compared to the results in Fig. 7(d) with a multi-loop PI control strategy, the low frequency ripple suppression effect using MPC multi-loop control strategy is better. Figure 8(e) shows the drain-source voltage waveforms of the switch S_0 and S_1. Since the drain-source voltages of S_2~S_4 are similar to those of S_1, they are not given here. It can be seen from Figs. 8(f)–(k) that the inverter can still output high quality v_o and i_o under resistive-inductive and resistive-capacitive loads, and can also well suppress the low frequency ripple of the input current.

In summary, in order to achieve better input current low frequency ripple suppression effect, in the experiment, MPC multi-loop compound control strategy is selected as the inverter control method to further verify the conclusions obtained.

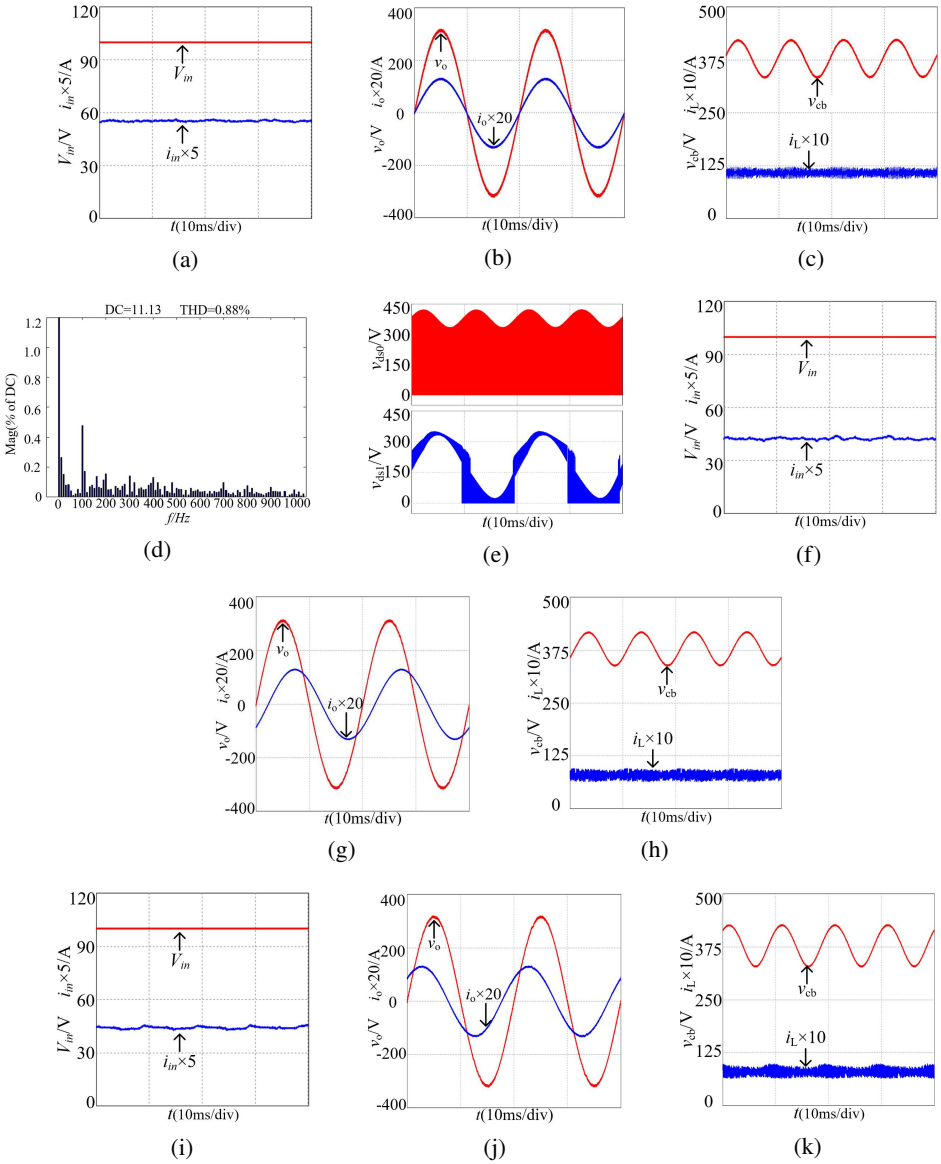


Fig. 8. Full-load steady-state simulation waveform with MPC multi-loop composite control strategy: resistive full-load input voltage V_{in}, input current i_{in} (a); V_{in} = 100 V resistive load output voltage v_o, output current i_o (b); resistive full-load buffer capacitor voltage v_{cb}, energy storage inductor current i_L (c); FFT of input current i_{in} (d); resistive full-load S_0, S_1 drain-source voltage v_{ds0}, v_{ds1} (e); resistive-inductive full-load ($\cos\varphi = 0.75$) input voltage V_{in}, input current i_{in} (f); V_{in} = 100 V resistive-inductive full-load ($\cos\varphi = 0.75$) output voltage v_o, output current i_o (g); V_{in} = 100 V resistive-inductive full-load ($\cos\varphi = 0.75$) buffer capacitor voltage v_{cb}, energy storage inductor current i_L (h); resistive-capacitive full-load ($\cos\varphi = 0.75$) input voltage V_{in}, input current i_{in} (i); V_{in} = 100 V resistive-capacitive full-load ($\cos\varphi = 0.75$) output voltage v_o, output current i_o (j); V_{in} = 100 V resistive-capacitive full-load ($\cos\varphi = 0.75$) buffer capacitor voltage v_{cb}, energy storage inductor current i_L (k)

5.2. Experimental results

Under the parameters in Table 1, using the MPC multi-loop composite control strategy, a 1 000VA/100VDC/220VAC50Hz single-stage boost inverter experimental device with a buffer unit was designed and built. The main circuit power switches S_0~S_4 use IXFX66N85X, and the diodes D_{s1}, D_{s2} and D_1~D_4 use DSEI60-10A.

Figure 9 shows the resistive full-load experimental waveform of the inverter. It can be seen from Fig. 9(a) that the input voltage V_{in} is 100 V DC voltage, and the input current i_{in} is a DC current with high frequency pulsation and basically has no low frequency ripple component, indicating that the proposed research scheme has a good low frequency ripple suppression effect on the input current. According to Fig. 9(b), the waveform quality of inverter output voltage v_o and output current i_o is relatively high. From Fig. 9(c), it can be seen that the buffer capacitor voltage v_{cb} pulsates at double frequency around its average reference value 380 V, and the v_{cb} is greater than $|v_o|$ in the whole low frequency cycle, which meets the design requirements. Energy storage inductor current i_L is a DC current with high-frequency pulsation and no low frequency ripple component. Figures 9(d)–(f) respectively show the drain-source voltage waveforms of S_0~S_4. Among them, S_0 always works in the high frequency switching state, and the voltage envelope at both ends is the buffer capacitor voltage v_{cb}, whose maximum value is about 400 V; switches S_1~S_4 work in the high frequency switching state in half of the low frequency cycle, and are in the cut-off state in the other half of the low frequency cycle, and the voltage envelopes at both ends are $(v_{cb} - v_o)/2$.

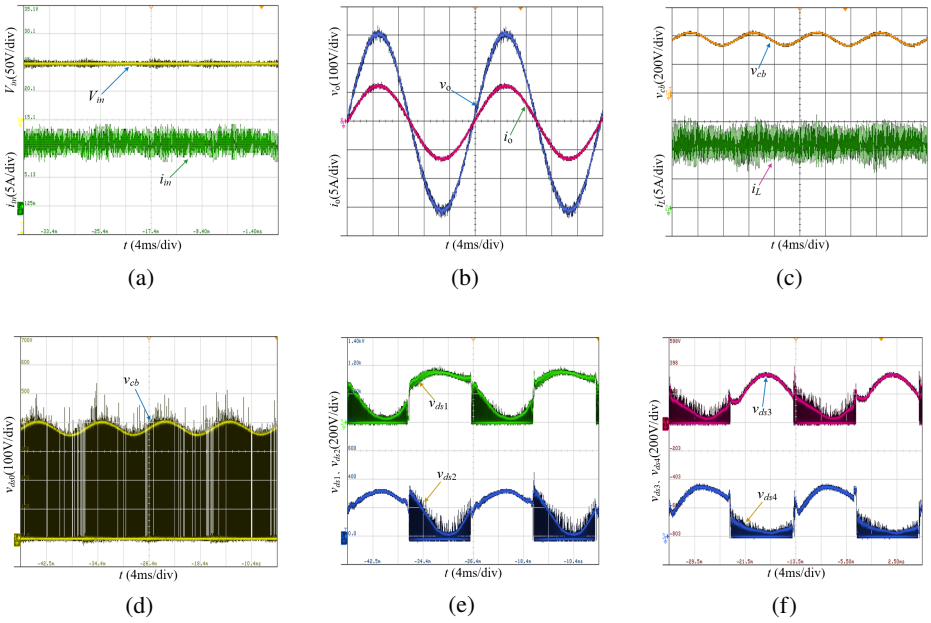


Fig. 9. Steady-state experimental waveform of resistive full-load: Input voltage V_{in}, input current i_{in} (a); output voltage v_o, output current i_o (b); buffer capacitor voltage v_{cb}, energy storage inductor current i_L (c); drain-source voltage v_{ds0} (d); drain-source voltage v_{ds1}, v_{ds2} (e); drain-source voltage v_{ds3}, v_{ds4} (f)

Figure 10 shows the experimental waveforms of the inverter working under resistive-inductive full-load (PF = 0.75) and resistive-capacitive full-load (PF = 0.75). It can be seen from Fig. 10 that the inverter can also output good v_o and i_o waveforms in the case of resistive-inductive and resistive-capacitive loads, i_{in} and i_L still have good low frequency ripple suppression effect. In comparison, the i_{in} and i_L under resistive-capacitive load have larger high frequency pulsations, and there are some low frequency pulsations.

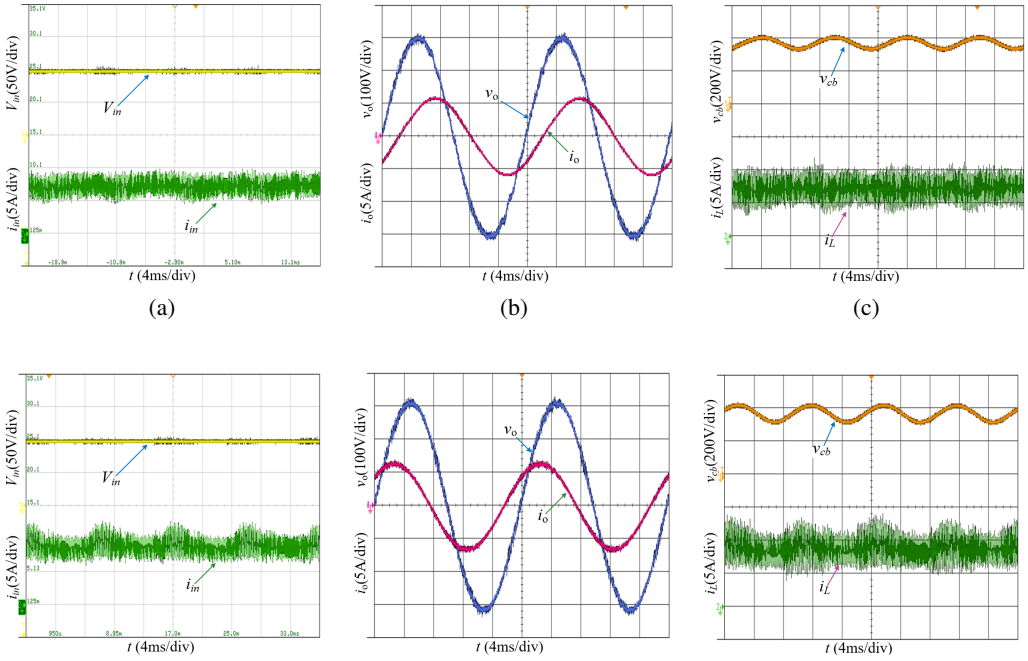
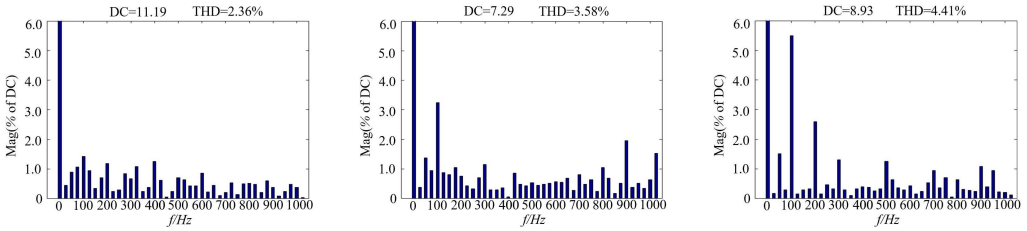


Fig. 10. Steady-state experimental waveform of resistive-inductive and resistive-capacitive full-load: resistive-inductive full-load ($\cos\varphi = 0.75$) input voltage V_{in}, input current i_{in} (a); resistive-inductive full-load ($\cos\varphi = 0.75$) output voltage v_o, output current i_o (b); resistive-inductive full-load ($\cos\varphi = 0.75$) buffer capacitor voltage v_{cb}, energy storage inductor current i_L (c); resistive-capacitive full-load ($\cos\varphi = 0.75$) input voltage V_{in}, input current i_{in} (d); resistive-capacitive full-load ($\cos\varphi = 0.75$) output voltage v_o, output current i_o (e); resistive-capacitive full-load ($\cos\varphi = 0.75$) buffer capacitor voltage v_{cb}, energy storage inductor current i_L (f)

The FFT of input current i_{in} under the resistive, resistive-inductive and resistive-capacitive loads are shown in Fig. 11, and it can be seen from Fig. 11 that harmonic content of the input current under the resistive, resistive-inductive and resistive-capacitive loads is maximum at 100 Hz frequency, which is about 1.50%, 3.20% and 5.50% respectively, and the THD value of the input current i_{in} under the resistive, resistive-inductive and resistive-capacitive loads is 2.36%, 3.58%, 4.41% respectively, and it shows that the inverter can effectively suppress the low frequency ripple of the input current under the MPC control.



(a) (b) (c)

Fig. 11. FFT of input current: resistive full-load FFT of input current (a); resistive-inductive full-load ($\cos\varphi = 0.75$) FFT of input current (b); resistive-capacitive full-load ($\cos\varphi = 0.75$) FFT of input current (c)

6. Conclusions

1. The multi-loop PI control strategy based on three-modal modulation is analyzed, and a two-modal modulation strategy and MPC multi-loop composite control strategy with the minimum inductor current error as the cost function are proposed. By deducing the inductor current maximum variation period $T_{s0\,\max}$ of the proposed control strategy, it is theoretically demonstrated that the proposed MPC multi-loop composite control strategy has stronger low frequency ripple suppression capability than the multi-loop PI control strategy.
2. The two control strategies are compared and analyzed by simulation. It can be seen from the simulation data that the low frequency ripple content of the input current under the MPC multi-loop control strategy is lower than that of the multi-loop PI control strategy, which proves the proposed MPC multi-loop control strategy has better low frequency ripple suppression effect.
3. In the experiment, the MPC multi-loop composite control strategy was adopted, and an experimental device of a 1 000VA/100VDC/220VAC50Hz single-stage boost inverter was designed and built. The experimental waveforms and data further verify that the proposed research scheme has a good low frequency ripple suppression effect and has strong adaptability to different types of loads.

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