UiT The Arctic University of Norway

Department of Electrical Technology

Study and Analysis of Alternative Power Switches with Reverse-Voltage-Blocking Capability

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Abstract

The current source inverters are becoming competitors of the voltage source inverters largely due to the reduced complexity, improved reliability and potentially improved efficiency. This paper describes the functionality of current source inverters and why they're becoming increasingly popular. It also discusses about the benefits of SiC over other semiconductors and the use of SiC MOSFETS with reverse voltage blocking capability in current source inverters. Double pulse testing is carried out through simulations on different switch configurations under different conditions using Ltspice, MATLAB and Simulink to determine the turn-on and turn-off switching losses. The tests are performed on a single MOSFET and also in the anti-parallel and half-bridge scenario. Altium Designer is used for the PCB design in order to observe the behavior o C3M0075120K which is Cree's 3rd Generation SiC MOSFET through hardware implementation.

Keywords: Current source inverter, power semiconductor switches, SiC-MOSFET, double pulse test

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1 Introduction

Power electronics is the branch of electrical engineering that deals with the processing of voltages and currents to deliver power that supports a variety of needs. From household electronics to equipment in space applications, these areas all need stable and reliable electric power with the desired specifications [1]. Considering the power sources, there are two main types, namely alternating current (AC) and direct current (DC). This forms four basic types of power electronics circuits namely AC-to-DC converters (commonly known as rectifiers), DC to-DC converters, DC-to-AC converters (commonly known as inverters) and AC-to-AC converters.

The converters can be categorized as being voltage source or current source and the building block of these are the semiconductor switches. Power electronic converters are be- coming more and more important mainly due to the increasing penetration of renewable energy sources and electrification of the transportation sector [2]. This report will focus on current source inverters (CSI) and how they can prove advantageous and effective than the more widely preferred voltage source inverters (VSI).

2 Literature Review

VSIs are considered as a mature and well-developed technology because the semiconductor switches used in them are readily available and manufactured. VSIs have the advantage of having a less complicated design, featuring minimum costs, high efficiency, and high reliability for the rectifying stage. The output voltage is independent of the load that is used, and more than one motor can be operated using a single VSI.

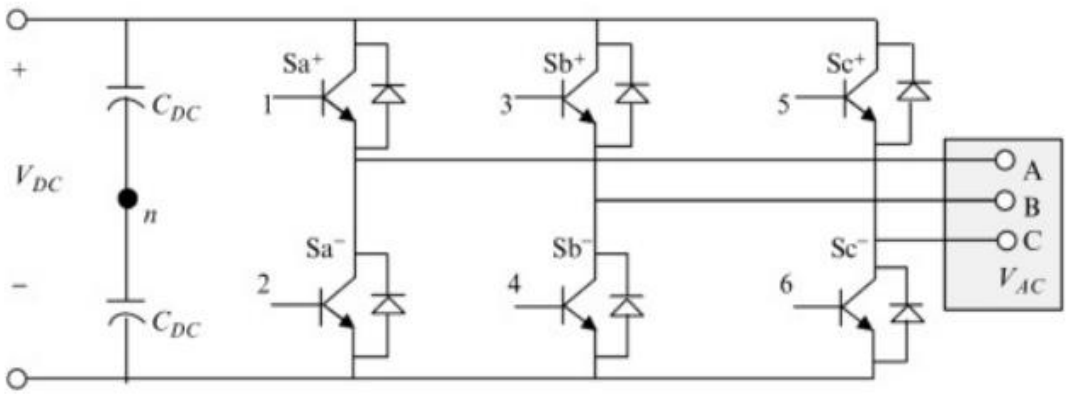


Figure 1: Three Phase Voltage Source Inverter [3]

The main disadvantage of VSI converters is the generation of high dv/dt transients on the motor insulation depending on the impedance which if not filtered, can reduce the motor lifetime significantly [4]. Another drawback of this topology is the generation of common-mode voltages, also affecting motor insulation and motor bearings. [5].

On the other hand, CSIs have the advantage of providing voltage boost from a lower magnitude input source, significantly reduced electromagnetic interference because of the capacitive voltage filters located directly on the inverter output, and the converter offers an additional short-circuit protection provided by the dc-link choke (current source) [6]. The output current waveform is determined by the circuit's topology and switching sequence, while the output voltage waveform is determined by the nature of the load.

Hence, CSIs can be useful in applications where their advantages outweigh the obvious fundamental CSI disadvantage of dc series inductor losses [8]. CSIs are already appreciated in medium voltage, large power induction drives [9], [10], and are currently being investigated even in the low-power range in place of VSIs [11], [12]. In [13], a modified CSI topology named CSI7 is proposed for PV applications. With the aim of reducing conduction losses, an additional switch (S_7) is added to the traditional CSI bridge. Thus, during the freewheeling phases, the DC current flows uniquely through S_7.

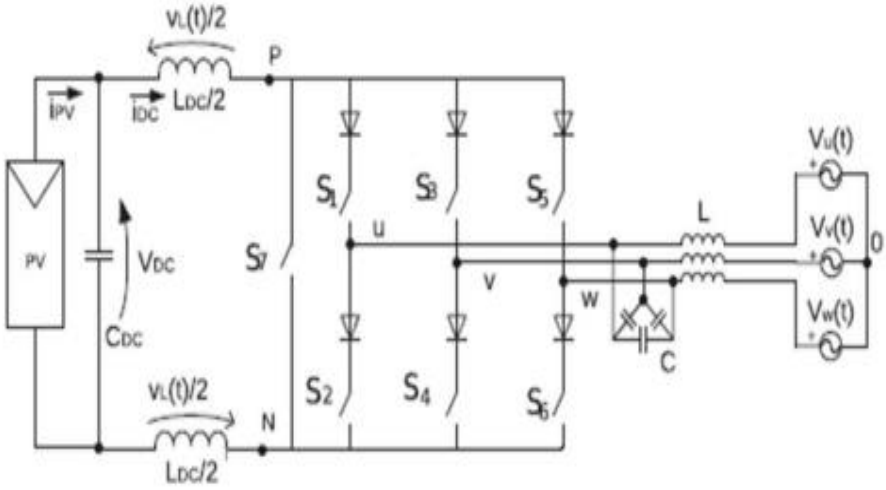


Figure 2: CSI7 Topology [14]

2.1 Operation of CSI

The three-phase CSI topology is shown in Figure 3. The inverter bridge is composed of six current-unidirectional switches with reverse voltage blocking capability. On the DC side, a DC-link choke ensures the converter's current-source based characteristic by preventing fluctuations in the current flow and since its value is large, the current is nearly constant. A filtering capacitor is normally added in order to attenuate the current ripple in the DC source and to stabilize its voltage.

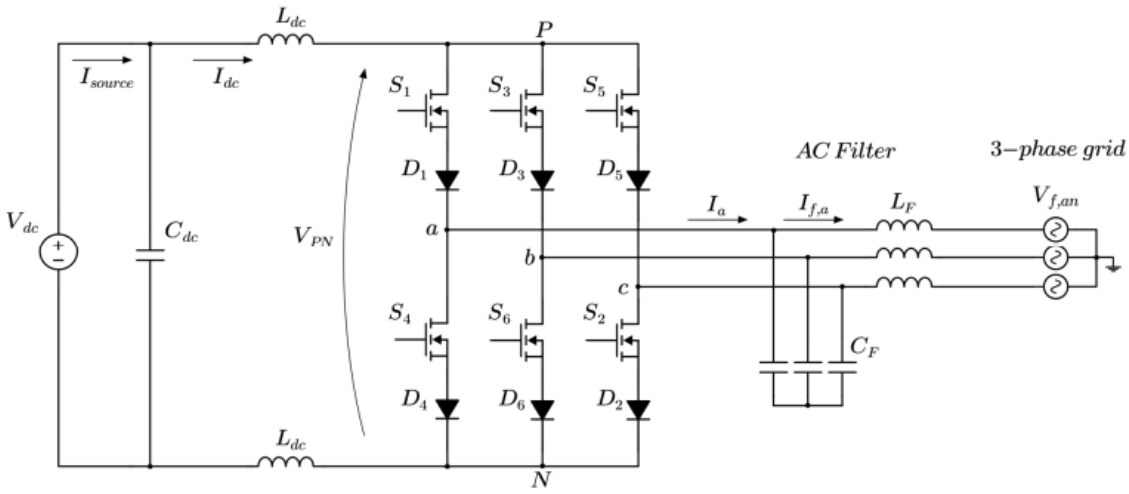


Figure 3: Three Phase Current Source Inverter [14]

On the other hand, the CSI bridge is connected to the mains through a three-phase C-L filter. The presence of C_F guarantees the mains instantaneous voltage source behavior allowing the interconnection of DC and AC sources - and is responsible for filtering the AC line current, together with the line inductor. With an appropriate control, the CSI is capable of injecting sinusoidal current waveforms into the grid [15].

2.1.1 Switches

For CSIs to function, the pulse width modulation (PWM) technique is employed. For that reason, the use of fully controlled turn-on and turn-off switches is required [16]. Figure 4 shows four possible switch realizations that can be used as CSI power devices. Considering the case where the voltage bidirectional device is made out of a serial connection of an IGBT and a diode, the need for an IGBT anti-parallel diode should be pointed out. Although it does not conduct any current, this additional diode is necessary since IGBTs are not designed to withstand reverse voltages [17]. Diversely, if MOSFETs are employed, any anti-parallel device is enough due to the intrinsic body-diode presence within the MOSFET structure.

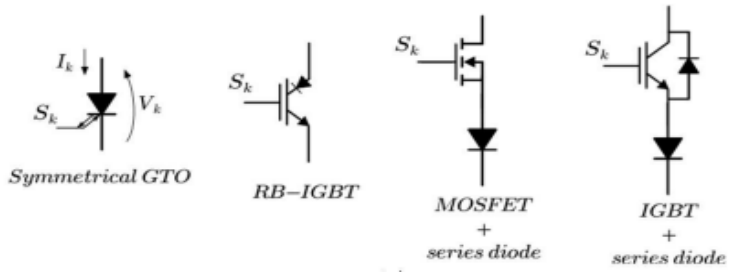


Figure 4: Possible switch realizations for CSIs [18]

2.2 VSIs vs CSIs

VSI requires constant DC-link voltage and generates AC voltages in the form of voltage pulses. It requires DC-link capacitor at the input side and AC filter inductors at the output side. VSI is vulnerable to leg short circuit fault hence requires dead time in switching upper and lower switches in the same leg. It is a buck inverter (magnitude of ac voltage is always smaller or equal to the dc voltage) but a boost rectifier.

CSI requires constant DC-link current and generates AC currents in the form of current pulses. It requires DC-link inductor at the input side and AC filter capacitors at the output side. CSI is vulnerable to leg open-circuit fault hence requires overlap time in switching upper and lower switches in the same leg. CSI is a boost inverter but a buck rectifier [19].

2.3 SiC

Silicon (Si) has long been the dominant semiconductor of choice for high-voltage power electronics applications. However, high temperatures are expected in a variety of measurement and control applications. Si based electronics are problematic when ambient temperature exceeds 200°C due to high internal junction temperature and large leakage currents. If Si and silicon carbide (SiC) are compared based on the specific ON-resistance versus breakdown voltage, the following graph is achieved.

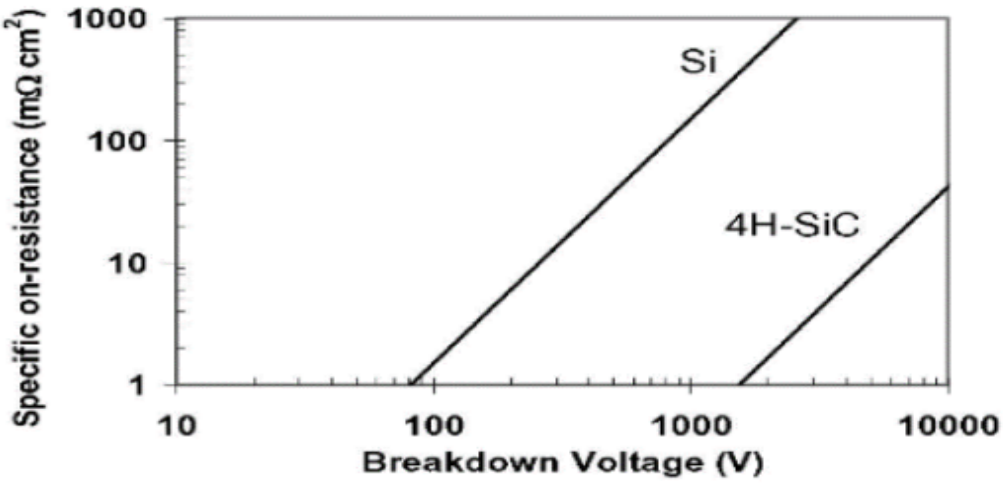


Figure 5: Breakdown Voltage of Si vs SiC [20]

The wide bandgap nature of SiC produces a dramatic reduction in the intrinsic carrier density and allows for more stable high-temperature electronics. In addition to outstanding electronic properties, SiCs excellent mechanical and thermal stability as well as chemical inertness and radiation hardness are well suited to gas sensing and UV detection in hostile environments [21], [22]. Also, the high drift velocity of SiC offers electrons to move fast in SiC devices that will gradually increase the switching speed and introduces the possibility of operating at high frequency.

Table 1: Physical Properties of SiC compared with other materials [23]

Sr. No.	Properties	GaN	GaAs	Si	SiC	Unit
1.	Crystal Structure	Hexagonal	Zincblende	Diamond	Hexagonal	-
2.	Thermal Conductivity	1.3	0.5	1.5	4.9	W/cm
3.	Energy Gap	3.5	1.43	1.12	3.26	eV
4.	Breakdown Field	3	0.4	0.3	3	$V/cm \times 10^6$
5.	Drift Velocity	2.7	2	1	2.7	$cm/s \times 10^7$
6.	Relative Dielectric Constant	9.5	12.8	11.8	9.7	-
7.	Electron Mobility	1250	8500	1400	900	cm^2/V_s

2.4 MOSFETs

Among all power-device structures, the metal–oxide– semi- conductor (MOS)-controlled devices are favorable due to their high input impedance and low switching losses, which make power electronic circuits more controllable with higher efficiency [24].

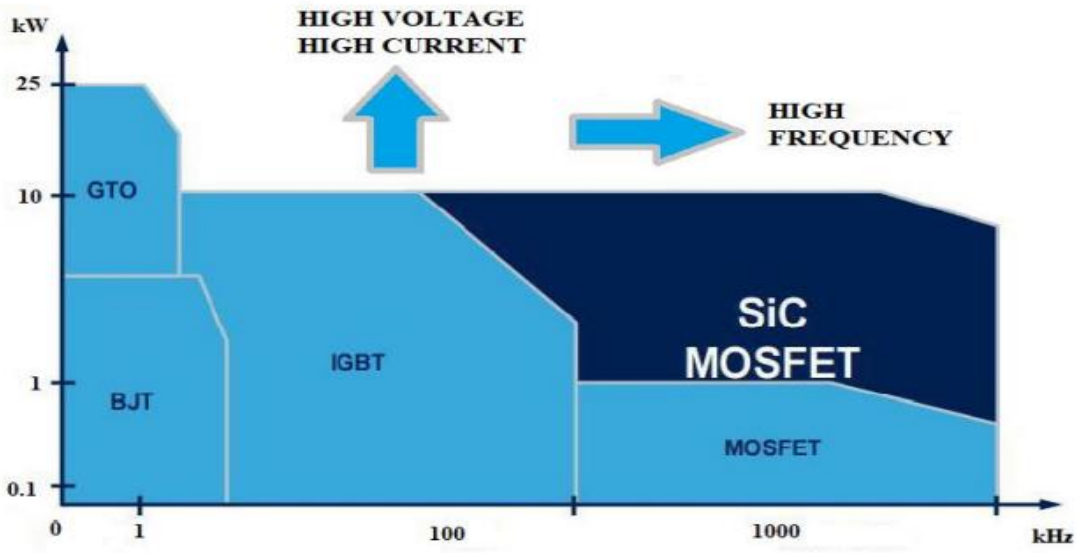


Figure 6: Comparison of SiC MOSFETs with other switches [25]

In general, MOSFETs are voltage controlled and operate in three regions:

1. *Cut-off* region is where the MOSFET behaves like an open switch as no current will flow through it.
2. *Linear* region is where the current I_{DS} increases with an increase in the value of V_{DS}.
3. In the *saturation* region, I_{DS} is constant in spite of an increase in V_{DS} and occurs once it exceeds the value of pinch-off voltage V_P. Under this condition, the device will act like a closed switch through which a saturated value of I_{DS} flows.

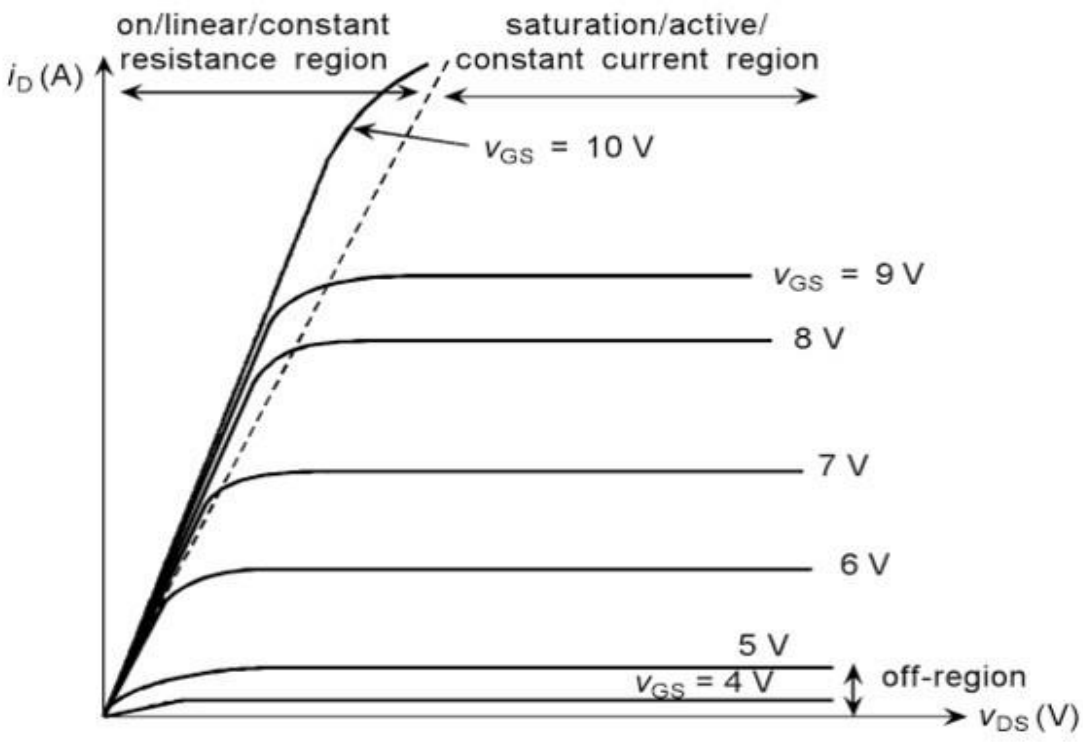


Figure 7: MOSFET IV Characteristics [26]

3 Simulations

The software used for this is LTSpice with the graphical data being plotted using MATLAB. The switch used here is C3M0075120K SiC MOSFET and the gate driver is IXYS IXDN609 (Appendix A).

C3M0075120K is a 3rd Generation SiC MOSFET technology (Appendix B) and consists of a seperate driver source pin (Kelvin Source). This pin allows bypassing the parasitic inductance of the traditional source pin. It also decouples the path of the load current from the path of the control current, leading to improved switching characteristics.

The purpose of the gate driver is to amplify the current supplied to the gate of the switch under control. This is required to obtain the fast switching times typically required for power electronic converters.

3.1 Experiment 1

The first simulation shows a simple circuit to check the working of the switch. The switch is connected to a dc voltage source of 30V and a 1mH series inductor. The gate driver provides the pulses from 15V to -4V (V_{GSop}), to turn the MOSFET on and off respectively. The reason

for providing -4V instead of the regular 0V for switching the MOSFET off is to avoid the miller effect caused by the paristic gate-drain capacitance which in turn limits switching speed.

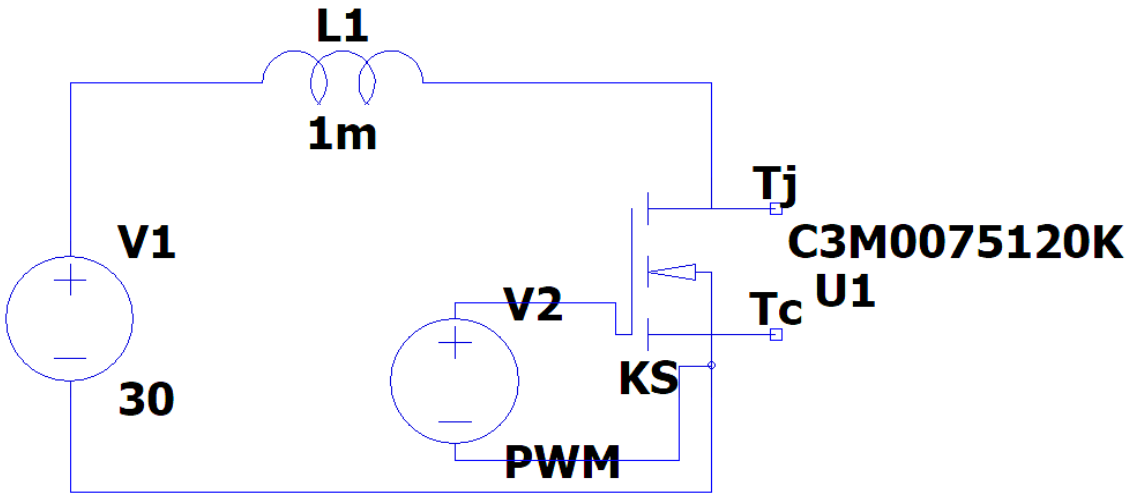


Figure 8: C3M0075120K testing

The results show large inductive spikes of upto 1600V across the drain and source. This is because when the MOSFET turns off it creates an open circuit but the inductor opposes the sudden change in current. Therefore the stored energy in the inductor converts into electrical energy at the open end causing overshoots.

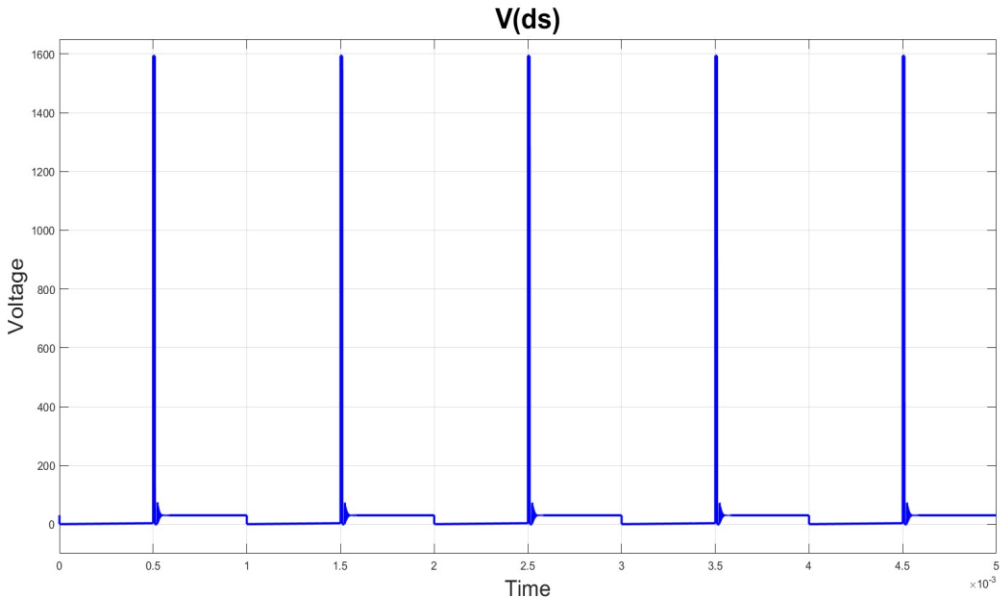


Figure 9: Vds across C3M0075120K

The simplest way to overcome this problem is to add a diode in parallel with the inductor with it's cathode facing the voltage source. Now when an open circuit forms, the stored energy takes the path through the diode and towards the voltage source instead of the open end where the MOSFET is in it’s off state when a negative pulse is provided by the gate driver.

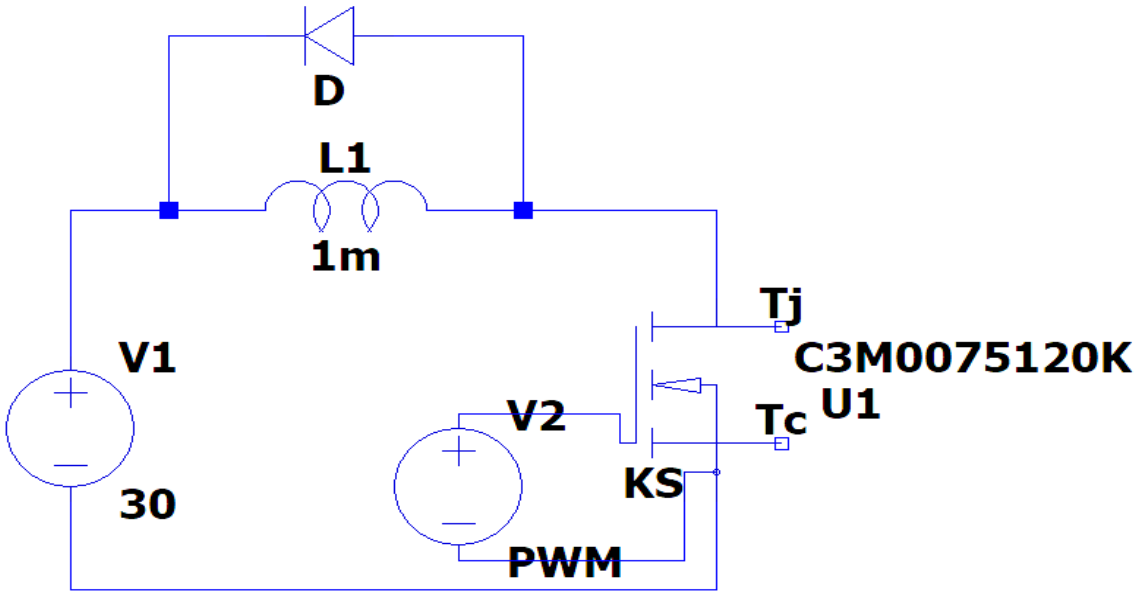


Figure 10: C3M0075120K testing with diode

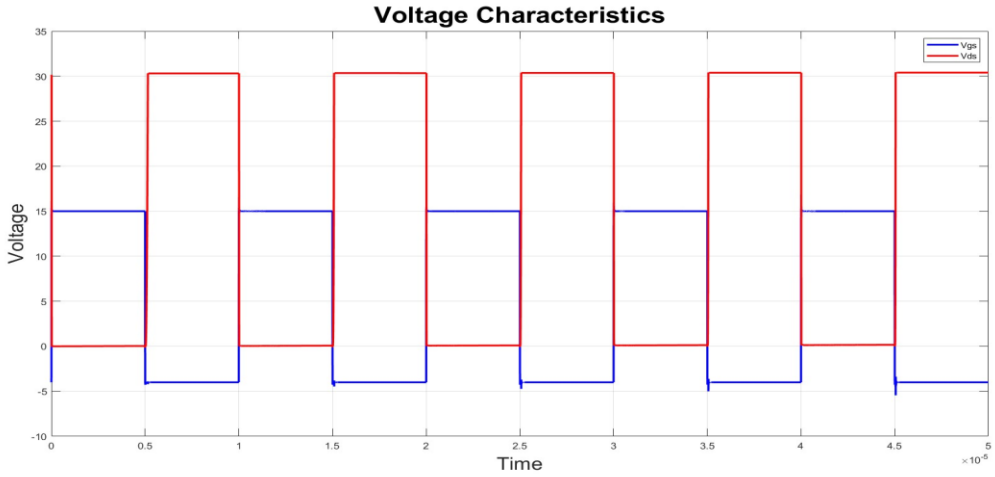


Figure 11: Vds and Vgs

3.2 Experiment 2

The SiC MOSFET is implemented in common-drain (CD) and common-source (CS) bidirectional switch topologies here. Both configurations are operated in two modes to compare the switching behavior and energy losses.

- *Mode 1*: driving the gate of one switch while applying a +15V bias to the other switch's gate to keep it on at all times. This will help realize current flow through internal channels of the SiC MOSFETs.
- *Mode 2*: driving the gate of one switch while applying a -4V bias to the other switch's gate to keep it off at all times. This will help realize current flow through the internal channel of one MOSFET and the body diode of the other.

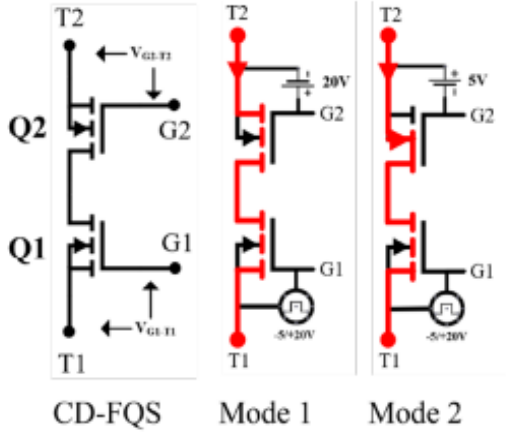


Figure 12: CD Configuration in Mode 1 and Mode 2 [27]

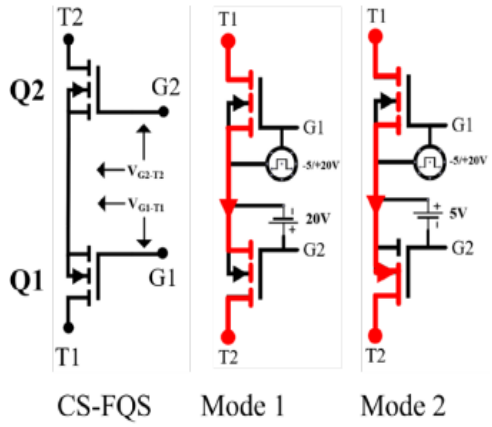


Figure 13: CS Configuration in Mode 1 and Mode 2 [27]

3.2.1 Case 1

C3M0075120K SiC MOSFET was tested for both topologies in operating Mode 1 and Mode 2 with a dc-link inductor of 1mH at a dc link voltage of 50V, a current of 5A and case temperature of 25°C. Double pulse testing (DPT) was performed using gate drives of -4/15V and the results are shown in the following figures. By using the in-built functionality of Ltspice, the energy loss of the switch being tested in each mode is also determined.

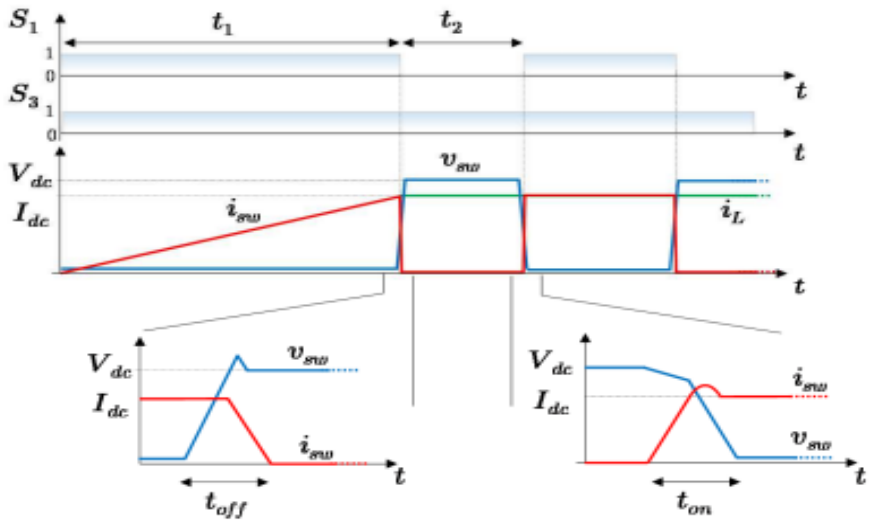


Figure 14: Double Pulse Testing [28]

The DPT technique allows to obtain the semiconductor switching energies by transitorily applying the nominal load current to the switching cell. For that reason, devices can be fully characterized at nominal operation conditions, but with minimal power requirement. From Figure 14, the duration of the first pulse is adjusted to rise the inductor current to the desired value (in our case 5A). At the end of t_1, the LS switch is turned off at (V_{dc}, I_{dc}) and the turn-off losses (E_{OFF}) are computed. At the end of t_2, the LS switch is turned-on again, but at (V_{dc}, I_{dc}) and turn-on losses (E_{ON}) are computed [29].

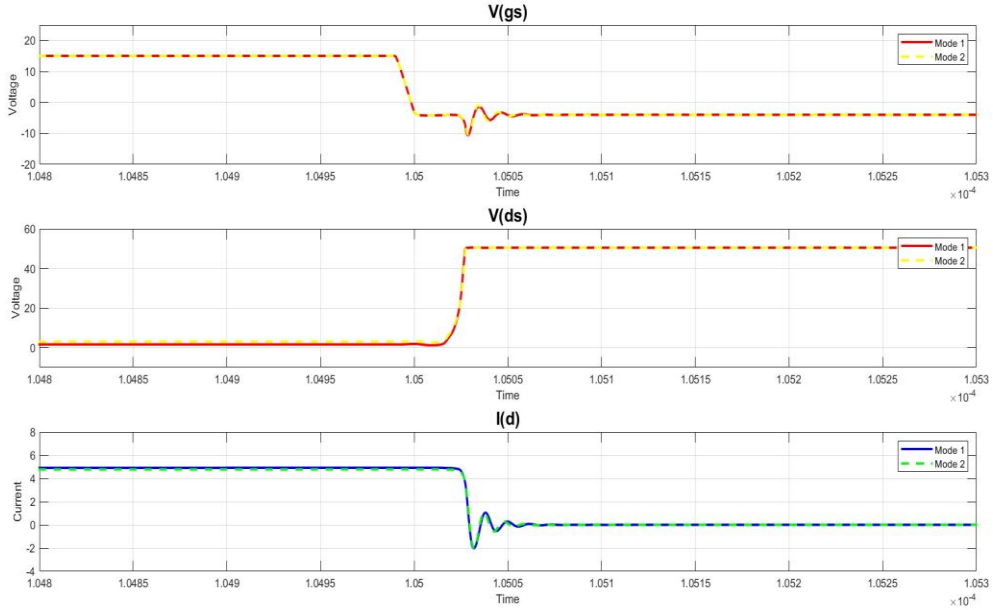


Figure 15: Switching waveforms for the turn-off transition of the CD configuration in Mode 1 and Mode 2

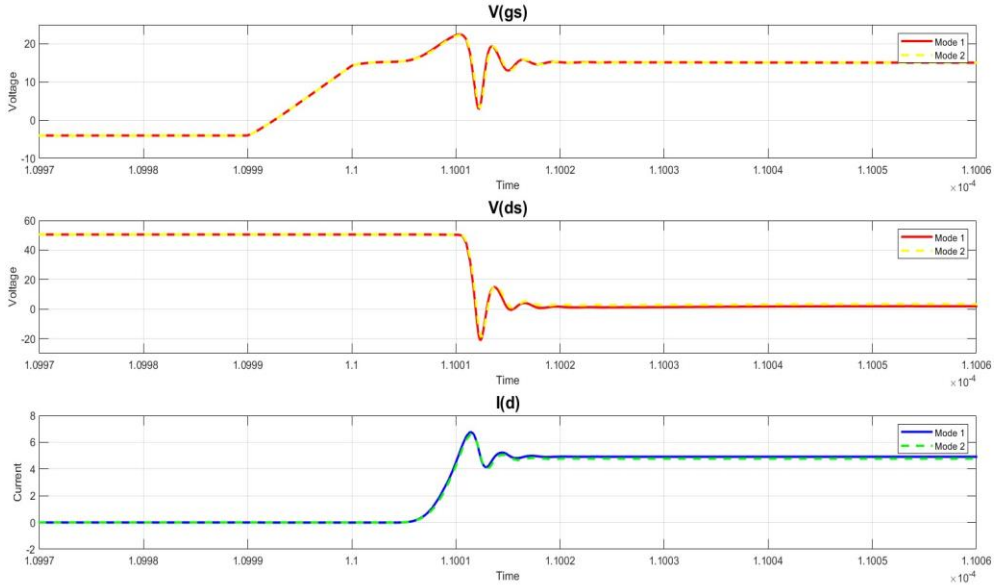


Figure 16: Switching waveforms for the turn-on transition of the CD configuration in Mode 1 and Mode 2

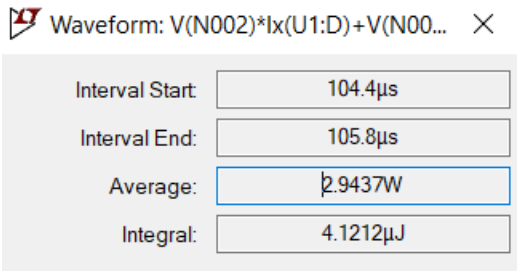


Figure 17: Turn-off switching power and energy losses for Mode 1 of the CD configuration on LTspice

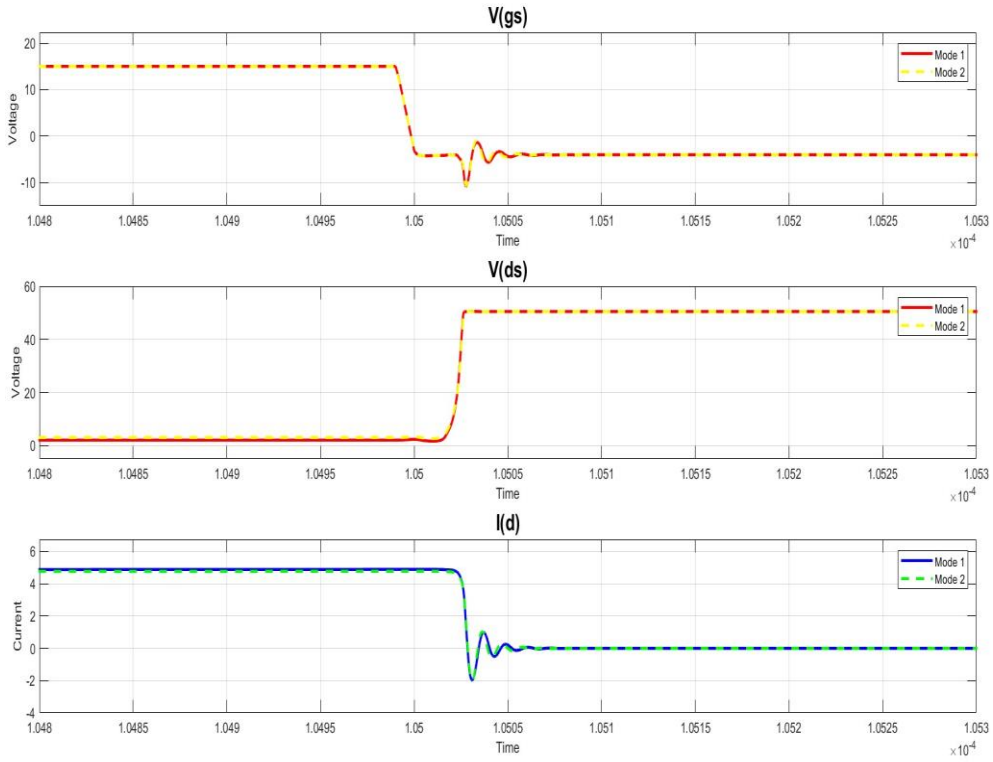


Figure 18: Switching waveforms for the turn-off transition of the CS configuration in Mode 1 and Mode 2

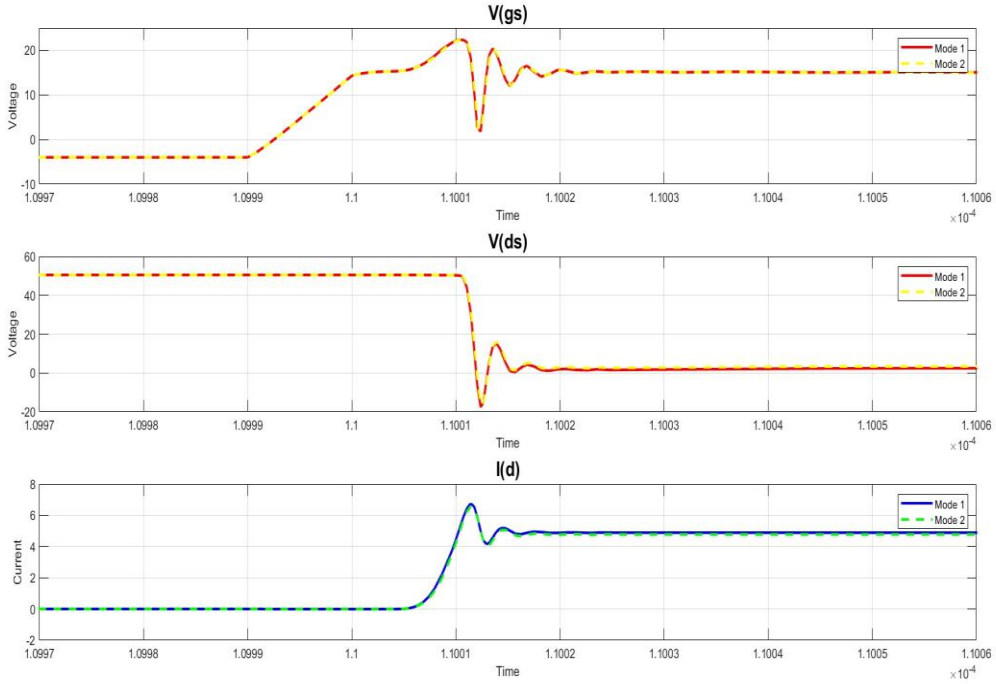


Figure 19: Switching waveforms for the turn-on transition of the CS configuration in Mode 1 and Mode 2

The CD configuration had a turn-on switching loss (E_{ON}) of 18.453 µJ in Mode 1 and 16.947 µJ in Mode 2, and a turn-off switching loss (E_{OFF}) of 4.121 µJ in Mode 1 and 6.017 µJ in Mode 2. The CS configuration had a turn-on switching loss of 15.835 µJ in Mode 1 and 14.656 µJ in Mode 2, and a turn-off switching loss of 5.969 µJ in Mode 1 and 6.331 µJ in Mode 2.

Table 2: Switching losses in Mode 1 and Mode 2 for the CD and CS configurations

Configuration	**Mode**	**E_{ON} (µJ)**	**E_{OFF} (µJ)**	**E_{TOT} (µJ)**
Common Drain	Mode 1	18.453	4.121	22.574
	Mode 2	16.947	6.017	22.964
Common Source	Mode 1	15.835	5.969	21.804
	Mode 2	14.656	6.331	20.987

The CD configuration shows a significant change in both E_{ON} and E_{OFF} when shifting from Mode 1 to Mode 2 but the total energy loss (E_{TOT}) is almost the same. The CS configuration shows a decrease in E_{ON} when going from Mode 1 to Mode 2 and an increase in E_{OFF}.

3.2.2 Case 2

This test compared the switching losses of the CD and CS configurations shown in Figure 12 and 13 at currents of 5A and 10A at case temperatures of 75° and 125°C. DPT was performed using gate drives of -4/15V at a dc link voltage of 50V with a dc-link inductor of 1mH.

3.2.2.1 CD Mode 1

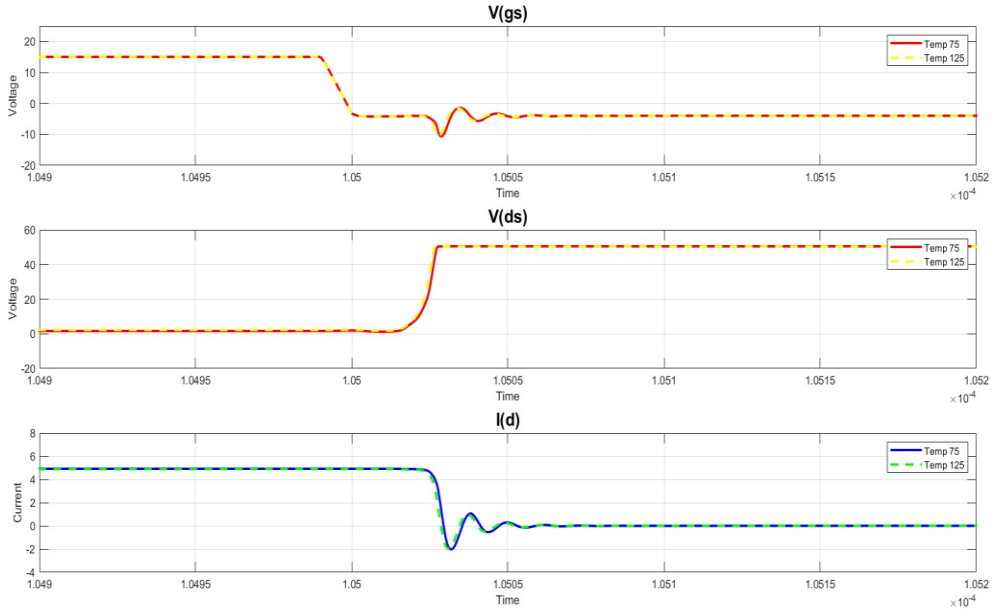


Figure 20: Switching waveforms for the turn-off transition of the CD configuration in Mode 1 at different temperatures for 5A

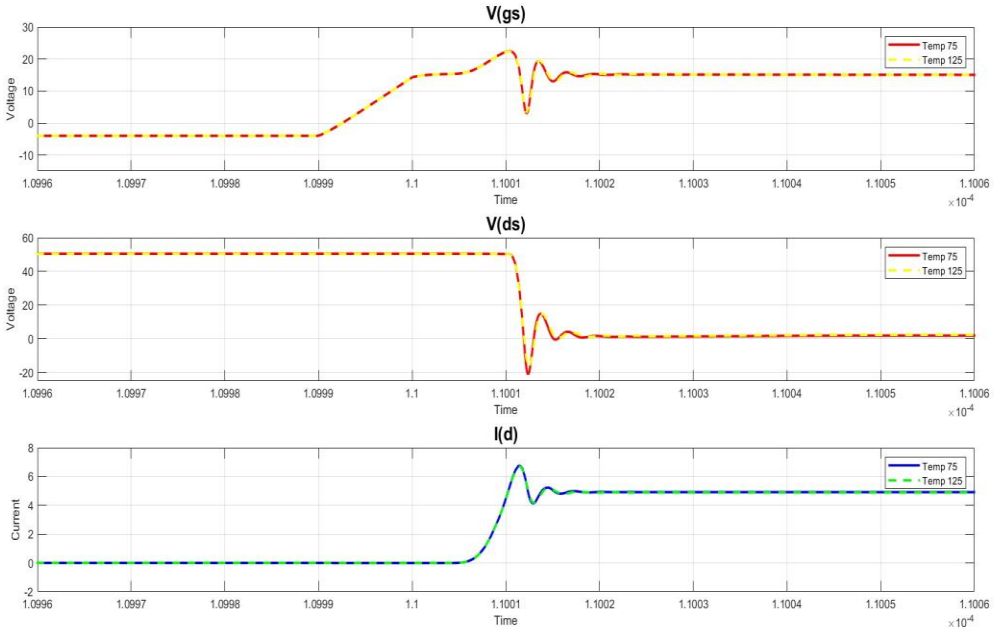


Figure 21: Switching waveforms for the turn-on transition of the CD configuration in Mode 1 at different temperatures for 5A

3.2.2.2 CD Mode 2

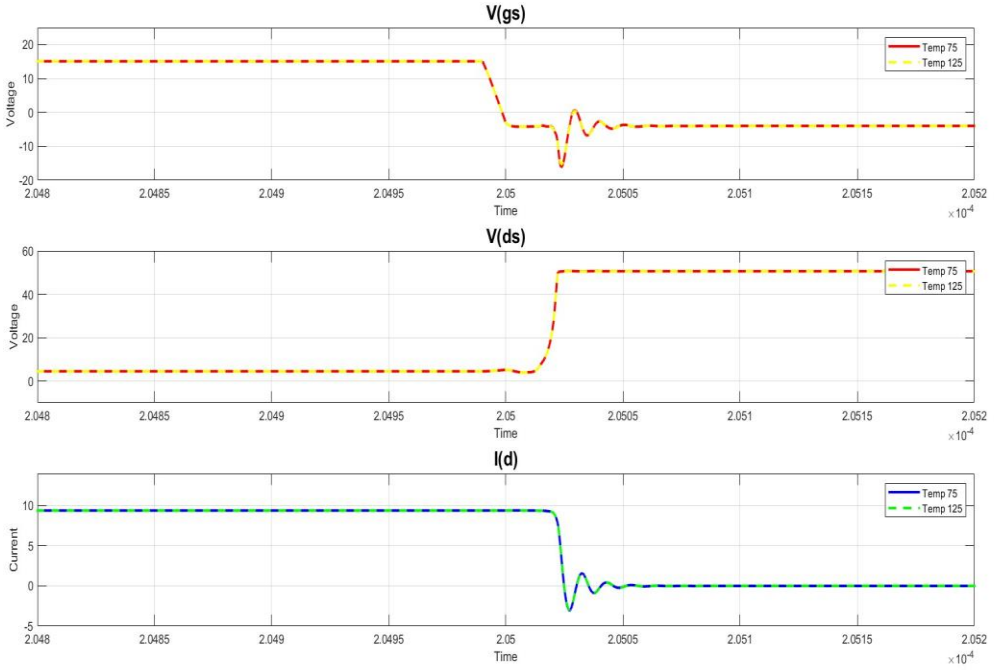


Figure 22: Switching waveforms for the turn-off transition of the CD configuration in Mode 2 at different temperatures for 10A

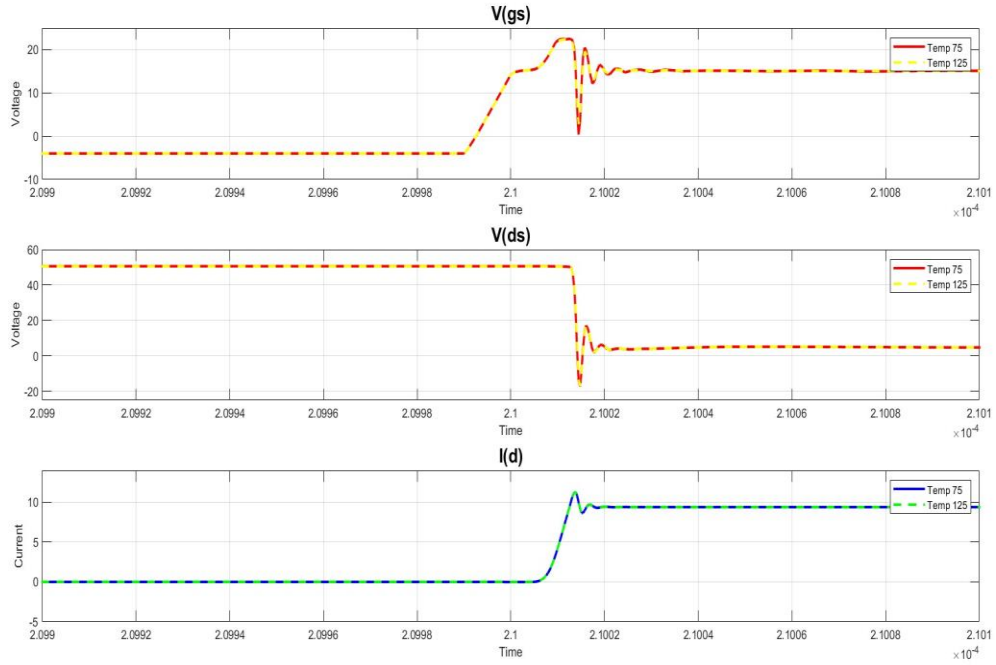


Figure 23: Switching waveforms for the turn-on transition of the CD configuration in Mode 2 at different temperatures for 10A

Table 3: Switching losses in Mode 1 for the CD configuration at 75°C at different currents

I_D (A)	E_{ON} (µJ)	E_{OFF} (µJ)	E_{TOT} (µJ)	$I_{ON,PK}$ (A)
5	15.835	3.779	19.614	6.4
10	19.722	7.074	26.796	11.6

Table 4: Switching losses in Mode 1 for the CD configuration at 125°C at different currents

I_D (A)	E_{ON} (µJ)	E_{OFF} (µJ)	E_{TOT} (µJ)	$I_{ON,PK}$ (A)
5	12.541	3.204	15.745	6.8
10	16.083	5.520	21.603	11.9

3.2.2.3 CS Mode 1

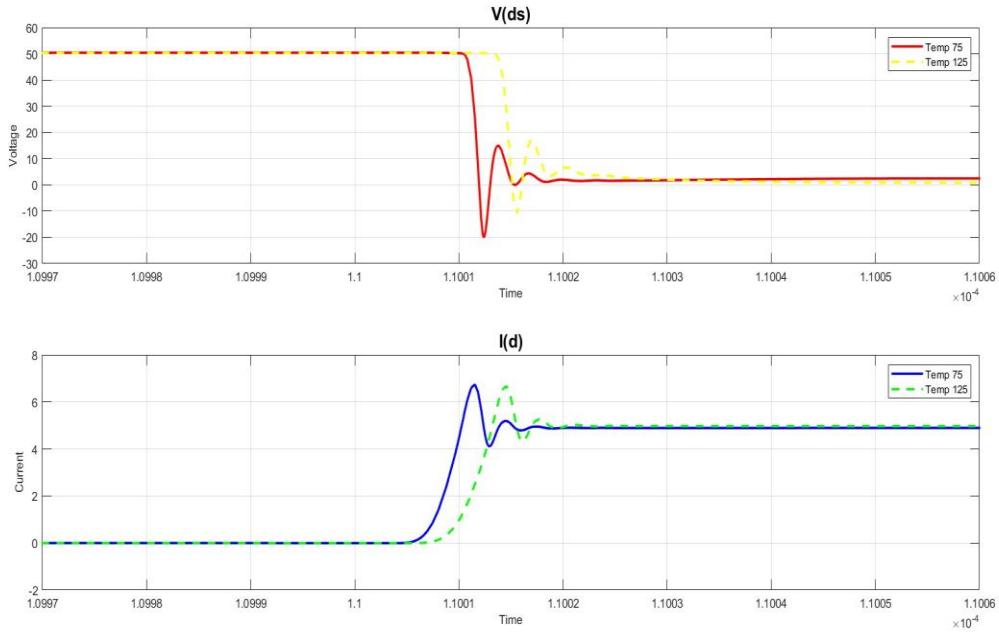


Figure 24: Switching waveforms for the turn-on transition of the CS configuration in Mode 1 at different temperatures for 5A

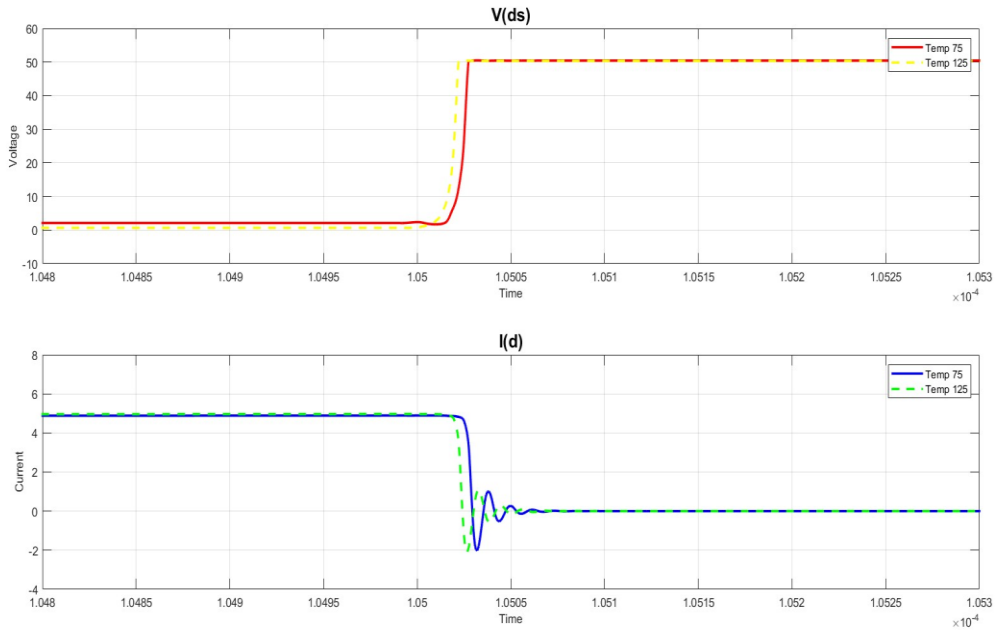


Figure 25: Switching waveforms for the turn-off transition of the CS configuration in Mode 1 at different temperatures for 5A

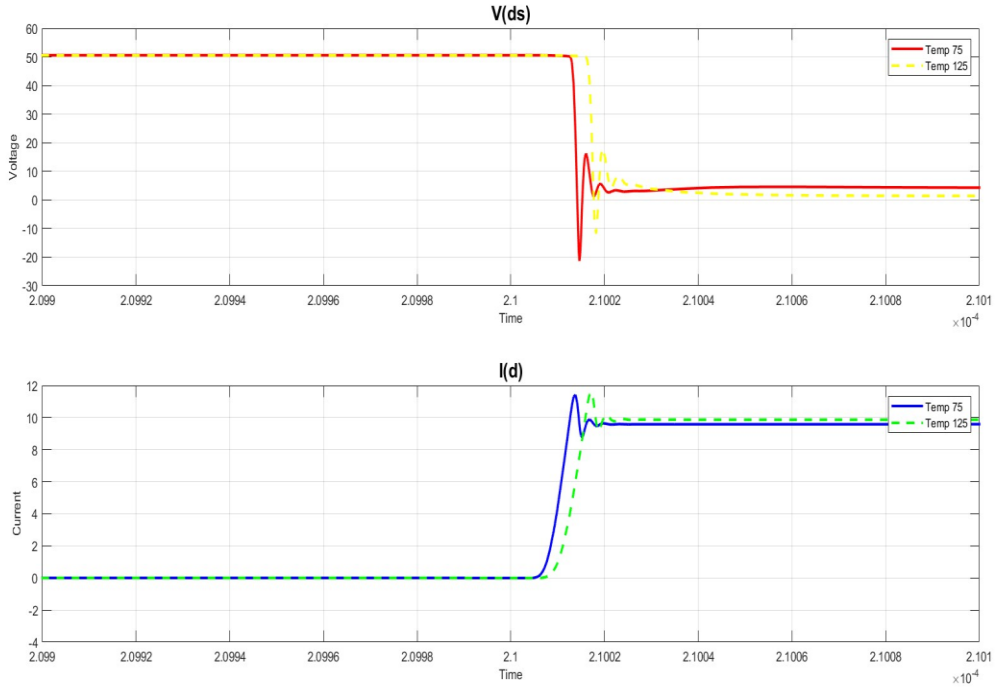


Figure 26: Switching waveforms for the turn-on transition of the CS configuration in Mode 1 at different temperatures for 10A

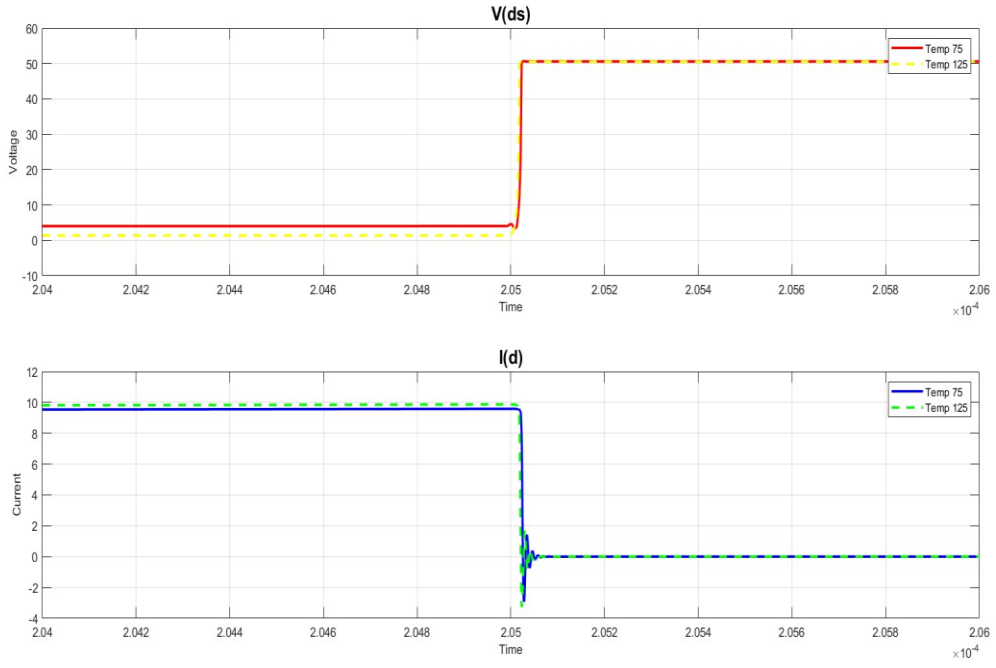


Figure 27: Switching waveforms for the turn-off transition of the CS configuration in Mode 1 at different temperatures for 10A

3.2.2.4 CS Mode 2

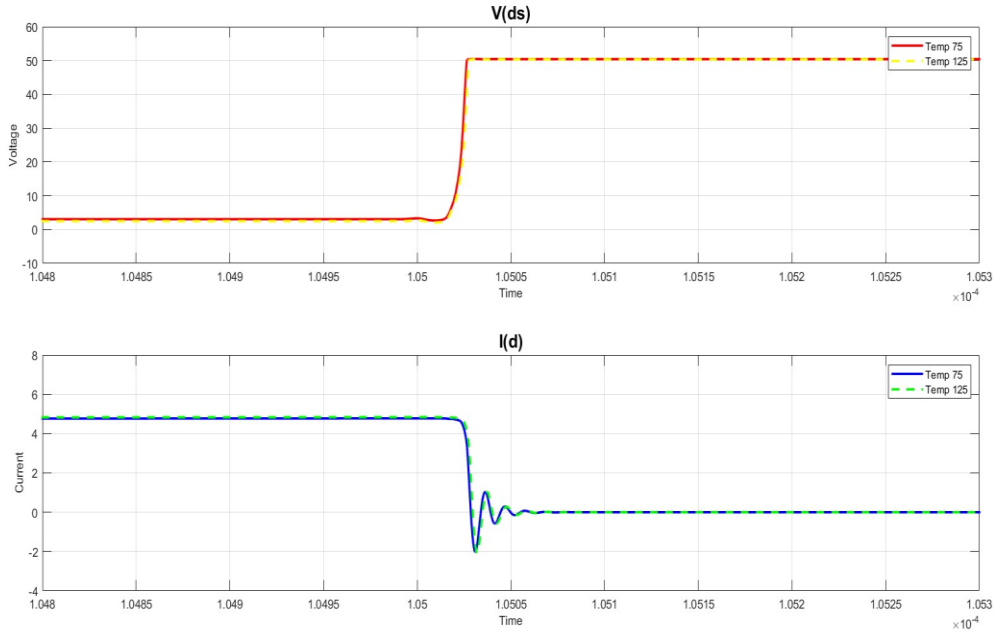


Figure 28: Switching waveforms for the turn-off transition of the CS configuration in Mode 2 at different temperatures for 5A

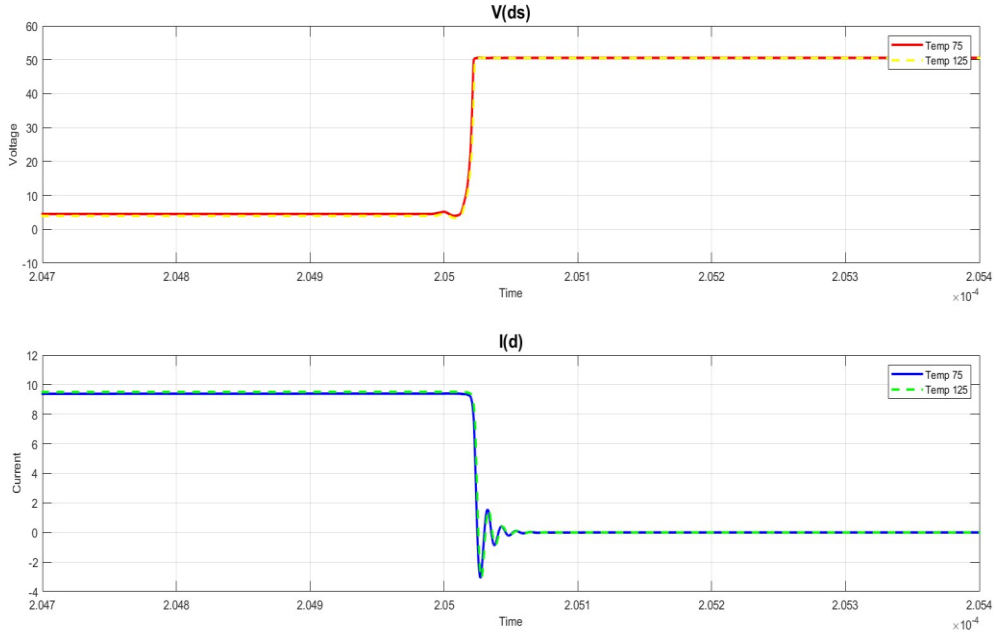


Figure 29: Switching waveforms for the turn-off transition of the CS configuration in Mode 2 at different temperatures for 10A

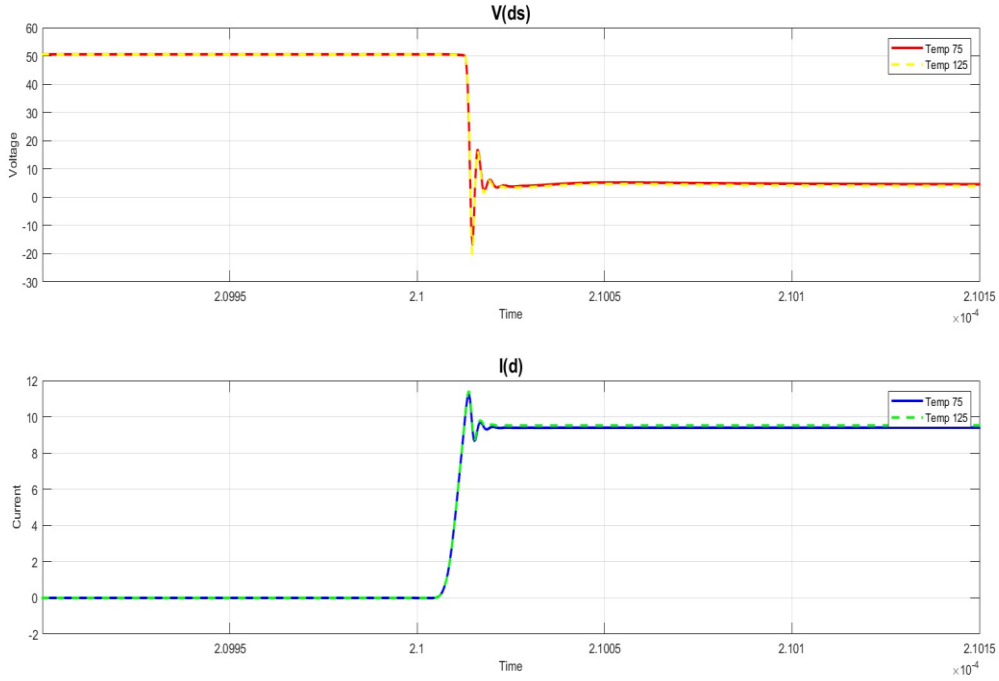


Figure 30: Switching waveforms for the turn-on transition of the CS configuration in Mode 2 at different temperatures for 10A

Table 5: Switching losses in Mode 1 for the CS configuration at 75°C at different currents

I_D (A)	E_{ON} (µJ)	E_{OFF} (µJ)	E_{TOT} (µJ)	$I_{ON,PK}$ (A)
5	15.323	7.162	22.485	6.3
10	19.734	9.283	29.017	11.4

Table 6: Switching losses in Mode 1 for the CS configuration at 125°C at different currents

I_D (A)	E_{ON} (µJ)	E_{OFF} (µJ)	E_{TOT} (µJ)	$I_{ON,PK}$ (A)
5	12.763	4.939	17.702	6.8
10	23.825	7.827	31.652	11.7

3.2.2.5 Results

These results demonstrate that for the CD configuration there is a decrease in E_{ON} and E_{OFF} with an increase in case temperature. For the CS configuration there is an increase in E_{OFF} and a decrease in E_{ON} with increasing case due to the decrease in the threshold voltage at higher temperatures. Due to this there is a significant change in E_{TOT} for an increase in current and temperature.

3.3 Experiment 3

The half bridge circuit was simulated under both CS and CD configurations of the SiC MOSFETs. DPT was performed using gate drives of -4/15V on the top switch at a dc link voltage of 50V with a dc-link inductor of 1mH. The switch below the device under test (DUT) was kept at 15V for Mode 1 and at -4V for Mode 2. The rest of the switches are gated as follows.

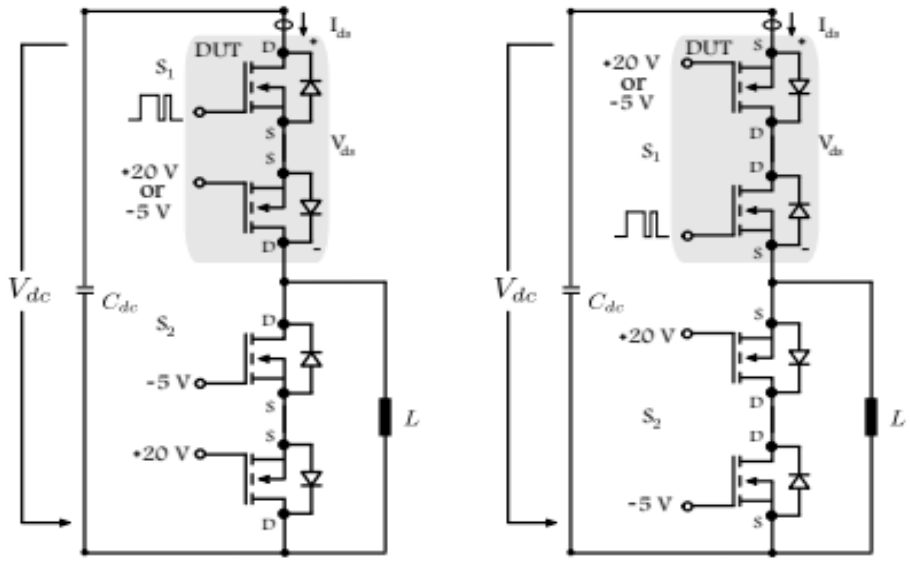


Figure 31: CS and CD configuration for half bridge simulation [30]

3.3.1 CS Configuration

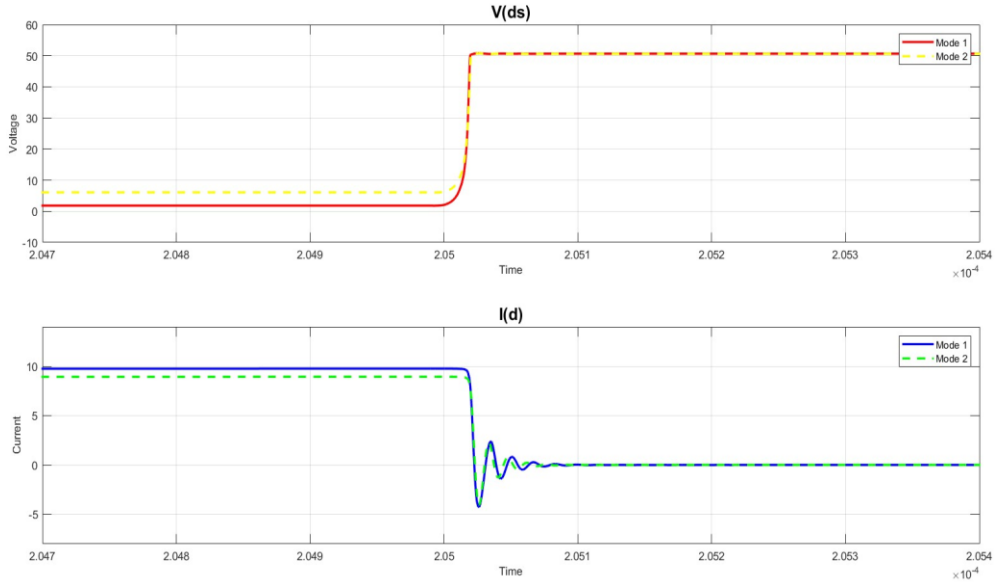


Figure 32: Switching waveforms for the turn-off transition of the CS configuration in the half bridge

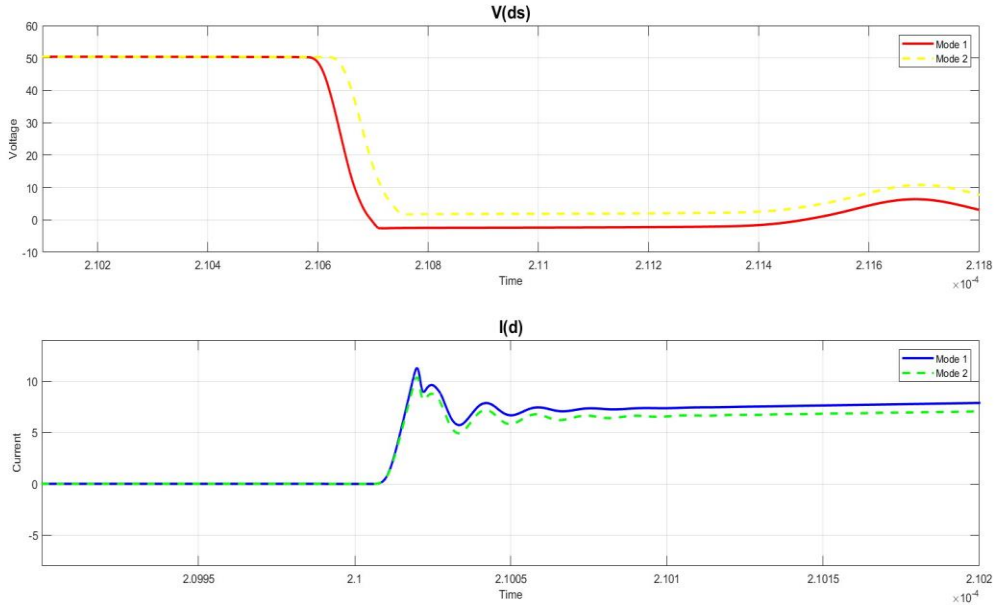


Figure 33: Switching waveforms for the turn-on transition of the CS configuration in the half bridge

3.3.2 CD Configuration

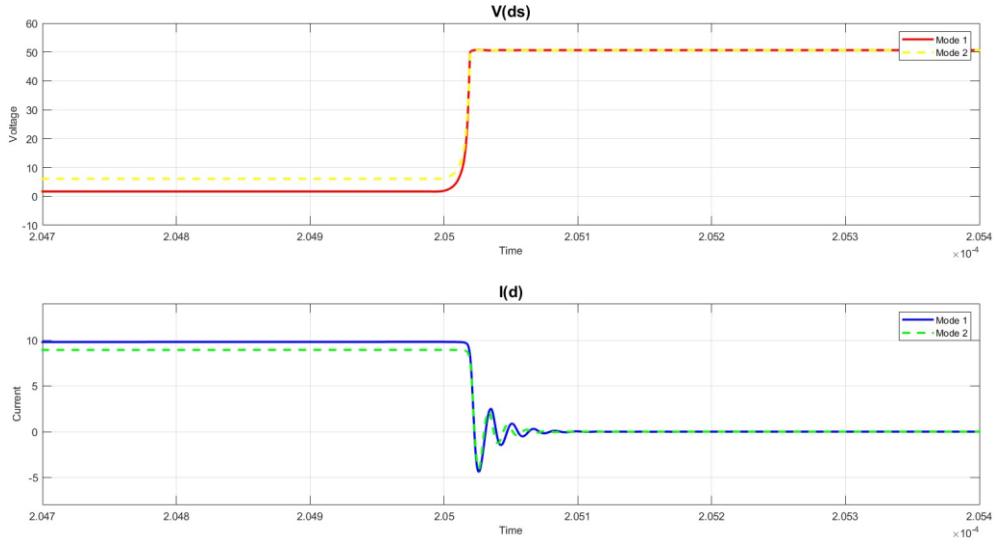


Figure 34: Switching waveforms for the turn-off transition of the CD configuration in the half bridge

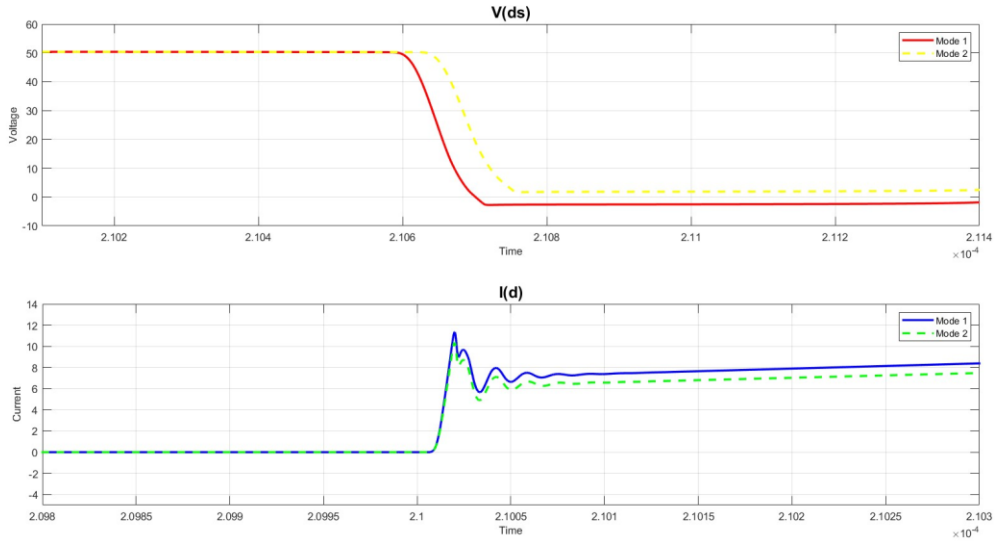


Figure 35: Switching waveforms for the turn-on transition of the CS configuration in the half bridge

3.3.3 Results

The graphs for Mode 1 in both configurations in the turn-on and turn-off stages follows but lags behind Mode 2 and takes longer to settle. This displays an increase in switching losses (E_{ON}, E_{OFF}) in Mode 1 and also contributes towards slower switching of the MOSFET.

3.4 Experiment 4

A three phase CSI was simulated using MATLAB and Simulink. The PWM given to the MOSFETs was generated by comparing a sawtooth wave with three 120° shifted sine waves as displayed in Figure 36.

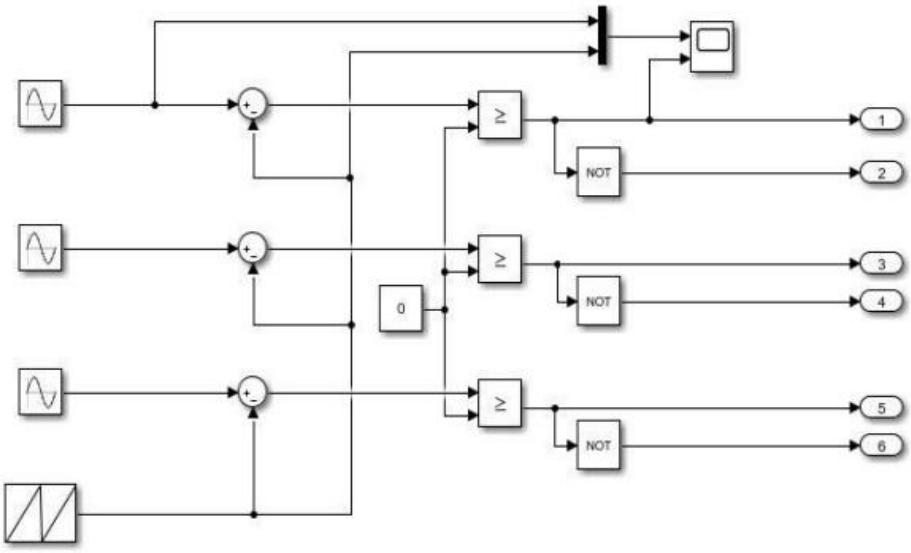


Figure 36: PWM Generator

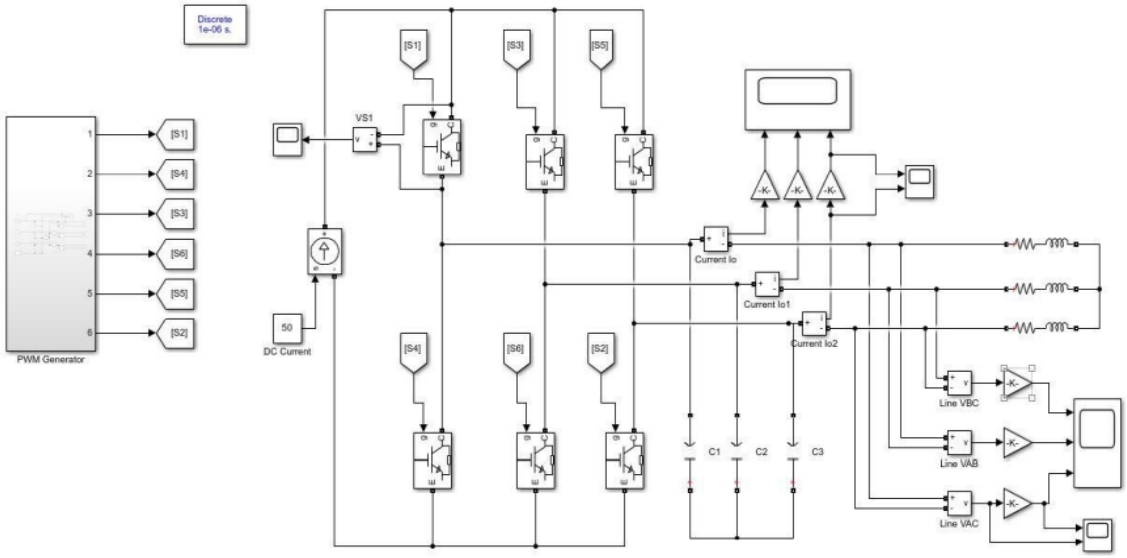


Figure 37: Three Phase CSI on Simulink

Figure 37 shows the three phase star connected inverter with a RL load. An ac current source of 50A is used at the input. The gains are used to create RMS values of voltages and current from peak values at all phases. The resistor and inductor load per phase are 15Ω and 0.006H respectively. The circuit has been tested at a frequency of 5kHz.

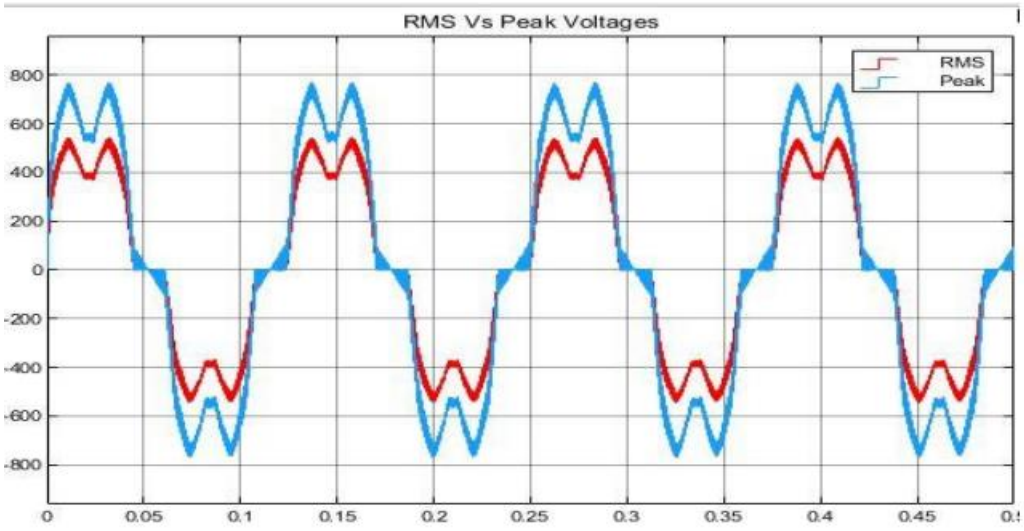


Figure 38: Comparison between RMS and Peak voltages

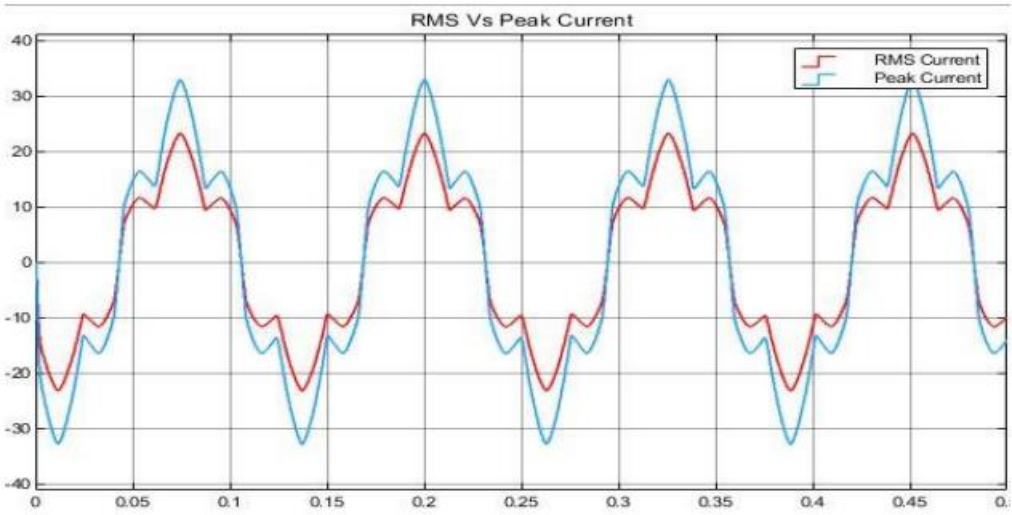


Figure 39: Comparison between RMS and Peak currents

4 Hardware Implementation

The testing of Cree's N-channel 3rd generation C3M0075120K SiC MOSFET was done using CGD15SG00D2 which is an isolated gate driver board (Appendix C) which generates the PWM and also provides isolation through a built-in optocoupler. The pin configurations for both are as follows.

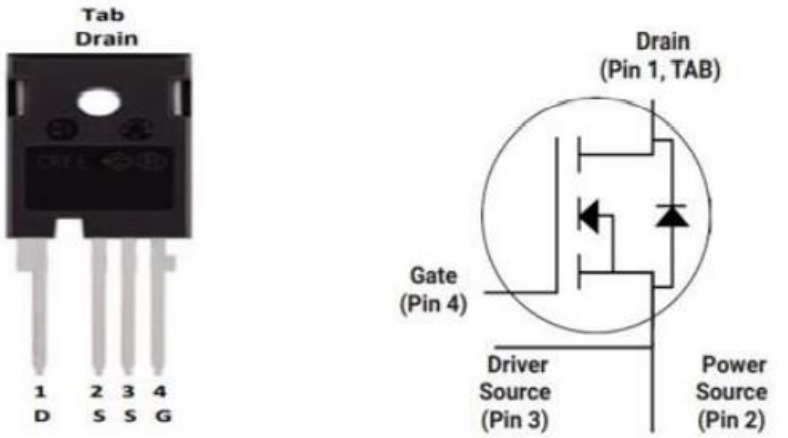
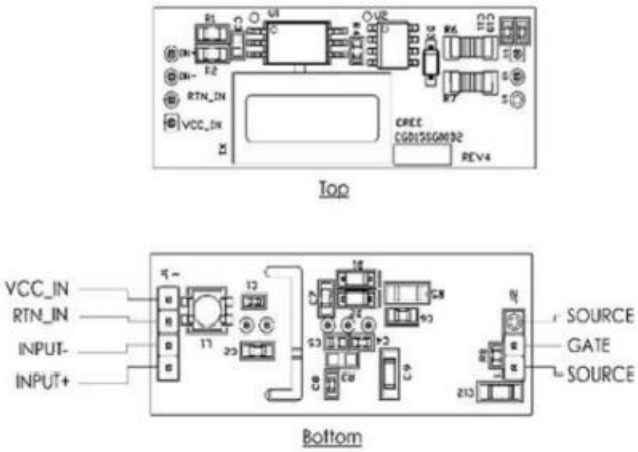


Figure 40: Pin configuration of C3M0075120K SiC MOSFET



VCC_IN	12V Input
RTN_IN	12V Return
INPUT-	PWM Return
INPUT	PWM Input
Source	MOSFET Source
Gate	MOSFET GATE

Figure 41: Pin configuration of CGD15SG00D2 gate driver board

4.1 Single switch testing

The C3M0075120K SiC MOSFET was tested on a breadboard with a resistive load of 22Ω and a dc input voltage of 15V. The 0/5V input PWM to the gate driver circuit board was provided with a signal generator. The results are below.

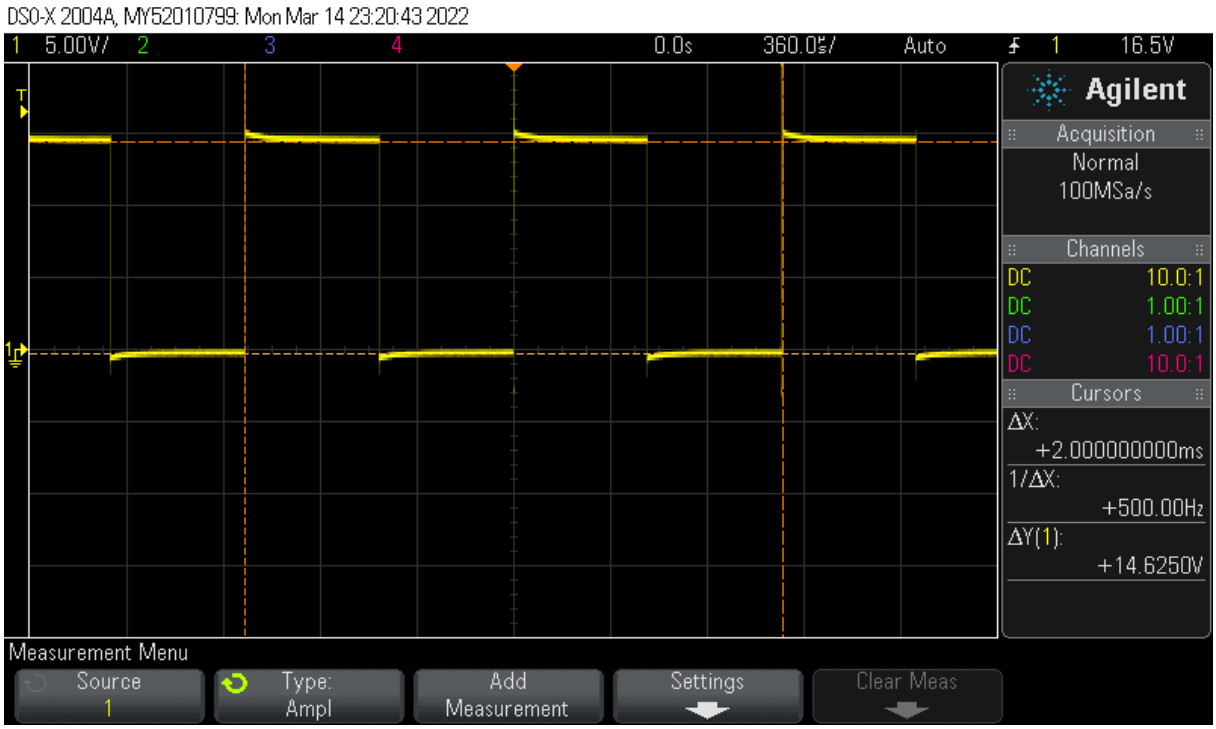


Figure 42: Drain to Source voltage across C3M0075120K

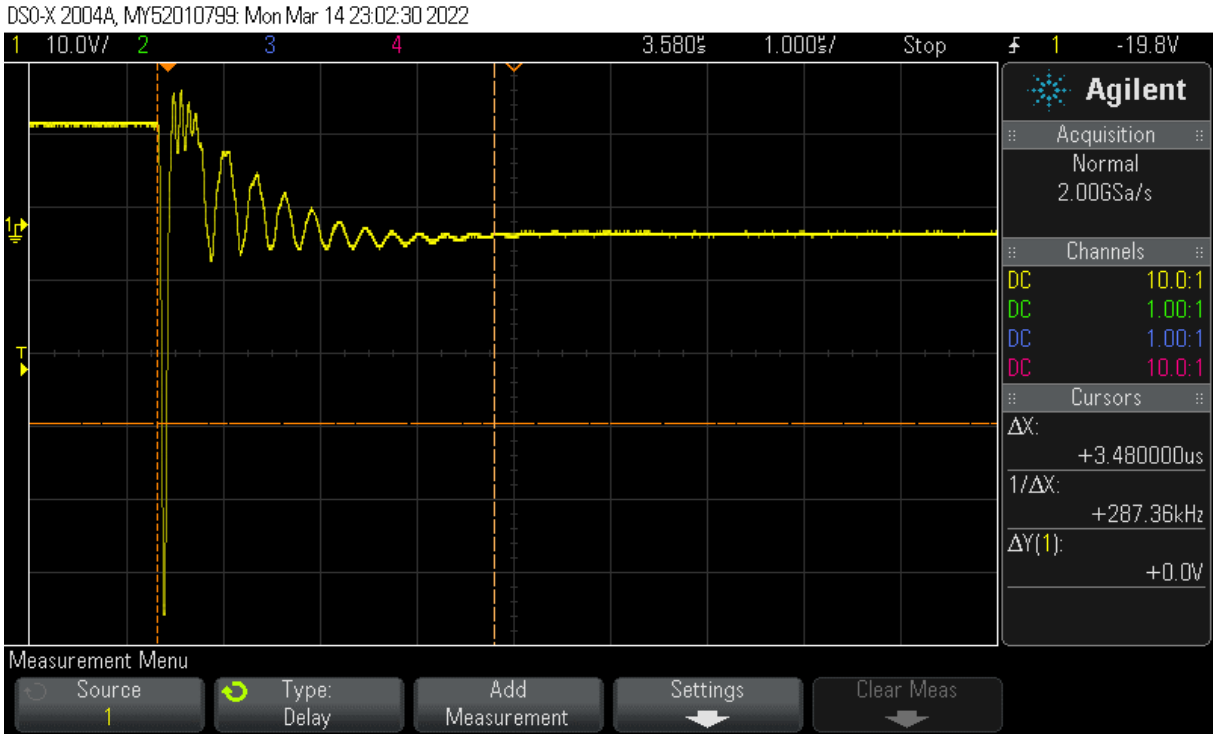


Figure 43: Turn-off transition of Vgs

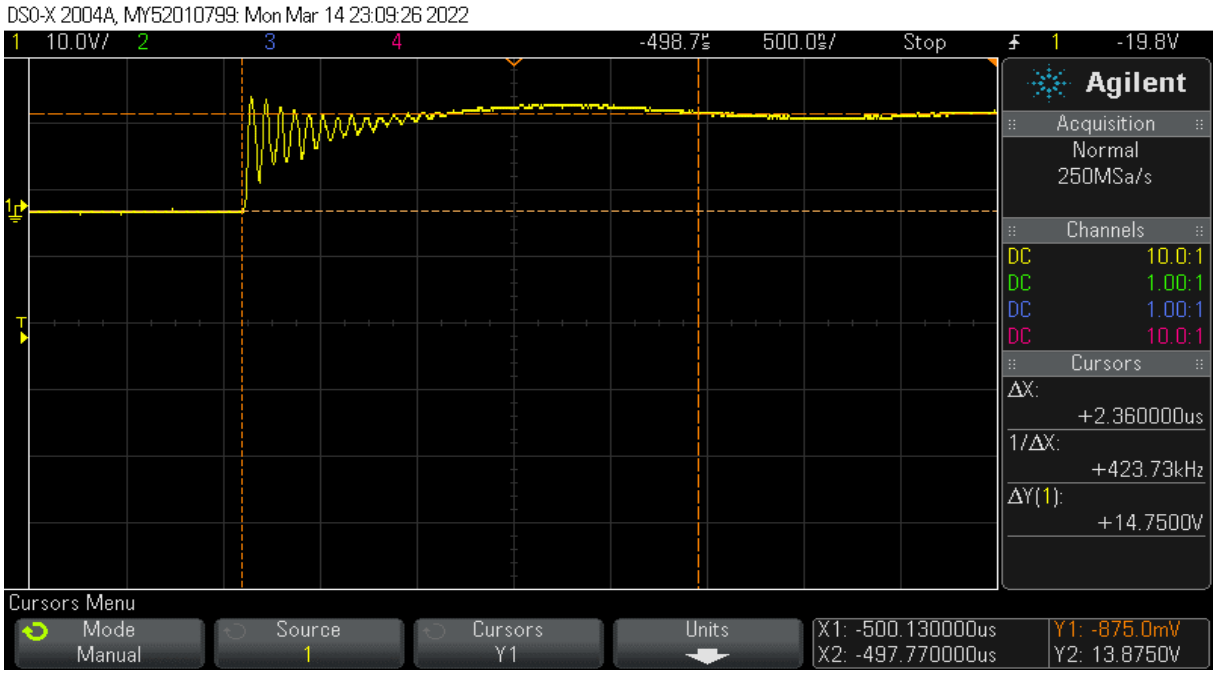


Figure 44: Turn-on transition of Vgs

Due to the noise being observed in the results, a PCB was designed and used in the latter experiment to mitigate it.

4.2 PCB Design

Altium Designer was used to make the schematic displayed in Figure 45 and design it into a PCB. The MOSFETs on either side are in CS configuration and the two legs are independent of one another. Hence this can be used to test a single leg and also a half bridge circuit.

Junctions J1, J2, J6 and J7 are ports used to provide the PWM to function the gate driver board whereas J3 and J8 provide the V_{CC}. Junctions J4 and J5 are for the dc input voltage for the switches.

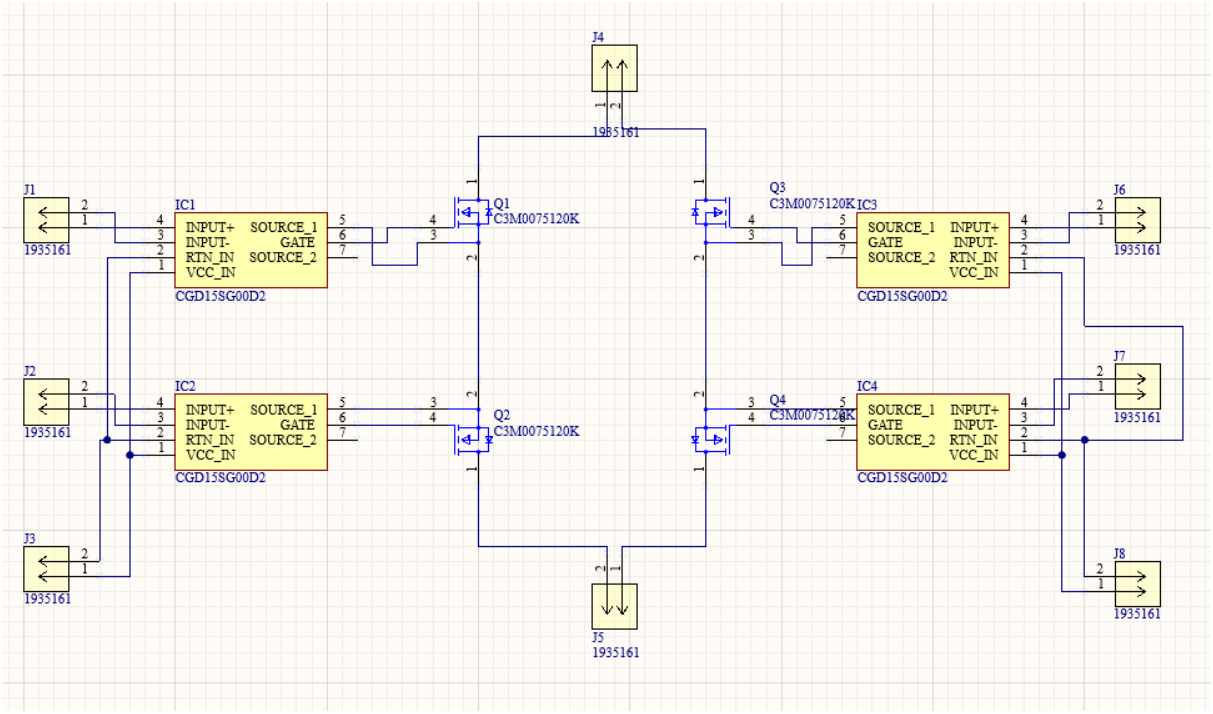


Figure 45: PCB Schematic

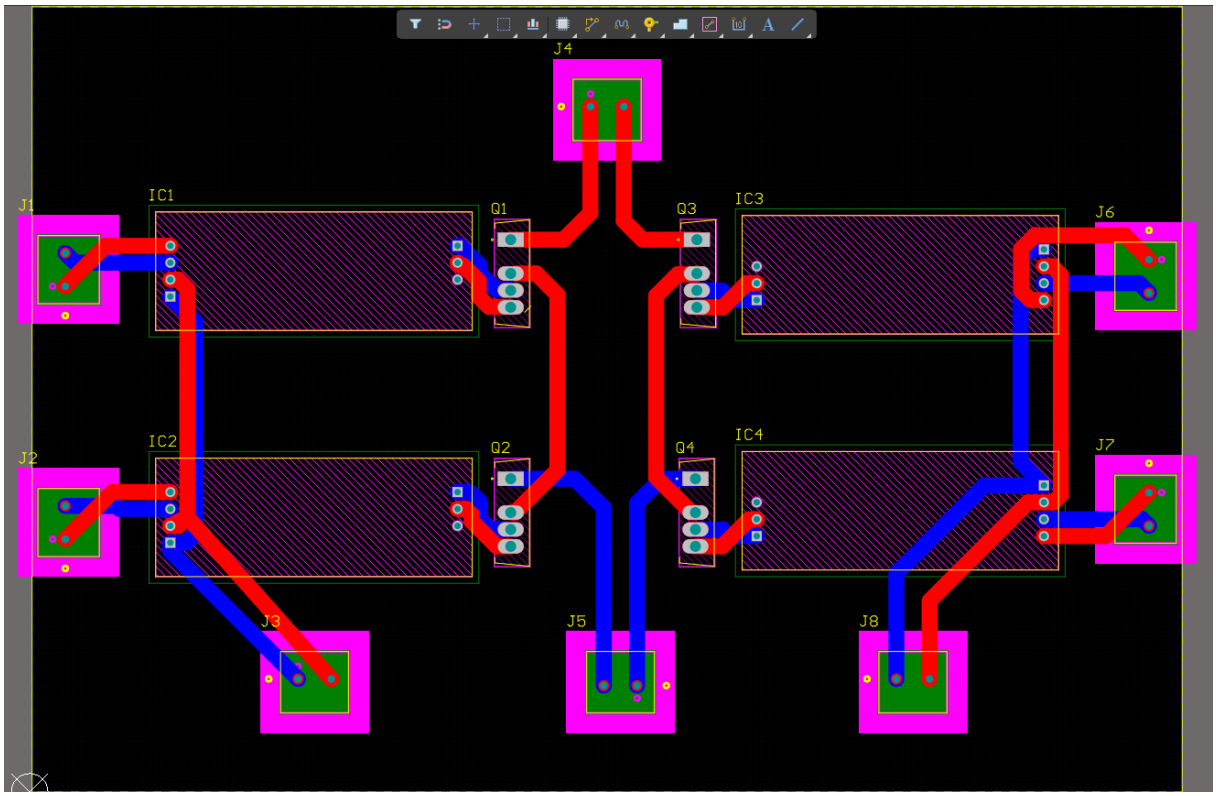


Figure 46: PCB Design

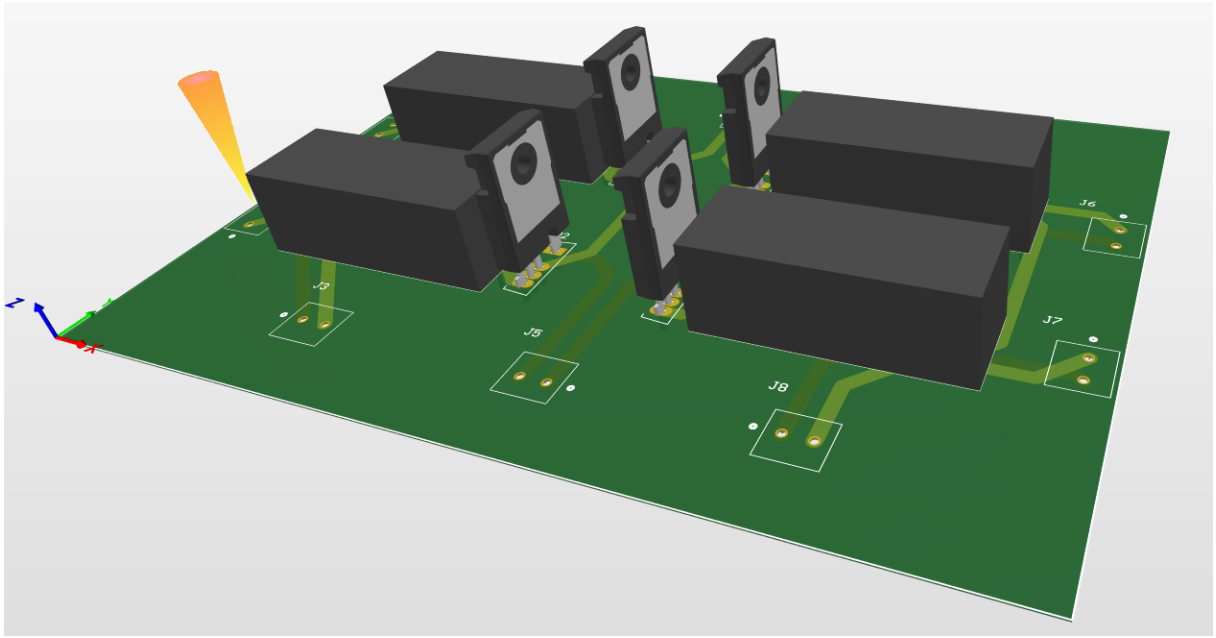


Figure 47: 3D Model of PCB

4.3 Anti-parallel MOSFET testing

The PCB in Figure 46 was used to test the C3M0075120K SiC MOSFETs in CS configuration for reverse voltage blocking. A single gate driver board was used to provide the gate to both the switches.

A dc input voltage of 15V was used with a resistive load of 22Ω. The 0/5V input PWM to the gate driver circuit board was provided with a signal generator. The results are below.

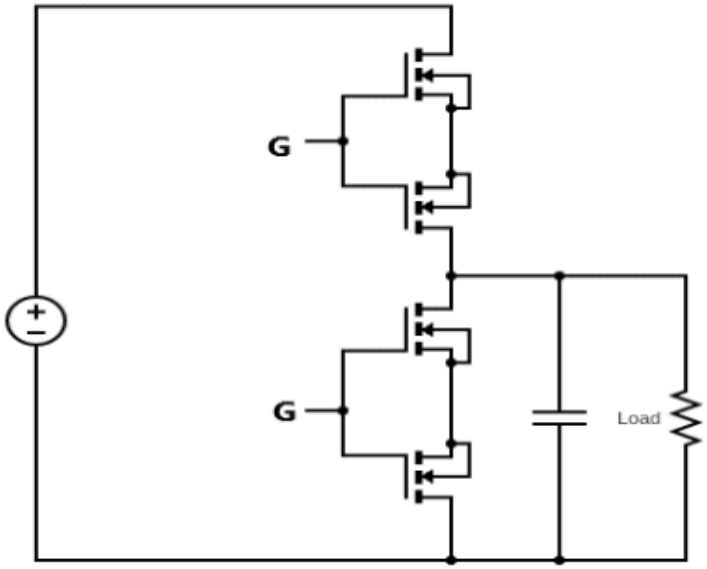


Figure 48: Anti-parallel MOSFETs

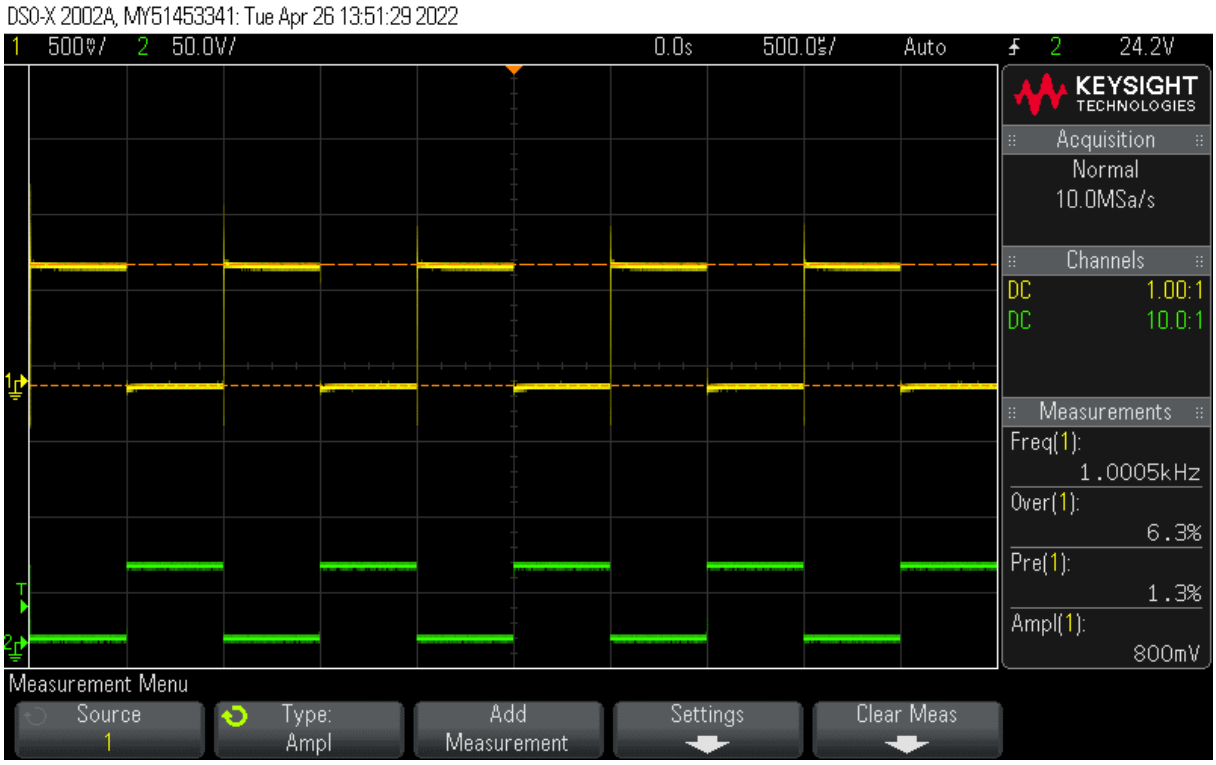


Figure 49: Vgs and Vds across the MOSFETs

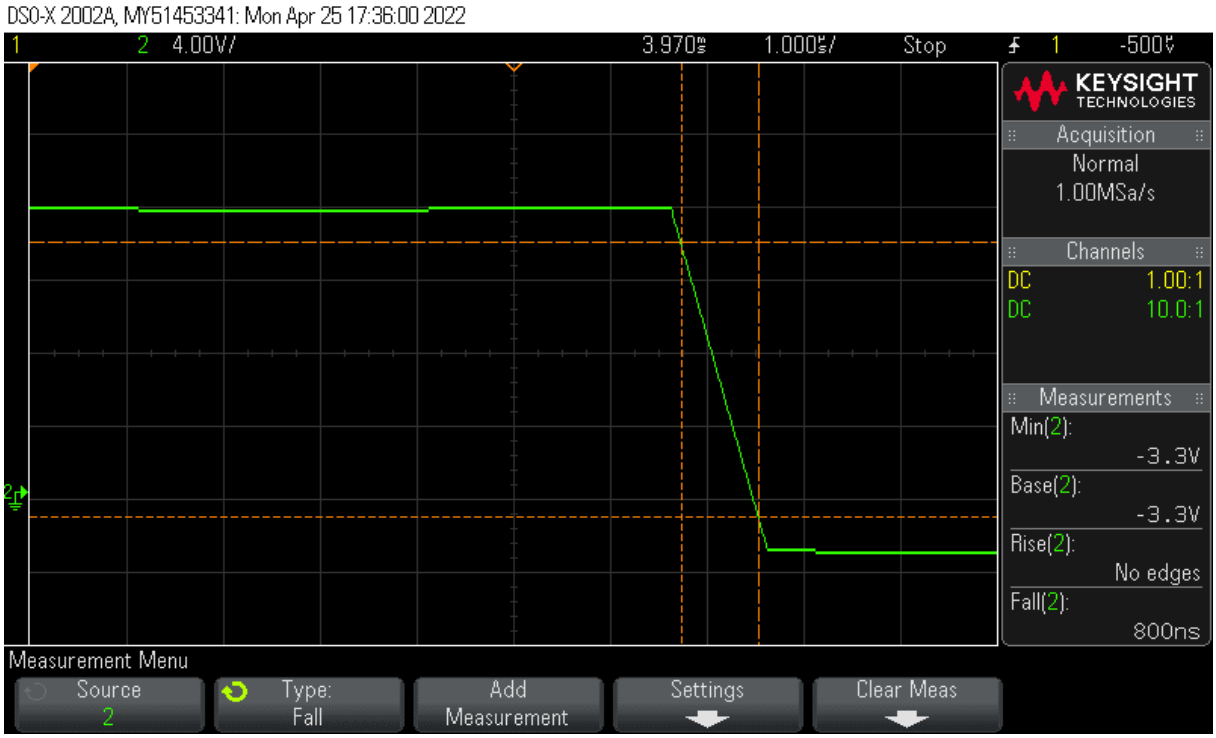


Figure 50: Turn-off transition of Vgs

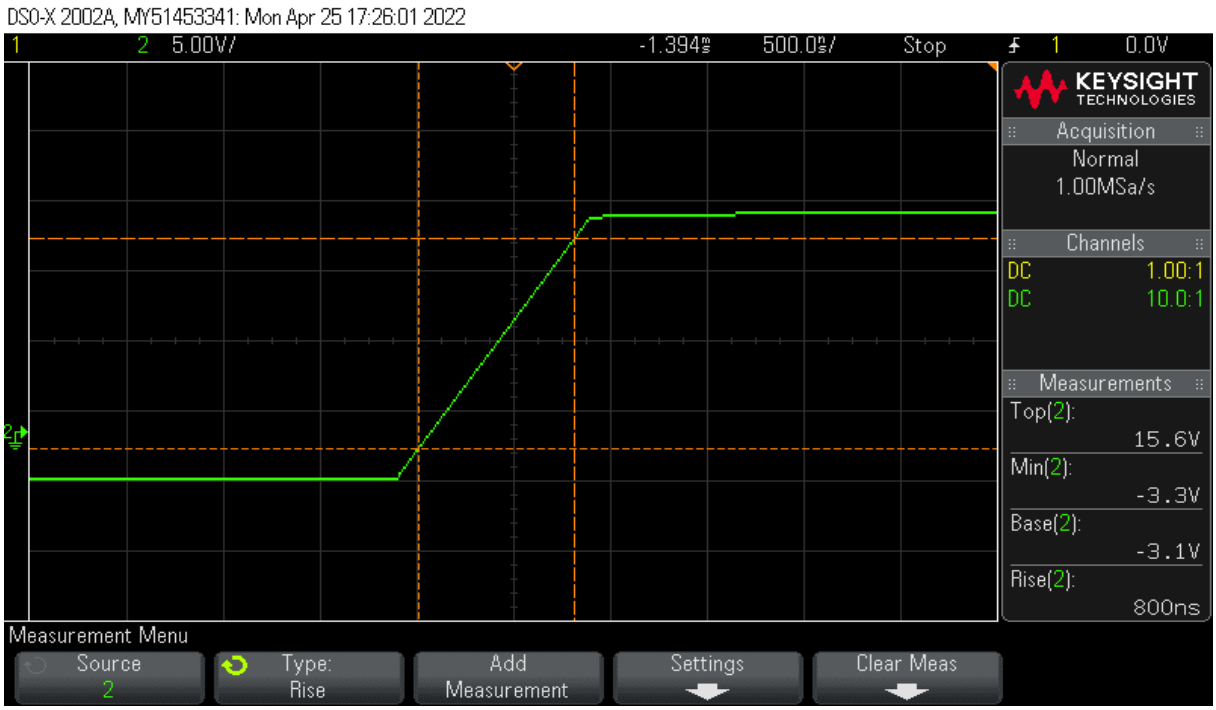


Figure 51: Turn-on transition of Vgs

5 Conclusion

The advantages of CSIs over VSIs were discussed in this paper and how to implement CSIs using switches with reverse voltage blocking capability. In this case the SiC MOSFET was chosen and double pulse tested in anti-parallel and half-bridge scenarios. The graphical data and energy losses were determined for different configurations under different conditions.

The recent advances in power electronic semiconductors have made possible to improve the performances of CSIs by reducing conduction losses and increasing switching frequency at the same time. Therefore there is a lot of room for advancements and adaptation. SiC is an efficient, fast switching device that contains many properties that are beneficial in many applications for their capability to work with high power and high frequency circuits.

Similar tests presented in this paper can be performed on other switching devices for comparison and to select the most suited for CSI functionality and applications. Also the PCB design and simulations on Altium Designer and Ltspice respectively can be used as a foundation for future work for both software and hardware implementations.

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Appendices

Appendix A:

Label 1: Recommended Operating Conditions of IXDN609

Parameter	Conditions	Symbol	Minimum	Typical	Maximum	Units
Input Voltage, High	$4.5V \le V_{CC} \le 18V$	V_{IH}	3.0	-	-	V
Input Voltage, Low	$4.5V \le V_{CC} \le 18V$	V_{IL}	-	-	0.8	
Input Current	$0V \le V_{IN} \le V_{CC}$	I_{IN}	-	-	±10	µA
EN Input Voltage, High	IXDD609SI only	V_{ENH}	$2/3V_{CC}$	-	-	V
EN Input Voltage, Low	IXDD609SI only	V_{ENL}	-	-	$1/3V_{CC}$	
Output Voltage, High	-	V_{OH}	V_{CC}-0.025	-	-	V
Output Voltage, Low	-	V_{OL}	-	-	0.025	
Output Resistance, High State	V_{CC}=18V, I_{OUT}=-100mA	R_{OH}	-	0.6	1	Ω
Output Resistance, Low State	V_{CC}=18V, I_{OUT}=100mA	R_{OL}	-	0.4	0.8	
Output Current, Continuous	Limited by package power dissipation	I_{DC}	-	-	±2	A
Rise Time	V_{CC}=18V, C_{LOAD}=10nF	t_r	-	22	35	ns
Fall Time	V_{CC}=18V, C_{LOAD}=10nF	t_f	-	15	25	
On-Time Propagation Delay	V_{CC}=18V, C_{LOAD}=10nF	t_{ondly}	-	40	60	
Off-Time Propagation Delay	V_{CC}=18V, C_{LOAD}=10nF	t_{offdly}	-	42	60	
Enable to Output-High Delay Time (IXDD609SI Only)	V_{CC}=18V	t_{ENOH}	-	25	60	
Disable to High Impedance State Delay Time (IXDD609SI Only)	V_{CC}=18V	t_{DOLD}	-	35	60	
Enable Pull-Up Resistor	-	R_{EN}	-	200	-	kΩ
Power Supply Current	V_{CC}=18V, V_{IN}=3.5V	I_{CC}	-	1	2	mA
	V_{CC}=18V, V_{IN}=0V		-	<1	10	µA
	V_{CC}=18V, V_{IN}=V_{CC}		-	<1	10	

Appendix B:

Label 2: Maximum Ratings of C3M0075120K

Symbol	Parameter	Value	Unit	Test Conditions	Note
V_{DSmax}	Drain - Source Voltage	1200	V	V_{GS} = 0 V, I_D = 100 µA	
V_{GSmax}	Gate - Source Voltage (dynamic)	-8/+19	V	AC (f >1 Hz)	Note: 1
V_{GSop}	Gate - Source Voltage (static)	-4/+15	V	Static	Note: 2
I_D	Continuous Drain Current	30	A	V_{GS} = 15 V, T_C = 25˚C	Fig. 19
		19.7		V_{GS} = 15 V, T_C = 100˚C	
$I_{D(pulse)}$	Pulsed Drain Current	80	A	Pulse width t_P limited by T_{jmax}	Fig. 22
P_D	Power Dissipation	113.6	W	T_C=25˚C, T_J = 150 ˚C	Fig. 20
T_J , T_{stg}	Operating Junction and Storage Temperature	-55 to +150	˚C		
T_L	Solder Temperature	260	˚C	1.6mm (0.063") from case for 10s	

Appendix C:

Label 3: Operating Conditions of CGD15SG00D2

Operating Conditions					
Symbol	**Parameter**	**Min**	**Typical**	**Max**	**Unit**
Vs	Power Supply Voltage	11	12	12.5	V
V_{iH}	Input threshold voltage HIGH	10		15	V
V_{iL}	Input threshold voltage LOW	0		1	V
I_{o_pk}	Output peak current			±9*	A
P_{O_AVG}	Output power per gate		1		W
V_{isol}	Input to output isolation voltage		±1700		V
dv/dt	Rate of change of output to input voltage		50,000		V/µs
W	Weight		9		g
MTBF	Operating temperature		-35 to 85		°C
Top	Storage temperature		-40 to 85		°C