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Modeling and Nonlinear Control of dc–dc Converters for Microgrid Applications

Jorge A. Solsona *, Sebastian Gomez Jorge and Claudio A. Busada

Instituto de Investigaciones en Ingeniería Eléctrica (IIIE), Universidad Nacional del Sur (UNS)-CONICET and Dpto. Ing. Eléctrica y de Computadoras, UNS, Av. Alem 1253, Bahía Blanca 8000, Argentina
* Correspondence: jsolsona@uns.edu.ar

Abstract: This paper proposes a high-performance control strategy for dc–dc converters supplying combined loads (constant current/power, and/or linear loads). This strategy combines a feedback law with a feedforward compensation. The feedback law is based on full feedback linearization, which guarantees that zero dynamics are avoided. To design a single controller for the three basic converter topologies (i.e., buck, boost and buck–boost), a unified model for these converters is introduced. From the resulting combined control law, the specific control law for each type of converter can be obtained by setting three constant coefficient to 0 or 1. The feedforward compensation is based on the estimated values of the load obtained via a nonlinear observer. The main advantage of this unified approach is that it is implemented by using a single algorithm which can be executed in a dedicated hardware, for instance, a single integrated circuit, providing a unified solution for the control of the mentioned topologies. The good performance of the proposed scheme is verified through simulations and tested via experimental application cases, concluding that this is a good unified solution to control dc–dc converters used in microgrid applications.

Keywords: dc microgrids; dc–dc converters; nonlinear control

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1. Introduction

dc–dc converters have been in use for a long time. However, in the last two decades, their applications have increased significantly. For instance, these converters are used for integrating different kinds of power sources to the dc microgrid [1,2]. Other times, they are combined with dc–ac converters for obtaining ac power sources [3,4]. There are many reasons for the increase in the number of applications. Among others, the integration of generation based on renewable energies, transport applications, dc–dc micro and nanogrids and other smart grid applications can be mentioned [5–9]. It is remarkable that the converters in several of these applications feed constant power loads (CPLs) and that the number of these applications is increasing at an enormous rate [10]. However, many times, the same converter must supply other types of loads, such as linear loads and constant current loads (CCLs) and/or a combination of these (i.e., linear loads, CCLs and CPLs).

As mentioned, connection of energy sources and loads through electric power converters is used for building electric power distribution networks. Considering the new paradigm of electric power generation, transmission and distribution, called smart grid [11,12], it is relevant to remark that microgrids are emerging as an important tool to satisfy new standards set for environmental reasons. There are mainly two kinds of microgrids: ac microgrids and dc microgrids [13,14]. dc microgrids are implemented in several applications. Among others, it is possible to use dc microgrids in rural and residential electrification [15,16]. When dc microgrids are designed, dc–dc electronic power converters must be used for adjusting voltage levels between different stages of the dc microgrids. The power flow in microgrids can be controlled by using different control strategies [17–19]. The main component to control the power flow in a dc microgrid is the dc–dc electronic power converter [20].

Although there are different types of dc–dc converters, the main three basic topologies are the buck converter (step-down), the boost converter (step-up) and the buck–boost converter (step-down and step-up). From the point of view of the system, these converters present a bilinear state space model when they are loaded with a linear load. However, when they drive CPLs, the bilinear nature of the model is broken because a state variable appears dividing a disturbance input. In such cases, the load introduces a negative incremental resistive effect, causing instability in the system [21,22]. In recent years, many nonlinear control techniques have been applied to obtain high performance when supplying linear loads, CCLs or CPLs, separately. Most of these techniques are inherited from those used for bilinear descriptions. However, with the boom in dc–dc microgrids development [23–25], it is increasingly common for dc–dc converters to supply a combination of this type of loads.

In the bilinear models of dc–dc converters, it is well-known that the command signal switches between two values, 0 and 1, which originates switched bilinear networks. A common method to design the command signal is to use an average model [26] to compute a continuous control signal. This signal is then used to modulate the width of a signal pulsating between 0 and 1. Different methods can be found in the literature to design the continuous control signal. Sliding mode control [27–31], passivity-based strategies [32–34], predictive control [35–40], fuzzy controllers [41] and feedback linearization control (FL) [42] are widely used strategies. FL has been applied in both partial [43–46] and full mode [47].

An important difference between full FL and the other techniques is the elimination of zero dynamics. Using the average model of the system, full FL is obtained by selecting an output whose relative degree is equal to the order of the system. This output is called a flat output [48], and prevents zero dynamics. On the other techniques, the relative degree of the output is usually less than the order of the system. As a consequence, nonlinear zero dynamics is present in the closed-loop system, and the behavior of this dynamics must be studied in order to guarantee the stability of the closed-loop system.

Although, the three dc–dc converter basic topologies are different, it is possible to design a unified control strategy for all of them, choosing an adequate output to be fed back. The main advantage of a unified approach is that it can be used to design a single integrated circuit (IC) solution that can control any of these converters. To this end, this paper introduces a unique average model for all three converters, and uses a unique flat output for designing a nonlinear controller based on a full FL control strategy. If the load power is considered a disturbance input, and is not included in the design of the feedback controller, this controller will still be able to track load power changes. In this case, the disturbance tracking dynamics will be the same as the reference tracking dynamics. However, it is well-known that disturbance rejection performance can be improved by feedforwarding the load power instantaneous value. Since it is usually not convenient to measure the load power value, it is possible to estimate it using an observer built from the measurements of the state variables [49]. With this in mind, the unified control law proposed in this paper feedforwards estimates of the load power value and its time derivative, improving the transient performance when the load power changes. Additionally, the proposed controller is tested for different types of loads (CPL, CCL and resistive load), and it is found to be stable and have good performance in all cases. Both the proposed controller and observer are easy to tune. A procedure to obtain their feedback gains, based on the desired settling time, is described. Since both the controller and observer apply for the three topologies, after the gains are chosen, it is easy to obtain the control law for each converter. This is done here by setting three coefficients (named α, β and γ in this paper) to 0 or 1.

The rest of the paper is organized as follows. Section 2 describes the unified model of the three converters feeding a combined load. Section 3 shows the proposed full FL scheme with feedforward compensation. In Section 4, the load power observer is proposed, and its tuning criterion is described. Section 5 shows the proposed control scheme for the linearized system, and its tuning criterion. Simulation and experimental results that

validate the proposal are shown in Sections 6 and 7, respectively. Finally, in Section 8, conclusions are drawn.

2. Unified Average Model of the Converters

Figure 1 shows the topologies of the synchronous buck, boost and buck–boost converters. For all the converters, E is the input voltage, v_c the output voltage, i_l the inductor current and u the gate signal for the top switch. The combined load is modeled as a resistive load (R_o) in parallel with a CPL (P_o) (modeled through a current source) and a CCL (I_o).

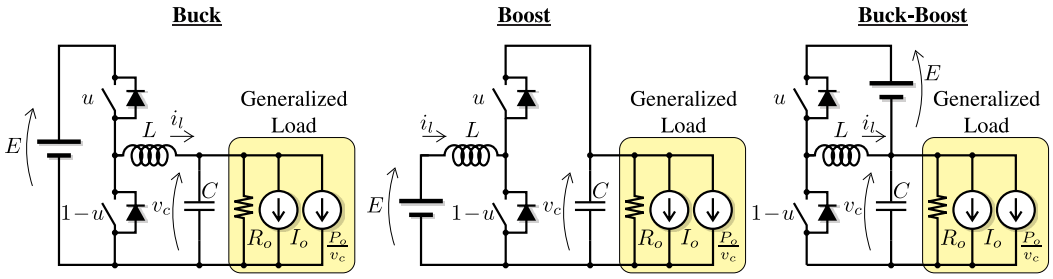

Figure 1. Topologies of the synchronous buck, boost and buck–boost converters.

In the continuous conduction mode, the continuous time average models of these converters are merged together into two differential equations using a set of constant coefficients α, β and γ:

$$L\dot{i}_l = -[\alpha+\gamma+(\beta-\gamma)u^*]v_c + [\beta+(\alpha+\gamma)u^*]E, \tag{1}$$

$$C\dot{v}_c = [\alpha+\gamma+(\beta-\gamma)u^*]i_l - \frac{P_L}{v_c}, \tag{2}$$

where P_L is a variable modeling the combined effect of a CPL, a CCL and resistive load:

$$P_L = P_o + I_o v_c + \frac{v_c^2}{R_o}.$$

From Equations (1) and (2), the well-known average models for the buck, boost and buck–boost can be obtained, setting $[\alpha\ \beta\ \gamma] = [1\ 0\ 0]$, $[\alpha\ \beta\ \gamma] = [0\ 1\ 0]$ and $[\alpha\ \beta\ \gamma] = [0\ 0\ 1]$, respectively. Here, u^* is the control action, and it is a continuous (derivable) signal that can take any value between 0 and 1. This signal represents the average value, over one switching cycle, of gate signal u of Figure 1. For the purpose of load estimation, it is assumed that P_L can change its value following a ramp profile (constant slope):

$$\dot{P}_L = m, \tag{3}$$

$$\dot{m} = 0. \tag{4}$$

Note that slope m can be equal to zero. Using Equations (1)–(4), in the following section, a unified full FL scheme is proposed.

3. Proposed Full FL Scheme

A full input–output FL is proposed in this section. By choosing a flat output allows to avoid closed-loop zero dynamics. This implies, for the second-order system (1) and (2), finding an output with relative degree two (the control action u^* only appears after differentiating the output twice with respect to time). The flat output proposed here is

$$y = \frac{1}{2}Li_l^2(\beta+\gamma) + \frac{1}{2}C(v_c+E\gamma)^2. \tag{5}$$

To show that this output is indeed flat, we differentiate this output with respect to time, assuming input voltage E is constant:

$$\dot{y} = L\dot{i}_l i_l(\beta+\gamma)+C\dot{v}_c(v_c+E\gamma). \tag{6}$$

Replacing Equations (1) and (2) in (6) results in

$$\dot{y} = \alpha i_l v_c+(\beta+\gamma)Ei_l-\gamma\frac{EP_L}{v_c}-P_L. \tag{7}$$

It is clear that control action u^* is not present in $\dot{y}$. Differentiating with respect to time once more, assuming the load power as defined in Equations (3) and (4), the second time derivative of y results in

$$\ddot{y} = \frac{\alpha_1}{CLv_c^3}+\frac{\alpha_2}{CLv_c^2}u^*, \tag{8}$$

where

$$\begin{aligned}\alpha_1 \quad &= -\alpha Cv_c^5-\gamma CEv_c^4+(\beta CE^2+\alpha Li_l^2-CLm)v_c^3- \\ &(\alpha LP_L i_l+\gamma CELm)v_c^2+(\gamma ELP_L i_l)v_c-\gamma ELP_L^2,\end{aligned} \tag{9}$$

$$\alpha_2 = (\alpha-\beta+\gamma)CEv_c^3+(\gamma CE^2)v_c^2-\gamma ELP_L i_l. \tag{10}$$

Since u^* is present in Equation (8), we can see that the relative degree of output y is the same as the order of system (1) and (2). Therefore, y is a flat output.

From Equations (5)–(7), it is now possible to define a second-order linear system. The states of this linear system, defined as z_1 and z_2, are

$$z_1 = y = \frac{1}{2}Li_l^2(\beta+\gamma)+\frac{1}{2}C(v_c+E\gamma)^2, \tag{11}$$

$$z_2 = \dot{y} = \alpha i_l v_c+(\beta+\gamma)Ei_l-\gamma\frac{EP_L}{v_c}-P_L. \tag{12}$$

Then, the dynamics of z_1 and z_2 result

$$\dot{z}_1 = \dot{y} = z_2, \tag{13}$$

$$\dot{z}_2 = \ddot{y} = \frac{\alpha_1}{CLv_c^3}+\frac{\alpha_2}{CLv_c^2}u^* = \omega, \tag{14}$$

where we used Equation (8), and ω is the input (control action) of the linear system since it contains control action u^*. It is now possible to design a controller for (13) and (14) applying linear control techniques. The output of this linear controller is signal ω. From ω, the actual control action u^*, which will be applied to the real system (1) and (2), must be computed. From Equation (8), u^* results in

$$u^* = \frac{CLv_c^3\omega-\alpha_1}{\alpha_2 v_c}. \tag{15}$$

Table 1 summarizes Equation (15) for the different converter topologies. It can be seen that the results for the buck converter match those shown in [47] when the converter feeds a CPL.

Table 1. Computation of control action u^* from ω for the different converter topologies.

Buck	$u^* = \frac{Cv_c^3+(CLm-Li_l^2+CL\omega)v_c+LP_L i_l}{CEv_c^2}$
Boost	$u^* = -\frac{Lm-E^2+L\omega}{Ev_c}$
Buck–Boost	$u^* = \frac{CEv_c^4+CL(m+\omega)v_c^3+CELmv_c^2-ELP_L i_l v_c+ELP_L^2}{CEv_c^4+CE^2v_c^3-ELP_L i_l v_c}$

From Equations (11) and (12) it is clear that to perform the full FL, knowledge of v_c, i_l, P_L and m is required. Assuming the first two variables are measured and parameters E, L and C are known, in the next section, an observer is proposed to estimate the combined load power P_L and its slope m.

4. Combined Load Power Observer

Considering that the combined load power is modeled by Equations (3) and (4), either a reduced-order observer [47] or a full-order observer can be designed. The full-order observer is better when the measured signals are noisy since it provides additional filtering. The compromise is a slightly slower response since the full-order observer has more states. For a given sampling frequency, the effect of the noise on the quality of the observer estimations is more significant as the speed of the observer is increased. After some testing, it was concluded that, for the desired controller and observer speeds and the available hardware, it is better to implement a full-order observer.

To implement the load power observer from the measured signals, first consider the energy in the capacitor:

$$E_c = \frac{1}{2} C v_c^2. \tag{16}$$

Differentiating Equation (16) with respect to time and using Equation (2), the energy variation results in

$$\dot{E}_c = [\alpha+\gamma+(\beta-\gamma)u^*] i_l v_c - P_L. \tag{17}$$

From Equations (3), (4) and (17), the following full-order observer is proposed:

$$\dot{\hat{E}}_c = [\alpha+\gamma+(\beta-\gamma)u^*] i_l v_c - \hat{P}_L + K_{o1}(E_c-\hat{E}_c), \tag{18}$$

$$\dot{\hat{P}}_L = \hat{m} + K_{o2}(E_c-\hat{E}_c), \tag{19}$$

$$\dot{\hat{m}} = K_{o3}(E_c-\hat{E}_c), \tag{20}$$

where K_{o1}, K_{o2} and K_{o3} are constant gains that define the dynamics of the observer.

Defining the error signals $e_{E_c} = E_c - \hat{E}_c$, $e_{P_L} = P_L - \hat{P}_L$ and $e_m = m - \hat{m}$, the observer error dynamics result in

$$\begin{bmatrix} \dot{e}_{E_c} \\ \dot{e}_{P_L} \\ \dot{e}_m \end{bmatrix} = \underbrace{\begin{bmatrix} -K_{o1} & -1 & 0 \\ -K_{o2} & 0 & 1 \\ -K_{o3} & 0 & 0 \end{bmatrix}}_{A_o} \begin{bmatrix} e_{E_c} \\ e_{P_L} \\ e_m \end{bmatrix}. \tag{21}$$

Tuning Criteria

The poles of the observer are the eigenvalues of A_o, and can be placed at any desired locations, as can be seen in computing the characteristic polynomial of A_o. This polynomial is obtained computing the determinant of $sI - A_o$:

$$\lambda_o = s^3 + K_{o1}s^2 - K_{o2}s - K_{o1}, \tag{22}$$

where s is the Laplace transform variable and I is the 3×3 identity matrix. A criterion for choosing these pole locations is to set two complex conjugate poles using the classical control second-order system and setting the third pole equal to the real part of the other poles (or a multiple p_o of the real part for faster convergence of this pole). This allows to select a damping ζ_o and a settling time T_{seto} for the response of the observer. Even though the resulting damping will not be the desired one due to the zeros of the system, the settling time will be very close to the desired one [50]. By assuming $\zeta_o = 1$ and T_{seto}, the desired

settling time to 1% of the final value, the natural resonance frequency of the second-order system is

$$\omega_{no} = \frac{4.6}{T_{seto}}. \tag{23}$$

Then, the desired closed-loop characteristic polynomial results in

$$\begin{aligned} \lambda_o^* &= (s^2+2\omega_{no}s+\omega_{no}^2)(s+p_o\omega_n), \\ &= s^3+(p_o+2)\omega_{no}s^2+(1+2p_o)\omega_{no}^2 s+p_o\omega_{no}^3. \end{aligned} \tag{24}$$

Equating Equation (22) with Equation (24), the gains of the observer result in

$$K_{o1} = (p_o + 2)\omega_{no}, \tag{25}$$

$$K_{o2} = -(1 + 2p_o)\omega_{no}^2, \tag{26}$$

$$K_{o3} = -p_o\omega_{no}^3, \tag{27}$$

where $p_o \geq 1$ is how many times faster the third pole is than the complex conjugate poles. Using observer (18)–(20), variables z_1 and z_2 of the linearized system can be computed through Equations (11) and (12), and a linear controller can be implemented. This controller is described in the following section.

5. Proposed Controller for the Linearized System

In this section, a linear controller for systems (13) and (14) is proposed. This controller will be implemented using full state feedback, which allows to place the closed loop poles of the system at any desired locations.

First, the reference signals z_1^r and z_2^r must be defined. The control objective is to keep output voltage v_c at a constant reference level v_c^r. From Equation (11), since i_l is required for both the boost and buck–boost converters, it is clear that a current reference i_l^r must be found. To find this reference, notice that in steady state $\dot{i}_l = \dot{v}_c = 0$, and assuming the references are reached, $v_c = v_c^r$ and $i_l = i_l^r$. Using these assumptions in Equations (1) and (2), and the fact that the reference is only required for the boost and buck–boost converters, the current reference results in

$$i_l^r = \frac{P_L}{E}(\beta + \gamma\frac{E + v_c^r}{v_c^r}). \tag{28}$$

Now the references for the controller are defined as follows:

$$z_1^r = \frac{1}{2}L(i_l^r)^2(\beta+\gamma)+\frac{1}{2}C(v_c^r+E\gamma)^2, \tag{29}$$

$$z_2^r = \dot{z}_1^r = 0. \tag{30}$$

To improve the performance in the presence of parametric uncertainties, and achieve zero steady-state error when following a constant reference z_1^r, an integrator is added to the linear system. Applying full-state feedback, the control action results in

$$\omega = -K_1(z_1 - z_1^r) - K_2z_2 - K_3z_3, \tag{31}$$

where z_3 is the integrator state, with the following differential equation:

$$\dot{z}_3 = z_1 - z_1^r. \tag{32}$$

By combining Equations (13) and (14) with Equations (31) and (32), the closed-loop system dynamics result in

$$\begin{bmatrix} \dot{z}_1 \\ \dot{z}_2 \\ \dot{z}_3 \end{bmatrix} = \underbrace{\begin{bmatrix} 0 & 1 & 0 \\ -K_1 & -K_2 & -K_3 \\ 1 & 0 & 0 \end{bmatrix}}_{A} \begin{bmatrix} z_1 \\ z_2 \\ z_3 \end{bmatrix} + \begin{bmatrix} 0 \\ K_1 \\ -1 \end{bmatrix} z_1^r \tag{33}$$

5.1. Tuning Criteria

The poles of the closed loop controller are the eigenvalues of A, and can be placed at any desired locations, as can be seen by computing the characteristic polynomial of A:

$$\lambda_c = s^3 + K_2 s^2 + K_1 s + K_3. \tag{34}$$

We will use the same criteria as for the observer (a second-order classical control system plus a real pole p_c times the real part of the complex poles). Assuming the damping is $\zeta_c = 1$, and the desired settling time to 1% of the final value, T_{setc}, is given, the natural resonance frequency of the second-order system is

$$\omega_{nc} = \frac{4.6}{T_{setc}}. \tag{35}$$

Then, the desired closed loop characteristic polynomial results in

$$\begin{aligned} \lambda_c^* &= (s^2 + 2\omega_{nc}s + \omega_{nc}^2)(s + p_c\omega_c), \\ &= s^3 + (p_c+2)\omega_{nc}s^2 + (1+2p_c)\omega_{nc}^2 s + p_c\omega_{nc}^3. \end{aligned} \tag{36}$$

Equating Equation (34) with Equation (36), the gains of the controller result in

$$K_1 = (2p_c + 1)\omega_{nc}^2, \tag{37}$$

$$K_2 = (2 + p_c)\omega_{nc}, \tag{38}$$

$$K_3 = p_c\omega_{nc}^3, \tag{39}$$

where $p_c \geq 1$ is how many times faster the third pole is than the complex conjugate poles.

5.2. Control Loop Summary

The implementation of the control loop is shown schematically in Figure 2. It can be summarized as follows:

- From measured signals v_c and i_l, and the observed load power $\hat{P}_L$ compute the change of variables z_1 and z_2 through Equations (11) and (12), respectively.
- If necessary, compute reference i_l^r through Equation (28) and then compute reference z_1^r through Equation (29).
- Compute control action ω through Equation (31).
- Using measured signals v_c and i_l, the observed load power $\hat{P}_L$, its slope $\hat{m}$, and control action ω, compute control action u^* through Equation (15). This signal is sent to the pulse width modulator (PWM) to generate the gate trigger signals for the switches (u and $1-u$ in Figure 1).
- From measured signal v_c, compute the capacitor energy E_c through Equation (16). Then, using E_c and measured signals i_l and v_c, update the observed load power $\hat{P}_L$ and its slope $\hat{m}$ through Equations (18)–(20).
- Update the controller integrator state z_3 through Equation (32).

Note that the three different dc–dc topologies can be controlled using the same IC. It is enough to design only one IC, where a three-bit digital word can be input. These bits contain the values of α, β and γ set to 0 or 1 depending on the dc–dc topology. The IC

complexity is incremented a bit, but it allows to control three different topologies. In addition, it must be noted that the control strategy combines a feedback law based on full input–output FL and a feedforward compensator. This feedforward compensator improves the transient response in presence of load variations.

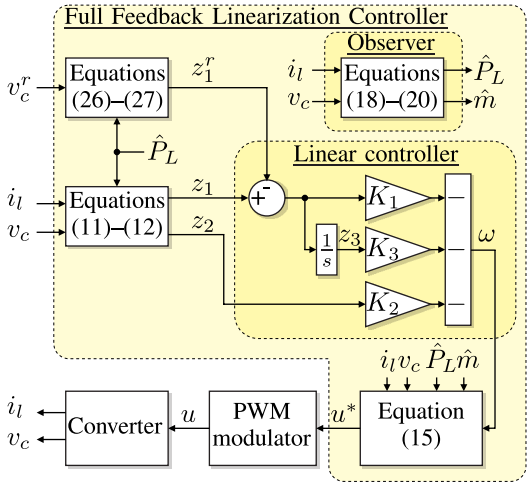

Figure 2. Controller scheme.

5.3. Comments about Other Strategies

The control of dc–dc converters has been explored by many researchers and there is an enormous number of works in the literature on this subject. Among others, the cascade double-loop control with voltage and current feedback and variants of this control are proposed in recent works. However, using this control has some drawbacks. On the one hand, in the case of boosting, the feedback of the capacitor voltage causes the transfer function obtained by using Taylor's linearized technique to have relative degree equal to one. This means that this transfer function presents two poles and a non-minimum phase zero [51]. This zero limits the maximum gain of the external loop since making this gain too large leads to instability. On the other hand, when the converter supplies constant power loads [10,52], the small-signal behavior is such that a positive feedback effect can occur, causing that, for fixed values of the controller parameters, the system becomes unstable in the presence of large and rapid load variations. For this reason, it is not possible to track abruptly changing references and widely varying loads, making these controllers relatively inefficient in applications where large state excursions are necessary.

Mainly for these reasons, several researchers have focused on developing non-linear control strategies to obtain better performance when large excursions of the states occur. Indeed, depending on the output chosen and the way in which the load is treated, the mentioned drawbacks can be mitigated or completely eliminated.

The strategy presented in this paper is especially useful to fully overcome these drawbacks. This is because a full feedback linearization non-linear control strategy with a flat output is implemented. This output presents a relative degree equal to two, matching the system's order and avoiding the appearance of zero dynamics [53]. Regarding constant power loads, the problem is addressed by introducing a feedforward compensation of the estimated load power. Thus, the strategy presented allows overcoming both drawbacks. In addition, its unified formulation allows the strategy to be applied to any of the basic topologies of dc–dc converters easily.

6. Simulation Results

This section shows the simulation results of the proposed control scheme. The three converters were simulated using the parameters described in Table 2. The controller was designed with a settling time $T_{setc} = 10$ ms and $p_c = 10$ [see Equations (37)–(39) for the gain computation], and the observer was designed with $T_{seto} = 1$ ms and $p_o = 10$

[see Equations (25)–(27) for the gain computation]. For the buck converter, the output voltage reference was $v_c^r = 100$ V, for the boost converter $v_c^r = 300$ V, and for the buck–boost converter $v_c^r = 200$ V.

Table 2. Simulation parameters.

Parameter	Value	Description
L	3.78 mH	Filter Inductor
C	470 µF	Filter Capacitor
K_1, K_2, K_3	4.4436×10^6, 5520, 973.36×10^6	Controller Gains
K_{o1}, K_{o2}, K_{o3}	$55, 200, -444.36 \times 10^6$, $-973,360 \times 10^6$	Observer Gains
E	200 V	Input Voltage

Figure 3 shows the simulation results to load variations for the buck converter, Figure 4 for the boost, and Figure 5 for the buck–boost converter. For these simulations, all converters start in the steady-state with no load. At $t = 10$ ms, a resistive load that drains 1 kW is connected and removed at $t = 50$ ms. As can be seen in all figures, this load produces the largest dc link voltage transient and observer error, which happens due to the sudden connection/disconnection (step load). At $t = 80$ ms, the power of the CPL connected to the dc link is increased from 0 to 1 kW within 5 ms following a soft profile, then, at $t = 115$ ms the load is decreased to 0 W following the same profile. As the figures show, the dc link transient and observer error are small for all the converters. Finally, at $t = 150$ ms, the CCL connected to the dc link has its current increased so that it takes 1 kW in steady state. This is done within 5 ms following a soft profile, similar to that of the CPL. Then, at $t = 185$ ms, the current is decreased to zero, tracking the same profile. In all cases, both the dc link voltage transient and observer error are also small.

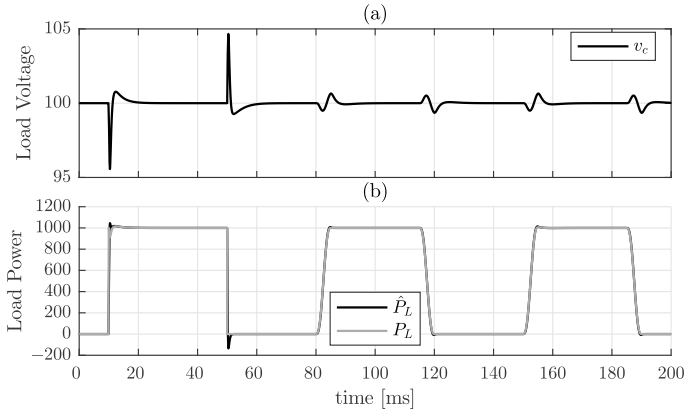

Figure 3. Simulation results for the buck converter with 1 kW load step changes. (**a**) dc link voltage. (**b**) Load power vs. observed load power.

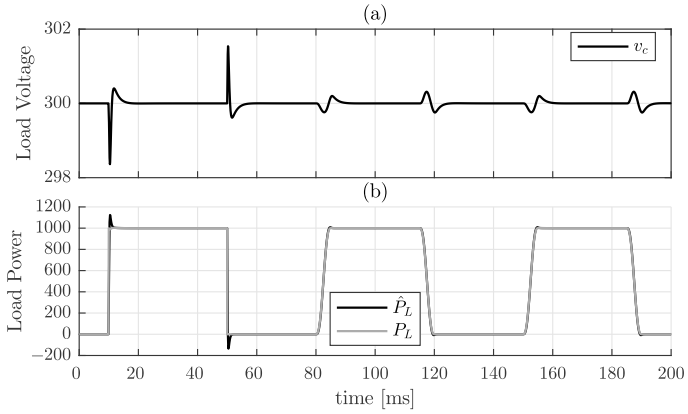

Figure 4. Simulation results for the boost converter with 1 kW load step changes. (**a**) dc link voltage. (**b**) Load power vs. observed load power.

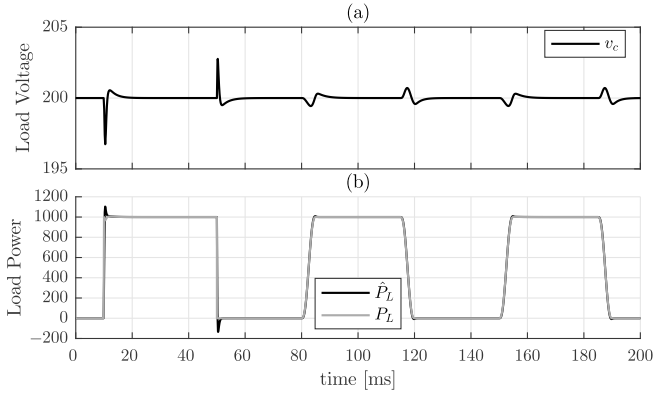

Figure 5. Simulation results for the buck–boost converter with 1 kW load step changes. (**a**) dc link voltage. (**b**) Load power vs. observed load power.

Although the input voltage variation is not considered when modeling the system, Figures 6–8 show the simulation results when the input voltage is varied, for the buck, boost and buck–boost converters, respectively. For these simulations, all converters start in steady-state with no load. At $t = 20$ ms, the input voltage is increased by $+20\%$ and then decreased to its nominal value at $t = 60$ ms. Then, at $t = 100$ ms, the load is increased to 1 kW (using a CPL). After this, at $t = 120$ ms, the input voltage is once again increased by $+20\%$ and then decreased to its nominal value at $t = 160$ ms. As can be seen in all figures, the effect of this sudden input voltage variation on the output voltage is very small, and is canceled by the controller as a disturbance within the designed settling time. This shows that the proposal is also robust to input voltage variations.

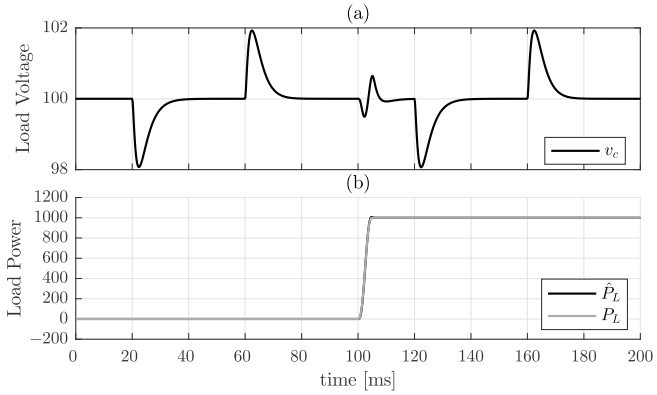

Figure 6. Simulation results for the buck converter with $+20\%$ input voltage changes. (**a**) dc link voltage. (**b**) Load power vs. observed load power.

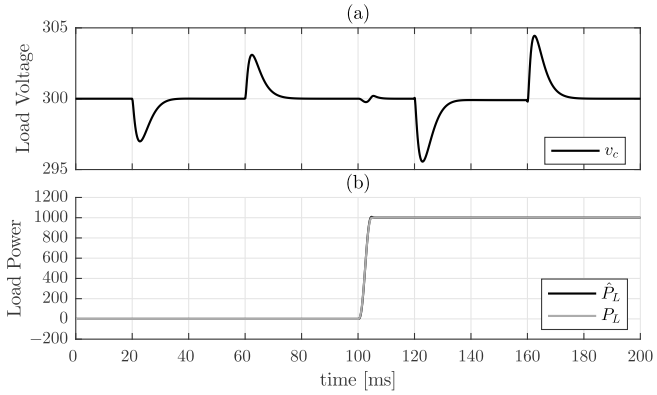

Figure 7. Simulation results for the boost converter with +20% input voltage changes. (**a**) dc link voltage. (**b**) Load power vs. observed load power.

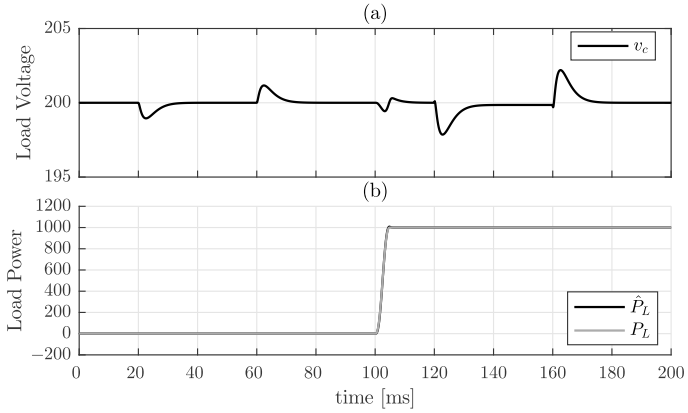

Figure 8. Simulation results for the buck–boost converter with +20% input voltage changes. (**a**) dc link voltage. (**b**) Load power vs. observed load power.

To show the dynamics of the output voltage to voltage reference changes, the previous simulations were repeated for the three converters, with no load and with nominal resistive load. These results are shown in Figure 9. Figure 9a,c,e, show the output voltage of the buck, boost and buck–boost converters, respectively, when the reference voltage is increased 20% from its nominal value, and the converters are operating with no load. As can be seen in these figures, the settling time for all converters is 10 ms, as was expected from the design conditions. Figure 9b,d,f show the same simulations but in these cases, the converters are loaded with a resistive load. In all cases, the resistive load value is selected so that it drains 1 kW after the voltage reference step. As can be seen, the settling time in this case is also 10 ms for all the converters. As can be seen, the responses to reference changes with or without load are very similar. This is expected, as the load is considered as part of the linearization transformation, and the load value is correctly estimated by the observer.

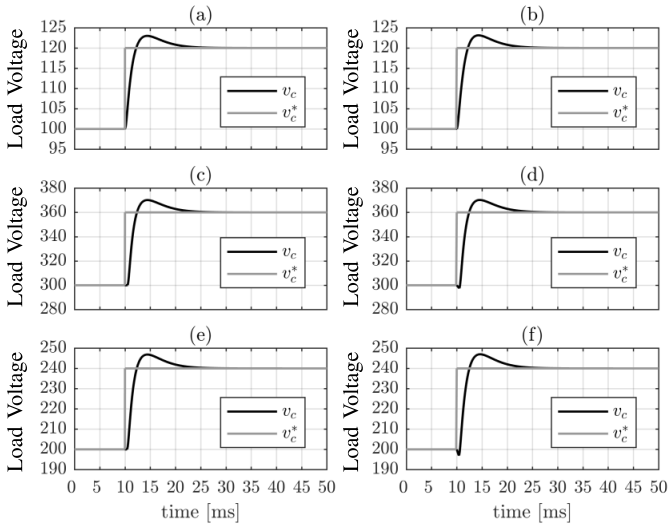

Figure 9. Simulation results: voltage reference 20% step. (**a**) Buck with no load. (**b**) Buck with resistive load. (**c**) Boost with no load. (**d**) Boost with resistive load. (**e**) Buck–boost with no load. (**f**) Buck–boost with resistive load.

7. Experimental Results: Application Cases

To validate the proposal three application cases are shown in this section.

7.1. Boost Converter with CCL

The proposed controller for a boost converter was implemented in a TMS320F28335 DSP, using a sampling time of $T = 50$ µs. The converter under test was built using IGBTs IRG4PH50UD, and the inductance and capacitance of this converter were the same as in the simulations ($L = 3.78$ mH, $C = 470$ µF) and so are the parameters of the controller. The switching frequency was 20 kHz, and the output reference was set to $v_c^r = 300$ V. The input voltage was provided by a 600 V × 25 A power dc voltage source, and was set to $E = 200$ V. As CCL a SLH-500-6-1800 AC/DC electronic load was used. A picture of the experimental setup is shown in Figure 10a. Here, only a leg of a three phase converter is used to implement the boost converter (block "Conv."). The block labeled "measure" is the measurement and level adaptation board, block "DSP" is the interface board connected to the DSP, and block "filter" is the boost inductor. In this configuration, the rated power of the converter is 2 kW.

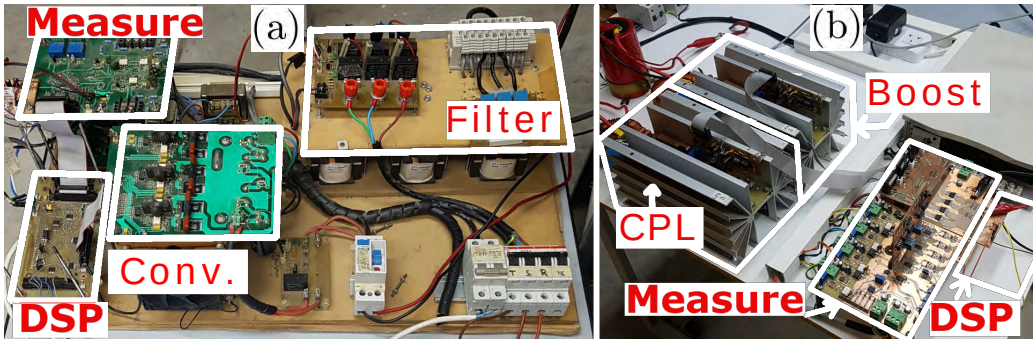

Figure 10. Experimental setup. (**a**) Converter for cases in Sections 7.1 and 7.3. (**b**) Converter for case in Section 7.2.

Figure 11a shows output voltage v_c and Figure 11b load power P_L. This load power is obtained by measuring the load current and multiplying it with the measured voltage using the MATH function of the oscilloscope. The experiment starts with the CCL set to zero, and the output voltage at its reference value v_c^r. At $t = 20$ ms, the CCL current is increased

to 3.3 A, so it drains 1 kW from the converter. As can be seen, the output voltage converges to its reference value within 2 ms with a transient similar to that in the simulation results.

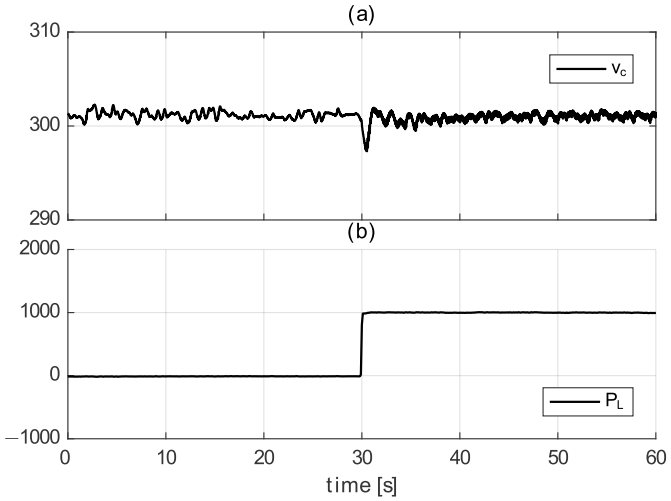

Figure 11. Experimental results: boost converter feeding a CCL. (**a**) dc link voltage v_c. (**b**) Load power P_L.

To show the importance of the feedforward term for improving the performance to load variations, Figure 12 shows the same experimental results as Figure 11, but in this case, the observed power is set to $\hat{P}_L = \hat{m} = 0$. As can be seen, when the current step is applied to the CCL, the transient is longer (approximately 10 ms) significantly longer than the transient of Figure 11.

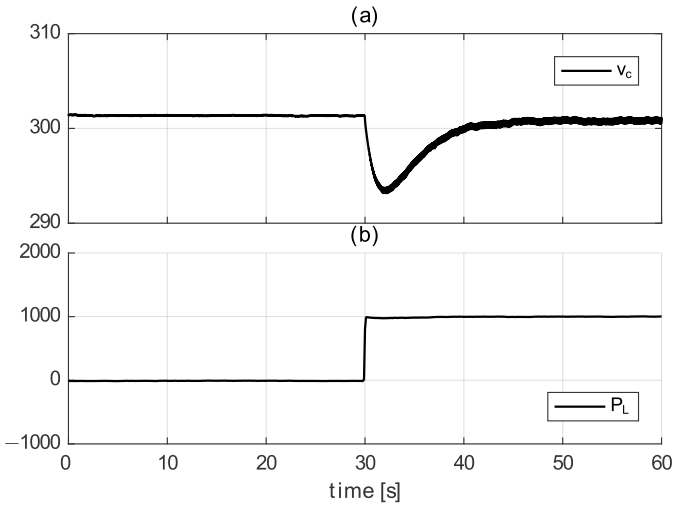

Figure 12. Experimental results: boost converter feeding a CCL without feedforward. (**a**) dc link voltage v_c. (**b**) Load power P_L.

7.2. Boost Converter with Resistive Load and CPL

For another application, the proposed controller for a boost converter was also implemented in a TMS320F28335 DSP, using a sampling time and PWM period of 50 µs. This converter uses IRFP4710 Mosfet switches. The parameters of the converter are shown in Table 3. The output voltage reference to $v_c^r = 48$ V. In this test, a CPL and a resistive load are connected to the output. The CPL is a buck converter built with the same Mosfet switches, feeding a 5.2 Ω resistive load. The resistive load, which is connected at a specified time, is 14.6 Ω. For this application, the controller was designed with a settling time $T_{setc} = 10$ ms and the observer with $T_{seto} = 2.5$ ms. A picture of the experimental setup is shown in

Figure 10b. In this figure the blocks labeled "CPL" and "boost" are identical legs, where one is configured as a boost converter and the other as a buck feeding a resistive load. The block labeled "measure" is the measurement and level adaptation board, block "DSP" is the interface board connected to the DSP. The filters of each converter are toroidal inductors which can be seen behind the heatsinks of each converter. In this configuration, the rated power of the converter is 700 W.

Table 3. Boost with resistive load and CPL parameters.

Parameter	Value	Description
L	800 µH	Filter Inductor
C	220 µF	Filter Capacitor
E	24 V	Input Voltage

The results of this test are shown in Figure 13. The converter starts with no load and the output voltage at its reference level v_c^r. At $t = 10$ ms, the resistive load is connected to the output, which results in a 10 ms transient, as expected. At approximately $t = 30$ ms the CPL power is increased from 0 to 150 W within 5 ms, following a soft profile, which results once again in a 10 ms transient of the output voltage. As shown in these results, the converter behaves as expected.

7.3. Buck Converter with CCL

For this application, a buck converter was implemented using IRG4PH50UD IGBTs, with the parameters of Table 4. The controller was also implemented in DSP with a sampling time and PWM period of 50 µs. The reference voltage was set to $v_c^r = 100$ V. The converter was loaded with a CCL (the one used in Section 7.1). In this application, the controller was designed with a settling time $T_{setc} = 10$ ms and the observer with $T_{seto} = 4$ ms. A picture of the experimental setup is shown in Figure 10a. In this case, a leg of the three-phase converter is used to implement the buck converter. In this configuration, the rated power of the converter is 1 kW.

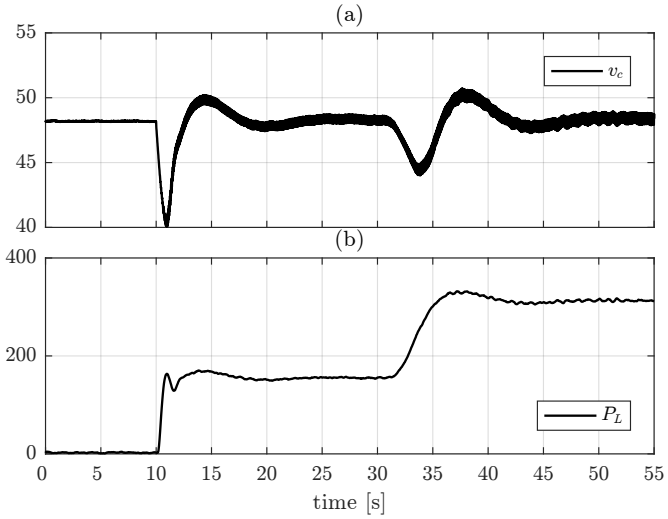

Figure 13. Experimental results: boost converter feeding a CPL and a resistive load. (**a**) dc link voltage v_c. (**b**) Load power P_L.

Table 4. Buck with CCL parameters.

Parameter	Value	Description
L	3.78 mH	Filter Inductor
C	100 μF	Filter Capacitor
E	200 V	Input Voltage

The experimental results are shown in Figure 14. The converter starts with a small load current (draining 67 W), and the output voltage at its reference value v_c^r. At $t = 20$ ms, the load current is increased to 2 A, increasing the load power to 200 W, and at $t = 73$ ms, it is decreased to its previous value. As can be seen, the output voltage transients are similar to those seen in the simulation results.

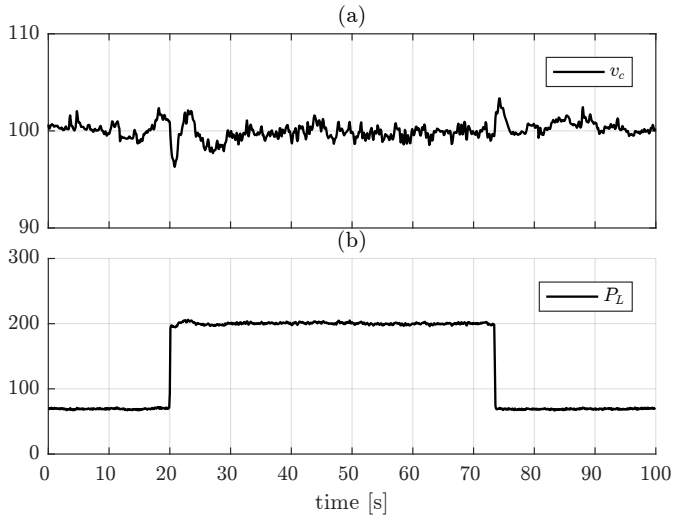

Figure 14. Experimental results: buck converter feeding a CCL. (**a**) dc link voltage v_c. (**b**) Load power P_L.

8. Conclusions

This paper introduces a control strategy to control the output voltage in dc–dc converters supplying combined loads. The proposed strategy combines full FL and feedforward compensation. Full FL is achieved by choosing a flat output, which eliminates zero dynamics. The unified proposal can be used in the three basic dc–dc converter topologies—buck, boost and buck–boost. In order to select the controller for a given topology, it is enough to set the values of three coefficients (α, β and γ) to 0 or 1, in concordance with the type of converter whose output voltage is to be controlled. The proposed controller presents high-performance in the presence of changes in the load value, even for combined linear and nonlinear loads. The proposal was validated through the use of both simulation and experimental results. This algorithm, based on full feedback linearization, is a unified solution for the control of three of the most popular dc–dc converters used in microgrid applications, and can be implemented in a single integrated circuit, allowing a convenient solution for the control of these converters.

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