Electrical Correlation of Double-Diffused Metal–Oxide–Semiconductor Transistors Exposed to Gamma Photons, Protons, and Hot Carriers

Felix Palumbo, *Member, IEEE*, Adrian Faigon, and Giuseppe Curro

***Abstract*—Double-diffused metal–oxide–semiconductor n-channel power transistor devices were subjected to a high electric-field stress, gamma photons (^{60}Co), and 10-MeV proton radiation, and were comparatively analyzed. The direct-current current–voltage and high-frequency capacitance–voltage techniques were used to characterize the two different regions under the gate oxide in this kind of devices. The Si–SiO_2 interfaces at the channel side and at the drain side are characterized after thermal annealing. The correlation of the interface states with the trapped charge is a good quantitative tool to compare the effects from different degradation mechanisms. It is shown that, under given conditions, each kind of stress exhibits its own signature in the interface states versus the oxide charge plot.**

***Index Terms*—metal–oxide–semiconductor (MOS), radiation effects, reliability.**

I. Introduction

THE IDENTIFICATION of a relationship between degradation due to tunnel charge injection across the oxide and irradiation of metal–oxide–semiconductor (MOS) devices is an important challenge for testing procedures in the microelectronic industry [1]–[3]. Since the determination of degradation effects by radiation at low dose rates to reproduce the space environment [3], [4] require a long time to be carried out, many accelerated tests are being investigated and implemented in order to ascertain the component reliability [1]–[3].

Usually, the efforts in correlating semiconductor device damages include the calculation of nonionizing and ionizing energy-loss rates from first principles based on differential cross sections and interaction kinematics, but they ignore the processes by which stable electrically active defects are formed. In addition, it has been shown that using fundamental information to derive more practical information is a very difficult task at best. The final configuration of electrically active defects formed by radiation has been a topic of many research works, but it is still not well understood [5]–[8].

Among all devices that are currently tested, some works have been focused on double-diffused MOS field-effect transistors (DMOSFETs) because aerospace satellites require the use of high-frequency switches in power supplies. This kind of device is characterized by the presence of two different regions under the gate oxide, an interface in the channel region, and another interface at the drain region. Most authors agree that both regions should be separately examined for a correct interpretation; however, there is no uniformity in the obtained results due to differences in the experimental techniques and procedures [9]–[13]. A recent work has analyzed both regions using X-rays and high fields, showing differences in the later condition [14]. The study of the DMOSFET reliability should contribute to the more general aim of understanding the wear-out data and dielectric breakdown (BD) phenomena in SiO_2.

In this paper, we present a detailed analysis of the degradation of the DMOSFET using different degradation mechanisms, i.e., constant-voltage pulses, gamma photons (^{60}Co), and 10-MeV protons. The interactions involved in the MOS stack under those radiation sources are quite different, making a physical-based correlation between them difficult. To overcome this situation, a semiempirical approach is proposed based on the comparison of the $Si-SiO_2$ interface states as a function of trapped charge, independently of its origin.

The experimental methodology is suitable to generate a gradual change in the electric characteristics reaching the maximum shift according to design rules. Charge trapping and interface-state generation on both interfaces have been studied using direct-current current–voltage (DCIV), subthreshold $I-V$, and $C-V$ techniques. The yield of oxide charge in the channel and drain regions is also studied after annealing to understand long-term effects.

The presented results should help in improving the understanding of the wearing-out data under different degradation mechanisms since each mechanism used in this paper exhibits its own signature in the interface states versus the oxide charge. From an applicative point of view, the results could contribute to the desirable target of developing a method for predicting

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F. Palumbo is with the Consejo Nacional de Investigaciones Científicas y Técnicas, C1033AAJ Buenos Aires, Argentina, and also with the Comision Nacional de Energia Atomica, 1650 Buenos Aires, Argentina (e-mail: palumbo@cnea.gov.ar).

A. Faigon is with the Consejo Nacional de Investigaciones Científicas y Técnicas, C1033AAJ Buenos Aires, Argentina, and also with the Engineering Faculty, University of Buenos Aires, C1063ACV Buenos Aires, Argentina (e-mail: afaigon@fi.uba.ar).

G. Curro is with the STMicroelectronics, 95121 Catania, Italy (e-mail: giuseppe.curro@st.com).

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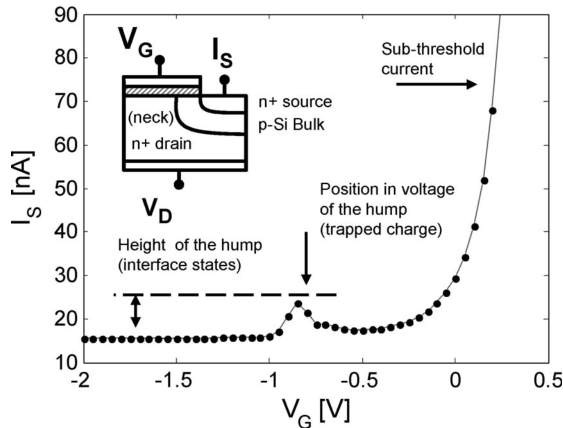

Fig. 1. Typical DCIV curve for an unstressed DMOS. The height of the hump is correlated with the density of interface states in the neck region, whereas the position in the voltage of the hump is correlated with the trapped charge in the gate oxide. (Inset) Simplified cross section of the device.

radiation effects in MOS devices through responses to the Fowler–Nordheim (FN) injections.

II. Experimental Details

The samples were n-channel power DMOS devices manufactured by STMicroelectronics, with different gate oxide thicknesses (SiO_2) of 23.8, 24.7, 31.3, 33.3, and 34.5 nm (see inset Fig. 1). Different sets of samples had been subjected to constant-voltage stresses (CVSs), gamma-irradiation stresses (GRS), and 10-MeV proton-irradiation stresses (PIS). For the high-field stress experiment, a constant voltage was applied to the gate, with source and drain terminals connected to the ground. In all cases, the gate voltage corresponded to an electric field of 7.5 MV/cm in the gate oxide layer, and the current was monitored during the stress. The gamma irradiation processes were from a ^{60}Co source with a dose rate of 0.9050 Gy/min, at the Comision Nacional de Energia Atomica (CNEA). Irradiation processes were performed up to an accumulated dose of 4.3 KGy.

The proton irradiation was performed at the TANDAR accelerator (TANDEM Van de Graaff Argentino) also at the CNEA, with a uniform proton beam of 10 MeV inside a vacuum chamber at 3×10^{10} ions/(cm$^2 \cdot$ min). [15]. The gamma and proton irradiation processes were performed in the darkness at room temperature, and the gate electrode was biased at +10 V.

Along the degradation process (the CVS, the GRS, or the PIS), the stress was periodically interrupted to perform *in situ* the following measurements: the DCIV technique [13], [14], [16], the high-frequency capacitance–voltage ($C-V$) technique [14], [17], and the subthreshold $I-V$ curves [17].

In all cases, the electrical characterization was shortly performed after the degradation pulse (radiation or high fields). Additional characterizations were performed after annealing at 100 °C to reveal long-term effects.

The consecutive steps of degradation were planned to generate a gradual change in the electric characteristics for the best possible resolution in the degradation rate, and totalizing a significant shift of the channel current was planned to predict the long-term reliability.

A. DCIV

The DCIV measurement is an accepted technique that reveals both the trapped charge in the gate oxide and the density of generation–recombination traps in the drain region at the $Si-SiO_2$ interface in power DMOSFET devices [13], [14], [16].

A typical result for unstressed devices is shown in Fig. 1, where the current was measured at the source contact that was forward biased with $V_D = -0.3$ V. The current peak in the measurement is proportional to the interface-trap concentration at the oxide/Si interface, and the shift in the voltage position is proportional to the stress-induced positive oxide charge. As the gate voltage is swept from negative to positive, the drain region (n-Si) of the DMOSFET transistor progresses from inversion to accumulation. The current of the forward-biased junction is affected by the adjacent gate area beneath the gate. When the area under the gate is depleted, the generation from interface traps occurs, generating a hump in the current (see Fig. 1), which rapidly decays toward both inversion and accumulation, in which the surface is dominated by one type of carrier; thus, no generation occurs.

Using the generation–recombination theory, it is possible to calculate the density of interface states N_{IT} from the discontinuity of the hump [21]–[23] according to

$$\Delta I = q \cdot A \cdot \frac{n_i}{2} \cdot \sigma \cdot v_{\mathrm{th}} \cdot N_{\mathrm{IT}} \qquad (1)$$

where ΔI is the discontinuity of the hump, q is the electron charge, A is the active area, n_i is the intrinsic density, v_{th} is the thermal velocity, and σ is the cross section of the generation–recombination traps. On the other hand, the density of the trapped charge N_{OT} could be calculated from the voltage shift of the hump [21]–[23], according to

$$\Delta V = -q \cdot N_{\mathrm{OT}}/C_{\mathrm{OX}} \qquad (2)$$

where N_{OT} is the trapped charge density assuming the centroid at the oxide/Si interface and C_{OX} is the gate oxide capacitance per unit area.

III. Wear-Out Under Different Degradation Mechanisms

The techniques described in Section II were applied to different sets of samples stressed with all degradation mechanisms GRS, CVS, and PIS.

Fig. 2(a)–(c) show typical consecutive DCIV curves for one particular device from the set of samples under study (31.3 nm), and Fig. 2(d)–(f) show the V_{TH} shift at 100 μA in the subthreshold region of the source current at $V_D = +0.3$ V, as a function of the degradation parameter that corresponds to each mechanism.

The general response for all cases is similar; the height of the current peak in the DCIV measurement, which is proportional to the $Si-SiO_2$ interface trap density, increases and moves toward negative V_G due to interface states and positive trapped charges, respectively. On the other hand, ΔV_{TH} also reveal the positive trapped charge due to a similar shift toward negative voltages.

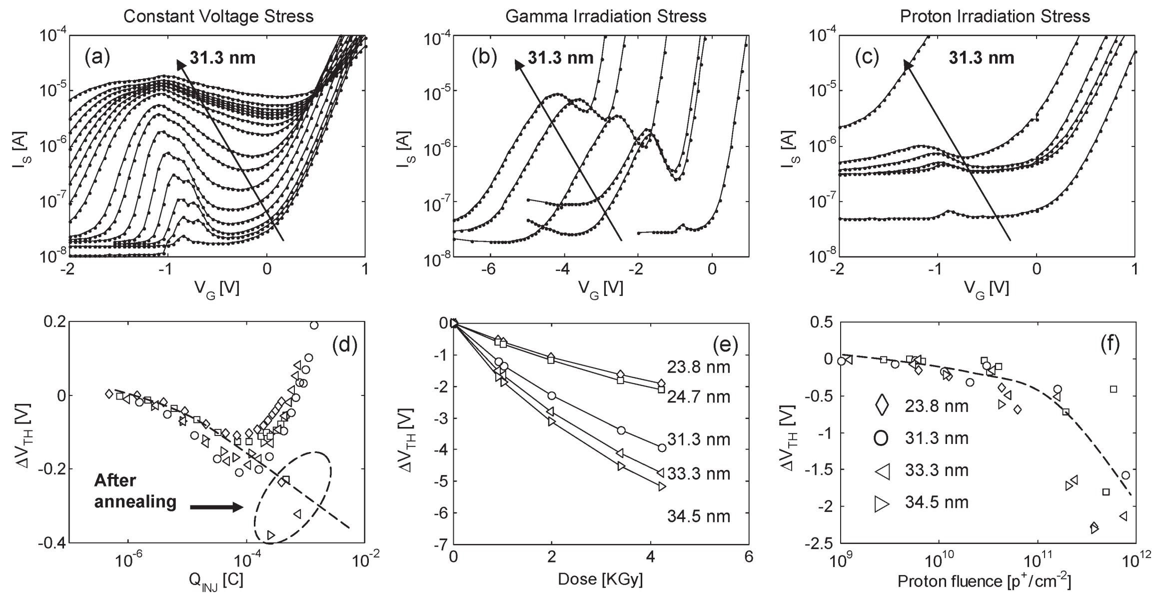

Fig. 2. Typical electrical characterization curves on DMOSFETs as function of the degradation parameter that corresponds to each mechanism. (a)–(d) Injected charge for the CVS. (b)–(e) Accumulated dose measured in grays for the GRS. (c)–(f) Proton fluence for the PIS. (a)–(c) are typical consecutive DCIV measurements (I_S vs. V_G at $V_D = -0.3$ V; p-n junction, forward) on a 31.3-nm gate oxide. (d)–(f) are the V_{TH} shifts at 10^{-4} A from consecutive subthreshold $I-V$ measurements (I_S vs. V_G at $V_D = +0.3$ V; p-n junction, reverse) for all oxides thicknesses of 23.8, 24.7, 31.3, 33.3, and 34.5 nm. (a) and (d) correspond to the CVS at 7.5 MV/cm. (b) and (e) correspond to the GRS irradiation (^{60}Co) at 0.9050 Gy/min. (c) and (f) correspond to the 10-MeV proton irradiation. During both cases of irradiation, the samples are biased at +10 V in the gate contact in the darkness at room temperature. Symbols "◇," "□," "○," "▷," and "◁" correspond to 23.8, 24.7, 31.3, 33.3, and 34.5 nm, respectively.

Fig. 2(d) shows ΔV_{TH} as a function of the injected charge Q_{INJ}. The measurements show a decrease in the voltage shift up to a minimum value as the degradation proceeds. Afterward, the general trend changes, and ΔV_{TH} increases with successive CVS pulses, exhibiting a turn-around effect.

In the case of the interaction with the ionizing radiation (GRS), the degradation level is represented by the accumulated dose measured in grays (Gy), which is the absorbed energy per mass unit [1]. Fig. 2(e) shows the threshold-voltage shift ΔV_{TH} as a function of the total accumulated dose. As expected, the generation of electron–hole pair due to the interaction of gamma photons results in the buildup of the positive trapped charge in the oxide and in the generation of $\mathrm{Si-SiO_2}$ interface states. The damage grows with the total dose, showing a clear dependence on t_{ox} consistent with previous results [1], [24].

For the 10-MeV proton irradiation, Fig. 2(f) shows a decrease in V_{TH} as a function of the particle fluence due to the buildup of the positive trapped charge.

In general, the stressed samples show a gradual increase in damage with stress. The amount of positive trapped charge is different for each case, and regarding the generation of $\mathrm{Si-SiO_2}$ interface states, only the samples stressed with the CVS and the GRS seem to reach saturation. The samples irradiated with 10-MeV protons also show an increase in the height of the current peak, accompanied by an increase in the leakage level. Note that, for the highest dose, the level of the leakage current is high enough to conceal the current peak.

A. Dynamic of Degradation in High-Field Stress

Fig. 3 shows a very reproducible gate current evolution during the stressing for a gate oxide of 31.3 nm subjected to the CVS at 7.5 MV/cm in the FN regime. The current rapidly increases, reaches the maximum, and then starts declining. It should be noted that, during the declining, in each stress pulse, the current increases and then decreases, joining a general trend. This behavior can be explained in terms of the charge buildup and the trapping of injected carriers [25]–[28].

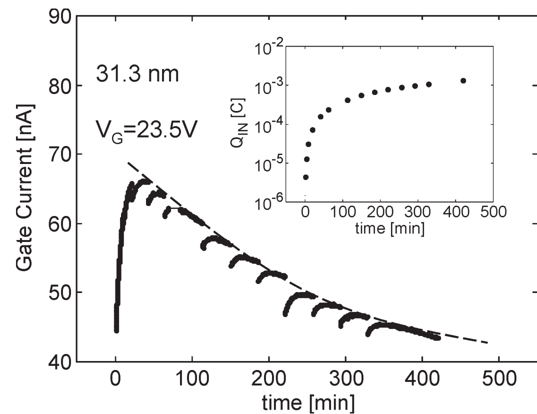

Fig. 3. Typical gate current as a function of the stress time for devices subjected to the CVS at 7.5 MV/cm and 23.5 V/33.1 nm. (Inset) Injected charge as a function of the stress time for the same case.

The initial rapid increase in the stress current could be a consequence of the narrowing of the barrier for electron tunneling due to the increase in the local electric field associated with the positive oxide charge buildup due to impact ionization [27]. Once the positive charge trapping at the gate oxide reaches a critical density, the trapping of injected electrons in trapped holes and/or related hydrogenous species and/or neutral traps becomes the dominant mechanism [23], [25], [26], [29], [30]. Hence, the stress current starts decreasing as a consequence of

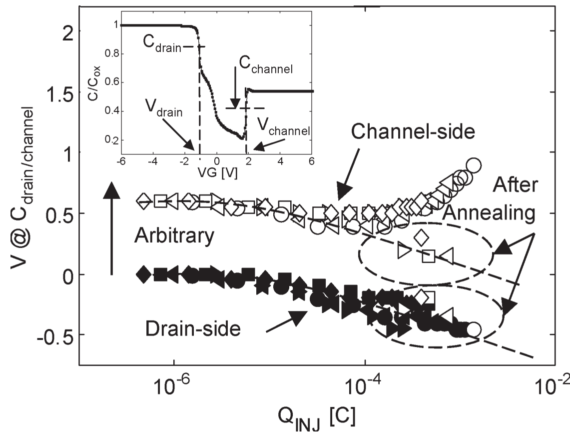

Fig. 4. Voltage shift at the constant capacitance of successive high-frequency $C-V$ measurements between the gate and the source subjected to the CVS at 7.5 MV/cm. There is an arbitrary separation of 0.6 V on the voltage in these curves for a better observation of their trends. The selected points correspond to measurements on the same devices after 30 h of annealing at 100 °C. Symbols "◇," "□," "◯," "▷," and "◁" correspond to 23.8, 24.7, 31.3, 33.3, and 34.5 nm, respectively. Open symbols correspond to the channel side, and closed symbols correspond to drain side. (Inset) Typical normalized high-frequency $C-V$ measurement and the regions from which the voltage shift is extracted.

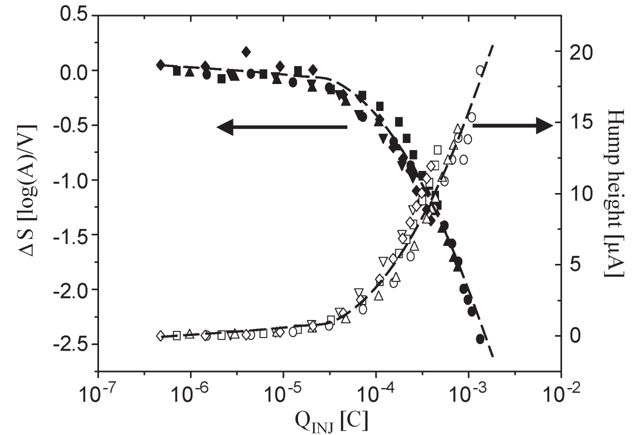

Fig. 5. Shift of the subthreshold slope from $I-V$ curves (I_S vs. V_G at $V_D = +0.3$ V; p-n junction, reverse) as a function of the injected charge. Symbols "◇," "□," "◯," "▷," and "◁" correspond to 23.8, 24.7, 31.3, 33.3, and 34.5 nm, respectively. Open symbols correspond to the hump height, and closed symbols correspond to the subthreshold slope.

the barrier widening due to the local field compensation of the electron trapping, generating the turn-around effect.

The inset of Fig. 3 shows the injected charge as function of the stress time after each stress pulse for the same measurement. The charge injected up to the peak being the same value required to change the trend of ΔV_{TH} in Fig. 2(d), the trapping of injected carriers could explain the turn-around effect.

Fig. 4 shows the voltage shifts of the high-frequency $C-V$ measurements according to the details of the inset. The $C-V$ measurement between the gate and source terminals is an accepted technique [14], [31] for distinguishing the degradation at the two interfaces of a DMOSFET device, i.e., the neck or drain-side interface and the channel-side interface (see inset of Fig. 1). The $C-V$ data (obtained between the gate and source terminals) essentially consist of capacitance components from the drain side, the channel side, and the insulator. The drain-side capacitance is the combination of the gate oxide capacitance under the drain region and of the epidrain capacitance, whereas the channel-side capacitance is the combination of the gate oxide capacitance under the channel region and of the channel-region ("body") capacitance. The contribution of these capacitance components to the measured capacitance depends on the surface potential at a given gate voltage. The $C-V$ data can be analyzed by separating it into the two regions, i.e., the drain-side interface and the channel-side interface, because a part of the $C-V$ data that results from the surface-potential variation in a given interface region does not affect the surface-potential variation in other interface parts of the sample. For example, the capacitance of the left-hand side in the $C-V$ data is from the n-type drain-side interface, whereas the step rise on the right-hand side of the curve is from the channel-side interface. Detailed analysis and modeling of the high-frequency $C-V$ data in a DMOSFET can be found elsewhere [14], [31]. As shown, there is a gradual increase in the positive trapped charge in both regions, but at one point (corresponding to the peak in the stress current in Fig. 3), the voltage shift at the channel-side interface moves away from the initial trend, giving rise to a net trapping charge of the opposite sign.

Fig. 5 shows the shift of the subthreshold slope of the $I-V$ characteristics, which is inversely proportional to the interface trap density under the channel-side interface, and the height of the hump, which is proportional to the interface trap density under the drain-side interface, as a function of the injected charge. The creation of interface states monitored in both regions does not exhibit differences or changes in the trend as in the case of ΔV_{TH} [see Figs. 2(d) and 4]. In Fig. 5, a monotonous growth of the density of interface states with the successive stress pulses is observed.

In resume, the analysis of the degradation with a high field reveals a nonuniform behavior for the two different regions under the gate oxide. Although both regions show an initial buildup of the positive trapped charge, the channel side reveals a turn-around effect that could be associated to trapping phenomena. In addition, the density of $Si-SiO_2$ interface states show no differences between them and increase with successive stress pulses.

B. Annealing

In order to gain information on the long-term effects of the working condition, all the samples were annealed to test the retention of the defects. In all cases, the annealing was performed at 100 °C for 30 h with all terminals grounded. Fig. 6(a) shows a typical measurement of the DCIV technique before and after the CVS stressing and the annealing. Under the stress, the curve shows an increase in the hump, a shift toward a negative voltage, and a decrease in the subthreshold slope, as mentioned in Section III-A. After the annealing, the DCIV curve moves toward positive voltages, and the height of the hump does not significantly change, meaning that the net positive charge diminishes without a change in the interface-state density at the drain side. This effect is present on both $C-V$ and V_{TH} measurements. The voltage shift of the $C-V$ curves on the channel side significantly decrease after the annealing, whereas the drain side remains almost unchanged (see Fig. 4). ΔV_{TH} shows

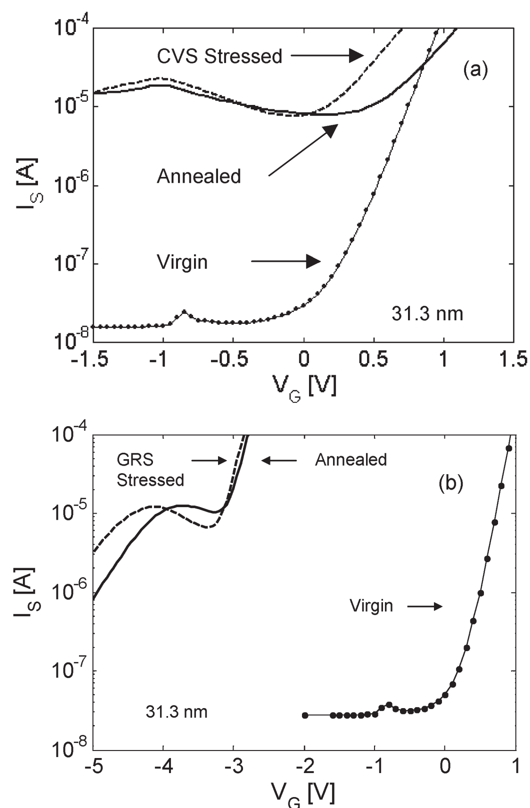

Fig. 6. Typical DCIV measurements (I_S vs. V_G at $V_D = -0.3$ V; p-n junction, forward) on a 31.3-nm gate oxide. The changes in the subthreshold slope, the height of the hump, and the trapped charge in the CVS stressed curve are evident. (a) For CVS. (b) For GRS. In both cases, the annealed curve is after 30 h of heating the device at 100 °C. It is observed that the amount of interface states remains almost the same but there is a shift toward positive voltages.

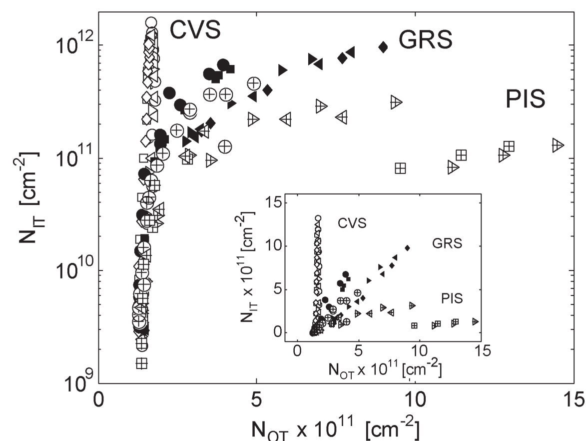

Fig. 7. Density of interface states (height of the DCIV hump) as a function of the density of the trapped charge (position in the voltage of the hump) for the CVS, the GRS, and the PIS. Symbols "◇," "□," "◯," "▷," and "◁" correspond to 23.8, 24.7, 31.3, 33.3, and 34.5 nm, respectively. Open symbols correspond to the CVS, closed symbols correspond to the GRS, and symbols "⊠" and "⊗" correspond to the PIS. (Inset) The same data in the linear scale.

284 the same behavior; the amount of positive charge is reduced 285 after the annealing [see Fig. 2(d)]. Hence, it is clear that only the 286 trapped charge at the channel side changes after the annealing, 287 whereas the trapped charge at the drain side does not show 288 significant changes.

289 This behavior is consistent with the results reported in other 290 papers, where the decrease in the trapped charge, maintaining 291 the density of interface states constant, is attributed to the 292 creation of latent traps in SiO_2 [32].

293 Fig. 6(b) shows the typical result of postradiation annealing 294 measurement of the DCIV technique. It is observed that the 295 curves do not show significant changes after the annealing in 296 both cases, maintaining the height of the hump and V_{TH} almost 297 constant.

298 IV. Correlation Between Gamma Photons, 299 Protons, and High-Field Stresses

300 Although the contention that there is no universal model 301 for the trapped charge and interface-state generation processes 302 valid under all circumstances is generally accepted [1], [29], 303 [30], [33], it is clear that there is a strong correlation between 304 them [1], [34]–[36].

305 Fig. 7 shows the density of $Si-SiO_2$ interface states N_{IT} 306 [from (1)] as a function of the density of the trapped charge 307 N_{OT} [from (2)] for all degradation mechanisms GRS, CVS, 308 and PIS. Divergent trends among the GRS, the CVS, and the PIS are clearly observed, even though there is an initial phase 309 where all degradation mechanisms overlap. 310

The large amount of interface states created by the CVS 311 shows the efficiency of the impact-ionization mechanism [29], 312 [30], [33] to damage the interface maintaining the buildup of 313 the trapped charge moderate. The GRS shows a linear increase 314 in the interface states with the dose, creating a state per trapped 315 charge. This one-to-one relation is in agreement with the re- 316 sults reported by other authors [35], [36] and consistent with 317 accepted models for ionizing radiation on MOS stacks [1], [35]. 318

In the case of the PIS, the first observation is the increase in 319 the background current to levels not observed in other cases. 320 This effect could be related to the creation of defects in the 321 substrate as has been reported elsewhere [37]. The second is 322 the very low generation of interface states. The overall picture 323 shown in Fig. 7 is that following a similar first stage of the 324 domination of the interface-state creation; once the interface- 325 state density is on the 10^{11} cm^{-2} range, each one of the stresses 326 investigated exhibits its own signature in the linear plot of N_{IT} 327 versus N_{OT} (see the inset of Fig. 7) with slopes close to 0 for 328 the PIS, close to 1 for the GRS, and close to infinity for the 329 CVS, at least for low total injection values. 330

Moreover, these results contribute to a better understanding 331 of the wear-out data under different degradation mechanisms. 332 It is well known that the BD of the gate oxide occurs when 333 the density of the defect reaches a critical level [29], [30]. The 334 presence of a different signature in the generation of interface 335 states and trapped charge for each degradation mechanism (see 336 Fig. 7) is a clear indication that the buildup rate of defects in the 337 gate oxide is also different. 338

V. Summary 339

Electrical changes in n-channel power DMOSFET devices 340 have been investigated through the DCIV and high-frequency 341 capacitance measurements after exposure to gamma photons 342 (^{60}Co), 10-MeV protons, and a high-field stress, and have been 343 comparatively analyzed. 344

345 The overall results have shown gradual changes in the elec-
346 trical characteristics after successive steps of stress pulses due
347 to the positive trapped charge and the interface states without
348 the occurrence of gate oxide BD.
349 To reproduce the long-term effects of the working condition,
350 all the samples have been annealed to test the retention of the
351 defects. No changes have been found after the annealing in irra-
352 diated devices, whereas in the case of the CVS samples, a major
353 change has been observed in the channel side, reverting the
354 turn-around effect. As a result of it, the degradation dynamics
355 of both regions (channel and drain interface processes) show
356 a similar trend, suggesting that both interface processes would
357 have a similar response in working conditions.
358 The correlation of the interface states with the trapped charge
359 is shown to be an adequate tool for comparing the effects from
360 different degradation mechanisms.
361 The results have shown an initial phase where all degradation
362 mechanisms overlap with similar dynamics of the interface-
363 state creation. Once on the range of 10^{11} cm^{-2} of interface-
364 state density, the relative efficiency in generating trapped charge
365 or states diverges and seems to be the characteristic for each
366 kind of stress. The CVS showed efficiency to produce interface
367 states with low buildup of the trapped charge. The GRS exhibits
368 a linear relation with a slope close to 1 between the trapped
369 charge and the interface states. Finally, the PIS showed a signif-
370 icant increase in the leakage current in the source current and a
371 large amount of trapped charge with low production of interface
372 states compared with the other degradation mechanisms.
373 The presented information may contribute to the desirable
374 target of predicting radiation effects on DMOSFET devices
375 through the effects of electrical stress.

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