Improved Superconducting Magnetic Energy Storage (SMES) Controller for High-Power Utility Applications

Marcelo Gustavo Molina, *Member, IEEE*, Pedro Enrique Mercado, *Senior Member, IEEE*, and Edson Hirokazu Watanabe, *Senior Member, IEEE*

***Abstract*—Superconducting magnetic energy storage (SMES) systems are getting increasing interest in applications of power flow stabilization and control in the transmission network level. This trend is mainly supported by the rising integration of large-scale renewable energy power plants into the high-power utility system and by major features of SMES units. In a SMES system, the power conditioning system (PCS) is the crucial component for controlling the power exchange between the superconducting coil and the ac system. The dynamics of the PCS directly influences the validity of the SMES in the dynamic control of the power system. This paper describes a novel PCS scheme of SMES to simultaneously perform both active and reactive power flow controls. Moreover, a detailed model of the SMES unit is derived and a three-level control scheme is designed, comprising a full decoupled current control strategy in the *d–q* reference frame with a novel controller to prevent PCS dc bus capacitors' voltage drift/imbalance. The dynamic performances of the proposed systems are fully validated by computer simulation.**

***Index Terms*—48-pulse voltage source converter (VSC), power conditioning system (PCS), superconducting magnetic energy storage (SMES), three-level control scheme, three-level dc/dc converter or chopper, transmission system.**

I. Introduction

In recent years, mainly due to the technology innovation, cost reduction, and government policy stimulus, there has been an extensive growth and rapid development in the exploitation of renewable energies, particularly wind and photovoltaic (PV) solar ones. Today, there exists an increasing penetration of large-scale wind farms and PV solar power plants into the high-power utility system all over the world [1]. This situation can lead to severe problems that dramatically jeopardize the power system security, particularly in a weak power system, i.e., system frequency oscillations due to insufficient system damping, and/or violations of transmission capability margin due to severe fluctuations of tie-line power flow, among others [2], [3]. Even more, because majority of these renewable energy plants with high installed capacity are connected to the transmission power system, their impacts are becoming more widespread. In addition, as presently deregulated power markets are taking place, generation and transmission resources are being utilized at higher efficiency rates, leading to a tighter control of the spare capacity [4].

To overcome this problem, superconducting magnetic energy storage (SMES) can be utilized as an effective device with the ability to rapidly exchange power with the ac power system [5]. The most important advantages of SMES devices include high power and energy density with outstanding conversion efficiency, and fast and independent power response in four quadrants. In a SMES system, the power conditioning system (PCS) is the interface that allows the effective connection to the power system. The dynamics of the PCS directly influences the validity of the SMES in the dynamic control of the power system. With the appropriate topology of the PCS and its control system design, the SMES unit is capable of simultaneously performing both instantaneous active and reactive power flow controls [6]–[11].

Various PCSs for SMES systems have been studied in the literature [5]–[9], including 24-pulse and 48-pulse converter designs among the most adequate for applications in the transmission network level, i.e., in high-voltage (hundreds of kilovolts) high-power (several megawatts) levels. However, 24-pulse (or lower) converter-based SMES systems require capacitor banks for harmonic filtering, which represents a limitation because besides creating additional power losses and decreasing the system performance, they usually introduce additional harmonic resonances with the power system line inductances and may become troublesome. On the other hand, 48-pulse converters employ eight transformers for coupling eight gate turnoff (GTO) thyristor full bridge inverters, which are bulky, heavy, and lossy. Moreover, all these proposed PCSs use a conventional two-level dc/dc converter as interface between the SMES coil and the converter.

This paper describes the design and implementation of a novel high-performance PCS of a SMES and its controller, for applications in the transmission network level. The proposed converter structure is a 48-pulse one, composed of four magnetic coupled three-level full bridges that have better dynamic performance than conventional structures and reduce to half the requirement of transformers. A full detailed model of the SMES controller is derived, including two power converters to provide the high-efficiency power conditioning system capability

Manuscript received March 2, 2010; revised July 22, 2010; accepted November 9, 2010. Date of publication January 6, 2011; date of current version May 18, 2011. This work was supported in part by the Argentinean National Agency for the Promotion of Science and Technology (ANPCyT) under Grant PICT 2005, 33407. Paper no. TEC-00101-2010.

M. G. Molina and P. E. Mercado are with the Argentinean National Council for Science and Technology Research (CONICET), National University of San Juan, San Juan J5400ARL, Argentina (e-mail: mgmolina@ieee.org; pmercado@ieee.org).

E. H. Watanabe is with the Alberto Luiz Coimbra Institute for Graduate Studies and Research in Engineering (COPPE), Federal University of Rio de Janeiro, Rio de Janeiro 21945-970, Brazil (e-mail: watanabe@coe.ufrj.br).

Digital Object Identifier 10.1109/TEC.2010.2093601

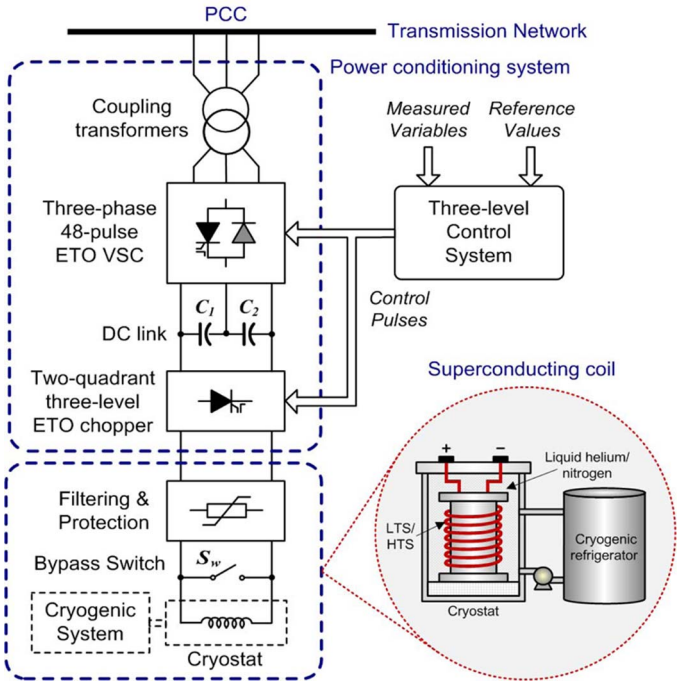


Fig 1. General components of the proposed SMES unit.

and the superconducting coil (SC), as depicted in Fig. 1. The PCS consists of a three-phase three-level multipulse ac/dc converter and incorporates a two-quadrant three-level dc/dc converter as interface with the SMES coil. Moreover, based on the state-space averaging method a three-level control scheme is designed, comprising a full decoupled current control strategy in the synchronous-rotating *d–q* reference frame with a novel controller to prevent the voltage drift/imbalance of the ac/dc converter dc bus capacitors. The dynamic performances of the proposed systems are fully validated by digital simulation carried out by using SimPowerSystems (SPS) of MATLAB/Simulink.

II. Modeling of the Proposed SMES System

Fig. 2 summarizes the proposed detailed model of the SMES controller for applications in the distribution network level. This model consists of the PCS and the SMES coil with its filtering and protection system.

A. Power Conditioning System

The PCS provides a power electronic interface between the electrical grid and the SC, aiming at achieving two goals: one is to convert electric power from dc to ac, and the other is to charge/discharge efficiently the SC. The major component of the proposed PCS is the well-known flexible ac transmission system (FACTS)-based static synchronous compensator (STATCOM). The application of FACTS controllers based on voltage source converters (VSC) has been settled worldwide as the next generation of fast reactive power compensators for improving both transient and dynamic stabilities [12]. In this sense, shunt compensation provided by STATCOM controllers has already proved its benefits on the existing transmission system. Since they can only exchange reactive power with the electric grid, which limits its degrees of freedom and therefore its impact on the power system operation, a STATCOM–SMES combination (also known simply as the SMES system) has been proposed as an improved controller, allowing simultaneous active and reactive power compensation with more valuable effects on counteracting PS disturbances [5], [8], [13]. These benefits include enhancement of reliability, dynamic stability, power quality, and area protection.

The STATCOM basically consists of the VSC with semiconductors devices having turnoff capabilities [emitter turnoff thyristor (ETO)], step-up transformers, and dc bus capacitors. High efficiency VSCs with reduced harmonic distortion can be implemented essentially through three feasible solutions: the conventional full bridge converter employing pulse width modulation (PWM), the multilevel converter, and the multipulse converter. In practice, conventional PWM switching techniques are regarded uneconomic for high-power applications since they produce very high switching losses [14]. The most relevant topologies of multilevel converters are diode-clamped (neutral-point clamped or NPC), capacitor-clamped (flying capacitors), and cascaded multicell with separate dc sources [15]. By increasing the number of levels in the converter, the output voltage waveforms have more steps generating a staircase approximation of a sinusoidal waveform, which has a reduced harmonic distortion. However, a high number of levels increase the control complexity and introduce voltage imbalance problems, voltage clamping requirements, circuit layout, and packaging constraints [16]. In practice, for the case of high-voltage high-power applications including active power exchange, the number of feasible voltage levels with adequate results is restricted to no more than 5. The traditional magnetic coupled multipulse converter using the harmonic cancellation technique has two or more bridges and synthesizes the staircase output voltage waveform by varying transformer turns ratio with zigzag connections. The magnetic transformer coupled converter is bulky, heavy, and lossy. Furthermore, the VSC should have a large number of bridges and transformers in order to increase the pulses number for minimizing the harmonic distortion produced. Nevertheless, practical high-voltage high-power applications in the transmission level demonstrate the adequacy of this topology [17].

Based on these facts, this study proposes the use of the fundamental frequency modulated multipulse ETO converter for building the VSC that interfaces a high-power high-energy SMES coil with the transmission utility grid. In order to avoid the use of ac capacitor banks for harmonic filtering and to meet the voltage total harmonic distortion requirements for transmission level applications, a pseudo 48-pulse ETO converter composed of four magnetic coupled three-level 12-pulse full bridges emerges as the most appropriate topology, as described in Fig. 2 (right side). This topology can be applied to reactive power generation almost without voltage imbalance problems. But when active power exchange is included, the ac/dc converter could not have balanced voltages without sacrificing output voltage performance and auxiliary converters would be needed in order to provide a compensating power flow between the capacitors of the dc link [17]. For this reason, the use of an advanced

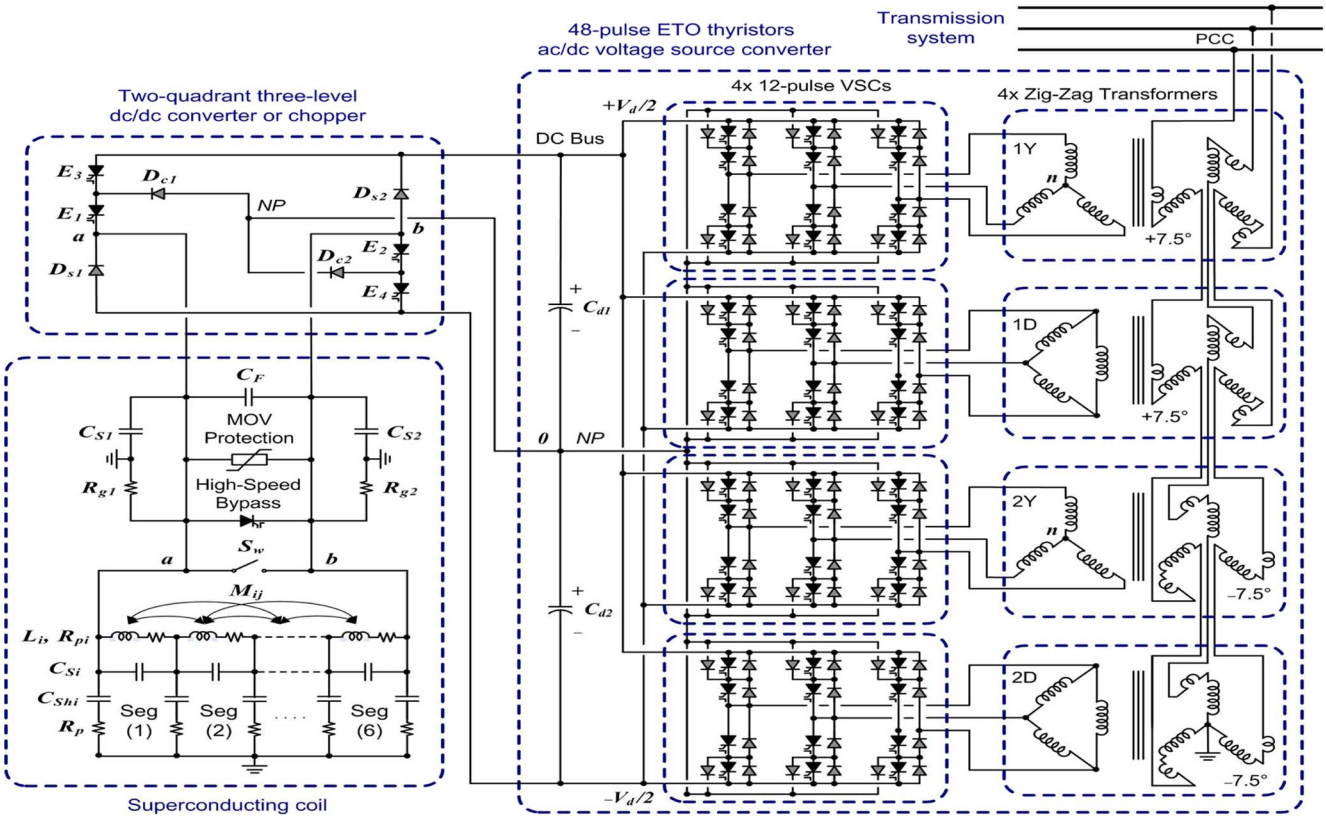
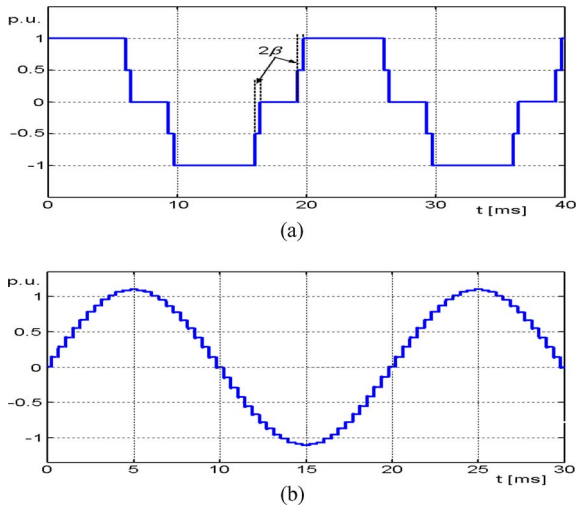


Fig. 2. Detailed model of the proposed SMES system, including the power conditioning system and the SC.



(a)

(b)

Fig. 3. Voltage source converter switching functions. (a) Basic 12-pulse VSC, S^{12}. (b) Equivalent 48-pulse VSC, S^{e48}.

dc/dc converter as interface between the VSC and the SMES is required, instead of a standard one.

Fig. 3(a) shows the switching function for phase "a" of each 12-pulse VSC, while the switching function of the resultant pseudo 48-pulse VSC is depicted in Fig. 3(b), and can be estimated by

$$S_a^{e48} \approx \sum_{h=1}^{\infty} \left[\frac{2}{h\pi} k_T \cos(h\beta) \sin(h\omega t) \right] \quad (1)$$

where $h = 48m \pm 1$ ($h = 1, 47, 49, \ldots$) and $m = 0, 1, 2, \ldots$; $k_T = 4(n_2/n_1)$ is the total voltage ratio of the zigzag transformers; and β is the dead angle (period) during which the VSC output voltage is zero ($\beta_{\text{optimum}} = 3.75°$).

If the switching functions are averaged, the peak value of the phase-to-neutral output voltage for the equivalent 48-pulse VSI can be expressed through

$$V_{\text{inv}} = S_{\text{av}}^{e48} \, V_d \quad (2)$$

being $S_{\text{av}}^{e48} = (2/\pi) k_T \cos\beta$ the average switching function for the VSC.

The inclusion of a SMES coil into the dc bus of the VSC demands the use of an improved interface to adapt the wide range of variation in voltage and current levels between both devices. Controlling the SMES coil rate of charge/discharge requires varying as much the coil voltage magnitude as the polarity according to the coil state-of-charge, while keeping essentially constant and balance the voltage of the VSC dc link capacitors. To this aim, a two-quadrant three-level ETO dc/dc converter or chopper is proposed to be employed, as shown in Fig. 2 (upper left side). This converter allows decreasing the ratings of the overall PCS (specifically VSC and transformers) by regulating the current flowing from the SMES coil to the inverter of the VSC and vice versa. In addition, it allows varying the amplitude of the output voltage of the VSC, keeping constant the conduction angle σ of the ETO thyristors. Major advantages of three-level chopper topologies compared to traditional two-level ones include reduction of voltage stress of each thyristor by half,

TABLE I
THREE-LEVEL CHOPPER OUTPUT VOLTAGE VECTORS AND THEIR CORRESPONDING ETO SWITCHING STATES

States	E_1	E_2	E_3	E_4	V_{ab}
1	1	1	1	1	$+V_d$
2	0	0	0	0	$-V_d$
3	0	1	0	1	*0*
4	1	0	1	0	*0*
5	1	1	0	0	*0*
6	1	1	0	1	$+V_d/2$
7	1	1	1	0	$+V_d/2$
8	1	0	0	0	$-V_d/2$
9	0	1	0	0	$-V_d/2$

permitting to increase the chopper power ratings while maintaining high dynamic performance and decreasing the harmonic distortion produced. Furthermore, it includes the availability of redundant switching states, which allow generating the same output voltage vector through various states. This last feature is very significant to reduce switching losses and VSC dc current ripple, but mainly to maintain the charge balance of the dc bus capacitors, thus avoiding contributing to the ac system with additional distortion.

Table I lists all possible combinations of the chopper output voltage vectors $V_{\rm ab}$ (defining the SMES side of the circuit as the output side) and their corresponding ETO switching states. As derived, the chopper can be thought of as a switching matrix device that combines various states for applying either a positive, negative, or null voltage to the SC coil. The addition of an extra level to the dc/dc chopper allows enlarging its degrees of freedom. As a result, the charge balance of the dc bus capacitors can be controlled by using the extra switching states, at the same time acting as an enhanced conventional dc/dc converter. The output voltage vectors can be selected based on the required SMES coil voltage and dc bus neutral point (*NP)* voltage. In this way, multiple subtopologies can be used in order to obtain output voltage vectors of magnitude 0 and $V_d/2$, in such a way that different vectors of magnitude $V_d/2$ produce opposite currents flowing from/to the neutral point. This condition causes a fluctuation in the *NP* potential that permits to maintain the charge balance of the dc link capacitors. By properly selecting the duration of the different output voltage vectors, an efficient dc/dc controller with *NP* voltage control abilities is obtained.

The dc/dc chopper has basically three modes of operation, namely the buck or charge mode, the standby or free-wheeling mode, and the boost or discharge mode. These modes are obtained in this study by using a buck-boost topology control mode contrary to a bang–bang control mode [18], [19], which is much simpler yet produces higher ac losses in the SC. The behavior of the chopper for each mode of operation can be explained in terms of operating a combination of three of the switching states shown in Table I during a switching cycle T_s. The purpose of the chopper is to apply a positive, null, or negative average voltage to the SMES coil, according to the mode of operation.

In the first mode of operation, that is the charge mode, the chopper works as a step-down (buck) converter. Since power is supplied to the SC from the electric power system, this mode can also be called powering mode, and makes use of a combination of positive and null vectors. This is achieved through the switching states 1, 5, and 6 or 7 in order to produce output voltage vectors $+V_d$, 0, and $+V_d/2$ with separate contribution of charge at the *NP* from capacitors C_{d1} and C_{d2}. As can be observed from Fig. 4(a), in this mode thyristors E_1 and E_2 are always kept ON, while thyristors E_3 and E_4 are modulated to obtain the appropriate output voltage, $V_{\rm ab}$, across the SMES coil. In this way, only subtopologies closest to the state 1 are used. In consequence, only one semiconductor device is switched per switching cycle; this reduces the switching losses compared to the standard two-level converter and thus also reduces the input/output current ripple.

Fig. 5(a) shows the switching function $S_{\rm ch}$ of the three-level chopper operating in buck mode. This function, which is stated in (3), is valid for the charge mode independently of the switching states utilized for maintaining the charge balance of the dc capacitors (state 6 or 7):

$$S_{\rm ch} = D_1 + D_2 + \sum_{h=1}^{\infty}\left[2\frac{\sin\left(h\,\pi D_2\right)}{h\pi}\cos\left[h\omega\left(t-\gamma_2-2\gamma_1\right)\right]\right] + \sum_{h=1}^{\infty}\left[\frac{\sin\left(2h\pi D_1\right)}{h\pi}\cos\left[h\omega\left(t-\gamma_1\right)\right]\right] \quad (3)$$

where

$h =$ 1, 2, 3, ...
$D_1 = t_{\rm on1}/2T_s$: duty cycle for switching state 6 or 7
$D_2 = t_{\rm on2}/T_s$: duty cycle for switching state 1
$\gamma_1 = D_1/f$: harmonic phase angle due to D_1
$\gamma_2 = D_2/2f$: harmonic phase angle due to D_2
with f being the fundamental electric grid frequency.

Once completed the charging of the SMES coil, the operating mode of the converter is changed to the standby mode, for which only the state 5 is used. As derived from Fig. 4(b), in this second mode of operation thyristors E_3 and E_4 are switched OFF, while thyristors E_1 and E_2 are kept ON all the time. In this way, the SMES coil current circulates in a closed loop, so that this mode is also known as free-wheeling mode, and the current remains fairly constant.

In the third mode of operation, that is the discharge mode, the chopper works as a step-up (boost) converter. Since power is returned back from the SC to the electric grid, this mode can also be called regenerative mode, and makes use of a combination of negative and null vectors. This is achieved through the switching states 2, 5, and 8 or 9 in order to produce output voltage vectors $-V_d$, 0, and $-V_d/2$ with independent contribution of charge at the *NP* from capacitors C_{d1} and C_{d2}. As can be observed from Fig. 4(c), in this mode thyristors E_3 and E_4 are constantly kept OFF while thyristors E_1 and E_2 are controlled to obtain the suitable voltage $V_{\rm ab}$, across the SMES coil. In this way, only subtopologies closest to the state 2 are used. In consequence, as in the case of the charge mode, only one semiconductor device is switched per switching cycle.

Fig. 5(b) shows the switching function $S_{d\rm ch}$ of the three-level chopper operating in boost mode. This function, which is stated

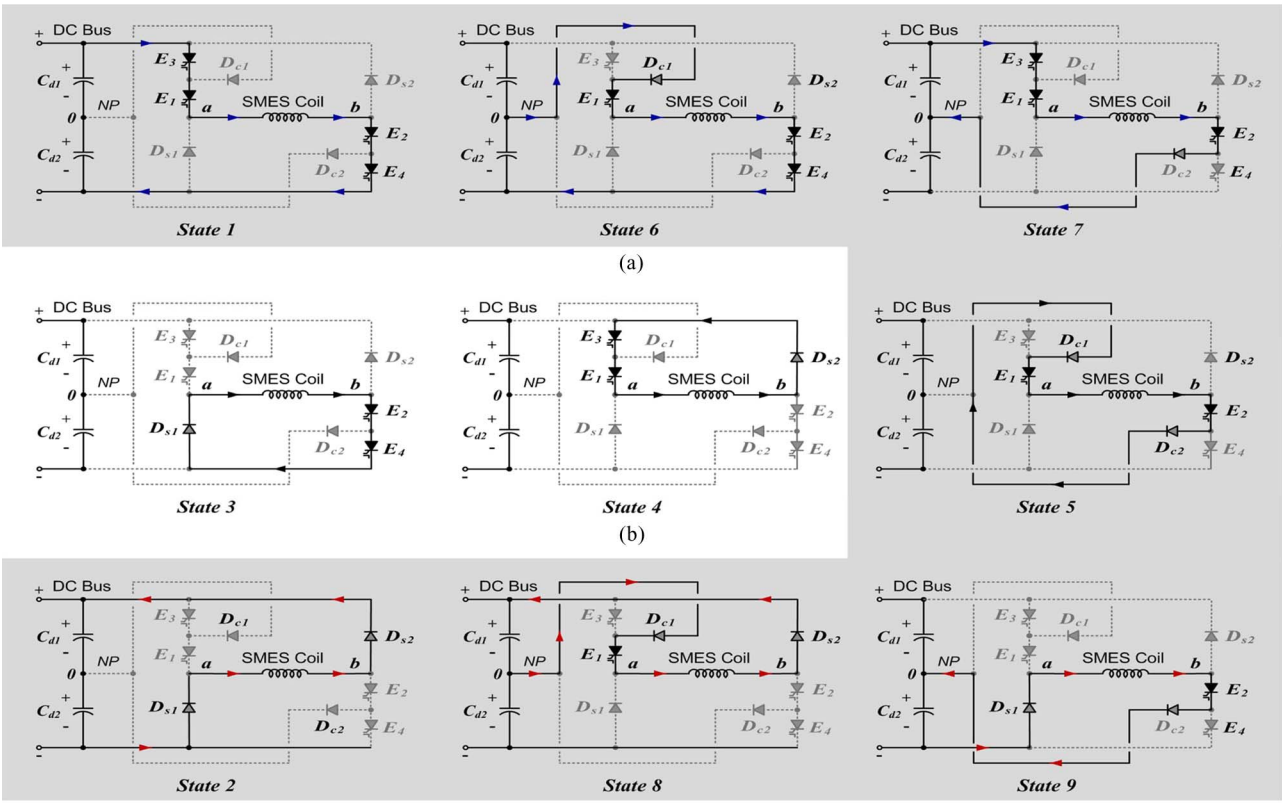


Fig. 4. Modes of operation and switching states of the two-quadrant three-level chopper. (a) Buck mode. (b) Standby mode. (c) Boost mode.

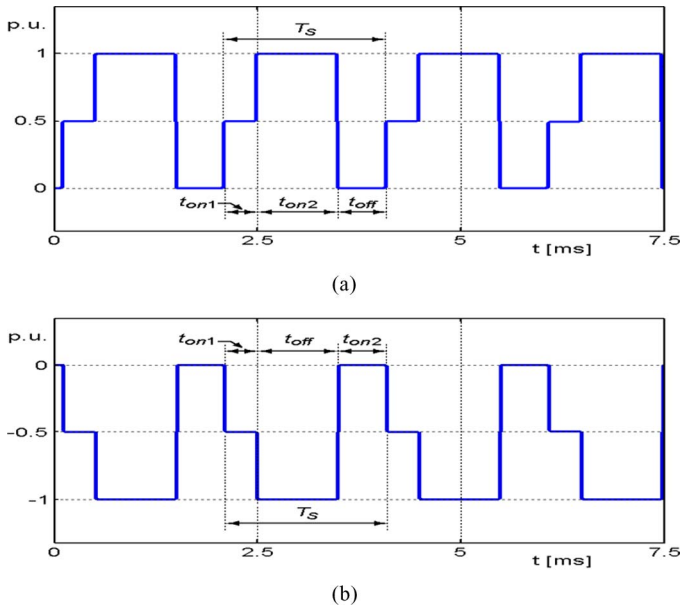


Fig. 5. Chopper switching functions. (a) Buck (charge) mode, $S_{\rm ch}$. (b) Boost (discharge) mode, $S_{d\rm ch}$.

in (4), is valid for the discharge mode independently of the switching states utilized for maintaining the charge balance of the dc capacitors (state 8 or 9):

$$-S_{d\rm ch} = 1 - D_1 - D_2 + \sum_{h=1}^{\infty}\left[2\frac{\sin\left(h\,\pi\,(1-D_2)\right)}{h\pi}\cos\left[h\omega\left(t-\zeta_2-2\zeta_1\right)\right]\right] + \sum_{h=1}^{\infty}\left[\frac{\sin\left(2h\,\pi\,(1-D_1)\right)}{h\pi}\cos\left[h\omega\left(t-\zeta_1\right)\right]\right] \quad (4)$$

where

$h = 1, 2, 3, \ldots$

$\zeta_1 = (1-D_1)/f$: harmonic phase angle due to D_1

$\zeta_2 = (1-D_2)/2f$: harmonic phase angle due to D_2.

By averaging the switching functions $S_{\rm ch}$ and $S_{d\rm ch}$, which is analogous to neglecting harmonics, a general expression relating the chopper average output voltage $V_{\rm ab}$ to the VSC average dc bus voltage V_d can be derived through

$$V_{\rm ab} = m\,V_d \quad (5)$$

being m the modulation index expressed as

$m = (D_1 + D_2)$: chopper in buck mode (charge)

$m = -(1 - D_1 - D_2)$: chopper in boost mode (discharge).

B. SMES Coil

A SMES system consists of several subsystems, which must be carefully designed. The base of the SMES unit is a large SC, whose basic structure is composed of the cold components itself and the cryogenic refrigerating system, as shown at the bottom side of Fig. 1. The cold components include the low-temperature

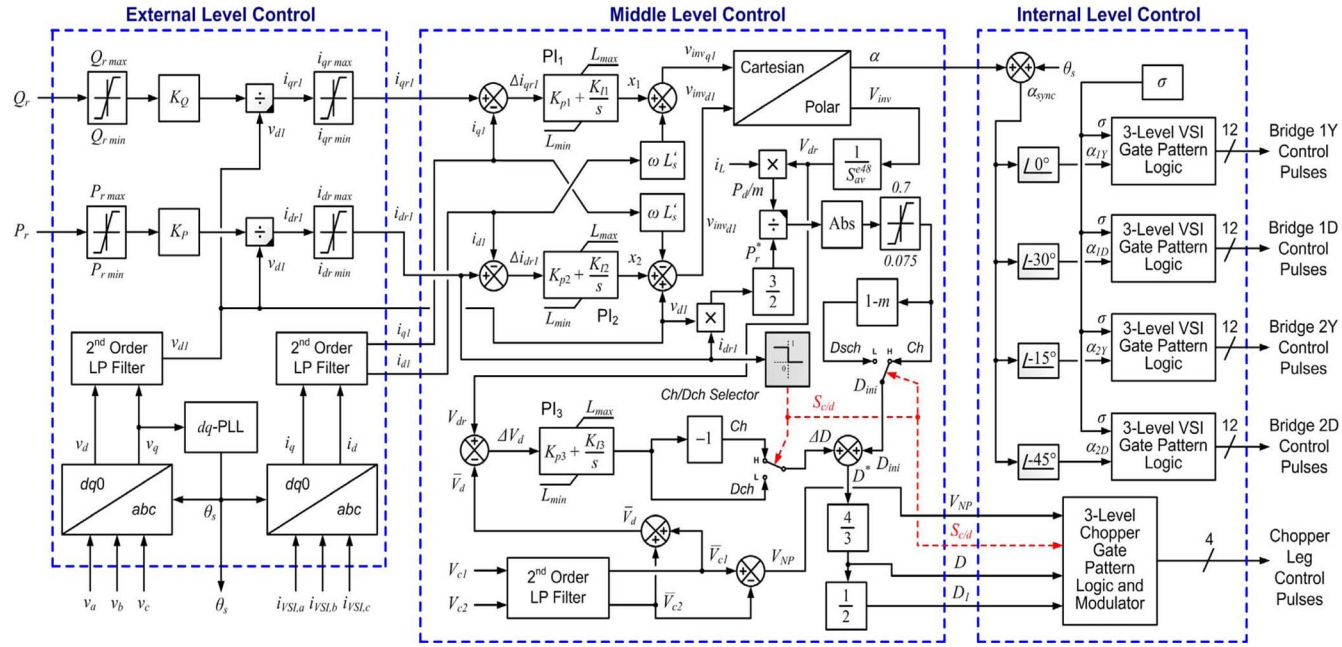


Fig. 6. Control system block diagram of the SMES device.

or high-temperature SC (LTS/HTS), with its support and connection components, and the cryostat.

The equivalent circuit of the SMES coil depicted at the bottom left side of Fig. 2 makes use of a lumped parameters network represented by a six-segment model comprising self inductances (L_i), mutual couplings between segments (i and j, $M_{\rm ij}$), ac loss resistances ($R_{\rm si}$), skin effect-related resistances ($R_{\rm pi}$), turn-ground (shunt—$C_{\rm Shi}$) and turn-turn capacitances (series—$C_{\rm Si}$). This model is based on the ones previously proposed in [10], [11], and is reasonably accurate for electric systems transients studies, over a frequency range from dc to several thousand Hertz. The inclusion of surge capacitors ($C_{\rm Sg1}$ and $C_{\rm Sg2}$) and a filter capacitor C_F in parallel with grounding-balance resistors (R_{g1} and R_{g2}) allows reducing the effect of resonances. A metal oxide semiconductor protection for transient voltage surge suppression is included between the SMES model and the dc/dc converter.

III. Proposed Control Scheme of the SMES System

The proposed three-level control scheme of the SMES unit consists of an external, middle, and internal level. Its design is based on concepts of instantaneous power on the synchronous-rotating *d–q* reference frame, as depicted in Fig. 6. This structure has the goal of rapidly and simultaneously controlling the active and reactive powers provided by the SMES. To this aim, the controller must ensure the instantaneous energy balance among all the SMES components. In this way, the stored energy is regulated through the PCS in a controlled manner for achieving the charging and discharging of the SC. In order to independently control the exchange of active and reactive powers, the dc bus voltage must be kept constant and the SMES charge/discharge is controlled by the chopper switching function. This control mode of the chopper is called voltage control mode (VCM) and exhibits a high controllability of the SMES system for meeting power flow control requirements. However, during off-peak periods, the SC should be charged as fast as possible to ensure that it is made ready when is required again. In this particular case, the VCM can be relatively slow because the rate of increase/decrease of the SMES coil current depends on the dc bus voltage and coil inductance, which both are constants. By controlling the chopper in the current-control mode (CCM), i.e., the charging current is forced to ramp up quickly in the SC to its maximum reference value determined by the critical current density independently of the dc bus voltage, the charging process can be greatly accelerated [21]. Evidently, this advantage is gained at expenses of not being able to control the SMES reactive power generated during this process, as can be done in the slower VCM.

A. External Level Control Design

The external level control, which is outlined in Fig. 6 (left side), is responsible for determining the active and reactive power exchange between the SMES device and the utility system. The control strategy applied can be designed for performing various control objectives with dissimilar priorities, as widely presented in the literature [22], [23]. In this paper, a general active and reactive power command to achieve the desired system response is provided. To this aim, the instantaneous voltage at the PCC is computed by employing a synchronous-rotating reference frame. In consequence, by applying Park's transformation, the instantaneous values of the three-phase ac bus voltages are transformed into *d–q* components, v_d and v_q, respectively. By defining the d-axis always coincident with the instantaneous voltage vector v, then v_d results in steady state equal to $|v|$ while v_q is null. Consequently, the d-axis current component of the VSC contributes to the instantaneous active power p while the

q-axis current component represents the instantaneous reactive power q, as stated in (6) and (7). Thus, to achieve a decoupled active and reactive power control, it is required to provide a decoupled control strategy for i_d and i_q:

$$p = \frac{3}{2}(v_d i_d + v_q i_q) = \frac{3}{2}|v|\ i_d \tag{6}$$

$$q = \frac{3}{2}(v_d i_q - v_q i_d) = \frac{3}{2}|v|\ i_q. \tag{7}$$

In this way, only v_d is used for computing the resultant current reference signals required for the desired SMES output active and reactive power. Independent limiters are used to restrict both the power and current signals before setting the references $i_{\rm dr}$ and $i_{\rm qr}$. Additionally, the instantaneous actual output currents of the SMES, i_d and i_q, are computed for use in the middle level control. In all cases, the signals are filtered by using second-order low-pass filters to obtain the fundamental components employed by the control system. A phase locked loop (PLL) is used for synchronizing, through the phase θ_s, the coordinate transformations from *abc* to *d–q* components in the voltage and current measurement system. The phase signal is derived from the positive sequence components of the ac-voltage vector measured at the PCC of the SMES.

B. Middle Level Control Design

The middle level control makes the expected output, i.e., positive sequence components of i_d and i_q, to dynamically track the reference values set by the external level. The middle level control design, which is depicted in Fig. 6 (middle side), is based on a linearization of the state-space averaged model of the SMES VSC in *d–q* coordinates, as follows:

$$s\begin{bmatrix} i_d \\ i_q \\ \cdots\cdots \\ V_d \end{bmatrix} = \begin{bmatrix} \frac{-R_s}{L'_s} & \omega & \vdots & \frac{S_d^{e48}}{L'_s} \\ -\omega & \frac{-R_s}{L'_s} & \vdots & \frac{S_q^{e48}}{L'_s} \\ \cdots\cdots & \cdots\cdots & \vdots & \cdots\cdots \\ -\frac{3}{C_d}S_d^{e48} & -\frac{3}{C_d}S_q^{e48} & & -\frac{2}{R_p C_d} \end{bmatrix} \times \begin{bmatrix} i_d \\ i_q \\ \cdots\cdots \\ V_d \end{bmatrix} - \begin{bmatrix} \frac{|v|}{L'_s} \\ 0 \\ \cdots\cdots \\ 0 \end{bmatrix} \tag{8}$$

where

- R_s equivalent resistance accounting for transformers winding resistance and VSC semiconductors conduction losses;
- L'_s equivalent leakage inductance in the *d–q* reference frame for the four VSC step-up transformers;
- C_d equivalent capacitance of the dc bus capacitors;
- ω synchronous angular speed of the network voltage.

The average switching functions for the 48-pulse VSC, transformed into the *d–q* reference frame, can be defined as

$$S_d^{e48} = S_{av}^{e48}\cos\alpha \tag{9}$$

$$S_q^{e48} = S_{av}^{e48}\sin\alpha, \tag{10}$$

with α the phase shift of the VSC output voltage from the reference position set by the instantaneous voltage vector measured at the point of common coupling (PCC).

Inspection of (8) shows a cross-coupling of both components of the SMES output current through ω. Therefore, in order to fully decouple the control of i_d and i_q, appropriate control signals have to be generated. To this aim, it is proposed the use of two control signals x_1 and x_2, which are derived from assumption of zero derivatives of currents (si_d and si_q) in the upper part (ac side) of (8). This condition is assured by employing conventional PI controllers with proper feedback of the SMES actual output current components, as shown in Fig. 6. Thus, i_d and i_q respond in steady state to x_1 and x_2, respectively, with no cross-coupling, as derived from (11). As can be noticed, with the introduction of these new variables this control approach allows us to obtain a quite effective decoupled control with the VSC model (ac side) reduced to first-order functions

$$s\begin{bmatrix} i_d \\ i_q \end{bmatrix} = \begin{bmatrix} \frac{-R_s}{L'_s} & 0 \\ 0 & \frac{-R_s}{L'_s} \end{bmatrix}\begin{bmatrix} i_d \\ i_q \end{bmatrix} - \begin{bmatrix} x_1 \\ x_2 \end{bmatrix}. \tag{11}$$

The coordinate transformation from Cartesian to Polar yields the required magnitude of the output voltage vector $V_{\rm inv}$ produced by the VSC, and its absolute phase-shift rating α.

The three-level dc/dc converter control is designed by calculating the required voltage at the dc bus, $V_{\rm dr}$ according to the VSC output voltage vector $V_{\rm inv}$ earlier set, as stated in (2). The modulation index m is rapidly estimated through a balance of actual dc powers in the chopper, taking into consideration the active power injection/absorption ratings required from the SMES and the actual current of the SMES coil i_L. The duty cycle of the chopper ETO thyristors is then derived by relying on the mode of operation of the dc/dc chopper (charge/discharge), so that an initial value $D_{\rm ini}$ is determined for the thyristors duty cycle. This mode of operation is determined assessing the sign of the required positive sequence component of i_d ($i_{\rm dr1}$) via a charge/discharge selection block and producing a signal of mode $S_{c/d}$ that is also required by the internal level control. A corrective action of integral-type (PI controller) is needed for an accurate tracking of the actual duty cycle D^*, being D^* the total duty ratio of the three-level chopper. Therefore, dc bus voltage deviations ΔV_d caused by actual VSC switching losses and capacitors power losses can be quickly counteracted. Finally, duty cycles D_1 and D_2 are computed from D^* for balancing the dc link capacitors, as formerly explained. This novel extra dc voltage control block provides the availability of managing the redundant switching states of the chopper according to the capacitors charge unbalance measured through the neutral point voltage, $V_{\rm PN} = \overline{V_{\rm c1}} - \overline{V_{\rm c2}}$. This specific loop modifying the modulating waveforms of the internal level control is also proposed for reducing instability problems caused by harmonics as much in the SMES device as in the electric system. The application of a static determination of D_1 and D_2, such as the case of $D_1 = D_2 = D/2$ has proved to be good enough for reaching an efficient equalization of the dc bus capacitors over the full range of VSC output voltages and active/reactive power requirements.

C. Internal Level Control Design

The internal level provides dynamic control of input signals for the dc/dc and ac/dc converters. This level is responsible for generating the triggering and blocking control signals for the different valves of the pseudo 48-pulse three-level VSC and the three-level dc/dc chopper. Fig. 6 (right side) shows a basic scheme of the internal level control of the SMES unit. This level is mainly composed of a line synchronization module and a firing pulses generator for both the VSC and the chopper. The line synchronization module simply synchronizes the SMES device switching pulses with the positive sequence components of the ac voltage vector at the PCC through the PLL phase signal θ_s.

In the case of the VSC firing pulses generator block, the fundamental frequency modulator is made up of four basic twelve-pulse switching generators with specific phase shifting in order to obtain an overall 48-pulse structure. The phase shifting between control pulses of bridges 1Y and 1D makes an equivalent structure of a 24-pulse VSI. Hence, by lagging the control pulses of the second equivalent 24-pulse structure by 15° with respect to the first, according to the phase shifting of zigzag transformers primaries, an equivalent 48-pulse VSI is reached. Even though the ETOs conduction angle σ can be changed to control the output voltage amplitude of the VSC, in this paper the amplitude is controlled just by using the duty ratio m of the chopper. In this way, σ is kept constant at 172.5° in order to obtain the lowest voltage total harmonic distortion (THD) for this topology, independently of the output voltage amplitude.

In the case of the chopper firing pulses generator block, the three-level PWM modulator is built using a compound signal obtained as the difference of two standard two-level PWM signals. According to the mode of operation of the chopper (charge/discharge), the switching functions $S_{\rm ch}$ and $S_{d\rm ch}$ are synthesized using (2) and (3).

IV. Digital Simulation Results

The dynamic performance of the proposed full detailed modeling and control approach of the SMES system is assessed through digital simulations carried out in MATLAB/Simulink [24], by using SPS. Since the detailed model of the proposed SMES contains many states and nonlinear blocks such as power electronics switches, the discretization of the electrical system with a fixed-step of 25 μs is required so as to reduce the computation effort and thus to improve the simulation performance while maintaining accuracy of results. For the power system simulation, the following assumptions are made: voltages and currents of the ac source are sinusoidal and symmetrical, generator dynamics and saturations are neglected, and loads are linear and balanced. In the same way, for the power converter simulation the assumptions made are the subsequent: ETO thyristors are represented by ideal switches with resistive snubbers, turn-on and turn-off times are not modeled, forward voltages of ETOs and clamping diodes are neglected, and zigzag phase-shifting transformers are implemented using three single-phase, three-winding transformers without core saturations.

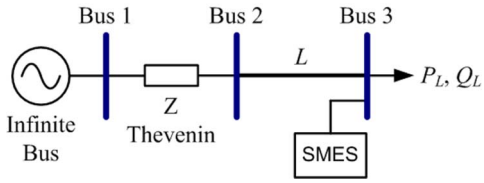


Fig. 7. Test power system with proposed SMES.

Fig. 7 depicts the single line diagram representing the test transmission system with the SMES unit. This basic three-bus power grid operates at 230 kV/50 Hz, and implements an 8.5-GW short circuit power level infinite bus through a Thevenin equivalent. A 120 MW/82 Mvar load modeled by constant impedances is connected to the grid via a 110-km power line. A 50 Mvar/86 MW/400 MJ SMES device is connected at bus 3. This SMES system is composed of a HTS coil with a total equivalent nominal inductance of 12 H operated at 30 K and a critical current of 4 kA. These SMES arrangement is capable of developing 96 MW (although restricted via control to 86 MW) and of storing 400 MJ when is fully charged. Major data of the test power system including the SMES unit are summarized in the Appendix.

For full performance studies, independent control of active and reactive powers exchanged between the SMES and the electric grid is carried out. To this aim, the SMES system is first evaluated during the SC charging process with an off-peak period in the power system, so that both the VCM and the CCM can be considered, as depicted in Fig. 8. In both control modes, the SC current is initially 500 A in the standby mode of operation and is forced to be increased to 750 A at $t = 0.1$ s for storing almost 14 MJ of energy, as shown in Fig. 8(a). In the VCM, given that the dc bus voltage must be kept constant at about 24 kV in order to allow an independent control of the active and reactive powers exchange, a slower charging response compared to the CCM is obtained. In the CCM, the SC current is forced to ramp up quickly to its maximum reference value independently of the dc bus voltage. Thus, the charging process can be greatly speeded up although the reactive power generated by the VSC is dependent on the active power being absorbing. As can be derived from Fig. 8(b), the charge time is reduced from 740 to 270 ms at the expense of a higher stress in the SC, as a consequence of having to support a larger voltage (around 45 kV), which is controlled at maximum permissible level. In addition, the power absorbed by the SC is augmented in the CCM, as depicted in Fig. 8(c), but the dc link capacitor voltages are balanced and controlled in a more efficient way. Fig. 8(d) and (e) shows the dc link capacitor voltages balance recovery transient during the charging process from $t = 0.1$ s as a consequence of activating the *NP* voltage control algorithm in the VCM and CCM control modes. As can be observed, the higher the stored current in the SC the greater the effect on the *NP* voltage equalization capability and then the faster the system recovers the dc link voltage balance. In both control modes, the proposed *NP* voltage balancing scheme ensures an effective transient voltage sharing between capacitors. Moreover, the dynamic response of

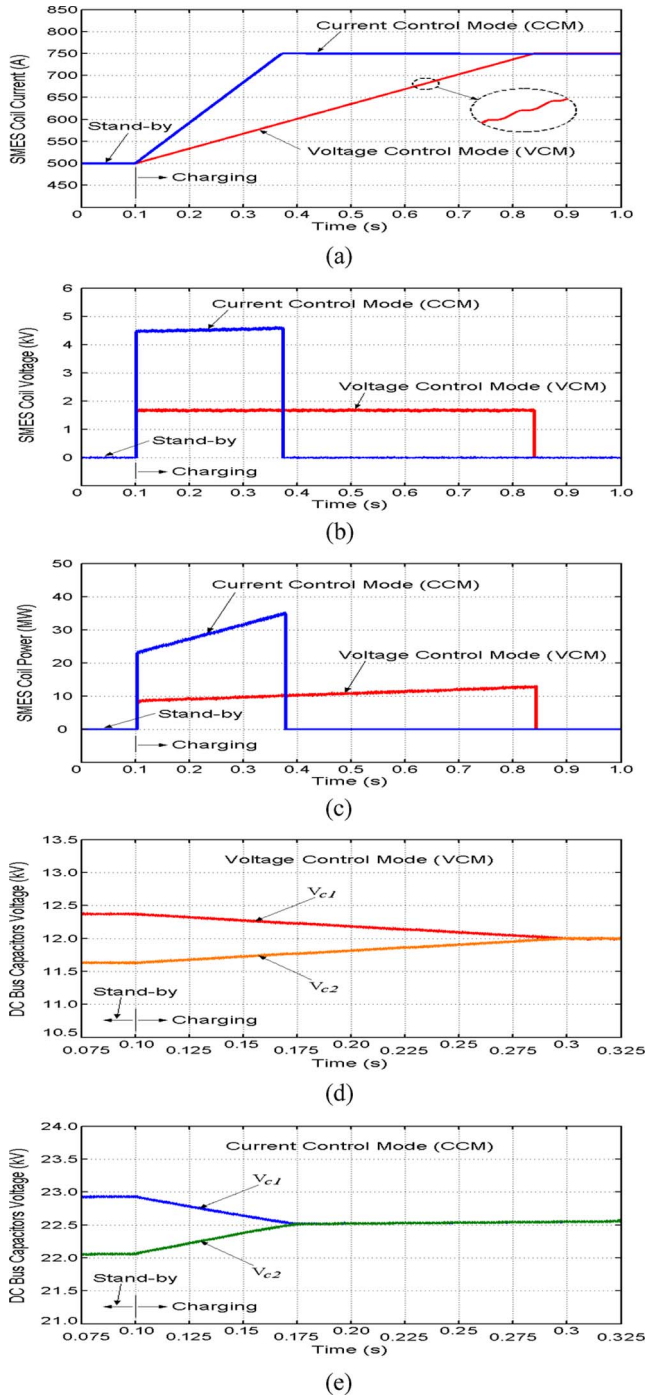


Fig. 8. SMES coil charging process with VCM and CCM. (a) SC current. (b) SC average voltage. (c) SC power. (d) DC link capacitors voltage in CCM. (e) DC link capacitors voltage in VCM.

the equalization method is better than that obtained with other alternatives proposed in the literature [25]–[27].

The full dynamic response in controlling the active power flow injected/absorbed by the SMES unit independently of the reactive power generated is now analyzed through the simulation results of Fig. 9. In this case, an active power command P_r is set to make step changes of 50 MW (maximum compensation

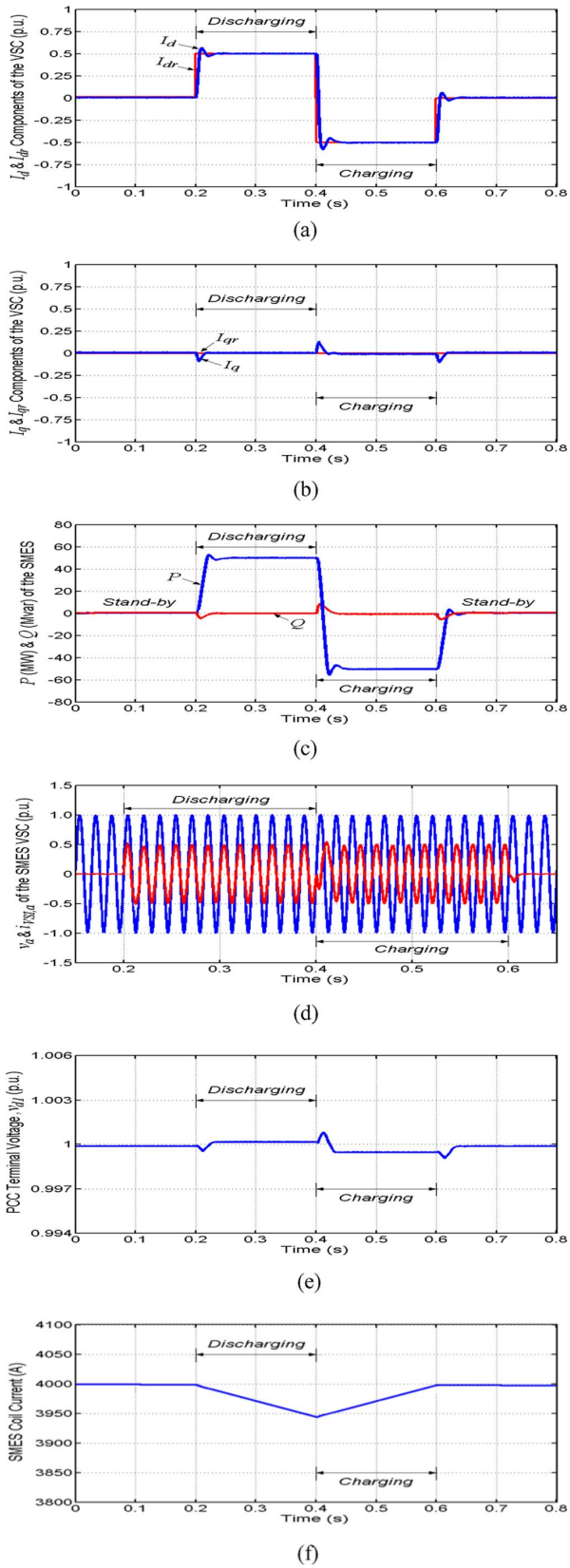


Fig. 9. Dynamic response of the proposed controller in active power control. (a) SMES VSC i_d components. (b) SMES VSC i_q components. (c) SMES P and Q. (d) SMES phase "a" V and I. (e) PCC terminal voltage. (f) SMES coil current.

active power set at 86 MW) during 200 ms as much in the discharge as in the charge modes of operation with the control scheme in VCM. Thus, an active power of approximately 40% of the active power demanded by the load is injected/absorbed by the SMES coil at bus 3 (PCC) while maintaining null the generated reactive power. As can be noted from actual and reference values of i_d and i_q shown in Fig. 9(a)–(c), only active power is rapidly exchanged with the utility system, in both discharge and charge modes of operation, independently of the reactive power. Since the SMES coil is initially fully charged at 4 kA, the dynamic response is excellent in both discharge/charge modes with the controller in VCM. When the SMES is sufficiently discharged (minimum operating current set at 200 A), the charging process can be quickly changed to the CCM so that the recovery of lost energy can be regained in the shortest possible time but with no control of the active power within this period. As can be seen from Fig. 9(c), there exists a very low transient coupling between the active and reactive powers exchanged by the SMES due to the full decoupled current control strategy in the synchronous-rotating *d–q* reference frame. Fig. 9(d) shows the phase "a" voltage at the PCC (bus 3), which is in-phase with the SMES VSC output current during the active power injection (discharge mode) and in opposite phase during the active power absorption (charge mode). This active power exchange produces slight changes in the terminal voltage v_{d1}, as seen in Fig. 9(e). The discharging and charging processes performed produce a variation of about 10.2 MJ of the energy stored in the SMES coil, which can be derived from the SC current response of Fig. 9(f).

The dynamic response in controlling the reactive power locally generated by the SMES VSC independently of the active power exchange is now studied through the simulation results of Fig. 10. In this case, as in the previous case study (with P) but now with Q, a reactive power command Q_r is set to make step changes of 50 Mvar (maximum compensation reactive power) during 200 ms as much in the capacitive as in the inductive modes of operation with the control scheme in VCM. Consequently, a reactive power of about 60% of the reactive power demanded by the load is generated capacitively/inductively by the SMES VSC at bus 3 (PCC) while maintaining null the exchanged active power. As can be noted from actual and reference values of i_d and i_q shown in Fig. 10(a)–(c), only reactive power is rapidly exchanged with the power grid, in both capacitive and inductive modes of operation, independently of the active power. For this operation, a conventional STATCOM with only reactive power control capabilities would be adequate [28]. However, the proposed SMES device with both active and reactive power capabilities allows performing a superior performance even with only reactive power generation, as compared to Fig. 10(c). In this way, the SMES coil is used for maintaining the required voltage at the STATCOM dc bus and for balancing the capacitors charge. This supplementary action allows enhancing the dynamic performance of the STATCOM and reducing the harmonics content generated in the VSC ac side. This is a consequence of the ripple reduction in the VSC dc link, which occurs as much in the charging as in the discharging processes of the

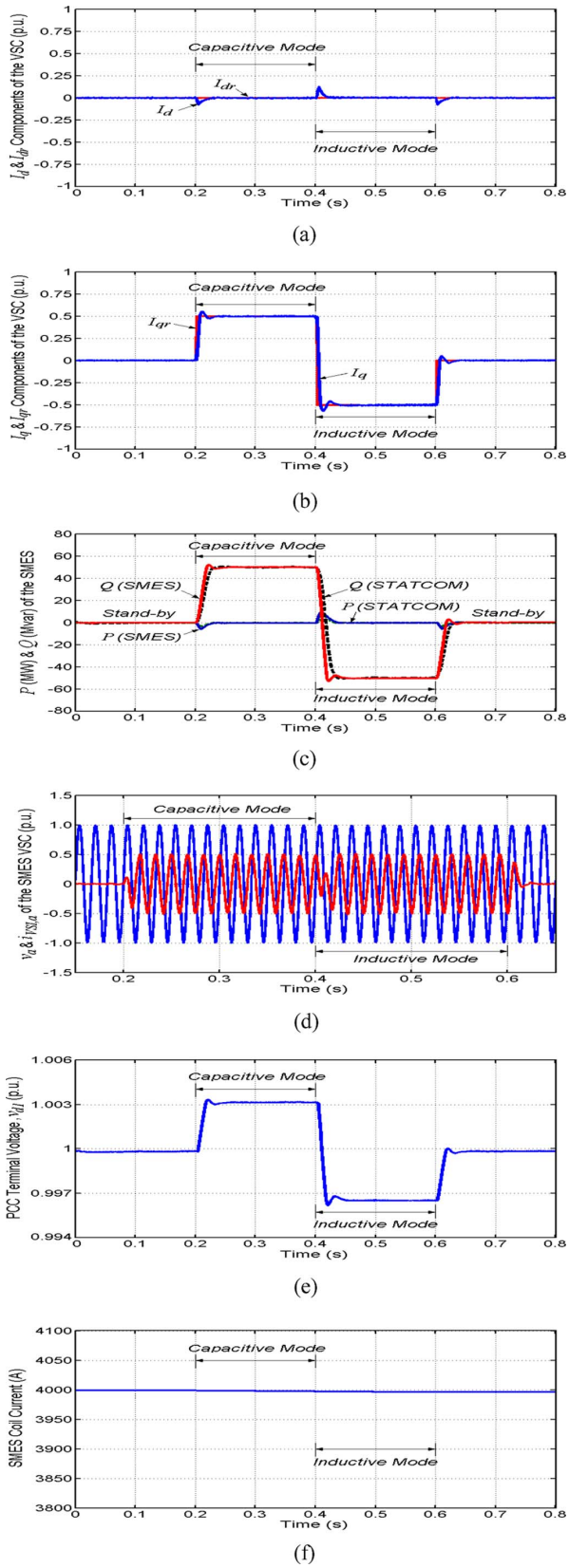


Fig. 10. Dynamic response of the proposed controller in reactive power control. (a) SMES VSC i_d components. (b) SMES VSC i_q components. (c) SMES P and Q. (d) SMES phase "a" V and I. (e) PCC terminal voltage. (f) SMES coil current.

SMES coil. In this case, the device is switched from the standby mode to the discharge mode for achieving the reactive power goals with a higher performance than the conventional STATCOM. As can be seen from Fig. 10(c), the decoupling characteristics between the active and reactive powers exchanged by the SMES are satisfactory because of the full decoupled current control strategy implemented in the *d–q* frame. Fig. 10(d) shows the phase "a" voltage at bus 3 (PCC), which is 90° phase shifted in lag with respect to the SMES VSC output current during the reactive power injection (capacitive mode) and quadrature phase shifted in lead during the reactive power absorption (inductive mode). This reactive power exchange greatly influences the terminal voltage v_{d1}, as seen in Fig. 10(e), contrary to former analyses (see Fig. 9). Thus, this approach allows quickly regulating the voltage at the PCC. This discharging process causes a slight variation of the energy stored in the SMES coil, which can be noted from the SC current response of Fig. 10(f).

Eventually, simulation results of Fig. 11 show the full dynamic response in controlling the active power flow injected/absorbed by the SMES unit simultaneously and independently of the reactive power (capacitive/inductive) locally generated. In this case, an active power command P_r is set to make step changes at maximum compensation active power of 86 MW during 200 ms as much in the discharge as in the charge modes of operation with the control scheme in VCM. At the same time, a reactive power command Q_r is set to make step changes at maximum compensation reactive power of 50 Mvar as much in the capacitive as in the inductive modes of operation. As can be observed from actual and reference values of i_d and i_q shown in Fig. 11(a)–(c), both active and reactive powers are effectively exchanged (simultaneously and independently) with the utility grid in a similar way as in previous studies. Moreover, at this maximum power compensation the current control strategy in *d–q* coordinates ensures full decoupled current and power control under all conditions. Since the SMES coil is fully charged, the dynamic response is outstanding in both discharge/charge and capacitive/inductive modes with the controller in VCM. Indeed, the active power can be provided by the SMES during approximately 0.92 s while reactive power can be constantly generated. The discharging and charging processes performed produce a change of around 20.6 MJ of the energy stored in the SMES coil, as can be noted from the SC current response of Fig. 11(d).

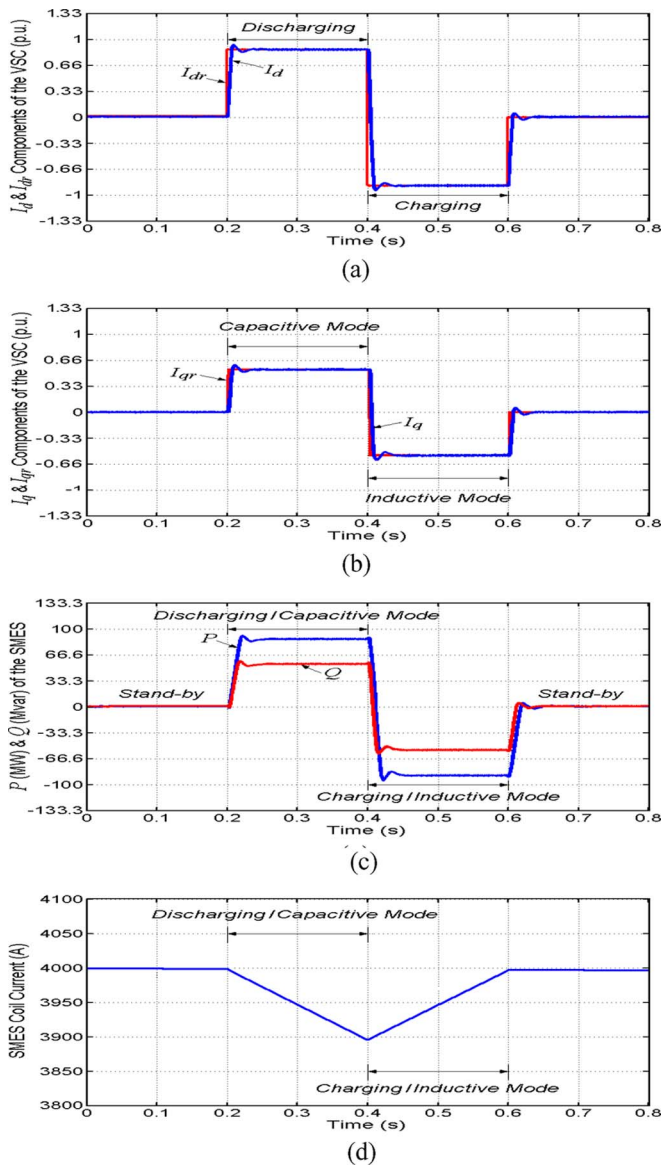


Fig. 11. Dynamic response of the proposed controller in simultaneous active and reactive power control. (a) SMES VSC i_d components. (b) SMES VSC i_q components. (c) SMES P and Q. (d) SMES coil current.

V. Preliminary Experimental Evaluation

In order to verify the actual performance of the proposed PCS of the SMES and its control scheme, a 3-kVA laboratory-scale prototype was designed and implemented. The VSC converter was built with insulated gate bipolar transistors (IGBTs) including reverse diodes and fast clamping diodes. These power electronics devices were chosen due to their low conduction and switching losses. The VSC was connected to the 50 Hz frequency utility grid at the 380 V line voltage level via four 95/60-V step-up coupling transformers. Since the SMES coil has a quite large inductance, its behavior was roughly emulated using a controlled 20-A dc current source. The bidirectional dc/dc converter interfacing the current source to the 80-V dc bus of the VSC was design to operate at 5 kHz and also built with IGBTs and fast diodes.

The proposed three-level control scheme was entirely implemented on a high-performance 32-bit fixed-point digital signal processor (DSP) TMS320F2812 of Texas Instruments operating at 150 MHz. This processor includes an advanced 12-bit analog-to-digital converter (ADC) with a fast conversion time which makes it possible real-time sampling with high accuracy and real-time *abc* to synchronous *d–q* frame coordinate transformation, so that the proposed multiobjective control block can be successfully carried out. The DSP was operated with a selected sample rate of 160 ksps and low-pass filters were implemented using fifth-order low-pass filters based on Sallen and

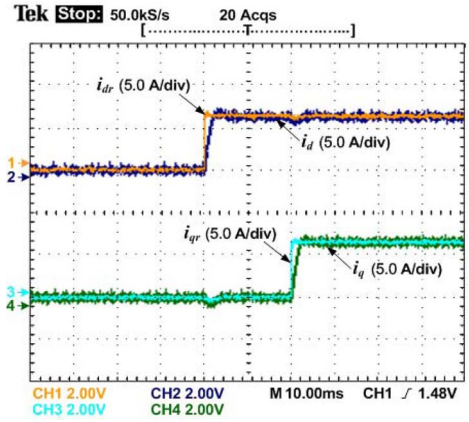


Fig. 12. SMES *d–q* coordinates actual output currents in the time domain for a step change in the active and reactive powers exchanged with the grid.

Key designs. The control pulses for the VSC and the chopper were generated by employing two DSP integrated pattern generators (event managers). The gate-driver board of the IGBTs was designed to adapt the wide differences of voltage and current levels with the DSP and to provide digital and analog isolation. All the source code was written in C++ by using the build-in DSP compiler.

The experimental results of the proposed controller in simultaneous active and reactive power control are shown in Fig. 12. DC time domain waveforms for the PCS prototype with step changes of approximately 500 W and 500 var are provided. As can be noted, the independent nature of the control is evident since the change in the output direct current of around 6.25 A (providing the active power) causes a small response in the quadrature output current (giving the reactive power) and vice versa. Moreover, these results of small-scale experiments obtained are in good agreement with the previous simulated results of Fig. 11. Nevertheless, some differences would be expected with a noisy environment of real high-voltage high-power SMES systems. Further performance tests will be carried out with a real higher capacity HTS SMES prototype being currently developed.

VI. Conclusion

A novel power conditioning system of a SMES unit to simultaneously and independently control active and reactive power flows in the transmission network level, and its controller has been studied and implemented in this paper. The use of a three-phase three-level pseudo 48-pulse ETO voltage source converter coupled with a two-quadrant three-level ETO dc/dc converter as interface with the SMES coil allows charging and discharging in a fast and very controlled manner, and to implement an effective balancing technique of the dc link capacitors. Moreover, a real detailed full model of the SMES unit and a new three-level control scheme have been proposed, comprising a full decoupled current control strategy in the *d–q* reference frame with the novel controller to prevent dc bus capacitors voltage drift/imbalance. The dynamic performance of the proposed systems has been fully validated by digital simulations. The results show that the novel multilevel control scheme ensures fast controllability and minimum oscillatory behavior of the SMES operating in the four-quadrant modes, which enables to effectively increase the transient and dynamic stability of the power system.

Appendix

See Tables II–V.

TABLE II
Power System Parameters

Three-phase ac source				Transmission line				Load	
Rated voltage (kV)	Freq. (Hz)	S.C. level (GW)	X/R	L (km)	R (p.u.)	X (p.u.)	B (p.u.)	P_L (MW)	Q_L (Mvar)
230	50	8.5	10	110	0.022	0.123	0.294	120	82

TABLE III
SMES System Data

Coupling transformers			VSC			Chopper and SMES coil			
S_{max} (MVA)	Prim. Voltage (kV)	Sec. voltage (kV)	Q_{max} (Mvar)	V_d (kV)	C_{d1}, C_{d2} (mF)	P_{max} (MW)	$E_{SC,max}$ (MJ)	$I_{SC,max}$ (kA)	$V_{SC,max}$ (kV)
100	230	18	50	24	10	96	400	4	50

TABLE IV
SMES Coil Model Data

# Seg.	L_i (H)	M_{ij} (H)	C_{Si} (μF)	C_{Shi} (μF)	R_{pi} (Ω)	R_p (Ω)	C_{S1}, C_{S2} (μF)	R_{g1}, R_{g2} (kΩ)	C_F (μF)
6	8.334	3.12	0.01	0.488	0.05	5	1.1	27.5	6

TABLE V
SMES Controller Parameters

External level data				Internal level data				Internal level data
K_Q	K_P	K_p PLL	K_I PLL	K_{p1}, K_{p2}	K_{I1}, K_{I2}	K_{p3}	K_{I3}	σ (°)
1e-8	1e-8	60	1400	5	40	0.01	65	172.5

References

[1] A. Battaglini, J. Lilliestam, A. Haas, and A. Patt, "Development of Supersmart grids for a more efficient utilisation of electricity from renewable sources," *J. Cleaner Prod.*, vol. 17, no. 10, pp. 911–918, 2009.

[2] P. Pourbeik, P. S. Kundur, and C. W. Taylor, "The anatomy of a power grid blackout—Root causes and dynamics of recent major blackouts," *IEEE Power Energy Mag.*, vol. 4, no. 5, pp. 22–29, Sep./Oct. 2006.

[3] J. G. Slootweg and W. L. Kling, "The impact of large scale wind power generation on power system oscillations," *Electr. Power Syst. Res.*, vol. 67, no. 1, pp. 9–20, 2003.

[4] P. Pourbeik, M. Bahrman, E. John, and W. Wong, "Modern countermeasures to blackouts," *IEEE Power Energy Mag.*, vol. 4, no. 5, pp. 36–45, Sep./Oct. 2006.

[5] A. B. Arsoy, Y. Liu, P. F. Ribeiro, and F. Wang, "STATCOM-SMES," *IEEE Ind. App. Mag.*, vol. 9, no. 2, pp. 21–28, Mar./Apr. 2003.

[6] R. H. Lasseter and S. G. Lalali, "Power conditioning systems for superconductive magnetic energy storage," *IEEE Trans. Energy Convers.*, vol. 6, no. 3, pp. 381–387, Sep. 1991.

[7] R. H. Lasseter and S. J. Jalali, "Dynamic response of power conditioning systems for superconductive magnetic energy storage," *IEEE Trans. Energy Convers.*, vol. 6, no. 3, pp. 388–393, Sep. 1991.

[8] I. D. Hassan, R. M. Bucci, and K. T. Swe, "400-MW SMES power conditioning system development and simulation," *IEEE Trans. Power Electron.*, vol. 8, no. 3, pp. 237–249, Jul. 1993.
[9] B. M. Han and G. G. Karady, "A new power conditioning system for superconducting magnetic energy storage," *IEEE Trans. Energy Convers.*, vol. 8, no. 2, pp. 214–220, 1993.
[10] M. G. Molina, P. E. Mercado, and E. H. Watanabe, "Dynamic performance of a static synchronous compensator with superconducting magnetic energy storage," in *Proc. IEEE Power Electron. Spec. Conf.*, Jun. 2005, pp. 224–230.
[11] L. Chen, Y. Liu, A. B. Arsoy, P. F. Ribeiro, M. Steurer, and M. R. Iravani, "Detailed modeling of superconducting magnetic energy storage (SMES) system," *IEEE Trans. Power Del.*, vol. 21, no. 2, pp. 699–710, Jun. 2006.
[12] X. P. Zhang, C. Rehtanz, and B. Pal, *Flexible AC Transmission Systems: Modelling and Control (Power Systems)*, 2nd ed. Berlin, Germany: Springer-Verlag, 2009.
[13] H. Hayashi, Y. Hatabe, T. Nagafuchi, A. Taguchi, K. Terazono, T. Ishii, and S. Taniguchi, "Test results of power system control by experimental SMES," *IEEE Trans. Appl. Supercond.*, vol. 16, no. 2, pp. 598–601, Jun. 2006.
[14] J. Holtz, "Pulsewidth modulation—a survey," *IEEE Trans. Ind. Electron.*, vol. 39, no. 5, pp. 410–420, Oct. 1992.
[15] J. Rodriguez, J. S. Lai, and F. Z. Peng, "Multilevel inverters: A survey of topologies, controls, and applications," *IEEE Trans. Ind. Electron.*, vol. 49, no. 4, pp. 724–738, Aug. 2002.
[16] J. S. Lai and F. Z. Peng, "Multilevel converters-a new breed of power converters," *IEEE Trans. Ind. Appl.*, vol. 32, no. 3, pp. 509–517, 1996.
[17] D. Soto and T. C. Green, "A comparison of high-power converter topologies for the implementation of FACTS controllers," *IEEE Trans. Ind. Electron.*, vol. 49, no. 5, pp. 1072–1080, Oct. 2002.
[18] M. V. Aware and D. Sutanto, "SMES for protection of distributed critical loads," *IEEE Trans. Power Del.*, vol. 19, no. 3, pp. 1267–1275, Jul. 2004.
[19] M. H. Ali, T. Murata, and J. Tamura, "Transient stability enhancement by fuzzy logic-controlled SMES considering coordination with optimal reclosing of circuit breakers," *IEEE Trans. Power Syst.*, vol. 23, no. 2, pp. 631–640, May 2008.
[20] M. Steurer and W. Hribernik, "Frequency response characteristics of a 100-MJ SMES coil–measurements and model refinement," *IEEE Trans. Appl. Supercond.*, vol. 15, no. 2, pp. 1887–1890, Jun. 2005.
[21] M. V. Aware and D. Sutanto, "Improved controller for power conditioner using high-temperature superconducting magnetic energy storage (HTS-SMES)," *IEEE Trans. Appl. Supercond.*, vol. 13, no. 1, pp. 38–47, Mar. 2003.
[22] M. G. Molina, P. E. Mercado, and E. H. Watanabe, "Static synchronous compensator with superconducting magnetic energy storage for high power utility applications," *Energy Convers. Manage.*, vol. 48, no. 8, pp. 2316–2331, 2007.
[23] S. Dechanupaprittha, K. Hongesombut, M. Watanabe, Y. Mitani, and I. Ngamroo, "Stabilization of tie-line power flow by robust SMES controller for interconnected power system with wind farms," *IEEE Trans. Appl. Supercond.*, vol. 17, no. 2, pp. 2365–2368, Jun. 2007.
[24] *SimPowerSystems for Use With Simulink: User's Guide*, The MathWorks, Inc., Natick, MA, updated version for Simulink 7.3, 2009..
[25] A. Von Jouanne, S. Dai, and H. Zhang, "A multilevel inverter approach providing DC-link balancing, ride-through enhancement, and common-mode voltage elimination," *IEEE Trans. Ind. Electron.*, vol. 49, no. 4, pp. 739–745, Aug. 2002.
[26] S. Busquets-Monge, J. D. Ortega, J. Bordonau, J. A. Beristain, and J. Rocabert, "Closed-loop control of a three-phase neutral-point-clamped inverter using an optimized virtual-vector-based pulsewidth modulation," *IEEE Trans. Ind. Electron.*, vol. 55, no. 5, pp. 2061–2071, May 2008.
[27] G. P. Adam, S. J. Finney, A. M. Massoud, and B. W. Williams, "Capacitor balance issues of the diode-clamped multilevel inverter operated in a quasi two-state mode," *IEEE Trans. Ind. Electron.*, vol. 55, no. 8, pp. 3088–3099, Aug. 2008.
[28] M. S. El-Moursi and A. M. Sharaf, "Novel controllers for the 48-pulse VSC STATCOM and SSSC for voltage regulation and reactive power compensation," *IEEE Trans. Power Syst.*, vol. 20, no. 4, pp. 1985–1997, Nov. 2005.

Marcelo Gustavo Molina (S'01–M'05) was born in San Juan, Argentina. He received the Graduate degree in electronic engineering and the Ph.D. degree from the National University of San Juan (UNSJ), San Juan, Argentina, in 1997 and 2004, respectively.

In 2004, he was a Doctoral Research Fellow at the Federal University of Rio de Janeiro, Brazil, supported by CAPES. From 2005 to 2007, he worked as a Postdoctoral Research Fellow at the Argentinean National Council for Science and Technology Research (CONICET), UNSJ. In 2009, he was a Visiting Professor at the University of Siegen, Germany, sponsored by Deutscher Akademischer Austausch Dienst, and in 2010 at the Federal University of Rio de Janeiro, Brazil, supported by CAPES. Since 2004, he has been an Associate Professor at the UNSJ and a Researcher at the CONICET. His research interests include new energy technologies, simulation methods, power systems dynamics and control, power electronics modeling and design, renewable energy resources, and the application of energy storage in power systems.

Dr. Molina is a member of the IEEE Power Engineering Society and the IEEE Power Electronics Society.

Pedro Enrique Mercado (M'02–SM'02) was born in San Juan, Argentina. He received the graduate degree in electromechanical engineering from the National University of San Juan (UNSJ), San Juan, and the Ph.D. degree from the Aachen University of Technology, Aachen, Germany.

He is currently a Professor of Electrical Engineering at the UNSJ, and a Researcher at the Argentinean National Council for Science and Technology Research. His research interests include operation security, power electronics, renewable energy systems, and economic operation, and control of electric power systems.

Dr. Mercado is a Senior Member of the IEEE Power Engineering Society and the IEEE Power Electronics Society.

Edson Hirokazu Watanabe (M'76–SM'02) was born in Rio de Janeiro, Brazil. He received the B.Sc. and M.Sc. degrees both in electronic engineering from the Federal University of Rio de Janeiro (UFRJ), Rio de Janeiro, in 1975 and 1976, respectively, and the, the D.Eng. degree from the Tokyo Institute of Technology, Tokyo, Japan, in 1981.

In 1981, he was an Associate Professor in the National Council of Scientific and Technical Research, UFRJ, where he became a Professor in 1993. He teaches power electronics. His research interests include converter analysis, modeling and design, ac and dc drives, and theory and application of active power filters and FACTS technologies.

Dr. Watanabe is a member of the IEE Japan, the Brazilian Society for Automatic Control, the Brazilian Power Electronics Society and a member of the IEEE Power Electronics, Industrial Applications, Power Engineering, and Industrial Electronics Societies.