Evaluating the Effects of Combined Total Ionizing Dose Radiation and Electromagnetic Interference

J. Benfica, L. M. Bolzani Poehls, F. Vargas, J. Lipovetzky, A. Lutenberg,
S. E. García, E. Gatti, F. Hernandez

***Abstract*—Although measurement methods for Electromagnetic (EM) immunity and Total Ionizing Dose (TID) radiation are highly standardized, no effort has been made to evaluate the behavior of embedded systems under the combined effects. Considering realistic environment conditions only the measurement of these effects can guarantee reliable embedded systems for critical applications. A configurable platform to evaluate the effects of TID radiation and EM Interference (EMI) on embedded systems is presented. Experiments illustrate the consequences regarding delay and fault occurrence probability as well as current consumption and minimum power supply.**

***Index Terms*—Electromagnetic Immunity, Total Ionizing Dose Radiation, Embedded Systems.**

I. Introduction

WITH the widespread use of wireless technology-based embedded systems, the environment in which systems for critical applications have to operate has become increasingly hostile. Moreover, technology scaling continuously decreases the Integrated Circuit's (IC) supply voltage, reducing the noise margins and consequently increasing the circuit's susceptibility to Electromagnetic Interference (EMI) [1], which can cause transient faults and thereby reduces the system's reliability [2]. Furthermore, reliability under Total Ionizing Dose (TID) radiation is very important for military, aerospace or biomedical applications. TID increases the leakage currents and causes changes in current-voltage characteristics, causing functional failures due to the noise margin's and the propagation delay's variation. For very high doses, functional failures can be observed [3]. Up to now, these concerns have been treated as independent events, never taking into account the combined effects of the two issues. In more detail, assuming that a critical-safety embedded system has been certified by a set of experiments performed according to international standards related to EM immunity only. After a period of time operating exposed to a certain level of TID radiation, it will not be possible to guarantee that the system will still work properly. It is to be assumed, that the same assumption holds true for the TID radiation certified systems after operating in an environment with EM irradiation.

In this context, the always increasing level of noise in the environment has changed the scenario related to the design of reliable embedded systems. Nowadays, it is crucial to evaluate the behavior of these systems when exposed to EM noise as well as to TID radiation. Thus, the main goal of this paper is to present a configurable platform that allows the performance of combined tests of EM immunity and TID radiation for embedded systems to deal with the before mentioned issue. The platform attends the international standards for measurements on integrated circuits and embedded systems: (1) IEC 62.132-2, for radiated EM noise [4], (2) IEC 61.000-4-17 and (3) IEC 61.000-4-29, both for conducted EM noise [8] [9] and finally, (4) the 1019.8 method for TID Test Procedure of MIL-STD-883H [5].

The paper has been organized as follows: Section II summarizes the platform is described in details. Section III presents the experimental setup and Section IV the obtained results. Finally, in Section V we draw the conclusions.

II. Platform

In order to deal with the previously mentioned issue, a hardware platform has been developed. The platform's hardware is composed of two boards. Fig. 1 depicts the board dedicated to TID experiments and Fig. 2 the board adopted during the EM immunity tests. In more detail, Fig. 1a depicts the top side of the 6-layer board. The bottom side of the board dedicated to the TID experiment is shown in Fig. 1b. It is important to mention that the 6-layer board is placed inside the vacuum chamber of the Gamma Cell. Finally, Fig 2.a shows the top side of the 8-layer board for EM immunity tests and Fig. 2b its bottom side. Thus, the 6-layer board previously mentioned is dedicated to perform the 1019.8 method for TID test procedure according to the MIL-STD-883H standard [5]. Regarding the 8-layer board shown in Fig. 2, two different types of EM immunity evaluations can be performed:

- *Radiated Noise Immunity Test*: This type of experiment is performed in a Gigahertz Transverse Electromagnetic Cell (GTEM Cell) according to the IEC 62.132-2 standard [4].

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J. Benfica, L. M. Bolzani Poehls and F. Vargas are with the Catholic University of Rio Grande do Sul (PUCRS), Av. Ipiranga 6681, 90619-900, Porto Alegre, Brazil (e-mail: leticia@poehls.com).

J. Lipovetzky, A. Lutenberg, S. E. García are with Universidad de Buenos Aires, Buenos Aires, Argentina.

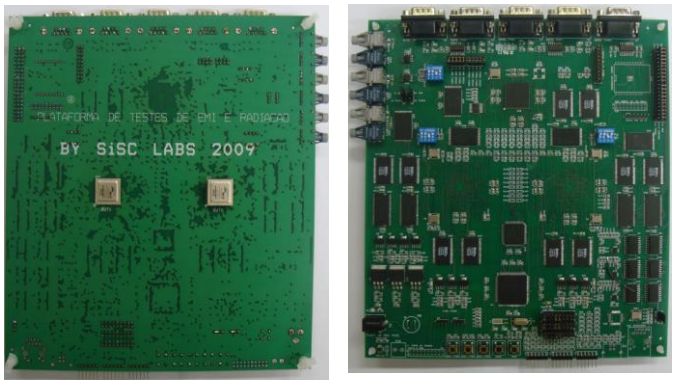
E. Gatti is with Instituto Nacional de Tecnologia Industrial (INTI), Buenos Aires, Argentina.

F. Hernandez is with Universidad ORT, Montevideo, Uruguay.

- *Conducted Noise Immunity Test:* This type of experiment is performed according to the IEC 61.000-4-17 standard for ripple power supply lines [8] and IEC 61.000-4-29 standard for voltage dips, voltage variations and short interruptions on the DC port of the electronic system [9].

(a) (b)

Fig. 1. Hardware Platform for TID radiation tests: (a) top and (b) bottom side of the 6-layer board.



(a) (b)

Fig. 2. Hardware Platform for EM immunity tests: (a) top and (b) bottom side of the board.

It is important to note that the most important component of both boards is the Xilinx Virtex 4 FPGA with the part number XC4VFX12-10SF363, used to map the System-on-Chip (SoC) under test. Further, an ARM7 processor, able to generate the Power Supply Disturbances (PSD) according to the two previously mentioned IEC standards for conducted noise immunity test and capable of monitoring the system during the execution of both EM immunity evaluations, is integrated on the 8-layer board. Thus, the platform is designed to evaluate different applications under one test condition related to TID radiation and two regarding EM immunity, respectively. In more detail, the three tests the platform is considering are: (1) TID Radiation Test (TIDRT), (2) Radiated Noise Immunity Test (RNIT) and (3) Conducted Noise Immunity Test (CNIT). Specific software developed to be used with the platform allows configuring and monitoring the test procedures at all time [6].

Finally, to execute the combined test, the FPGA under test is mounted on the 6-layer board and the TID radiation tests are performed. The radiated FPGA then is removed and fixed on the 8-layer board. On its second socket, a not-irradiated FPGA is mounted, to be used as Gold Reference and the EM immunity tests are performed. Figure 3 depicts the structure adopted to mount the FPGA under test on both boards.

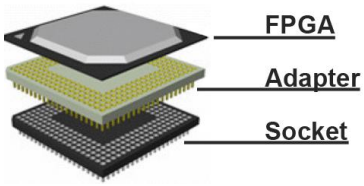


Fig. 3. Structure adopted to mount the FPGA on the two boards.

III. Experimental Setup

In order to evaluate the combined effects of TID radiation and EMI on embedded systems, a set of experiments has been performed according to the flow diagram presented in Fig. 4.

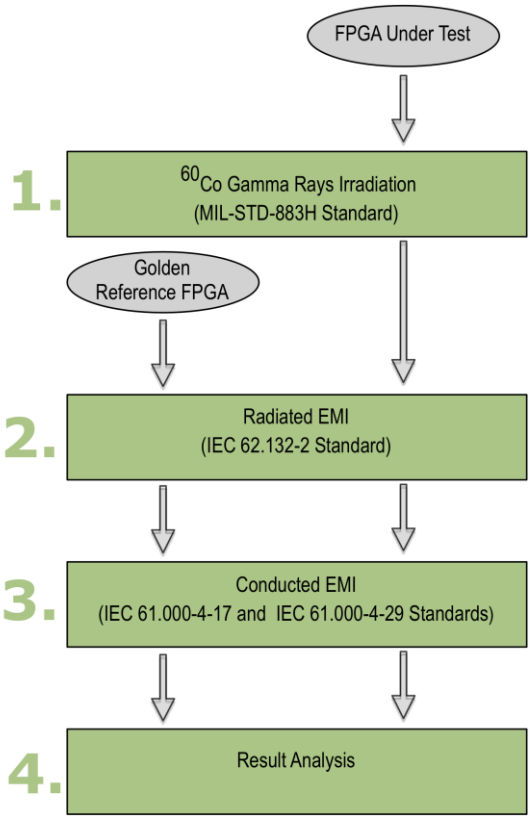


Fig. 4. Flow diagram of the experiments performed in order to evaluate the combined effects of TID radiation and EMI.

In more detail, four Virtex-4 (XC4VFX12-10SF363) FPGAs from the same lot have been irradiated using ^{60}Co gamma rays source in different doses in *Step 1*. The gamma ray irradiations have been performed following the standardized 1019.8 method for TIDRT of the MIL-STD-883H standard. The radiation source used during these experiments is the Gamma Cell shown in Fig. 5. Basically, the Gamma Cell allows a uniform irradiation of the samples when they are physically placed on known isodose surfaces. It is important to highlight that irradiations have been performed at

room temperature and with a dose rate of 0.75rads/s [7]. Silver-chromate dosimeters have been employed to measure the TID [10]. To evaluate how different levels of TID affect the FPGA's EM immunity, four different FPGAs mounted on the 6-layer boards have been irradiated to a wide span of doses, from 5krads to 325krads covering almost two orders of magnitude of total doses. Several works report that FPGAs fabricated in deep-submicron CMOS processes can withstand TID levels of a few hundreds of krads [11] [12] [13].

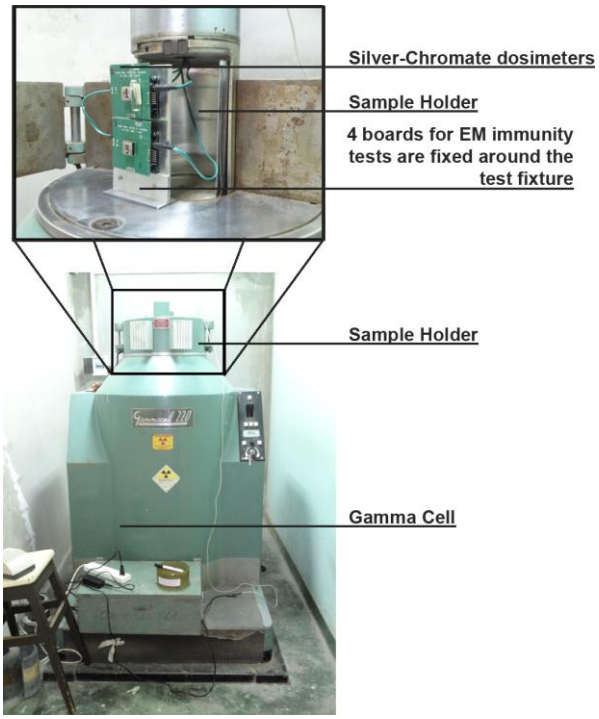


Fig. 5. Gamma rays radiation source used during the experiments (Centro Atómico Ezeiza, from the Comisión Nacional de Energía Atómica, Argentina).

In *Step 2*, the FPGAs exposed to different doses of TID radiation are submitted to Radiated EMI. In more detail, these FPGAs are mounted on the 8-layer board which is placed inside the shielding box which itself is inserted into the Gigahertz Transversal Electromagnetic Mode (GTEM) Cell, shown in Fig. 6. Specifically, the RNITs have been performed in the GTEM cell of the *Instituto Nacional de Tecnología Industrial (INTI)*, in Buenos Aires, Argentina. Test conditions according to the IEC 62.132-2 standard have been adopted. In more detail, the conditions can be stated as follows:

- *EM field range:* from 10 to 220 volts/meter;
- *Radiated signal frequency range:* [150KHz - 3GHz] (extended IEC 62.132-2);
- *Signal modulation format:* AM/FM 80%.

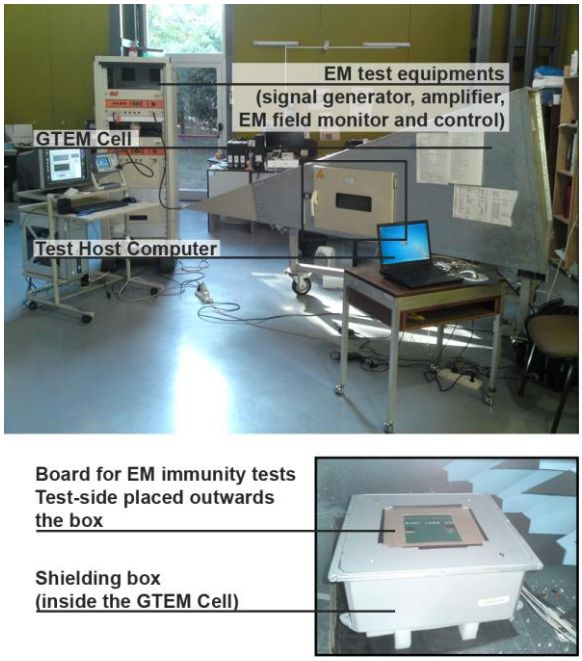


Fig. 6. Environment for RNIT.

In *Step 3* of the flow diagram presented in Fig. 4, CNITs have been performed in order to understand how TID radiation can affect the susceptibility of the FPGA when voltage dips according to IEC 61.000-4-29 are injected to the supply line of the FPGA under test. Fig. 7 shows the waveform of the applied voltage dips in more detail. It is important to note that in order to measure the FPGAs' degree of susceptibility, we step-by-step decreased the nominal V_{dd} from 1.2 volts until observing an erroneous output.

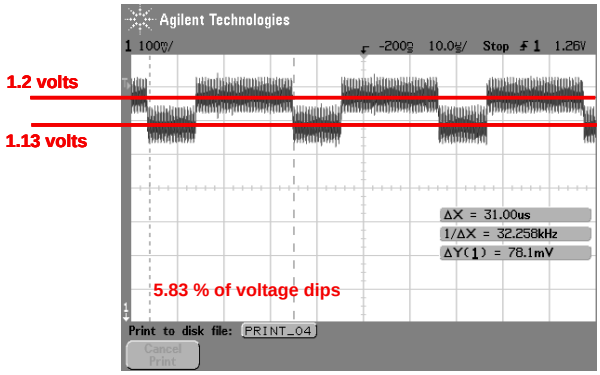


Fig. 7. Print screen: Oscilloscope for the conducted EMI injected in the FPGAs power supply pins according to the IEC 61.000-4-29.

Finally, in *Step 4* of the flow diagram the results obtained are analyzed.

It is important to highlight that depending on the experiments purpose, radiated and conducted EMI experiments are immediately performed using the FPGAs already exposed to gamma rays irradiation. Alternatively, test engineers may prefer to apply worst-case bias conditions to the FPGAs during a given period of time for post irradiation anneals [10] before performing EM immunity measurements.

In the latter case, it is worth remarking that special care has to be taken to ensure that all the samples will hold similar anneal times between the end of the TID irradiation and the beginning of the EM immunity tests. This will ensure that the different EM test results observed in the different FPGAs are due to TID level variations and not to different anneal times.

IV. Experimental Results

In this section, the case study adopted during the experiments and the results obtained during *Step 1*, *Step 2* and *Step 3* of the flow diagram depicted in Fig. 4 are presented. It is important to note that the results obtained regarding the four FPGAs exposed to TID radiation and EM immunity tests are compared to the results obtained from the non-irradiated FPGA, called Golden Reference.

In order to evaluate the platform, a Case Study composed of a SoC based on a Plasma microprocessor running a 10x10 Matrix Multiplication (MM) code has been used for the experimental evaluation procedure. In addition to the microprocessor, a chain containing 10,000 inverters has been designed.

The MM code has been stored in the FPGA's internal block Random Access Memories (RAMs). Additionally, the inverter's chain input and output have been directly connected to the FPGA I/O pins to allow precise measurement of the relation between TID radiation and delay. Thus, the gamma cell depicted in Fig. 5 has been adopted during *Step 1* of the experiments' flow diagram. This experiment followed the standardized 1019.8 method and has been applied at room temperature with a dose rate of 0.75 rads/s. To achieve different radiation doses, the FPGAs under test remained under radiation for different time periods. In more detail, the FPGA1 remained for few hours, while the FPGA4 was under radiation for five days. Silver-chromate dosimeters have been used to measure the TID. Thus, four FPGAs have been configured and submitted to different doses of TID radiation as summarized in Table I. It is important to point out, that FPGA0 is the reference device that not has been irradiated and consequently is the Golden Reference.

TABLE I. TID deposited on the four FPGAs

FPGA0 [krads]	**FPGA1 [krads]***	**FPGA2 [krads]***	**FPGA3 [krads]***	**FPGA4 [krads]***
0	5.6	51.9	111.0	216.0

** dose rate: 0.75 rads/s*

After finishing *Step 1*, two hours after stopping the radiation process, the delay of the inverter's chain has been measured for each FPGA in order to define the relation between TID and delay.

In *Step 2*, the FPGAs have been exposed to radiated EMI and the number of faults occurring in the Plasma microprocessor running the MM code has been measured. This measurement has been performed using the board depicted in Fig. 2 placed on the shielding box, inside the GTEM cell, as depicted in Fig. 6. The five FPGAs have been exposed to radiated EMI during a period of 8 hours. These experiments have been performed in compliance with the IEC international 62.132-2 standard. The faults observed in the Plasma microprocessor, when running the MM code under EMI, have been classified in hardware and software faults. While the former type of faults refers to those affecting the logic used to configure the FPGA, the latter one represents the number of faults corrupting the MM code execution. It is important to note that faults affecting the FPGA configuration logic have been detected by performing the *readback* operation of the component.

In *Step 3*, the susceptibility of the core to voltage dips applied to the power supply line has been evaluated. In more detail, the minimum core power supply voltage (V_{dd}) necessary to guarantee the proper functionality of the FPGAs running the MM code has been measured. The experiment features fault injection campaigns that have been performed according to the IEC 61.000-4-29 international standard by applying voltage dips to the core V_{dd} pins of the four irradiated FPGAs as well as to the Golden Reference. The nominal core V_{dd} is of 1.2 volts. During the experiment, voltage dips have been injected into the FPGA's V_{dd} pins at a frequency of 25.68 kHz.

V. Result Analysis

The results obtained during the experiments' different steps are presented and analyzed in the next paragraphs.

Fig. 8 depicts the results regarding the delay of the 5 FPGAs that have been exposed to different TIDs. It is easily observed that the delay is monotonically increasing with the increase of TID radiation. FPGA4 shows a 132% higher delay then the not-irradiated one.

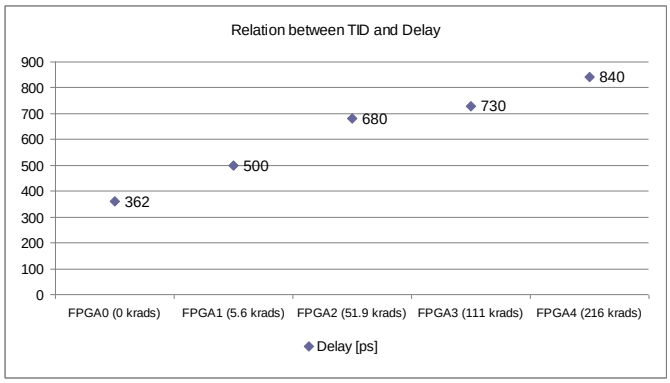


Fig. 8. Experimental result showing the relation between radiated dose and delay.

Fig. 9 shows the relation between TID and current consumption considering the nominal V_{dd} of 1.2 volts. The results illustrated in this figure demonstrate that the current consumption constantly increases in function of the TID the FPGA has been exposed to. In more detail, the Golden Reference consumed 73.4mA while FPGA4 consumed 87.2mA.

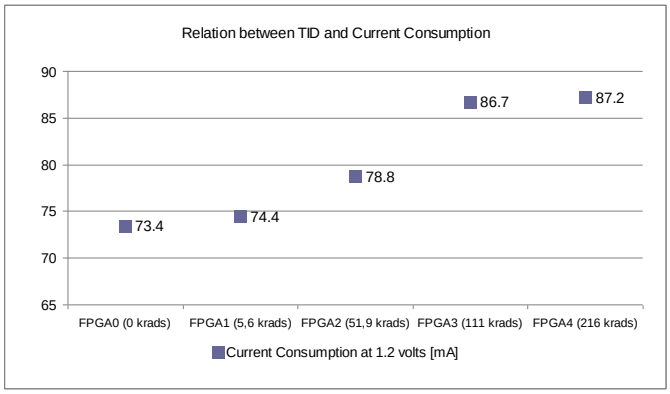


Fig. 9. Experimental result showing the relation between radiated dose and current .

Fig. 10 shows the relation between TID and fault occurrence observed during RNIT.

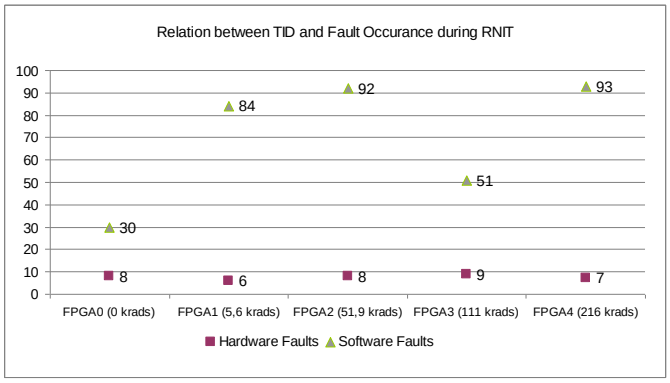


Fig. 10. Experimental result showing the relation between radiated dose and fault occurrence observed during RNIT.

The FPGA0 has been affected by 38 faults, while the four irradiated FPGAs demonstrate an average of about 88 fault occurrences. It is important to note that concerning the 38 faults observed in FPGA0, 30 have been categorized as software faults affecting user data registers and 8 have been identified as hardware faults affecting the FPGA0's configuration registers. Further, the delay increases only the occurrence of software faults, since the number of faults affecting the FPGA hardware part remains approximately constant, independent from the TID level that is deposited on the components. In average, about 8 hardware faults have been observed in all FPGAs.

Finally, Fig. 11 illustrates the relation between TID and power supply voltage. In more detail, the susceptibility of the FPGA related to PSD has been measured performing experiments according to the IEC 61.000-4-29.

Observing the results plotted in the graph, it is possible to conclude that the irradiated FPGAs require a higher power supply to work fault-free. In detail, the FPGA0 tolerated a minimum value of 0.90 volts, which means a voltage dip of about 25%. However, considering FPGA4, exposed to the highest radiation dose, it is possible to observe that the minimal acceptable V_{dd} is limited to 1.06 volts, which represents a voltage dip of about 11,67% with respect to the nominal V_{dd} of the core. In other words, the radiation made the FPGA more then twice as sensible to voltage dips. It should be noted that the value for the four radiated FPGAs differs only very slightly, between 1.06 and 1.08 volts, and we can therefore conclude that the minimum V_{dd} necessary for the irradiated FPGAs to run properly is independent from the accumulated radiation dose.

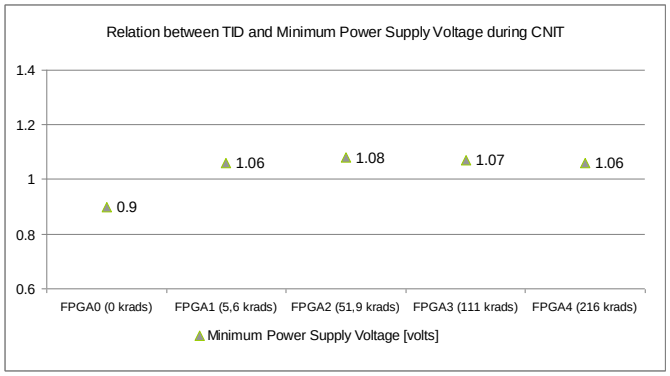


Fig. 11. Experimental results showing the relation between radiated dose and the minimum power supply voltage observed during CNIT.

VI. Conclusions

The performed combined tests demonstrate that TID radiation increases the delay, which may lead to functional faults due to the fact that the FPGA running the application does not meet its timing constraints. Further the experiments demonstrate that the power consumption increases with the radiation dose applied to the FPGA.

The results prove that the evaluation of EM immunity alone does not guarantee a reliable execution of the FPGA's functionality in the harsh environment to be expected today. It is important to highlight, that the reliability of safety-critical applications has to be guaranteed in a near-realistic environment. Therefore the evaluation of the combined effects of TID radiation and EMI is the only solution to correctly foresee the reliability of an FPGA.

In more detail, the presented experiments are able to evaluate such combined effects. They show that the fault occurrence for FPGAs subject to TID radiation and EMI are significantly higher then for FPGAs that suffered EMI only. Further, the combined effects of TID radiation an EMI caused a higher susceptibility towards voltage dips. The FPGAs exposed to TID radiation and EMI needed a substantially higher minimum supply voltage to function properly.

Consequently, the evaluation of EM immunity alone is not able to represent the environment to be expected today; only a combined test can guarantee realistic predictions for the embedded system's reliability.

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