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DC Fault Identification in Multiterminal HVDC Systems Based on Reactor Voltage Gradient

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ABSTRACT With the increasing number of renewable generations, the prospects of long-distance bulk power transmission impels the expansion of point-to-point High Voltage Direct Current (HVDC) grid to an emerging Multi-terminal high-voltage Direct Current (MTDC) grid. The DC grid protection with faster selectivity enhances the operational continuity of the MTDC grid. Based on the reactor voltage gradient (RVG), this paper proposes a fast and reliable fault identification technique with precise discrimination of internal and external DC faults. Considering the voltage developed across the modular multilevel converter (MMC) reactor and DC terminal reactor, the RVG is formulated to characterise an internal and external DC fault. With a window of four RVG samples, the fault is detected and discriminated by the proposed main protection scheme amidst a period of five sampling intervals. Depending on the reactor current increment, a backup protection scheme is also proposed to enhance the protection reliability. The performance of the proposed scheme is validated in a four-terminal MTDC grid. The results under meaningful fault events show that the proposed scheme is capable to identify the DC fault within millisecond. Moreover, the evaluation of the protection sensitivity and robustness reveals that the proposed scheme is highly selective for a wide range of fault resistances and locations, higher sampling frequencies, and irrelevant transient events. Furthermore, the comparison results exhibit that the proposed RVG method improves the discrimination performance of the protection scheme and thereby, proves to be a better choice for future DC fault identification.

INDEX TERMS Fault discrimination, fault identification, fault resistance, grid protection, HVDC transmission, multi-terminal DC systems, reactor voltage gradient.

I. INTRODUCTION

In the context of future grid infrastructure, the Multi-terminal high-voltage Direct Current (MTDC) grid is likely to become a backbone of the prevailing AC-dominated power network [1], [2]. Due to the improved controllability, operational flexibility, and effectual transmission, the MTDC grids offer massive integration of renewable sources and remote interconnection of asynchronous AC areas [2], [3]. With growing interests, the first ever four-terminal MTDC grid is constructed in Zhangbei, China with MMC's of ±500 kV/3000 MW [4]. However, as an emerging technology, several key challenges of the MTDC grids with more complex topologies, (i.e., meshed topologies) are yet to overcome [5]. The absence of zero-crossing fault current in a low impedance DC path poses a major threat to the DC protection scheme and thereby, treated as one of the significant concerns.

During the event of a DC fault, the discharging phenomena of the MMC sub-modules causes a rapid growth of the DC fault current. Without adequate protective measures, a large amount of fault current quickly propagates to the healthy parts of the MTDC grids within a few milliseconds. Consequently, a large part of the healthy grids is inevitable to remain de-energized for an extended period of time. To avoid this prolonged interruption, the Direct Current Circuit Breaker (DCCB) is a feasible solution for isolating the fault component [6], [7]. Moreover, a common practise is to use a current limiting DC reactor to enhance the fault clearing

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capability of the DCCB [7]. However, the interruption time of a DCCB is reasonably fast to break the fault current before exceeding its maximum capacity. Taking Zhangbei MTDC grid as an example, a minimum 3-ms fault detection time is required to interrupt a maximum possible fault current of 25 kA [4], [8]. Therefore, a fast DC fault identification with improved selectivity and reliability is indispensable for securing the operational continuity of the MTDC grids.

Based on the cosine distance criteria, a pilot protection scheme is proposed in [9]. With better selectivity, the effective identification of a DC fault is possible by this method. However, it may suffer from time delays associated with the communication links. The travelling wave based localized schemes with relatively lower sampling frequencies are proposed in [10] and [11]. However, a poor sensitivity is the impediment of the protection methods. The statistical method in [12] and high- frequency transient-signal based method in [13] are proposed to improve the protection sensitivity. However, the numerical computations associated with the methods are not straightforward. Hence, difficult to implement for the large MTDC grids.

To reduce the computational complexity, various protection methods have been proposed in the literature based on the electrical quantities of the DC reactor. The non-unit protection methods based on the reactor voltage derivative are proposed in [14] and [15]. More specifically, the protection method developed in [14] is based on the rate of change of reactor voltage measured at the line side of the reactor. This method presents a rapid detection of the DC line fault. However, the performance of the proposed method in [14] may suffer from large fault resistances and irrelevant transient events. The protection method proposed in [15] is based on the rate of change of reactor voltage measured across the DC reactor with greater sensitivity. However, the accurate estimation of the time interval for defining the threshold value is difficult in a large MTDC grid [15]. Furthermore, the scope of the derivative based methods proposed in [14] and [15] is limited to discriminate external bus fault from internal line fault. A unit protection scheme proposed in [16] is based on the voltage polarities of the terminal reactors at both ends of the DC line. Although the method can discriminate internal and external fault, it requires communication links with considerable time delay.

To reduce the communication dependency, the unit based backup protection is integrated with the non-unit based main protection schemes [17]– [19]. Based on the ratio of the transient voltage at both ends of the DC reactor and DC line, a successive main and backup protection scheme is developed in [17]. However, this method requires higher order digital filters to extract the noise sensitive transient voltage and might suffer from computational complexity. The authors in [18] proposed a relatively faster protection scheme based on the voltage across the DC reactor. However, the discrimination of internal and external DC faults are not properly justified in [18]. To identify internal and external DC faults, the protection method based on the reactor power and the current variation tendency is reported in [19]. However, for specific fault events, the reactor power takes considerable time to reach its peak value and thereby, the protection speed is relatively slow.

From the aforementioned literature review, it is evident that the reactor based protection methods lack a fast fault identification technique with the capability of internal and external DC fault discrimination. Therefore, this paper aims to address this issue and improve the performance of the reactor based DC protection scheme. Based on the value of the reactor voltage gradient (RVG), this paper proposes a fast, simple, and reliable DC fault identification method with an explicit criteria of the fault discrimination.

The rest of the paper is organized as follows. The basic principle of the proposed protection scheme is developed in Section II. This section established the RVG value as the key index for the proposed DC fault identification method. Section III presents the detection and discrimination criteria of the proposed method including the main and backup protection schemes. The test system with comprehensive simulation results are presented in Section IV. The sensitivity, robustness, and comparative studies of the proposed scheme are also presented in Section IV. Finally, Section V concludes the findings of the paper.

II. FAULT IDENTIFICATION PRINCIPLE

Relating to the current limiting reactor, the basis of the proposed fault identification technique (referred as RVG) is formulated in this section. To interpret the discrimination criteria evidently, characteristics of the internal and external DC faults are also examined supporting the proposed principle.

A. FORMULATION OF RVG

In order to formulate the RVG criteria, a small segment of the MTDC grid is considered as shown in Fig. 1. This section of DC system is subjected to a DC line fault, F_B. This causes a capacitive discharge of the MMC sub-modules (SMs) and adjacent healthy lines (line-A) to contribute the fault current (I_B). Hence, in a single-ended DC terminal, the rise of fault current is limited by the inductor values from three different sources: 1) DC reactor in faulty line (L_{L_B}), 2) DC reactor in adjacent healthy line (L_{L_A}), and 3) arm inductors in MMC (L_M). The proposed fault identification scheme is based on these inductors (L_{L_A}, L_{L_B}, and L_M) and collectively termed as the fault identification reactor (FIR).

In a steady-state condition, the voltage developed across the FIR is nearly zero [15]. Hence, the relevant reactor voltages are expressed as follows:

$$V_{L_A} = V_{L_B} = V_M \approx 0 \tag{1}$$

where V_{L_A}, V_{L_B}, and V_M are defined as the reactor voltage of the single-ended healthy line, faulty line, and MMC, respectively. Applying *KCL* at the node of DC bus, the pre-fault

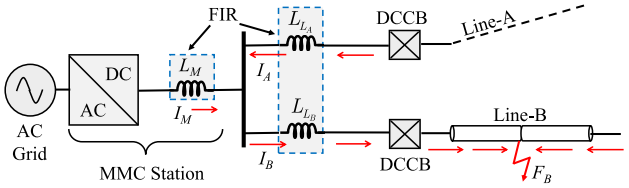

FIGURE 1. Single terminal of an MTDC grid with a DC fault.

current value is expressed as:

$$I_M = I_A + I_B \tag{2}$$

where I_A, I_B, and I_M are defined as the respective FIR currents.

After a DC fault (F_B) in line-B, the increment in fault current is presented as follows:

$$\Delta I_B = \Delta I_A + \Delta I_M \tag{3}$$

To simplify the computation, all the line reactor values are considered to be equal (i.e., $L_{L_A} = L_{L_B} = L_L$). Therefore, applying nodal analysis in (3), the relation of the FIR voltages can be expressed as follows:

$$V_M = \frac{L_M}{L_L}(V_{L_B} - V_{L_A}) \tag{4}$$

$$V_{L_B} = \left(\frac{1}{\alpha}\right)V_M + V_{L_A} \tag{5}$$

where the inductance ratio of the FIR is denoted as $\alpha = L_M/L_L$. The typical value of α is less than unity ($L_M < L_L$) [7], [18].

Moreover, from the MMC terminal voltage (V_T), the value of V_M can easily be determined by

$$V_M = V_{DC} - V_T \tag{6}$$

In more generalized form, (5) can be written as follows:

$$V_{L(Faulty)} = (1/\alpha)V_M + V_{L(Healthy)} \tag{7}$$

Due to the insignificant fault current contribution from adjacent healthy line [13], the relevant reactor voltage ($V_{L(Healthy)}$) can be neglected to rewrite (7) as follows:

$$V_{L(Faulty)} = (1/\alpha)V_M \tag{8}$$

The relationship expressed in (7) and (8) resemble the equation of straight lines as given in Fig. 2, where $1/\alpha$ is defined as the reactor voltage gradient (RVG). Moreover, (7) and (8) provide an exact and approximate solution of the RVG, respectively.

For a faulty line, the pre-fault zero RVG instantly appears to be a steeper value of positive gradient with an exact estimation of $1/\alpha$. On the contrary, the RVG approximation is nearly zero with a flat gradient for the healthy lines as discussed extensively in the following sections. Hence, the RVG is considered as a suitable index for the proposed fault identification scheme.

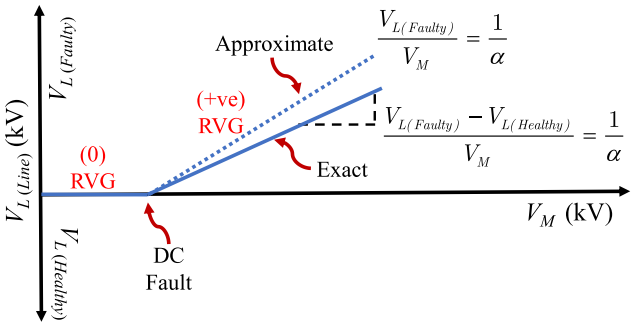

FIGURE 2. Reactor voltage gradient (RVG) for DC fault.

The RVG value does not depend on other line reactor values. Hence, the same RVG value ($1/\alpha = L_L/L_M$) can be used to identify the DC fault in multiple DC lines, even under the contingency of line outage. In case of different line reactor values in an MTDC grid, the RVG value with the highest line reactor (L_L) is used for the identification of the DC faults.

B. RVG FOR INTERNAL FAULT

The post-fault equivalent circuit of the MTDC grid is shown in Fig.3(a) for an internal DC line fault F_l. Consequently, the fault currents evolve into three different routes as shown in Fig.3(a). The total inductance value of the respective fault discharging paths are denoted as $L_{T1} = (L_M + L_L + L''_{12})$, $L_{T2} = (L_M + L_L + L'_{12})$, and $L_{T3} = (L_M + 3L_L + L_{13} + L''_{12})$. Compared to the inductance value, the DC line resistance is very small and thereby, neglected [20]. Hence, the fault current contribution can be described as follows:

$$\Delta I = \left[1/L_{T1}\right]\int_{t_0}^{t}(V_{DC1} - V_F)dt \tag{9}$$

$$\Delta I_A = \left[1/L_{T3}\right]\int_{t_0}^{t}(V_{DC3} - V_F)dt \tag{10}$$

$$\Delta I'_B = \Delta I' = \left[1/L_{T2}\right]\int_{t_0}^{t}(V_{DC2} - V_F)dt \tag{11}$$

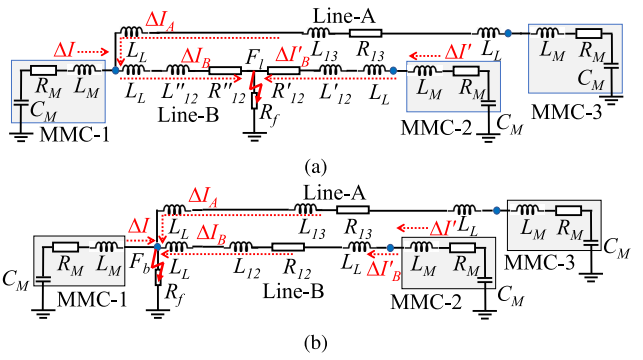

FIGURE 3. Post-fault equivalent circuit of the MTDC grid: (a) F_l DC fault; (b) F_b DC fault.

Moreover, the fault current ΔI_B is determined as follows:

$$\Delta I_B = \left[1/(L_L + L''_{12})\right] \int_{t_0}^{t} (V_T - V_F)dt$$
$$= \frac{1}{L_{T1}} \int_{t_0}^{t} (V_{DC1} - V_F)dt + \frac{1}{L_{T3}} \int_{t_0}^{t} (V_{DC3} - V_F)dt \quad (12)$$

where V_F is the fault point voltage and t_0 is the DC fault instant.

In favor of the main protection scheme embedded in MMC-1 side, the FIR voltages can be represented as follows:

$$V_{M1} = L_M \frac{dI}{dt} = \frac{L_M}{L_{T1}}(V_{DC1} - V_F) \quad (13)$$

$$V_{L_A} = L_L \frac{dI_A}{dt} = \frac{L_L}{L_{T3}}(V_{DC3} - V_F) \quad (14)$$

$$V_{L_B} = L_L \frac{dI_B}{dt} = \frac{L_L}{L_{T1}}(V_{DC1} - V_F) + \frac{L_L}{L_{T3}}(V_{DC3} - V_F) \quad (15)$$

In a lossless DC grid, the DC voltages can be approximated as $V_{DC1} = V_{DC2} = V_{DC3}$, and the RVG value is expressed as follows:

$$RVG_F = \frac{V_{L_B}}{V_{M1}} = \frac{L_L}{L_M}\left(1 + \frac{L_{T1}}{L_{T3}}\right) \quad (16)$$

$$RVG_H = \frac{V_{L_A}}{V_{M1}} = \frac{L_L}{L_M}\left(\frac{L_{T1}}{L_{T3}}\right) \quad (17)$$

For internal DC line fault, it is evident from (16) and (17) that the faulty line RVG (i.e., RVG_F) is greater than the healthy line RVG (i.e., RVG_H) value by an amount of L_L/L_M. Moreover, the value of L_{T1} is very small compared to L_{T3} ($L_{T1} \ll L_{T3}$) as reported earlier. Hence, the RVG_H value approaches to nearly 0. Therefore, the post-fault RVG with a positive and large gradient value ($L_L/L_M = 1/\alpha$), eventually discriminates the fault as an internal DC line fault.

C. RVG FOR EXTERNAL FAULT

The fault discharging paths for an external DC bus fault (F_b) is shown in Fig. 3(b). The inductance values of the respective fault paths are defined as $L_{T1} = L_M, L_{T2} = (L_M + 2L_L + L_{12})$, and $L_{T3} = (L_M + 2L_L + L_{13})$. With these modified inductance values, the fault current ΔI, ΔI_A, and ΔI_B ($\Delta I'_B = \Delta I_B = \Delta I'$) are evaluated by the same expressions presented in (9), (10), and (11), respectively. Similarly, the FIR voltages V_{M1}, V_{L_A}, and V_{L_B} are estimated by (13), (14), and (15), respectively, and represented as follows:

$$V_{M1} = L_M \frac{dI}{dt} = (V_{DC1} - V_F) \quad (18)$$

$$V_{L_A} = L_L \frac{dI_A}{dt} = \frac{L_L}{L_M + 2L_L + L_{13}}(V_{DC3} - V_F) \quad (19)$$

$$V_{L_B} = L_L \frac{dI_B}{dt} = \frac{L_L}{L_M + 2L_L + L_{12}}(V_{DC2} - V_F) \quad (20)$$

Consequently, the RVG values of the MMC-1 side protection scheme are determined from their FIR voltages as follows:

$$RVG_F = \frac{V_{L_B}}{V_{M1}} = \frac{L_L}{L_M + 2L_L + L_{12}} \quad (21)$$

$$RVG_H = \frac{V_{L_A}}{V_{M1}} = \frac{L_L}{L_M + 2L_L + L_{13}} \quad (22)$$

This is apparent from (21) and (22) that the RVG in faulty line (RVG_F) and healthy line (RVG_H) shows almost similar value for an external DC bus fault. Moreover, a large denominator value compared to the numerator eventually leads to a flat RVG. Therefore, a post-fault flat RVG distinguishes the fault as an external DC bus fault.

III. PROPOSED PROTECTION SCHEME

The proposed protection scheme is inclusive of a main protection and a back protection unit. The complete operation of each unit entails the protection steps of triggering, detection and discrimination of the fault. This section illustrates all the criteria of these protection steps in a sequential order.

A. MAIN PROTECTION

The samples of the FIR voltage exceeding the protection boundary indicate the presence of a DC fault in the MTDC grids. Hence, employing the line reactor voltage (V_L), the triggering criteria of the main protection scheme is represented as follows:

$$Cr\_1a : \left(|V_L|_i - |V_L|_{i-1}\right) > T \quad (23)$$

where $T = 140$ kV is the protection boundary, which separates the main scheme from the backup protection scheme.

To confirm the detection of the DC fault, three consecutive samples of the post-fault FIR voltage are taken into consideration by the main protection scheme. Hence, the fault detection criterion is expressed as follows:

$$Cr\_1b : \frac{1}{n}\sum_{i=1}^{n}\left(|V_L|\right)_i > T \quad (24)$$

where i is denoted as the number of samples in a window of n consecutive data. Moreover, $n = 3$ is the third consecutive sample after the DC fault, provided that $i = 0$ is the fault instant sample.

Thereafter, to differentiate an internal DC line fault from an external one, samples of the FIR voltages are passed through the fault discrimination criterion as follows:

$$Cr\_2 : Fault = \begin{cases} Int, & if \frac{1}{n}\sum_{i=1}^{n}\left(|\frac{V_L}{V_M}|\right)_i \geq \frac{1}{\alpha} \\ Ext, & otherwise \end{cases} \quad (25)$$

In the proposed method, the bus fault is also treated as an external DC fault. For a specific DC protection unit (PU), the existence of a DC fault (line or bus) is realized by the respective DC reactor voltage exceeding the protection boundary and further discriminated as a bus fault ($RVG < 1/\alpha$) or line fault ($RVG \geq 1/\alpha$), based on the RVG value. Thus, a bus fault is effectively distinguished

by the proposed RVG method. Any other external line fault outside the protection zone will be sensed by other external PUs as the corresponding internal fault to these PUs.

After identifying an internal DC fault, it can be further discriminated as a Pole to Ground (PG) or Pole to Pole (PP) fault. Using the pole-pair data, the discrimination criterion is described as follows:

$$Cr\_3 : Fault = \begin{cases} PP, & if \left[\frac{1}{n}\sum_{i=1}^{n}\left(|\frac{V_L}{V_M}|\right)_i\right]_k \geq \frac{1}{\alpha} \\ PG, & otherwise \end{cases} \quad (26)$$

where k is denoted as the paired DC pole (positive and negative pole) under an MMC station. Hence, the criteria is verified for both the poles to distinguish a PG or PP fault.

B. BACKUP PROTECTION

The DC fault which fails to trigger the main protection is detected by the backup protection scheme. Large fault resistance produces a small increment in the fault current and develops a lower value of FIR voltage, which can be detected effectively by the backup triggering criteria as given below:

$$Cr\_4a : M \leq \left(|V_L|_i - |V_L|_{i-1}\right) \leq T \quad (27)$$

After the activation of the backup protection scheme, the detection process is verified by the scheme following the backup detection criterion described as follows:

$$Cr\_4b : M \leq \frac{1}{n}\sum_{i=1}^{n}\left(|V_L|\right)_i \leq T \quad (28)$$

where $M = 40$ kV is the safety margin of the fault detection criteria. Hence, the backup protection scheme ranges from 40 kV to 140 kV and the over-voltage beyond this limit falls within the main protection scheme.

This is to be noted that the protection boundary T is merely used in the proposed method to differentiate the main and backup protection scheme. Hence, the protection boundary is not treated as the conventional threshold value. This requires extensive simulation scans to look for the critical set-points of the threshold settings.

To confirm the fault identification, the DC fault discrimination criterion of the backup protection scheme is employed as follows:

$$Cr\_5 : Fault = \begin{cases} Int, & if \Big[\Big(\sum_{i=1}^{n}\left(|\frac{\Delta I_L}{\Delta I_M}|\right)_i \geq 1\Big) \\ & \wedge \Big(\sum_{i=1}^{n}\left(|\frac{\Delta I'_L}{\Delta I'_M}|\right)_i \geq 1\Big)\Big] \\ Ext, & otherwise \end{cases} \quad (29)$$

where $\Delta I_{L,M}$ and $\Delta I'_{L,M}$ are the fault current increment in both ends of a DC line, respectively. More specifically, in (29), the current orientation (e.g., high, low or equal) of $\Delta I_L/\Delta I_M$ under one particular end of the DC line is utilized for $n = 3$ sampling values.

Finally, the internal fault is discriminated as PG or PP fault following the criterion reported by

$$Cr\_6 : \quad Fault = \begin{cases} PP, & if \;\; 0 \leq |N/D| \leq M_u \\ PG, & if \;\; M_l \leq |N/D| \leq 1 \end{cases} \quad (30)$$

where the numerator N and denominator D are defined as, $N = [|(\Delta I_L)_p| - |(\Delta I_L)_n|]$ and $D = [|(\Delta I_L)_p| + |(\Delta I_L)_n|]$, respectively. Considering the base of the current increment ratio as 1, the upper and lower limit of the safety margin is given as, $M_u = 0.1$, and $M_l = 0.9$, respectively.

C. OVERALL SCHEME

In the proposed protection scheme, the identification of a DC fault includes the detection and discrimination of the fault followed by a triggering of the main or backup protection unit. In the proposed algorithm, the voltage and current data of the FIR are continuously sampled and stored to perform the relaying operation. To begin with, each sample value of the FIR voltage is compared with the previous one to trigger the scheme. Based on the criteria of Cr_1a and Cr_4a, the respective main and backup protection unit start to operate and identify a DC fault, accordingly. The flowchart of the entire protection scheme is depicted in Fig. 4.

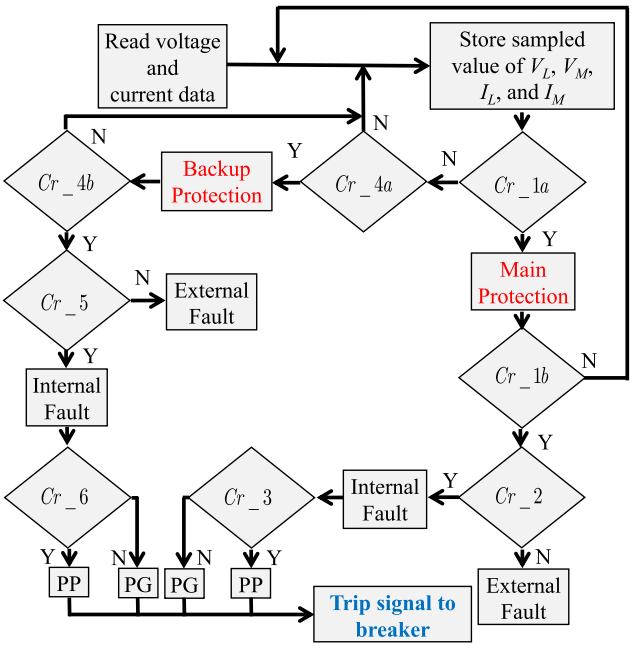

FIGURE 4. Fault identification scheme.

After triggering the main protection unit, the detection process is executed with a successful validation of the Cr_1b criterion. Following the detection of a DC fault, internal and external DC faults are discriminated based on the RVG criteria (Cr_2). Moreover, the internal faults are also classified as PG and PP faults satisfying the Cr_3 criterion. This finally terminates the fault identification process of the main protection unit and sends a trip signal to the respective DC breaker. The entire process is accomplished by

four consecutive samples of the FIR voltage. Hence, the proposed protection scheme is reasonably fast.

In case of backup protection scheme, the FIR voltage for detection (Cr_4b) and the reactor current increment for discrimination ($Cr\_5, 6$) are employed to identify the DC fault. For the discrimination of internal and external faults, only the binary information of the current increment orientation (higher or lower) is used. Hence, the data synchronization for both-ends communication is not required. Finally, the protection scheme ends up with the pole-pair current increment values to distinguish the PG and PP fault.

IV. RESULTS AND DISCUSSIONS

In this section, the selectivity of the proposed protection scheme is verified in a test simulation model with different fault events. The protection performance is also assessed in terms of sensitivity and robustness along with a detail comparative study.

A. TEST SYSTEM

In order to validate the proposed protection scheme, a four-terminal MTDC grid with mesh topology is adopted in this paper. The test system is shown in Fig. 5 and the associated grid parameters are provided in Table 1. The grid model is developed in DIgSILENT PowerFactory [21]. In terms of the MTDC grid operation [22], the MMCs-2, 3, and 4 are operated in $P-Q$ control mode to maintain the grid power balance. Alternatively, the regulation of DC voltage is provided by MMC-1 station with $V_{DC}-Q$ control mode.

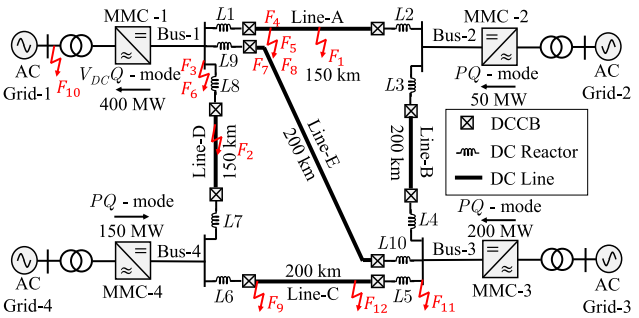

FIGURE 5. Four terminal MTDC grid with mesh topology.

The length of the transmission lines are given in Fig. 5 and a current limiting DC reactor of 100 mH is linked at both-ends of the respective DC lines. To simplify the computation, the overhead line (OHL) π-model with RL approximation is employed which is largely utilized for DC fault transients and protection studies with ample accuracy [15], [20], [23]. Moreover, for few milliseconds after the DC fault, the fault current in MMC dominates over the OHL and the OHL capacitance ($\sim 10^{-2}$ μF) is insignificant compared to MMC capacitance ($\sim 10^{2}$ μF) [24]. Therefore, for the OHL model used in this paper, the DC line capacitance is ignored.

All the faults are applied at 0.1 s and the fault events are briefly summarised in Table 2. For the protection scheme,

TABLE 1. Parameters of the MTDC grids.

System Parameters	Value	System Parameters	Value
Rated AC voltage	275.5 kV	SM capacitance	15 mF
DC voltage	±500 kV	Arm inductance	60 mH
Rated DC current	2 kA	Arm resistance	0.006 Ω
Transformer reactance	0.15 p.u.	DC line resistance	0.011 Ω/km
Rated MMC capacity	500 MVA	DC line inductance	0.519 mH/km
SMs per arm	200	DC reactor	100 mH

TABLE 2. Fault events at various locations of the MTDC grids.

Fault event	Fault type	Fault location	Fault resistance (Ω)
F_1	PG	line-A, 50%	10
F_2	PG	line-D, 10% from bus-1	10
F_3	PG	bus-1	10
F_4	PG	line-A, 10% from bus-1	10
F_5	PP	line-A, 10% from bus-1	10
F_6	PG	bus-1	200
F_7	PG	line-A, 10% from bus-1	800
F_8	PP	line-A, 10% from bus-1	800
F_9	PG	line-C, 50% and 100% from bus-3	10 and 800
F_{10}	AC	MMC-1, AC side	0
F_{11}	PG	bus-3	10
F_{12}	PG	line-C, 10% from bus-3	10

the sampling frequency F_s is taken as 10 kHz. The base value of the protection boundary T is considered to be 1000 kV. Moreover, considering the fluctuation of the practical data stream, a sufficient safety margin is considered for all the relevant protection criteria, (i.e., $M = 0.04$, $M_u = 0.1$, and $M_l = 0.9$). To reduce the measurement noise, first order lag filters with unity gain and a time constant of 1 ms are employed in the protection scheme [20].

B. MAIN PROTECTION VALIDATION

To evaluate the performance of the main protection scheme, the MTDC grid in Fig. 5 is subjected to three separate DC faults F_1, F_2, and F_3 with a fault resistance of 10 Ω. The DC fault F_1 is incepted at the middle of the line-A, F_2 is incepted in line-D at a fault distance of 10% from bus-1, and F_3 is applied at bus-1 under the MMC-1 station.

1) START-UP AND DETECTION

To start-up the single-ended main protection scheme, the detection criteria of the given DC faults (F_1, F_2, and F_3) are examined using the samples of the relevant FIR voltages (V_L), as shown in Fig. 6(a). For F_1 and F_2 DC line faults, the V_L voltage of $L1$ and $L8$ changes, respectively, and for F_3 bus fault, all the nearby V_L voltages ($L1$, $L8$ and $L9$) respond accordingly. Due to similar characteristics only $L9$ reactor voltage for F_3 DC fault is presented in Fig. 6(a). For all the given DC faults, it is apparent from Fig. 6(a) that the respective V_L voltage exceeds the protection boundary T, almost instantly (few microseconds) and satisfy Cr_1a criterion. This initiates the start-up unit of the main protection scheme. Subsequently, three samples of the post-fault V_L voltage are taken into consideration to satisfy Cr_1b criterion

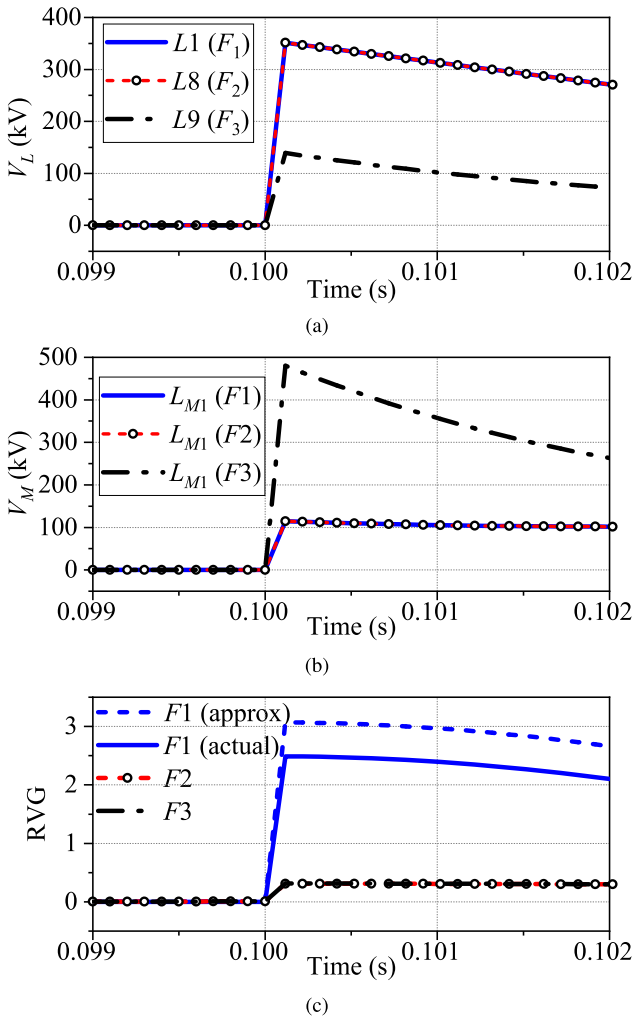

FIGURE 6. Main protection scheme: (a) Line reactor voltage; (b) MMC reactor voltage; (c) RVG for fault identification.

and finalize the detection of the DC fault. After detecting the DC fault, the algorithm of the protection scheme proceeds further to explicitly discriminate the DC fault as described in the following sections.

2) FAULT DISCRIMINATION

The DC fault discrimination criteria are verified using the RVG samples of the FIR voltages as shown in Fig. 6(c). The V_M voltages required to compute the RVG values are also illustrated in Fig.6(b). In order to distinguish an internal and external DC fault, the non-unit protection scheme embedded in MMC-1 side of line-A ($L1$) is taken into consideration.

Figure 6(c) reveals that the pre-fault RVG values are nearly 0 for a DC line. For F_1 DC fault, the post-fault RVG in $L1$ reactor abruptly reaches to a steeper value of approximately 3 with a positive gradient. The post-fault RVG values of three consecutive samples are found to be 3.07, 3.07, and 3.06, respectively. Moreover, the average value of the actual RVG is computed as nearly 2.5. Hence, Cr_2 is validated to classify F_1 fault as an internal DC fault. On contrary, the RVG value in $L1$ reactor remains nearly 0 for F_2 and F_3 DC faults as shown in Fig. 6(c) with a flat gradient. Therefore, F_2 and F_3 faults are discriminated as external DC faults by the proposed protection scheme. This is to be noted that, for the reference PU (line-A), the external F_3 fault is identified as a bus fault. Instead of line-A, F_2 fault is detected by the respective PU of line-D as an internal line fault.

Following the identification of an internal DC fault, it can be further discriminated to a PG or PP fault. To validate the discrimination performance of the proposed protection (reference) scheme a PG fault (F_4) and a PP fault (F_5) is incepted, separately, in line-A at a fault distance of 10% from bus-1. The RVG samples of the nearby DC reactor ($L1$) for the respective pole pairs (positive pole p and negative pole n) are depicted in Fig. 7. It is apparent from Fig. 7 that the RVG samples of the faulty pole merely switches to a positive gradient with an approximate value of 2.5 from the flat RVG values. Hence, only the single pole in F_4 fault and the pole pairs in F_5 fault exhibit the positive RVG values following the DC fault. Therefore, the fault identification criterion (Cr_3) of the proposed scheme is successfully validated for discriminating an internal DC fault.

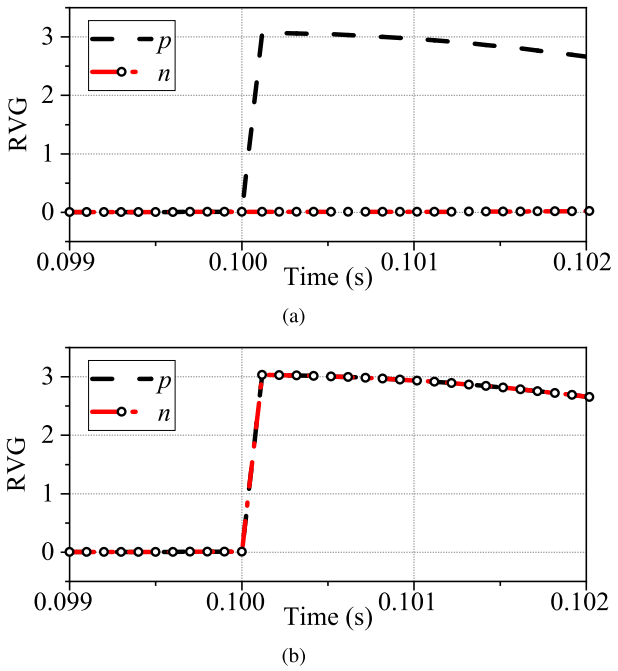

FIGURE 7. Internal fault discrimination: (a) PG; (b) PP.

The transition in RVG values from a pre-fault to a post-fault state is reasonably fast and appears almost instantly within 50 μs as shown in Fig. 6(c) and 7. Hence, a DC line fault is effectively identified within millisecond by adopting three consecutive RVG samples of the respective DC line reactor.

C. BACKUP PROTECTION VALIDATION

To validate the performance of the backup protection scheme, the MTDC grid in Fig. 5 is subjected to two DC faults F_6,

and F_7 with a large fault resistance of 200 Ω, and 800 Ω, respectively [18]. The fault F_6 is applied at bus-1 and the fault F_7 is incepted in line-A at a fault distance of 10% from bus-1.

1) START-UP AND DETECTION

Due to the high fault resistance, the samples of the V_L voltage in both ends of the faulty line (line-A) rises to a relatively smaller value of 78 kV for F_6 bus fault as shown in Fig.8(a). Moreover, the line fault F_7 also develops a voltage of 136 kV and 92 kV across the FIR $L1$ and $L2$, respectively, as shown in Fig.8(b). For both the cases (F_6, and F_7), the criterion Cr_4a is clearly satisfied to trigger the back-up protection scheme. The average value of V_L for three successive samples is computed as 67 kV and 45 kV in $L1$ and $L2$, respectively. Therefore, the detection process ends up with a successful validation of Cr_4b criterion from both ends of the faulty line-A.

2) DISCRIMINATION

For the same fault event F_7, the current increment in bus-1 side of line-A is found to be $\Delta I_L = 0.109$ kA, and $\Delta I_M = 0.088$ kA. Similarly, at bus-2 side, it is found as $\Delta I'_L = 0.074$ kA, and $\Delta I'_M = 0.067$ kA, as shown in Fig.8(d). Hence, the line current increment appears to be higher than the MMC current in both the ends of the faulty line. This clearly satisfies the fault discrimination criterion of Cr_5. Thereby, F_7 fault is successfully discriminated as an internal DC fault.

In case of F_6 fault, Fig.8(c) shows the increment of currents in both ends of the faulty line. It is evident from Fig.8(c) that the MMC current increment ΔI_M (0.47 kA) in bus-1 side is reasonably higher than the line current increment ΔI_L (0.06 kA). Hence, the criterion Cr_5 is validated to distinguish the fault F_6 as an external DC fault.

To further identify the internal DC fault as a PP or PG fault, a separate PP fault (F_8) is applied in line-A along with the PG fault (F_7). From the line current increment (ΔI_L) of the pole pairs, the value of N/D is computed as shown in Fig.8(e). For F_7 fault, the pre-fault 0 (zero) value of N/D term rapidly shifted to a value of nearly 1 and remains steady (zero) for F_8 DC fault. Hence, the criterion Cr_6 is successfully satisfied to discriminate the PP and PG faults.

D. TIME DELAY ANALYSIS

After a DC fault, the total time required to detect and discriminate the fault collectively defines the time delay (T_d) for the fault identification scheme [11]. For the proposed scheme, T_d includes the window of three sampling period (t_s), delay for the travelling wave propagation (t_{tp}), measurement and computational delay (t_{mc}), and communication delay (t_c) for the backup protection. Considering the propagation time of the overhead line and optical fiber communication [25], [26], the maximum value of T_d for F_9 DC fault is given in Table 3. The fault F_9 is applied in line-C at a fault distance (d) of 50%

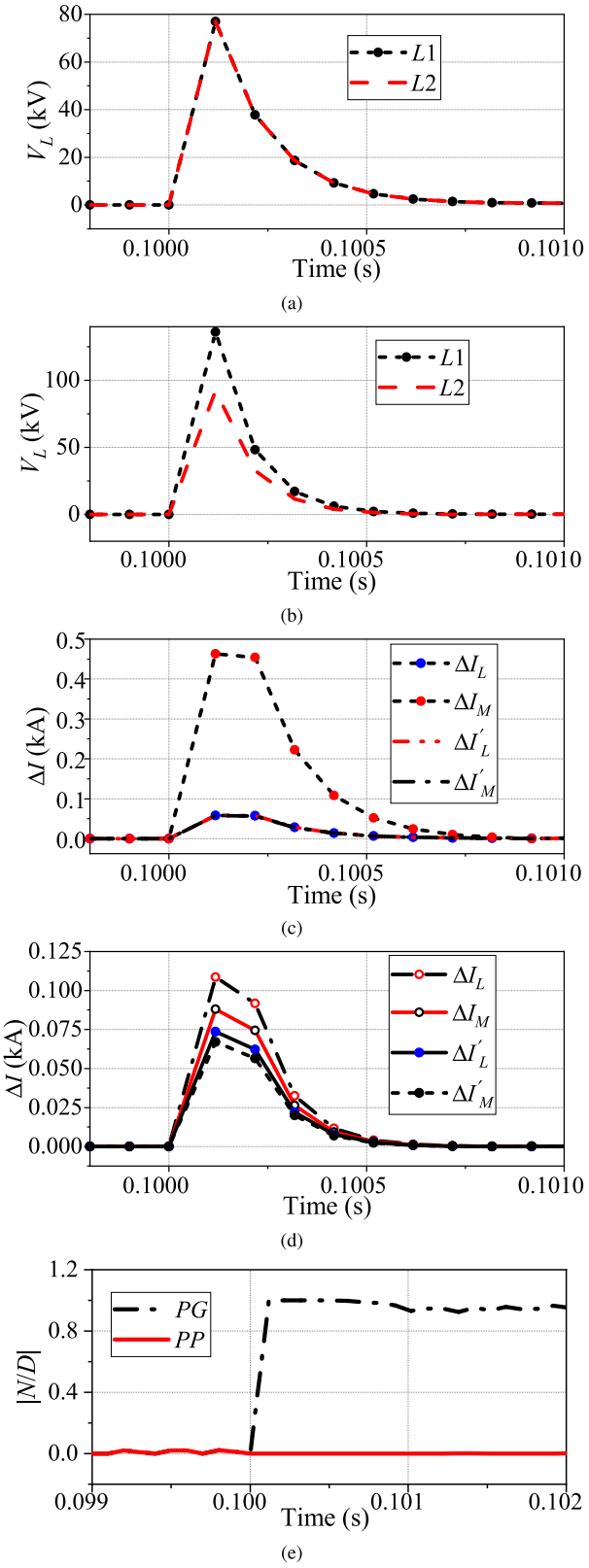

FIGURE 8. Backup protection scheme: (a) Line reactor voltage for F_6 fault detection; (b) Line reactor voltage for F_7 fault detection; (c) Current increment for F_6 fault discrimination; (d) Current increment for F_7 fault discrimination; (e) PG and PP fault discrimination.

TABLE 3. Maximum time delay of the proposed protection scheme.

Protection scheme	d (%)	t_s (ms)	t_{tp} (ms)	t_{mc} (ms)	t_c (ms)	T_d (ms)
Main	50	0.3	0.34	0.2	0	**0.84**
Backup	100	0.3	0.68	0.2	1	**2.18**

(100 km) and 100% (200 km) from bus-3 end for the main protection and backup protection scheme, respectively. This reflects the longest fault distance of the respective protection unit and thereby, results in a maximum time delay for the protection scheme. It is evident from Table 3 that the proposed scheme is quite fast to identify a DC fault effectively and satisfy the conventional speed requirement (≤3 ms) [27], [28] of the DC protection scheme.

E. SENSITIVITY ANALYSIS

The sensitivity of a protection scheme might get affected by various influencing factors. The sensing capability of the proposed scheme owing to the variation of the fault resistance, fault location, and sampling frequency is analysed in this section.

1) SENSITIVITY TO FAULT RESISTANCE AND FAULT LOCATION

The sensitivity of the fault identification scheme is evaluated with a variation of the fault resistance (R_f) and location (d) of the DC fault. The post-fault RVG values of the nearby protection scheme (bus-3 side) are illustrated in Fig. 9 for a DC fault in line-C. For a wide range of R_f (0 Ω to 800 Ω) and d (0% to 100%), the RVG values of the relevant reactors are determined. It is evident from Fig. 9(a) that the increasing values of R_f accelerates the decay rate of RVG values from it's post-fault positive gradient value of ∼3. However, the switching of RVG (from 0 to 3) is insensitive to R_f variation and the protection performance is not affected. Moreover, the Fig. 9(b) shows that the post-fault RVG values are almost indifferent (∼3) with a positive gradient for the wide variation of d. Hence, the proposed scheme is not affected by the resistance and location of the DC fault.

2) SENSITIVITY TO SAMPLING FREQUENCY

To evaluate the sensitivity of the protection scheme with different sampling frequencies (F_s), the signals are sampled in a range of 1 kHz to 20 kHz. For a DC fault in line-C with the given sampling frequencies, the results of the relevant FIR voltages and RVG values are provided in Table 4. The FIR voltage rises with the increasing values of F_s. However, the RVG values remain almost constant with the positive gradient value of ∼3, irrespective of the sampling frequencies. Therefore, the performance of the protection scheme is not influenced by F_s. The proposed scheme could respond effectively even with a lower sampling frequency.

F. ROBUSTNESS EVALUATION

A robust DC protection scheme should not respond to an extrinsic transient event which is irrelevant to the DC fault.

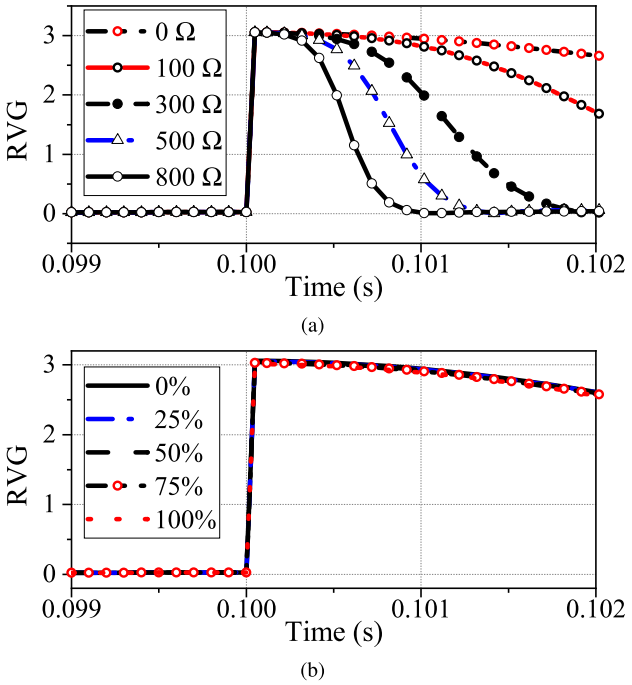

FIGURE 9. Protection sensitivity: (a) Fault resistance R_f; (b) Fault location d.

TABLE 4. Protection response to different sampling frequencies.

Sampling frequency (kHz)	FIR voltage $L5$ (kV)	FIR voltage L_{M3} (kV)	RVG
1	301.861	105.385	2.864
2	325.816	108.042	3.016
5	339.593	111.826	3.036
10	344.620	112.837	3.054
20	347.138	113.389	3.061

This section verifies the robustness of the proposed scheme relating to the AC fault and power variation transient events.

1) ROBUSTNESS TO AC FAULT

The robustness of the protection scheme is evaluated with a solid fault F_{10}, incepted at AC side of the MMC-1 for 80 ms. The FIR voltages (V_L) of the nearby reactors ($L1$, $L8$, and $L9$) are shown in Fig. 10. In response to F_{10} AC fault, the maximum FIR voltage is found as 2 kV (approx) in $L8$ reactor, which is much lower than the safety margin (40 kV) and protection boundary (140 kV). Hence, the protection scheme is non-responsive to the AC side faults and thereby, appears to be a robust scheme.

2) ROBUSTNESS TO POWER VARIATION

To assess the robustness of the protection scheme for power variation, the MTDC grid in Fig. 5 is subjected to a power switching event. In this transient event, a significant amount of MMC power is raised and reduced at 1 s and 2 s, successively. For both the cases, the variation of power is carried out in MMC-3 and MMC-4 with an amount of 0.25 p.u and 0.2 p.u, respectively. The power variation event causes

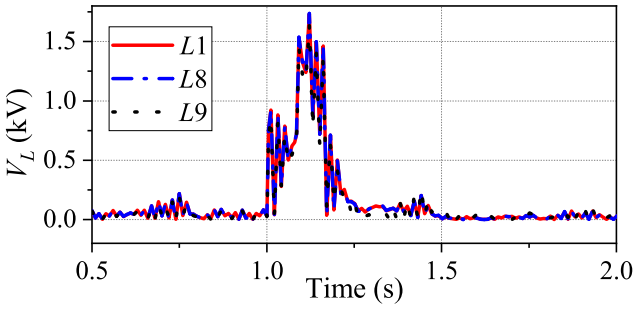

FIGURE 10. Protection response to AC fault.

the changes in DC line current as shown in Fig. 11(a). The post-fault FIR voltages ($L4$, $L5$, and $L10$) as shown in Fig. 11(b) appear to be very small ($\ll$ 40 kV) to trigger the protection scheme. Hence, the protection scheme remains non-responsive and deems robust to power variation transient event.

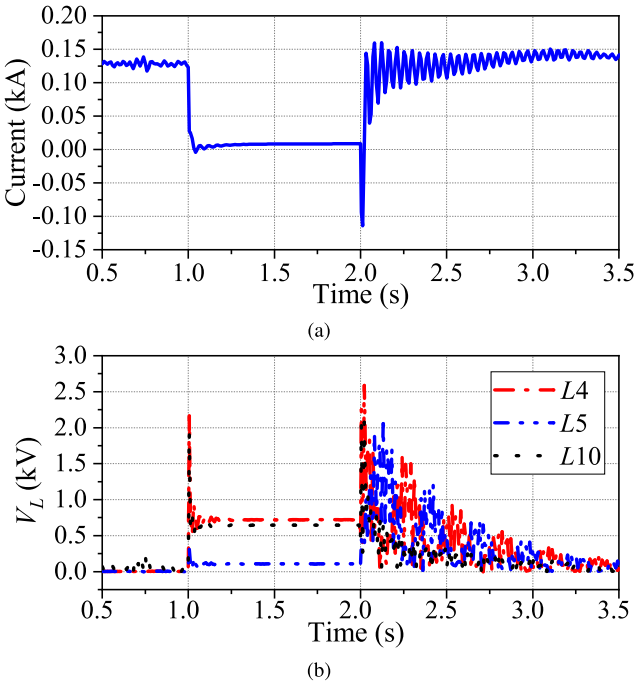

FIGURE 11. Protection response to power variation: (a) DC line current; (b) DC reactor voltage.

G. PERFORMANCE COMPARISON

Based on the electrical quantities of the DC reactor (i.e., reactor voltage (RV) [18], rate of change of reactor voltage (RRV) [15] and reactor power (RP) [19]), several protection methods have been proposed in the literature [15], [18], [19]. The wavelet transform based signal processing method [29] is also a prevalent tool for fault detection. In this section, the performance of the proposed RVG method is compared with the aforementioned protection schemes for an external DC bus fault F_{11} at bus-3, and an internal DC line fault F_{12} in line-C.

The protection schemes in the RV and RRV methods are reasonably fast to detect a DC fault. For the given DC faults F_{11} and F_{12}, Figs.12(a) and (b) reveal that the RV and RRV method can respond (detect) quickly by exceeding their respective threshold (Th_1 and Th_2) settings. However, the methods (RV and RRV) fail to discriminate the external bus fault (F_{11}) from the internal line fault (F_{12}). Moreover, to detect a DC fault in large MTDC grid, they require extensive simulation scans for threshold value settings. For example, the threshold values for RV ans RRV methods are determined through multiple simulations and considered to be $\text{Th}_1 = 100$ kV and $\text{Th}_2 = 30$ kV/ms, respectively for this paper.

In comparison with the RV and RRV methods, the proposed RVG method is independent of the threshold value requirement. Furthermore, in RVG method, the value of the gradient is always less than 1 (close to 0) irrespective of the external DC fault (F_{11}) as depicted in Fig.12(d). Therefore, the RVG method is capable to distinguish the internal and external DC faults, distinctively.

To discriminate the internal and external faults, the RP method relies on the maximum peak value of reactor power as shown in Fig.12(c). Hence, the protection scheme takes longer time (> 2 ms) to reach the power peak and the response is relatively delayed. Compared to the RP method, the proposed scheme in RVG responds almost instantly as shown in Fig.12(d) and identify a DC fault within a millisecond (< 1 ms). Therefore, the RVG method is quite fast with greater selectivity.

Considering the Daubechies3 (db3) wavelet and a 4-level decomposition, the desired frequency band of the given DC faults (F_{11} and F_{12}) is localised in (312.5 - 625) Hz for the WT based protection method [29]. With a sampling frequency of 10 kHz, the DC reactor voltage as shown in Fig. 12(e) is used as the non-stationary input (fault) signal for the WT method. The abrupt change of the post-fault reactor voltage is realised by the relevant co-efficient of the wavelet transform as depicted in Fig. 12(f). In this case, the threshold value (Th_3) of the wavelet co-efficient is considered to be ± 20. Fig. 12(f) implies that the post-fault voltage transient (fault inception at 0.1 s) causes the respective wavelet co-efficient of 415^{th} sample to exceed the threshold value with 1 sample delay and eventually identifies the DC faults within millisecond. However, the increasing level of wavelet decomposition gradually imposes filtering delays in the fault detection time. Although, the WT method can detect a DC fault rapidly, it fails to discriminate the bus faults and line faults of the MTDC grids. Moreover, the computational burden in the WT method makes the scheme relatively complex. Compared to the WT method, the proposed RVG method is very simple to implement with a fast fault discrimination technique.

In terms of the protection performance indicators (i.e., speed, selectivity, sensitivity and security), the performance comparison of the protection schemes is briefly discussed as follows:

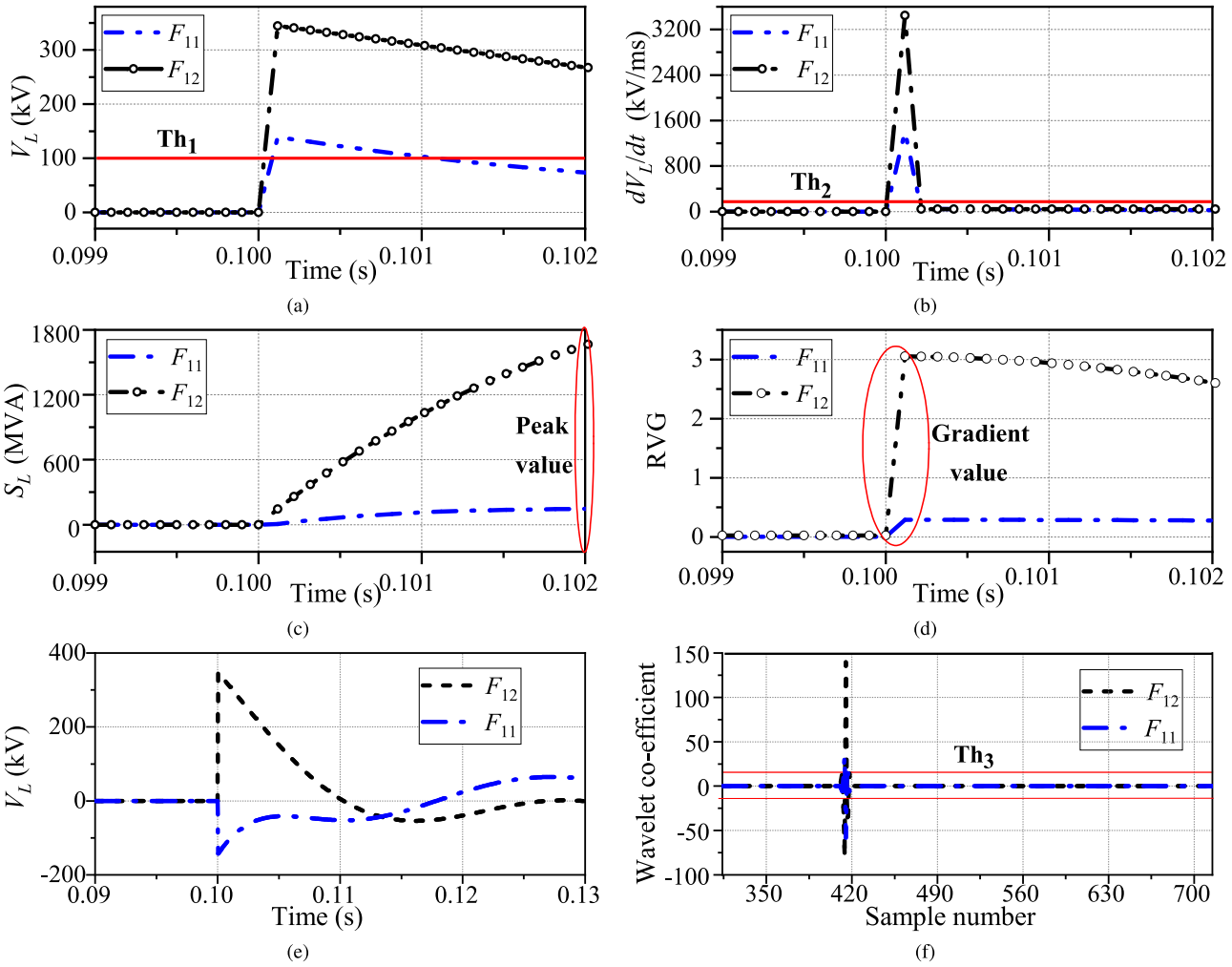

FIGURE 12. Performance of various protection schemes: (a) *RV* method; (b) *RRV* method; (c) *RP* method; (d) *RVG* method; (e) Fault signal (reactor voltage) for *WT* method; (f) Wavelet co-efficient for *WT* method.

1) Security: The discrimination of bus faults and line faults are not discussed in RV, RRV and WT methods. For these methods, the grid dependent threshold settings are required which need to be further investigated to improve the discrimination performance. Moreover, with a single line reactor value of the MTDC grid, selecting a threshold margin between the bus fault and line fault is difficult in RV and RRV methods. These drawbacks of the given methods might jeopardize the security of the protection scheme.

On the contrary, the proposed RVG method is capable to discriminate the bus faults and line faults, exclusively without any rigorous threshold value settings. Hence, in terms of protection security, the RVG method shows improved performance.

2) Speed: Compared to RV, RRV and WT methods, the RP method can discriminate the bus faults and line faults effectively. However, the RP method exhibits a relatively slow protection (>2 ms) method and the protection time increases with the increasing distance of fault location from the DC reactor. For example, the protection time in RP method is around 2.55 ms for a fault distance of 100 km [19]. Hence, for a larger fault distance, the protection time of the RP method may exceed the permissible time limit of 3 ms, which is not feasible for the DC protection scheme. Moreover, the RP method given in [19] is validated in a test network with point-to-point HVDC systems, which does not reveal the actual protection performance of the RP scheme in an MTDC grid.

Conversely, the RVG method is a faster protection (<1 ms) method for an MTDC grid irrespective of the DC fault location. Hence, in terms of the protection speed, the RVG method appears to be a fast protection method with an enhanced protection performance.

3) Sensitivity and Selectivity: All the protection methods (RV, RRV, RP, and WT) are selective in nature and dependent on the grid-oriented threshold value settings. Although the selection of large threshold value for the given methods improves the selectivity, the sensitivity of these methods

TABLE 5. Performance comparison with existing reactor based protection methods.

Protection method	Threshold settings	Protection sensitivity	Protection algorithm	Protection speed	Int-Ext fault discrimination
RV	required	medium	simple	fast (< 1 ms)	n/a
RRV	required	medium	relatively complex	fast (< 1 ms)	n/a
RP	required	low	simple	slow (> 2 ms)	exclusive feature
WT	required	high	complex	fast (< 1 ms)	n/a
RVG (proposed)	n/a	higher	simple	fast (< 1 ms)	exclusive feature

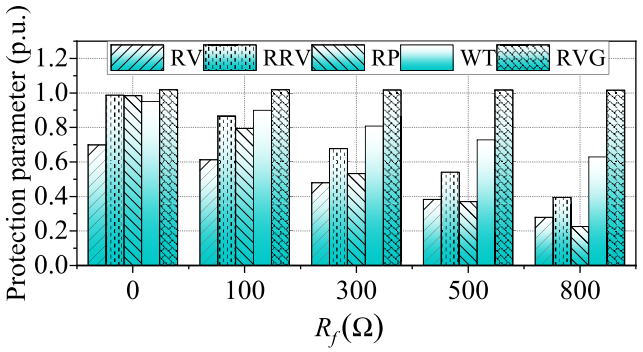

FIGURE 13. Sensitivity of various protection schemes for R_f variation.

is largely affected. The fault resistance (R_f) sensitivity of the protection methods given in Fig. 13 reveals that the performance of the RP method is relatively lower and the WT method is significantly higher compared to other protection methods.

On the other hand, the RVG scheme is free from extensive simulations for threshold value setting and thereby, the protection sensitivity remains unaffected. Hence, the RVG scheme shows better performance in terms of the protection sensitivity. The higher sensitivity and robustness eventually improve the selective performance of the proposed RVG method.

Based on the aforementioned analysis, a comparative study of the reactor based protection methods are summarised in Table 5. This is apparent from Table 5 that the proposed RVG method shows better performance compared to other protection methods. With an exclusive feature of fast fault discrimination (internal and external), the proposed method can be easily implemented due to its simplicity. Therefore, the proposed RVG method contributes to enhance the protection performance of the existing reactor based methods.

V. CONCLUSION

This paper proposes a fast fault identification method based on the reactor voltage gradient (RVG). The acceleration of the DC fault current is largely influenced by the inductance value of the fault identification reactor (FIR). This ultimately causes an abrupt change to the FIR voltage and shows distinct characteristics of the RVG values for specific fault events. Depending on the RVG criteria, the main protection scheme is developed here to identify a DC fault with four consecutive RVG samples. Excluding the complexity of data synchronization, the backup protection scheme is proposed based on the FIR current orientation. Simulation results with relevant fault events exhibit that the protection scheme is reasonably fast, easy to implement, and more selective to identify a DC fault effectively. More specifically, the discrimination of internal and external DC fault with improved protection speed is a distinctive feature of the proposed protection scheme. The sensitivity analysis shows that the proposed scheme can sense the DC faults with large fault resistance and fault location. Moreover, the selectivity of the main protection scheme is not altogether affected by lower sampling frequencies. Furthermore, the passiveness of the proposed scheme for irrelevant fault events indicates an improved robustness of the protection method. Therefore, the proposed scheme appears to be a fast, simple, and reliable protection method for future MTDC grid. The accurate estimation of the fault location in a complex DC grid will be studied and reported in the future.

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