Performance Analysis Of SRAM and Dram in Low Power Application

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Abstract—- All electronic systems must function quickly in the current environment, and 80 percent of electronic chips have memory components. SRAM (Static Random Access Memory) has thus become a major key component in many VLSI Chips in order to reduce the size of the memory chips, to increase the speed, to reduce leakage current, and to increase the power efficiency. Due to its high storage density and quick access time, it has also become a popular data storage device. SRAM has been given priority in the research community due to the recent sharp development in low power and low voltage memory devices. In this study, the design and performance of SRAM and DRAM cells were analyzed. This paper outlines the development and application of modified 6T SRAM cell with increased power efficiency.

KEY WORDS: *SRAM, DRAM, leakage current*

INTRODUCTION

Static Random Access Memory is known as SRAM. It is a kind of semiconductor memory that uses electronic switches to store data. SRAM does not require refreshing, which makes it faster and more power-efficient than Dynamic RAM (DRAM), which always needs to do so to keep the data[1]. SRAM is frequently utilized in computer systems as a cache memory because of its quick read and write access times. Moreover, it is utilized in microcontrollers, networking hardware, and other [2-4]

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As long as power is present, each memory cell in an SRAM chip stores a binary digit. A flip-flop will retain a value after storing a bit until the opposite value is held. Despite its size, SRAM provides speedy access to data. SRAM is also available as on-chip memory[5][11].

SRAM and DRAM each have benefits. SRAM, however, frequently performs more quickly than DRAM, with access times as little as ten nanoseconds. Moreover, unlike DRAM, which requires frequent refresh, SRAM does not require this. SRAM requires a constant, modest current and uses less energy than DRAM[6][15].

Disadvantages of SRAM, typically costs more and takes up more chip real estate. There is less memory on each chip, and they are more difficult to produce. SRAM requires nearly no power when idle since the amount of power it uses depends on how frequently it is accessed. At higher rates, SRAM will nevertheless use the same amount of power as DRAM[7][13].

DRAM is a form of semiconductor memory is called dynamic random access memory (DRAM). DRAM is frequently utilized to store program code that a computer's CPU needs to function. But, DRAM is also present in workstations, servers, and personal computers. RAM enables a computer's CPU to directly access any location in the memory, as opposed to working its way through it sequentially from the beginning. Compared to other forms of storage, such hard disks, RAM offers faster access to data. Due to its proximity to the computer's core, RAM is often speedier[8][16].

LITERATURE

CONVENTIONAL SRAM CELL

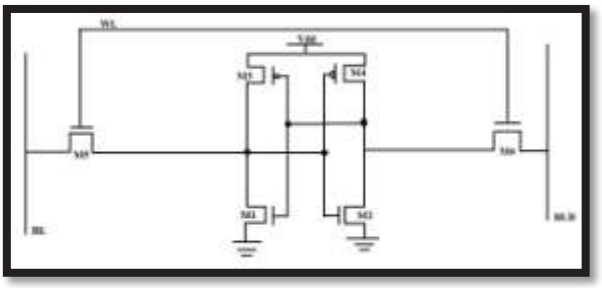

Fig 1conventional 6T SRAM

The conventional [fig 2] SRAM cell structure is composed of six transistors, two cross-coupled inverters, and two access transistors [1]. The two cross-coupled inverters form a positive feedback loop, which provides the memory function. The two access transistors provide the read and write functions.[17][18]

The two cross-coupled inverters are made up of four transistors: two PMOS transistors and two NMOS transistors. The gates of the PMOS transistors are connected to the drains of the NMOS transistors, and the gates of the NMOS transistors are connected to the drains of the PMOS transistors. This creates a positive feedback loop that maintains the state of the cell, either high or low. If the output of one inverter is high, it will drive the input of the other inverter low, which will then drive the output of the other inverter high, thus maintaining the state[2][9-10].

In summary, the conventional SRAM cell structure consists of six transistors, two cross-coupled inverters, and two access transistors. The two cross-coupled inverters form a positive feedback loop, which provides the memory function, while the two access transistors provide the read and write functions[4][12]. This basic structure has been widely used for many years due to its simplicity and reliability, although newer designs that use fewer transistors have been developed to reduce power consumption and increase density[14][19].

CONVENTIONAL DRAM CELL

Dynamic Random Access Memory (DRAM) is another type of volatile semiconductor memory that is commonly used in modern digital systems. Unlike SRAM, DRAM uses a single transistor and a capacitor to store a single bit of data. In this essay, we will discuss the conventional DRAM cell structure.

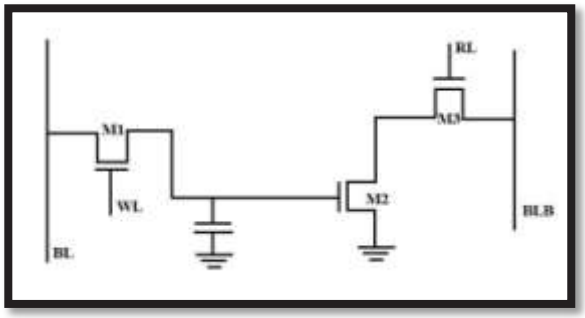

Fig 2 Conventional 3T DRAM

The conventional DRAM cell structure [7] consists of a single transistor and a capacitor. The transistor is typically an NMOS transistor, and the capacitor is made up of two metal plates separated by a dielectric material. The transistor is used to access the capacitor and charge or discharge it, while the capacitor is used to maintain the stored data, which can also lead to reliability issues if the refresh cycle is not performed correctly.[20][21]

In conclusion, the conventional DRAM cell structure consists of a single transistor and a capacitor and is used to store a single bit of data. It has a smaller cell size and lower power consumption than the conventional SRAM cell structure but is slower and requires periodic refreshing to maintain the stored data. Despite its drawbacks, DRAM is widely used in applications such as main memory in computers and mobile devices due to its high density and relatively low cost per bit.

PROPOSED SYSYTEM

The proposed 6T SRAM cell has less leakage current compared to the conventional 6T SRAM and 8T SRAM cell. The proposed 6T SRAM cell [6] has same performance and efficiency of the conventional SRAM cell has advantages over the power consumption.

WORKING

When the value "0" is stored in the cell, Qbar node links to VDD, M3 turns on, and M4 turns off. Qbar node charged as a result M2 turns off and the logic '1'. The voltage of the node Q will rise in a standard SRAM cell as a result of the current Ids-M2, which could result in a mistake. The subthreshold current of M1 works with the subthreshold voltage VIDLE to maintain the value of the Q node. The bit-line bar must be discharged to GND when the system is in idle mode in order to maintain the Q node's value. By adopting the technology of exploiting the leakage current to retain the value "0," this cell eliminates the need to refresh the data. As result of analysing the design is highly stable when ‘0’ is stored.

Data is 1: Q node and BLB-line are charged by VDD.The Qbar node will be dragged up to VDD-Vth by the NMOS access transistor (M1), turning on M4, and M2 will turn on as a result. M2 and M4 will then produce positive feedback.

Data is 0: BLB-line is kept at GND, Q node is pulled up to VDD by M1 while M3 is on, and Q node is pulled down to GND by M1. Cell enters idle state after the write process is finished.

Word-line is discharged to GND when the cell is in read operation and M6 is turned on. Before reading, the bit-line is charged to VDD. Bitline will continue to operate at a high level even when Q node voltage is high. When the Q node stores the value "0," the bitline is released to GND. Then, using a sensing amplifier connected to a bit-line, we can read data.

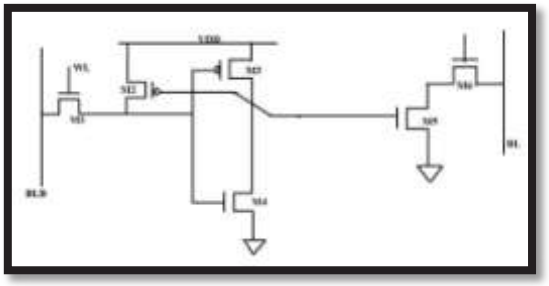

Fig 3 6t SRAM cell proposed

RESULT AND DISCUSSION

Thus the proposed 6T SRAM cell has less static noise margin compared to the conventional 6T SRAM cell and conventional 8T SRAM cell. It has less leakage current and power consumption compared to the other two SRAM cells.

Fig 46T SRAM proposed schematic

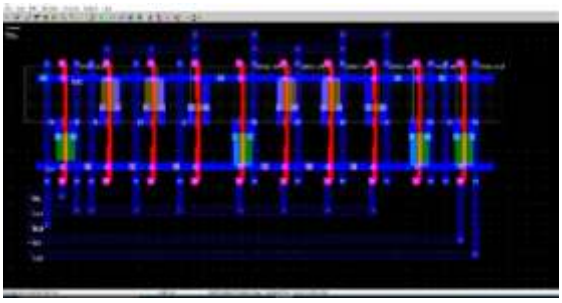

Fig 56T SRAM proposed simulation

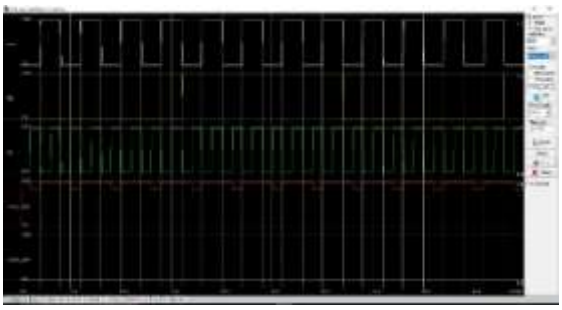

Fig 66T SRAM proposed simulation output

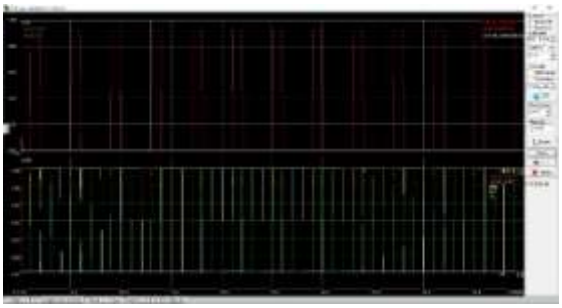

Fig 7 Proposed 6T SRAM cell V&I output

Fig 86T SRAM cell proposed tanner schematic

FOUNDARY		PROPOSED 6T SRAM CELL	CONVENTIONAL 6T SRAM CELL	8T SRAM CELL
90NM	**P**	0.262mw	0.155mw	0.209mw
	Idd	0.237mA	0.918mA	0.920mA
	Vdd	1.2v	1.2v	1.2v
65NM	**P**	0.123mw	58.533uw	81.959uw
	Idd	0.163mA	0.636mA	0.706mA
	Vdd	0.7v	0.7v	0.7v
45NM	**P**	0.114uw	14.461uw	17.493uw
	Idd	0.051mA	0.155mA	0.18mA
	Vdd	0.4v	0.4v	0.4v

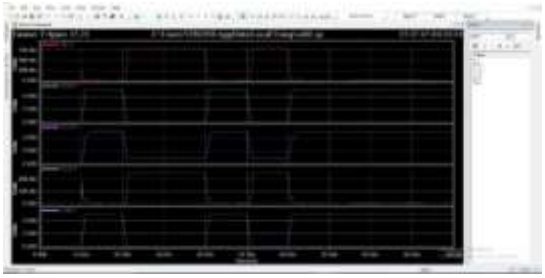

Fig 9VI characteristics of SRAM in Tanner

TABLE 1 Comparison of SRAM cell power consumption

CONCLUSION

So the proposed method of 6T SRAM consumes less power compared conventional 6T and 8T SRAM cell, it is as efficient as the conventional SRAM and DRAM. This research introduces a novel, 65nm-based, very stable 6T-SRAM. Only one bitline is functional in each operation, and this new structure uses separate write and read operation modes. As a result, the new cell uses less power, which is crucial for cache.

The new cell cuts power usage by around 22.56%, according to simulation results. Word-line voltage remains at V_{idle} when the cell is in idle mode. Without using a refresh cycle, the cell saves data vialeakage current and positive feedback. By segregating read and write operations, the novel structure improves the static noise margin.

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