Analyzing Radiation-induced Transient Errors on SRAM-based FPGAs by Propagation of Broadening Effect

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ABSTRACT SRAM-based FPGAs are widely used in mission critical applications, such as aerospace and avionics. Due to the increasing working frequency and technology scaling of ultra-nanometer technology, Single Event Transients (SETs) are becoming a major source of errors for these devices. In this paper, we propose a workflow for evaluating the behavior of SETs in SRAM-based FPGAs. The method is able to compute the Propagation-induced Pulse Broadening (PIPB) effect introduced by the logic resources traversed by transient pulses. Besides, we developed an accurate Look Up Table (LUT) layout model able to effectively predict the kinds of SETs induced by radiation-particle and to accurately mimic the phenomena of the SET generation and propagation. The proposed methodology is applicable to any recent technology to provide SET analysis, necessary for an efficient mitigation technology. Experimental results achieved from a set of benchmark circuits mapped on a 28 nm SRAM-based FPGA and compared with fault injection experiments demonstrate the effectiveness of our technique.

INDEX TERMS Function Generator, Propagation Induced Pulse Broadening, LUTs, Single Event Transients, SRAM-based FPGA.

I. INTRODUCTION

In the last decades, Field Programmable Gate Arrays (FPGAs) have been used in many applications such as aerospace and avionics due to their programmability and reconfigurability. Exploiting FPGAs, the development of customized electronic circuits can be achieved without the high costs and efforts of applying Application Specific Integrated Circuit (ASIC) solutions. Furthermore, using FPGA, the lifetime of applications can increase due to reconfiguration, allowing to meet different mission requirements of the development phases, test phases, or directly in the field. Unfortunately, FPGAs used in space environment can be subjected to cosmic rays and high energy particles that may cause several effects in the devices, undermining their dependability and reliability. Different failures and errors may be caused in FPGAs by space radiation environment, induced by Single Event Effects (SEEs) or Total Ionizing Dose (TID) [1]. On one hand, the accumulation of ionizing radiation, called TID, may cause performance degradation in electronic devices, making them slower and increasing power-consumption, finally ending with misbehaviors or failures. On the other hand, SEEs failure modes can be destructive to the device (e.g., Single Event Latch-up) or induce soft errors in data (e.g., Single Event Upset and Single Event Transient). A SEU is an undesired bitflip in a memory element of the device, usually overwritten in the next clock cycle. SETs are temporary voltage glitches that occur in routing or combinational logic, which may cause SEUs in digital circuits when sampled by memory elements, i.e. flip-flops. When a SET is generated in a sensitive logic node, it propagates through a logic path until a memory element is reached. If the pulse with suitable amplitude and duration arrives during the memory cell "window of vulnerability" (i.e. around the clock edge of the Flip-Flops) it can be sampled, causing SEUs. Nowadays, commercially available FPGAs are widely used in space applications, especially when radiation-hardened ones cannot meet performance needs and cost limits of the missions [2]. Two main FPGA families are adopted in aerospace applications: Flash-based and SRAM-based FPGAs. Flash-based FPGAs have an intrinsic immunity to SEUs in the configuration memory. Differently, SRAM-based FPGAs require various applied techniques (e.g. scrubbing) in order to handle Single-event Functionality Interruptions (SEFIs) caused by SEUs which occur in the SRAM-cells of the configuration memory [3]. However, SRAM-based FPGA families make use of latest silicon manufacturing processes (e.g. 16 nm for Xilinx UltraScale+) and has a higher TID tolerance that make them the usual choice for high-performances and long-term missions. Consequently, many works about SETs in Flash-based FPGAs have been carried out, since SETs in logic gates and wires are one of the main sources of soft errors for these devices [7][8]. Differently, very few works can be found about SETs in SRAM-based

FPGAs, where SEUs in the device configuration memory account for the most part of their errors. Nevertheless, due to the increasing of work frequency and the technology scaling that strongly characterize SRAM-based FPGAs, SETs are becoming a major source of errors that should be analyzed and mitigated also in these devices [9][10][8].

In this work, we propose a workflow to statically analyze the SETs propagation in SRAM-based FPGAs. To do so, an architectural model of function generators in SRAM-based FPGAs has been proposed. Starting from this model, with respect to a performed SETs characterization, we carried out transient 3D simulations to acquire information on how SETs with different characteristics propagate through function generators in SRAM-based FPGAs. The acquired knowledge has been used to develop a framework to statically analyze how much a SET may be subject to Propagation-induced Pulse Broadening while it propagates through Look-Up Tables of SRAM-based FPGAs. The proposed workflow has been applied to a set of benchmark circuits analyzing their sensitivity to SETs. Finally, we compared the obtained results with fault injection experiments performed on physical devices.

This paper is organized in five sections. Section II provides background and an overview of previous works on these topics. Section III explains our developed workflow, focusing on the SETs characterization, the PIPB effects introduced by function generators and the tools to perform design analysis. In section IV, the obtained results are shown and SETs sensitivity analysis is performed on a set of benchmarks applying our approach. Lastly in section V, conclusions and future works are discussed.

II. BACKGROUND AND RELATED WORKS

A. PROPAGATION INDUCED PULSE BROADENING AND ERRORS

When a charged radiation particle is interacting with an FPGA, it generates a voltage glitch known as Single Event Transient. A SET pulse, generated in a sensitive node, propagates through a logic path, which includes several logic gates and routing interconnections. The propagation of the pulse continues until it reaches a memory element, where it can be latched and become a soft error [9]. It is well known that a SET propagating through a logical gate chain may suffer from different effects (i.e. broadening or compression) that strongly affect its probability to be sampled. The Propagation-induced Pulse Broadening effect, called PIPB, is of crucial importance to estimate if a SET could eventually produce a soft error [11][11]. In [12], it has been shown that an initially narrow SET (i.e., 200 ps) can be broadened into the nanosecond range when it propagates through several combinational logic. The pulse broadening combined with the higher work frequencies and the higher technology scaling of SRAM-based FPGAs make SEUs induced by SETs sampling a common source of errors for them, more than in Flash-based FPGAs [13]. In order to assert how much a memory element can be affected by soft errors caused by SETs, the value of the PIPB introduced by the combinational logic located between the node where the pulse

is generated, and the input of the memory element is fundamental [14].

B. FUNCTION GENERATORS IN SRAM-BASED FGPAS BY XILINX

An FPGA consists of arrays of programmable elements that can be configured to perform specific functions. The Configurable Logic Block (CLB) is the basic element which provides logic resources for implementing sequential and combinational circuits. In 7 series FPGAs by Xilinx [15], the function generators in the CLBs are implemented as six-input Look-Up Tables (LUTs). Though Xilinx does not disclose implementation details about their physical architecture, a description of the generable functions is provided in [16]. Starting from this description, it has been possible to propose a model of the internal structure of the function generators in the Xilinx 7 series FPGAs, which is described in section III-B. In previous works, LUTs have been used for implementing chain of logical gates to observe their effects on SETs. In [17] and in [18], PIPBs introduced by LUTs with different configurations have been investigated and different behaviors have been observed. In SRAM-based FPGAs, the most part of combinational logic is implemented using LUTs. Thus, it is essential to understand the behavior of SETs propagating through LUTs with respect to the PIPB effect.

C. SETS CHARACTERIZATIONS AND EMULATION

the study of SETs in electronic circuits, generating SET pulses and measuring the propagated pulse are two main issues for fully emulate the SETs in the devices. There are three main methods for generating SET pulses such as radiation test, laser test and electrical injection. Though radiation test is the most similar to the real phenomenon, it lacks controllability of the SET's characteristics and the topological injection. Even if laser test reaches a finer control over generated SETs, it is still not good enough. Moreover, these tests can be performed exclusively in specialized facilities. Considering the electrical injection, the use of external pulse injection and measurement is deprecated, mainly because of the distortion caused by I/O pads on the pulses. Differently, internal electrical injection provides the finest controllability of SETs characteristics among the three methods and it can be used to inject SETs into specific nodes in the electronic circuit. Nevertheless, the full controllability featured by internal electrical injection needs to be supported by an in-depth knowledge of the characteristics of the SETs induced by the real phenomena. In [17] and [18], internal electrical injection has been used and the group of SETs widths to inject has been arbitrarily chosen between 300 ps and 2 ns. It has been reported in [17] and shown in the following subsection that, PIPB effect caused by combinational logic (i.e. LUTs) in SRAM-based FPGAs is dependent on SETs characteristics. Thus, a realistic SETs characterization is crucial to perform meaningful experiments related to SETs

III. THE PROPOSED APPROACH

The goal of the proposed workflow is to evaluate the behavior of SETs in SRAM-based FPGAs. The workflow consists of three phases: firstly, the SET characterization which is

dedicated to predict the features of radiation-induced SET such as amplitude and width of the pulse. Secondly, the development of an accurate LUT layout model for evaluating the behavior of SET propagating and broadening through the LUT. Finally, the SET characterizations are used to analyze the PIPB effect of the implemented design. Figure 1 represents the developed workflow.
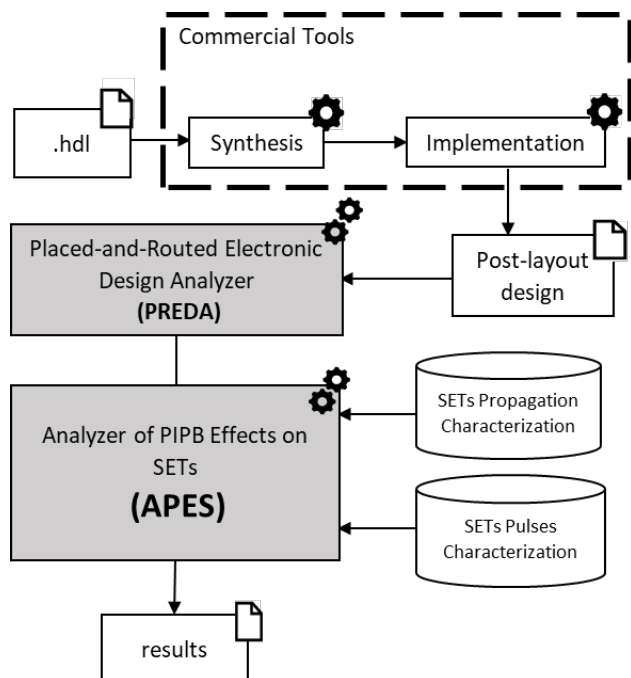

FIGURE 1. The developed workflow for analyzing the sensitivity of SRAN-based LUTs regarding Single Event Transient.

A. SETs CHARACTERISTICS

In order to order to predict the radiation-induced SET pulses, we developed a tool for analyzing the effect of ionized particles striking electronic devices. The tool takes into account several parameters regarding radiation environment and device under the study such as the incident angle, the LET of the particle, the type of particle. As a result, it predicts characteristics of the possible generated SET pulses such as width and amplitude. To elaborate more, the tool considers a set of radiation particles, interacting with the device under the study and it evaluates the behavior of the particle passing through the device. Basically, the tool is calculating if the energy of particle is enough to generate a SET pulse. If so, it predicts the generated SET pulses, width and amplitude of them. At the end, it provides a classification of SET pulses in terms of width and amplitude.

B. FUNCTION GENERATOR MODEL

The function generator consists of two LUTs with five shared inputs (A1, A2, A3, A4 and A5) and an output each, which are fed into a multiplexer. Another signal (A6) is used to select one of the inputs of the multiplexer to be forwarded on the primary output (O6) of the function generator. The secondary output of the function generator (O5) is driven by one of LUT output. Precisely, it is driven by the output which is selected as the multiplexer output when A6 is 0. The described model is shown in Figure 2.

We assumed that the LUTs with five inputs were implemented with five cascade stages of multiplexers as shown in figure 3. The LUT truth table is stored in the cell memories of the configuration memory dedicated to that LUT. The LUT output will be chosen by the inputs selecting the value to propagate to the output through the chain of multiplexer. In order to obtain a characterization of the function generators behavior regarding SETs propagation, we carried out SET injection using electrical simulations. They are illustrated in section IV-B.
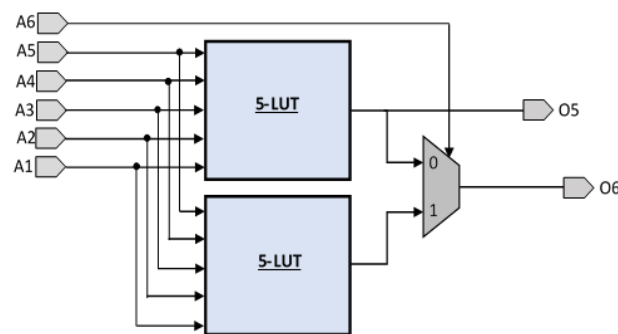

FIGURE 2. The proposed model for function generators architecture.

C. ANALYZER OF PIPB EFFECT ON SETS FOR SRAM-BASED FPGAS

In order to evaluate the sensitivity of a user memory element to SETs, we developed a framework for the analysis of SETs propagation in a placed-and-routed design. A framework named PREDA (Placed-and-Routed Electronic Design Analyzer) has been developed in Python and it is able to extract graphs from Vivado implemented checkpoints to describe and analyze their logical and physical architectures. PREDA interfaces with Vivado using tcl language. However, the approach can be easily extended to any commercial tools which allow to extract information about a post-layout design.
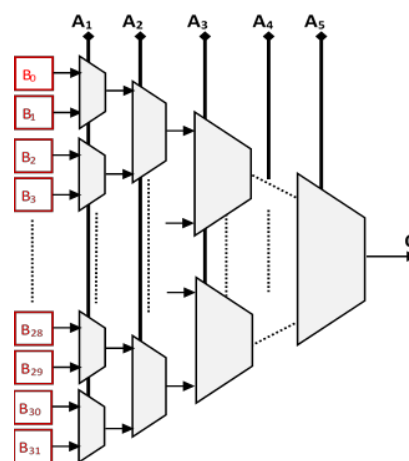

FIGURE 3. The proposed model for five inputs LUT.

Moreover, our developed tool, named APES (Analyzer of PIPB effect on SETs), integrates PREDA with the function generator model and the SETs characterization previously exposed. APES can exploit PREDA graph structures to analyze the effects induced by the LUTs on SETs propagation.

Using APES, it is possible to obtain information about how much SETs with a chosen starting width are broadened when they propagate until a memory element, through several LUTs on a specific path of the design under test. Therefore, the algorithm computes and combines the different contributes of the LUTs along the path considering the width of the SETs characterization and the LUT pins along which they propagate.

```
1   #SETs_sensitivity
2   def SETs_sensitivity (self, ff):
3       visited = []
4       to_visit = []
5       chk_lock = []
6       for N in self.nodes():
7           If ( self.has_predecessors(N) == False or
8           self.nodes[N]['TYPE'] == 'FLOP_LATCH'):
8               visited.append(N)
9
10      for e in self.out_edges ( visited ):
11          e['wPIPB'] = 1
12
13      for v in visited:
14          for c in self.children_of( v )
15              if c not in to_visit + visited:
16                  to_visit.append(c)
17
18      while (visited != chk_lock and to_visit != []):
19          chk_lock = visited[:]
20          visited_now = []
21          for tv in to_visit:
22              if set(self.parent_of(tv)).issubset(visited):
23                  to_visit.remove(tv)
24                  self.compute_and_update_wPIPB_for(tv)
25                  visited.append(tv)
26                  visited_now.append(tv)
27              for vn in visited_now:
28                  for c in self.children_of(vn):
29                      if c not in visited + to_visit:
30                          to_visit.append(c)
31
33      if chk_lock == visited:
34          return -1 # combinational cycle has been detected
35      return self.in_edges(ff)[ 'wPIPB']
```

FIGURE 4. Pseudo Code of the developed algorithm for analyzing SET propagation.

Using PREDA, a graph is built from an implemented design checkpoint in Vivado. The graph includes information about logic cells such as their placement, their primitive type and the connections between them. PREDA can obtain the subgraph describing the logic cone of each user memory element, which is the group of combinational logic and connection nets bordered by non-combinational logic (e.g. memory elements, I/O ports) and the memory element under test. These subgraphs are used by APES to analyze the broadening of propagated SET pulses reaching the memory element. The analysis can be performed to obtain the PIPB value which may affect a SET generated in a target node and reaching a memory element under test or it can be executed to obtain the worst broadening effects that may affect SETs which reach the memory element under test.

Thereore, the worst PIPB coefficient on their output is tagged as 1, which means that the worst SET observable in that position is the one that is generated there, without any broadening effect possible. Differently, if the PIPB coefficient for that node output is tagged greater than 1, it means that the

worst SET on that node will be a SET broadened by the elements it is passed through. Then the nodes connected to these elements are marked as candidates to have their worst PIPB computed.
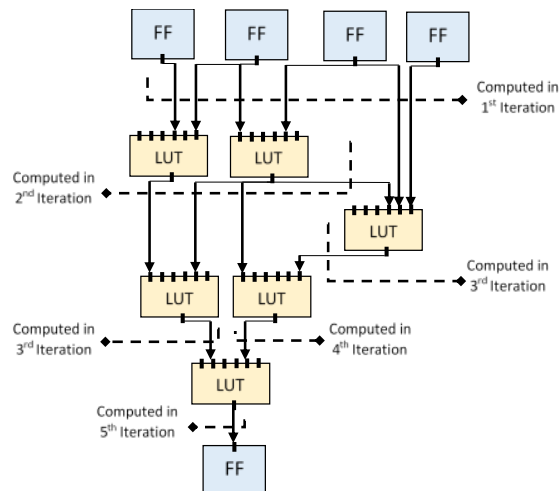

FIGURE 5. A conceptual scheme of the SET propagation analysis.

In each iteration, the worst PIPB is computed on the output of all the candidates which have each one of their inputs with a worst PIPB assigned. After that, the nodes they fed are added to the candidates set. This procedure is iterated until when the worst PIPB effect on the input of the flip-flops is found. Figure 4 shows a simplified version of this procedure and a conceptual scheme of its functioning is illustrated in Figure 5, while Figure 6 reports the code which describes the various steps to perform the analysis of a design.

```
1   #SETs Analysis
2
3   f_dcp = physical_layout_description_file
4   f_res = results_file
5   s_width = 300 #ps
6   ser = serialize_dcp(f_dcp)
7   G = serial2Graph(ser)
8   ffs = G.get_nodes_with('type','FLOP_LATCH')
9   for ff_ut in ffs:
10      subg = G.logic_cone(ff_ut)
11      PIPB = subg.SETs_sensitivity(ff_ut, s_width)
12      store(f_res, ff_ut, PIPB)
```

FIGURE 6. Pseudo code representing the algorithm for executing an analysis of a design for SETs of 300ps.

IV. EXPERIMENTAL ANALYSIS AND RESULTS

The proposed workflow has been experimentally evaluated on a set of different benchmark circuits. In this section, the developed 28nm LUT model is described, the results regarding SETs characterization and function generators model are reported. The results of analysis of the benchmark designs are also presented. Finally, these results have been compared with fault injection experiments exposed in [17].

A. A 28nm LOOK-UP-TABLE (LUT) LAYOUT MODELING
On the basis of the proposed model for five inputs LUT, we implemented the physical layout of the LUT using an open-source gate library at 28nm including three different types of

cells: the two input MUXes, the input Buffer and the 2SRAM cell storing two configuration memory bits. The overall LUT physical layout is illustrated in Figure 7.
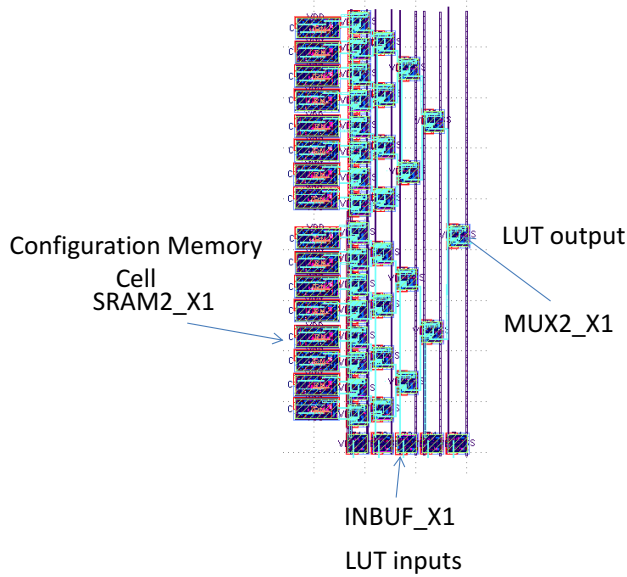

FIGURE 7. Overall GDS layout of the developed 28nm LUT used for the SET characterization: SRAM2 cells allocate configuration memory bits. Vice versa, INBUF is connected to the LUT input signals.

The LUT model area usage is reported in Table I, please note that the empty areas between the MUXes do not influence the SET generation and propagation.

TABLE I
PHYSICAL LAYOUT AREA IF THE DEVELOPED 28NM LUT CELL.

Resource Type	Total Cells	Area [μm^2]
SRAM2 X1	16	29.97
MUX2 X1	31	79.68
INBUF X1	5	4.17

In order to simulate the SET phenomena induced by radiation particles, the LUT layout geometry (that includes each single cell, the routing between them and the VCC and GND rails) has been exported to the developed SET characterization tool. Please note that the electrical transient behavior of the LUT layout has been tuned according to the transient signal propagation on various LUT configuration performed on an effective Xilinx Kintex-7 SRAM-based FPGA.

B. SETS CHARACTERIZATION

We developed a tool to mimic the propagation of heavy ion radiation particles through the physical layout of the 28-nm 5-inputs LUT. Then, we performed an analysis of the SETs characteristics generated by six elements (C, Ne, Al, Cr, Ni, Xe) commonly used in heavy ions radiation tests. For each of these elements, one thousand SETs have been generated using our tools. From the collection obtained we extracted the subsets composed of the SETs having a voltage amplitude greater than a critical threshold. The critical threshold is the minimum voltage value which can be sampled by the memory elements of the device. According with the technology under test, it has

been chosen a threshold of 0.4 Volt. The percentage of SETs with amplitude greater than 0.4 Volt generated by ionized particles for each element is shown in Table II.

TABLE II
PERCENTAGE OF SETs NOT ELECTRICALLY MASKED FOR EACH ELEMENT.

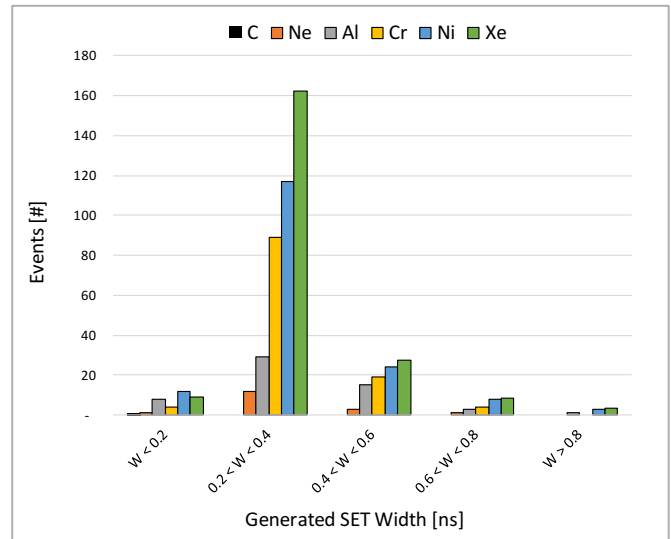| Elements	C	Ne	Al	Cr	Ni	Xe
SET Amplitude >0.4 V	0.1%	1.7%	5.6 %	11.6%	16.4%	21.1%

FIGURE8. **Classification of SETs not electrically masked according to their width.**

Figure 8 shows the distribution, among different width intervals, of the SETs with a voltage greater than the critical threshold. The classification clearly shows that the most part of the critical (i.e. which may cause SEUs) SETs, belong to the interval [200ps, 600ps]. Thus, the SETs in this range are the ones taken in accounts in our experiments and analyses.

C. BENHCMARK ANALYSIS

We applied the workflow exposed in subsection III-C to a set of benchmark circuits. Four designs have been chosen from ITC'99 benchmark collection [19] and implemented on a Xilinx Kintex-7 SRAM-based FPGAs. Table III provides information on the complexity of each design such as number of flip-flops cells, number of LUT cells, average depth of flip-flops logic cones and maximum depth among flip-flops logic cones. The workflow has been used to obtain an overview of the sensitivity to PIPB effects of the designs.

TABLE III
THE CHARACTERISTICS OF THE DESIGNS UNDER THE STUDY.

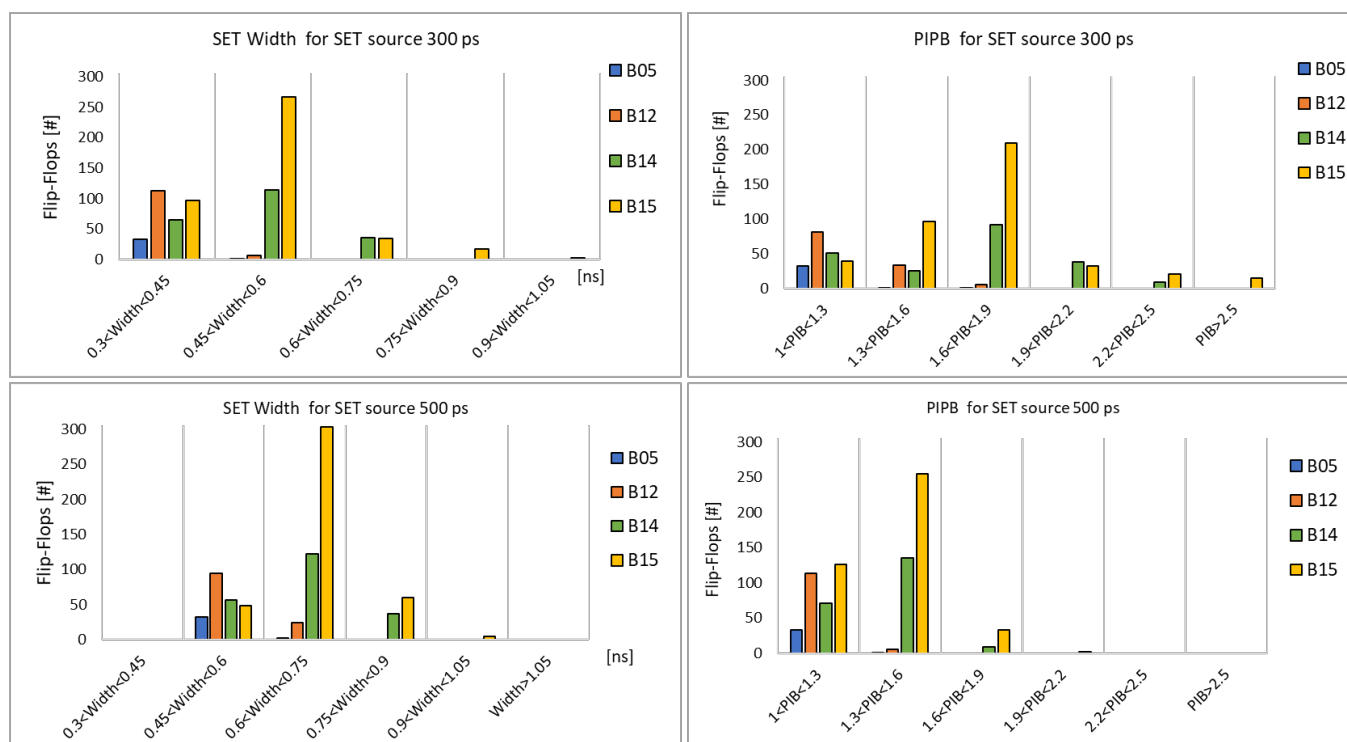| Circuits	Design Characteristics			
	FF CELL [#]	LUT CELL [#]	Max FF Logic Cone Depth	Average FF Logic Cone Depth
B05	34	91	6	3.2
B12	119	251	6	4.1
B14	215	1.071	14	11.1
B15	416	1.390	14	9.2

FIGURE 9. Classification of the flip-flops of the benchmarks designs according to PIPB value and SET width on the output for starting SETs of 300 ps and 500 ps

Figure 10 shows a figure of merit of each benchmark design. In details, the graph reports the PIPB worst-case in an ascending order for each Flip-Flop ID. Please note that the FF numbers of the benchmarks are normalized on the x-axis.
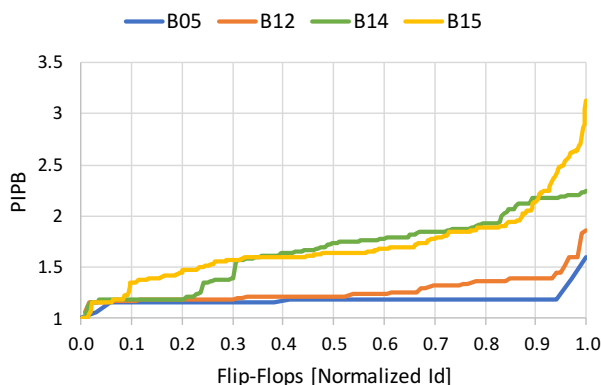

FIGURE 10. Propagation-induced Pulse Broadening (PIPB) Figure of Merit of the benchmark designs.

In Figure 9, we performed a classification of the flip-flops in the benchmark designs according to their worst PIPB value and SET width on their input. The analyzed pulses have been selected with a width of 300 ps and 500 ps, accordingly with results exposed in subsection IV-B. B14 and B15 circuits implement respectively a subset of Viper and 80386 processors. These two circuits have a greater complexity and longer combinational chains than B05 and B12 making them more sensitive to PIPB effect. Indeed, function generators can introduce both compression and broadening of the pulses, but the broadening phenomenon affects a greater number of input pins than compression effect. Moreover, compressions effect

is usually weaker than the broadening effects, and it affects mainly wide pulses. For these reasons, designs with longer combinational chains are affected by greater PIPB effects. Moreover, we observed that SETs with an initial width of 500 and 700 ps are subjected to a weaker PIPB effect when reach the memory elements. Anyway, due to their greater initial width, even if they are subjected to a weaker PIPB coefficient, they are still wider than the SETs with a starting width of 300ps when they reach the memory elements and thence more critical.

The results we obtained are comparable to the ones reported in [17] for designs B12 and B14. In details, our experiments report for B12 and B14, in case of SET width of 300 ps, PIPB effects of 1.86 and 3.12 respectively. Similarly, the experiments described in [17] showed a PIPB effects on SETs with width 400 ps of respectively 2 and 3.

V. CONCLUSION

In this paper, we present a new workflow for analyzing the design reliability regarding SETs for circuits implemented on SRAM-based FPGAs. The methodology starts with predicting the generated SET with respect to the radiation particles and the device under the study. A new LUT layout model for SRAM based FPGA has been proposed which is used for modeling the behavior of SET propagating through the circuit. The developed workflow has been evaluated on ITC99 testbenches implemented on Xilinx Kintex-7 SRAM-based FPGA, identifying the critical memory elements of the selected testbench.

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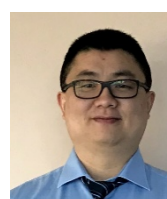
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