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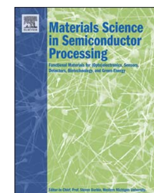

Trapping phenomena and degradation mechanisms in GaN-based power HEMTs

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ABSTRACT

This paper reports an overview of the most relevant trapping and degradation mechanisms that limit the performance and lifetime of GaN-based transistors for application in power electronics. Results obtained on state-of-the-art devices are described and discussed throughout the paper, with the aim of providing a clear description of the topic. The first part of the paper deals with the issue of dynamic-R_{on}: after describing a robust test strategy for the analysis of the pulsed characteristics of the devices, we discuss the voltage- and temperature-dependent pulsed I-V characteristics of 650 V-rated transistors, and the physical origin of dynamic R_{on} in these devices. The results demonstrate that through proper buffer optimization it is possible to reach negligible trapping at high voltage. The properties of the traps responsible for dynamic-R_{on} are also discussed in detail in the paper, based on drain-current transient data. A specific discussion is devoted to hot-electron trapping processes, that – under hard switching conditions – may lead to significant modifications in the resistance of the 2DEG.

The second part of the paper deals with device degradation: based on a wide set of experimental results, we describe the physical mechanisms responsible for the worsening of the properties of the devices. More specifically, we demonstrate that stress in off-state conditions may result in measurable changes in the pinch-off voltage, mostly consisting in a negative-threshold instability (NBTI). The origin of this shift is discussed in detail; we also demonstrate that in a real-life cascode configuration (where a low, subthreshold leakage current flows through the device in the off-state), NBTI effects are mitigated. Finally, we discuss the stability of the gate-stack, induced by the exposure to positive gate bias.

1. Introduction

Energy efficiency is one of the biggest challenges for electric and electronic engineers. Everywhere energy is generated, stored and transformed, there are losses, that must be minimized in order to reduce our environmental fingerprint. Nearly 10% of global electricity consumption goes into conversion losses. Power converters are everywhere, from laptop chargers to photovoltaic plants and electric vehicles. The key element of a switching power converter is the switch, a transistor which is continuously switched on- and off- with the aim of transferring energy from a source (mains, battery, PV modules, …) to the load (car engine, …). To fabricate low loss converters, it is necessary to improve and optimize the properties of the switching element. Silicon transistors have excellent structure and performance but, owing to the low breakdown field of Si (0.3 MV/cm) they have intrinsic limitations in terms of on-resistance. Recently, other semiconductors have emerged as alternatives to silicon, including GaN, SiC, Ga_2O_3. These materials have a wide energy gap, and therefore can be used for power applications. Among these, GaN has shown impressive advantages: first of all, the wide energy gap (3.4 eV) allows to reach high operating temperatures (> 350 °C [1]), thus permitting to minimize the size and weight of the heat sinks. A second advantage is the high mobility (> 1200 cm^2/V s) of the 2-dimensional electron gas (2DEG) formed at the interface between AlGaN and GaN, which leads to low channel resistance and high current density (> 1 A/mm [2]). The breakdown field of GaN (3.3 MV/cm) is 11 times higher than that of silicon (0.3 MV/cm): this has a direct impact on the on-resistance of the transistors. In fact, for the same breakdown voltage, a device based on GaN can be 11 times smaller than its silicon counterpart. Finally, GaN transistors have a low R_{on}*Q_g product (< 1 Ω*nC [3]), and this allows the minimization of the switching losses at system level, and to increase the operating switching frequency to the 100 kHz–MHz range. This

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permits to reduce the size of the passive components (capacitors and inductors), and thus of the power converters.

These properties of GaN have led device engineers to consider this material as an excellent candidate for the fabrication of the next generation power converters. Based on GaN, kW-range converters with efficiency in excess of 99% have already been demonstrated [4].

Several device technologies have been proposed and evaluated throughout the years. Schottky-gated HEMTs have the simplest structure, at the expense of a slightly higher gate leakage current with respect to the insulated-gate counterpart. Based on this approach, devices with breakdown voltage higher than 1100 V have been demonstrated in the literature [5]. An approach to reduce the gate leakage current while maintaining a good dynamic performance and reliability is to add a thin insulator under the gate, thus adopting a metal-insulator-semiconductor (MIS) approach. Also this approach allows to reach a high breakdown voltage, having the further advantage of permitting operation at positive gate bias without measurable gate current. MIS structures can be fabricated either by recessing the AlGaN layer under the gate (in this case, a positive threshold voltage – i.e. a normally-off behavior – is obtained) or by keeping the full AlGaN thickness both in the access regions and under the gate. In the latter case, the threshold voltage is negative. To achieve normally-off behavior, the devices are connected in cascode configuration with a silicon MOSFET [6]; both transistors are placed in the same package, to minimize space occupation and parasitic capacitances/inductances.

Normally-off operation can be obtained also by implementing specific strategies at device levels. Fluorine implantation in the gate region permits to deplete the channel under the gate, thus leading to a positive threshold voltage [7]. The stability of threshold voltage strongly depends on the optimization of the implantation process. Early papers indicated that F-ions may be unstable under bias/temperature stress [8], while more updated reports were able to demonstrate highly stable devices [9]. A further approach [10] consists in using a p-InGaN cap layer; this allows to reach normally-off operation by employing the polarization-induced field in the InGaN cap and the negative charge in the p-InGaN. Normally-off devices were also demonstrated by using a self-aligned n^{++}GaN/InAlN/AlN/GaN MOS approach, capable of threshold voltages between 1.3 and 3.7 V depending on the gate oxide thickness [11]. Another, widely used, approach for normally-off operation consists in adding a p-GaN layer under the gate metal [12]. The use of a p-GaN layer, due to the high-acceptor doping, leads to a significant depletion of the channel beneath the gate, thus permitting to reach threshold voltage levels in the range 1–2 V.

Independently of the structure, for power devices the robustness against high voltage/high temperature stress represents the most important target to be satisfied. Several publications (see for instance [13–17]) pointed out that GaN power transistors may show a recoverable increase in on-resistance (often referred to as dynamic-R_{on} increase), when they are exposed to high off-state bias. This may originate to trap states located either at the surface or in the buffer. Surface trapping can be solved through a careful optimization of the surface treatments. On the other hand, buffer trapping still remains an issue, if the properties of the epitaxial structure are not carefully engineered [18]. In the first part of this paper we will discuss the physical processes responsible for buffer trapping in GaN-based power HEMTs. Without loss of generality, the results will refer to insulated-gate devices rated for 650 V operation. We demonstrate that through the optimization of device structure it is possible to achieve negligible-dynamic R_{on} at 600 V, 150 °C. This result indicates that GaN transistors can be highly competitive with their silicon counterpart for application in power switching devices. In addition, we discuss also the trapping processes related to the presence of hot-electrons, which may affect device performance when the transistors are operated in hard-switching conditions.

With regard to stability and reliability, we describe the impact of stress in off-state conditions, and we discuss the threshold voltage instabilities induced by off-state stress. We also analyze the impact of positive gate stress on MIS-type transistors.

The up-to-date data presented within this paper provide a detailed overview on the state-of-the-art of normally-on GaN technology for power conversion. Several considerations (e.g. those related to buffer trapping processes) can be extended also to normally-off devices, thus providing general guidelines to minimize the impact of charge trapping processes. Normally-off GaN devices may suffer from gate-related degradation processes similar to those described within this paper, if they are based on the MIS/MOS approach; other factors may affect the performance of transistors with a p-type gate, due to the specific nature of their structures and materials.

2. Experimental details

The results described within this paper were obtained on GaN-on-Silicon power transistors. The epitaxial structure was grown by metal-organic chemical vapour deposition (MOCVD), and consists of an AlN/AlGaN/GaN strain relief layer, a thick C-doped GaN layer, an unintentionally-doped GaN channel layer, and an AlGaN barrier layer. The final step in the fabrication process was the in-situ growth of the 50 nm SiN layer, which was used both as a gate insulator and as a first passivation in the access regions. The fabricated devices have a threshold voltage around −10 V, and are designed for use in cascode configuration. The maximum voltage/current rating of this technology is 650 V/100 A, with on-resistance below 10 mΩ. For most of the experiments we used small test structures, having a gate width of 200 µm. To investigate the charge trapping processes, the devices were submitted to pulsed and transient characterization at several temperature/current levels. Details on the measurement setup and conditions are given below. A set of stress tests was then carried out under off-state and semi-on state conditions; data on the main device parameters (on-resistance, threshold current, electroluminescence signal, …) were collected throughout the experiments, with the aim of describing the stress kinetics and gathering information on the degradation processes.

3. Results and discussion

3.1. Physical origin of dynamic-R_{on}

Several strategies have been implemented for the investigation of dynamic-R_{on} in GaN-based power HEMTs. In our case, we developed a custom setup, which gives us the maximum freedom of changing the main measurement parameters, and the possibility of exploring different time/voltage/temperature ranges.

Fig. 1 reports a detailed schematic of the custom system used for the execution of pulsed and transient measurements on GaN-based power HEMTs. Two large bandwidth arbitrary waveforms generators (AWGs) are used to generate the control pulses to be applied to the gate and the drain. The signal is then amplified through two power amplifiers having proper dynamic response, and used as an input to the gate and drain terminals. Between the drain amplifier (V_{DD}) and drain terminal (V_{DS}), a load resistor is placed. This load resistor is used to measure the drain current, by evaluating its voltage drop through a differential voltage probe. The drain-source voltage is also measured, with the aim of providing a full characterization of device properties.

The system can operate both in pulsed and in transient mode. In pulsed mode, an off-state bias (V_{GSQ}, V_{DSQ}) (with a gate voltage smaller than the threshold voltage and a high drain bias) is used to induce charge trapping. A pre-trapping phase (typically 10–100 s) is applied, to fill all the traps and reach a steady-state condition. Then, a square wave bias is applied to the gate and the drain of the devices, as schematically shown in Fig. 2. The off/on ratio is typically very high, around 99%, to maximize the effects of charge trapping. During the off-state phase (which lasts 2 ms in Fig. 2), the traps are filled, while the current is measured during short (20 µs) on-state pulses, in order to avoid charge

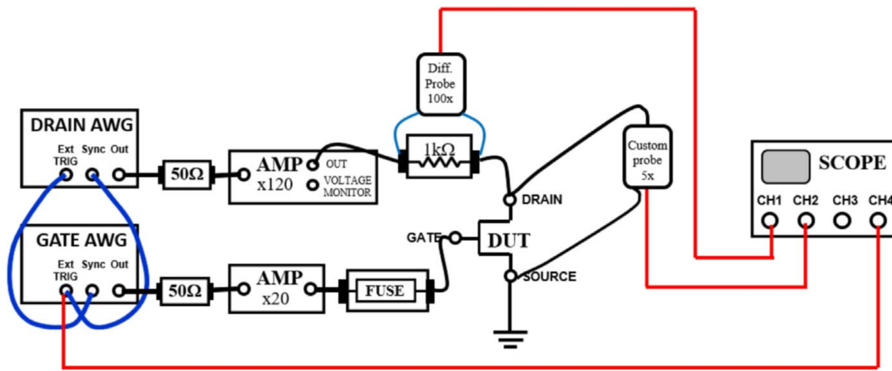

Fig. 1. Schematic drawing of the custom system used for the execution of pulsed and transient measurements on power GaN HEMTs.

de-trapping during the pulsed current-voltage (PIV) measurement. It can be easily understood that these conditions constitute a worst-case scenario. In fact, in real-life operation, the devices are operated with a much smaller off/on ratio, and may have time to de-trap part of the carriers during the on-state phase. The measurements are carried out at several trapping voltages and temperatures, in order to evaluate how the main driving forces (temperature, electric field) favor charge trapping during operation.

Fig. 3 reports the pulsed-IV curves measured on a state-of-the-art device at room temperature, with a maximum trapping voltage of 600 V. As can be noticed, the device shows negligible increase in on-resistance, at 600 V. The on-resistance peaks at trapping voltages near 200–300 V, and then decreases again at higher trapping bias.

A more detailed description of dynamic-R_{on} is given in Fig. 4, which reports the dependence of on-resistance on the trapping voltage and temperature, in the range 0–600 V and 30–150 °C, which is relevant for real-life operation [15]. As can be noticed, the on-resistance has a non-monotonic dependence on the trapping voltage in the whole set of measurement conditions. Such behavior can be explained by considering the schematic diagram in Fig. 5. When a moderate trapping voltage is applied to the devices in the off-state (e.g. $V_{GSQ} = -20$ V, $V_{DSQ} = 200$ V, region A in Fig. 4), the carbon-doped buffer is partly depleted. The carbon acceptors are located at Ev + 0.9 eV, and are then ionized, thus acquiring a negative charge state. As a consequence, dynamic R_{on} increases in the voltage range up to 2–300 V.

For higher voltages (V > 200–300 V, region B in Fig. 4), charge is re-distributed within the structure due to the increase in the drain-to-substrate leakage components. Band-to-band leakage processes may also lead to a positive charge storage at the interface with the strain-relief layer [18], due to the neutralization of the ionized acceptors or to the ionization of donor states (Fig. 5). This explains why for voltages higher than 2–300 V the dynamic-R_{on} shows a decrease and recovery. It is worth noticing that this recovery is almost complete at 600 V (Fig. 4), thus indicating that current device technologies allow to reach negligible-dynamic-R_{on} at high voltage levels. A lateral redistribution of charge may also take place and influence the overall dynamic on-resistance [19].

Vertical leakage current increases with temperature [20]: this explains why the transition between region A and B in Fig. 4 moves towards lower voltages at higher temperatures. The results described above provide a clear indication of the pathway for minimizing dynamic on-resistance in GaN-based transistors. First, the influence of carbon doping on 2DEG concentration must be minimized, through proper optimization of the C-doping level and of the thickness of the unintentionally-doped GaN. Second, leakage through the unintentionally-doped GaN layer must be optimized, in order to favor charge-redistribution through the structure (that leads to a complete suppression of dynamic R_{on}) without reaching an excessive vertical leakage current. Based on this optimization, devices with negligible dynamic-R_{on} both at room temperature and high temperature have been demonstrated within this work, as shown by the dynamic-R_{on} measurements in Fig. 6.

The properties of the trap levels responsible for dynamic-R_{on} can be investigated by means of drain-current transient measurements. Here

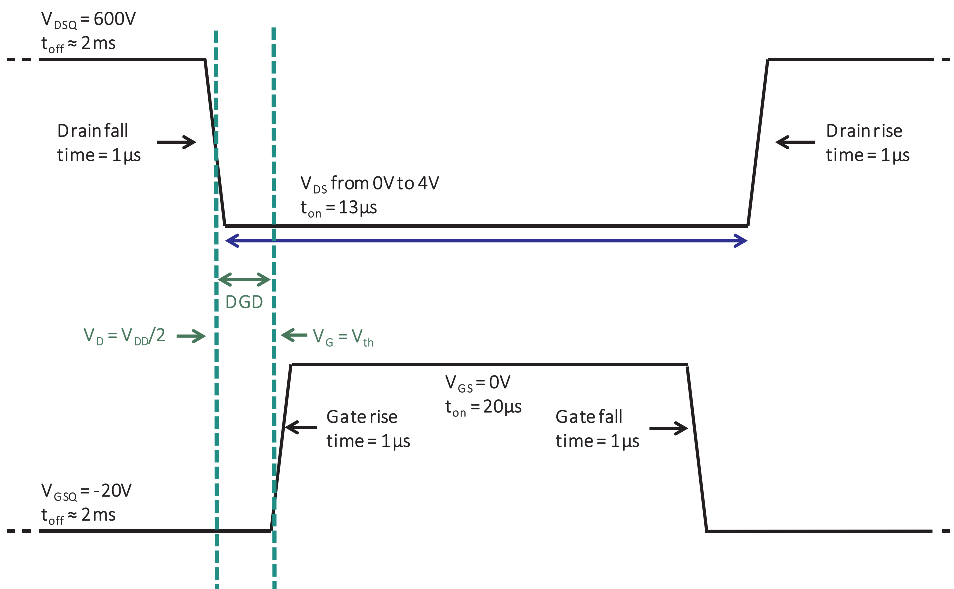

Fig. 2. Schematic drawing of the experimental conditions used for pulsed current-voltage measurements.

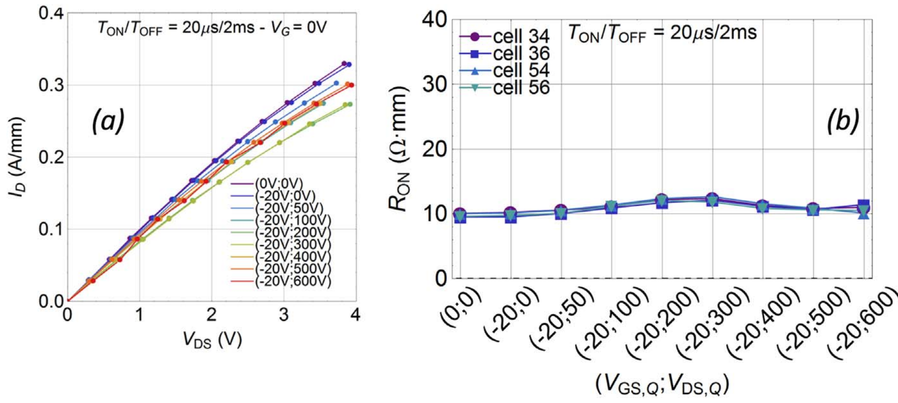

Fig. 3. (a) Pulsed-IV curves measured at room temperature on a GaN-based power HEMT. (b) Dependence of on-resistance on the applied trapping bias (the four lines refer to four devices sitting on different locations on the wafer).

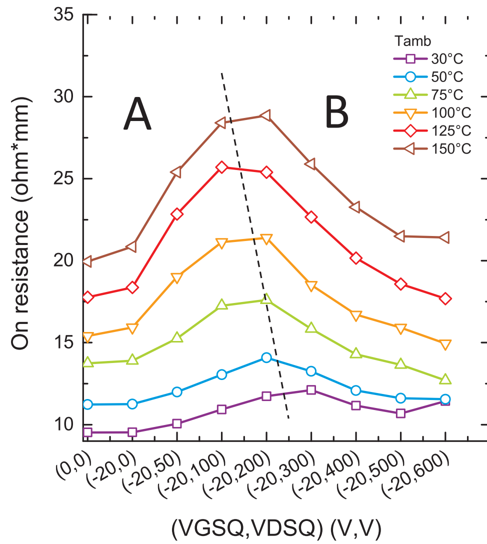

Fig. 4. Dependence of dynamic-R_{on} (as measured from pulsed I-V measurements) on trapping voltage and temperature.

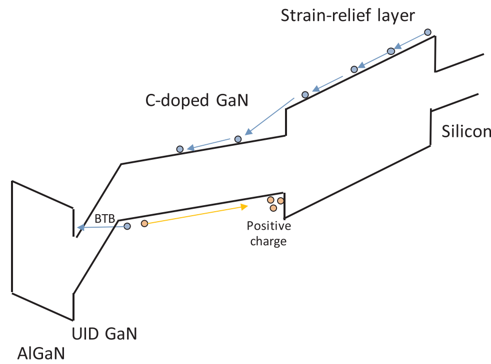

Fig. 5. Schematic representation of the mechanisms responsible for non-monotonic dynamic-R_{on} as a function of trapping voltage.

the idea is the following: an off-state (trapping) bias is applied for a relatively long time (100 s), by means of the setup in Fig. 1. The device is then switched to the on-state, and the variation of on-resistance over time is evaluated in the time-range between 100 µs and 1000 s. The measurement is then repeated at several temperature levels, in order to extrapolate the activation energy of the traps. The derivative of the R_{on} transients is then plotted, to describe the time constants as a series of peaks. Fig. 7 reports the results obtained on the same samples as in Fig. 4. As can be noticed, the time constant of the de-trapping process ranges between 0.3 s and 10 s in the temperature range between 110 °C and 170 °C. A single de-trapping process is observed, having activation energy around 0.63 eV (see the Arrhenius plot in Fig. 8). Activation energies in the range 0.6–0.9 eV are typically ascribed to carbon acceptors in GaN [21,22]. The predicted energy of carbon on nitrogen site (C_N) is 0.9 eV; however, the recovery kinetics of R_{on} may be significantly influenced by the vertical and lateral redistribution of carriers through the structures [23], and this may slightly change the activation energies with respect to theoretical predictions.

The trapping mechanisms described above are induced by the exposure to off-state conditions, i.e. by the ionization of buffer traps, or by the flow of leakage current through the structure. During real-life operation, GaN transistors can be subject also to hard-switching transitions, when they are switched from off- to on-state. A peculiar aspect of hard switching events is that the devices are simultaneously subject to high electric field and high 2DEG current. Under these conditions, a second factor promotes charge trapping: the presence of hot electrons. Hard switching conditions may be present in a boost power converter, see the schematic drawing in Fig. 9. When the transistor is turned on, its drain-source voltage is very high (600 V), and has to decrease rapidly, as the device reaches the linear region. At the same time, the transistor turns on, and current starts flowing through the channel. The electrons that flow through the 2DEG during the switching event are significantly accelerated by the electric field, thus becoming "hot", and may be injected either into the buffer or at the surface, thus leading to an increase in on-resistance.

In order to understand if under hard-switching conditions there are additional trapping processes that promote charge trapping with respect to off-state operation, we developed a specific experimental setup, whose operating principle is similar to that reported in Fig. 2, but with variable overlapping between the drain and gate pulses. The transistor has a resistive load, and the gate and drain terminals are controlled by two independent pulsers. The timing of the pulsers can be modified, by changing the delay between gate and drain (drain-gate delay, DGD), with the aim of obtaining negligible overlapping between the gate and drain waveforms (no hot electron trapping, DGD > 0), or considerable hot-electron trapping (with DGD < 0). DGD is defined as the time from when the drain voltage decreases to 50% of its maximum value to when the gate voltage increases above the threshold voltage of the device (i.e. when current starts flowing through the channel).

Fig. 10 reports the pulsed I-V curves measured starting from different quiescent bias points under soft switching (DGD > 0) and hard switching (DGD < 0) conditions. As can be noticed, the curves measured under soft switching conditions (DGD = 2.2 µs and DGD = 0.2 µs) show the same behavior already described in Fig. 3, i.e. a non-monotonic increase in on-resistance as trapping voltage is increased from V_{DSQ} = 0 V to V_{DSQ} = 600 V. On the other hand, when the switching transition is "hard", i.e. when there is a considerable overlapping between the drain and gate waveforms, dynamic-R_{on} increases monotonically with voltage. A better description of this behavior is

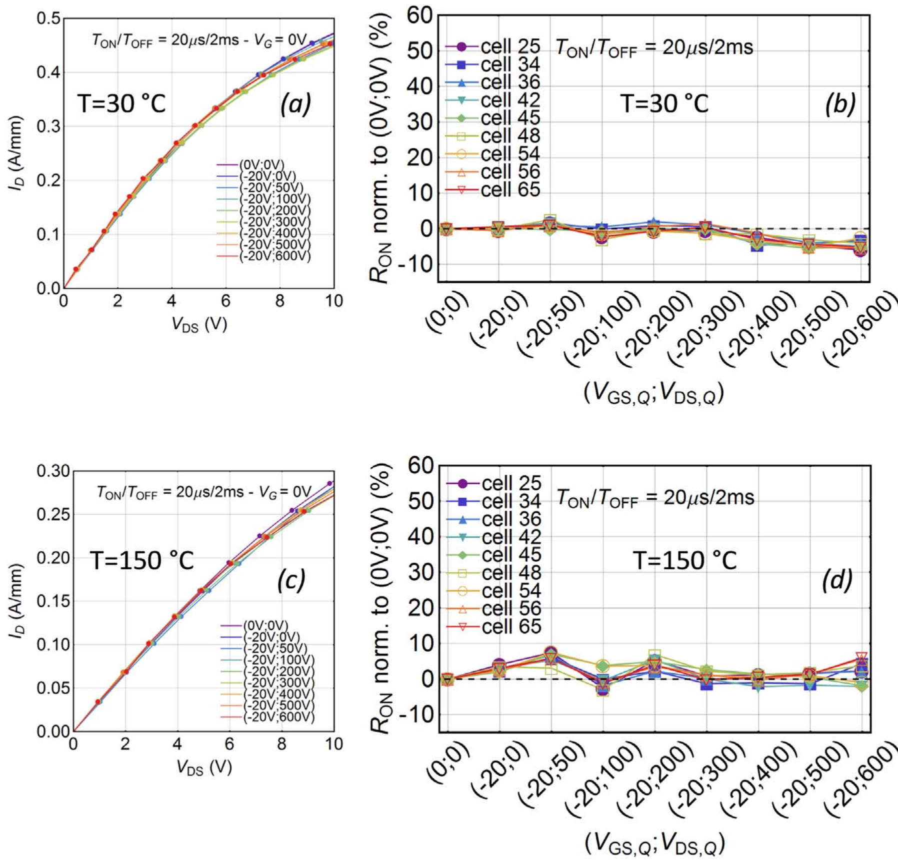

Fig. 6. Results of pulsed-IV measurements carried out on an optimized device up to V_{DSQ} = 600 V, both at room temperature (a) and high temperature (c). (b) and (d) represent the dependence of dynamic-R_{on} (normalized to the value measured with no trapping bias) on trapping voltage. Each line refers to an individual device on the wafer. The measurements are shown both at 30 °C (b) and 150 °C (d).

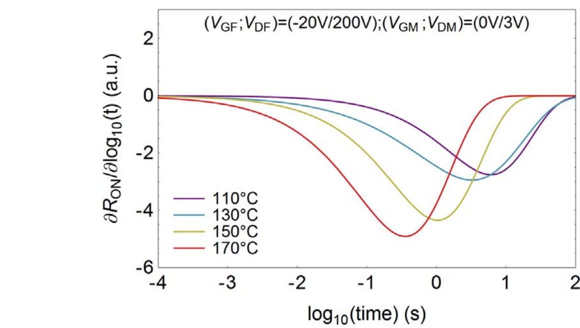

Fig. 7. Drain-current transient spectra (derivatives of the dynamic on-resistance transients) measured with a trapping bias of V_{GSQ} = −20 V, V_{DSQ} = 200 V at different temperature levels.

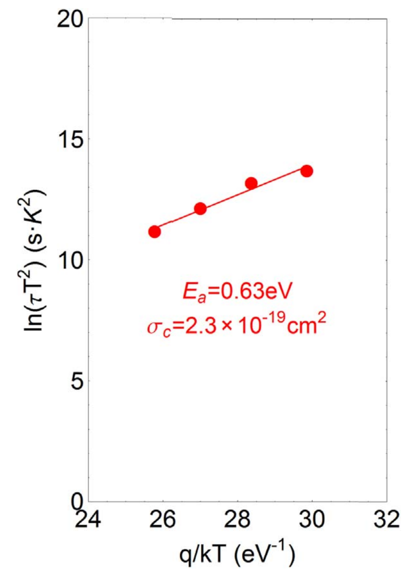

Fig. 8. Arrhenius plot for the de-trapping process shown in Fig. 7.

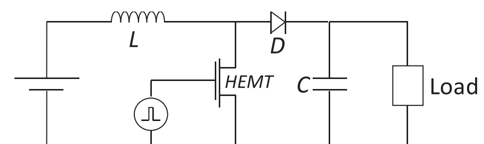

Fig. 9. Schematic representation of a boost power converter.

given by Fig. 11, that reports the dependence of dynamic-R_{on} on the trapping voltage and on the overlapping between gate and drain waveforms DGD. As can be noticed, for DGD < 0 (i.e. for a hard switching transition) dynamic-R_{on} is considerably enhanced with respect to soft-switching transitions, for high V_{DSQ} > 400 V. It is worth noticing that the hard switching intervals reached during these tests (≈ 1 μs) are more stressful than in real-life operation (10–100 ns). This choice was done to reproduce the worst-case scenario in our tests.

To confirm the role of hot electrons in favoring charge trapping during a hard switching transition we carried out electroluminescence measurements during pulsed operation with different values of DGD. Typically, HEMTs emit a weak electroluminescence signal, which originates from the deceleration of the highly-energetic electrons present in the channel (Bremsstrahlung). The intensity of the EL signal is proportional to both the amount of electrons in the channel (drain current, I_D) and to the accelerating field. Fig. 12 reports three frames, representing the EL signal measured during pulsed operation in soft-switching (DGD > 0) and hard switching (DGD < 0). As can be noticed, no significant EL signal is measured in soft switching operation, since no current flows through the channel of the devices. On the contrary, a

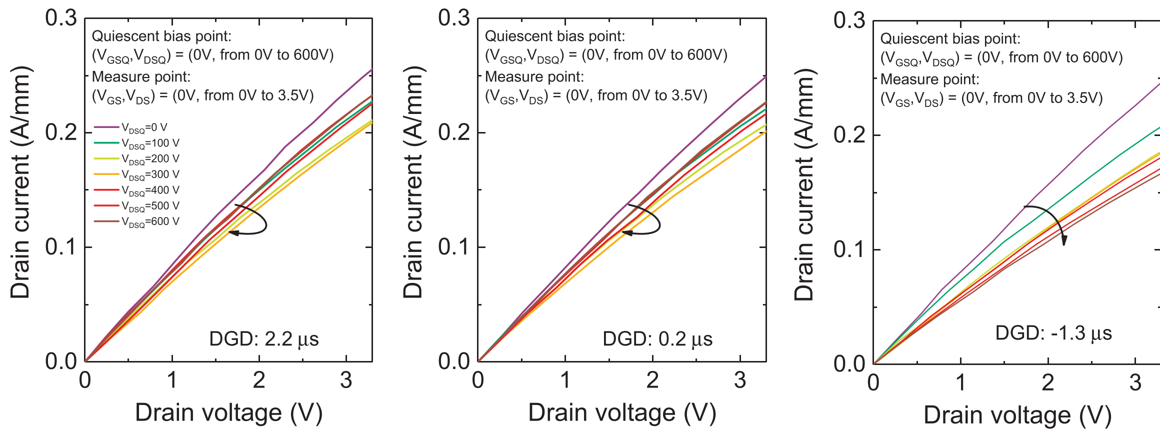

Fig. 10. Pulsed I-V curves collected by inducing trapping in three different conditions: soft-switching (DGD > 0 and DGD ≈ 0), and hard switching (DGD < 0).

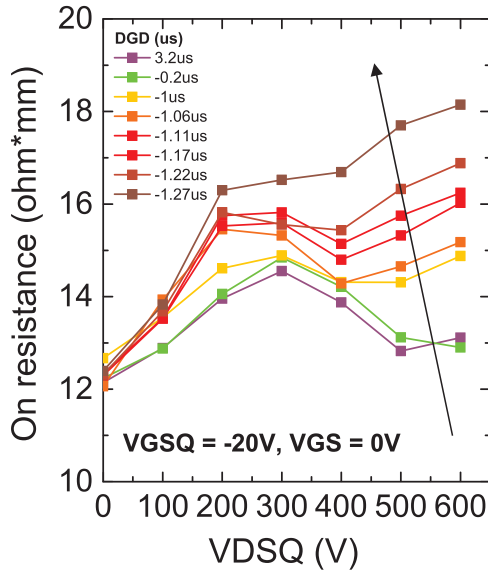

Fig. 11. Dependence of dynamic-R_{on} on the trapping voltage V_{DSQ} and on the overlapping (DGD) between the gate and drain waveforms.

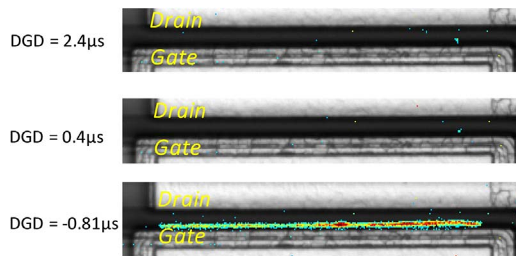

Fig. 12. EL patterns measured during soft and hard switching transitions.

significant EL signal is emitted during hard switching transitions (DGD < 0). The luminescence signal is emitted evenly along the channel, and peaks on the gate edge on the drain side, i.e. where the electric field is maximum. Remarkably, the on-resistance increase induced by hot-electrons was found to decrease at higher temperatures (not shown here for brevity). This is consistent with the hypothesis that hot electrons are responsible for trapping. In fact, at higher temperatures the average energy of the electrons in the channel decreases, due to the increased scattering with the lattice and to the corresponding decrease in the mean-free path over which the electrons are accelerated. For this reason, hot-electron effects are less prominent at high temperature levels.

3.2. Degradation processes

GaN-based transistors are designed to operate at high voltages (> 600 V) and temperature (> 125 °C) levels. For this reason, it is of fundamental importance to study the field-related and the temperature-activated degradation processes. Degradation may be gradual or catastrophic. Typically, gradual degradation consists in a parametric shift in threshold voltage and/or in on-resistance, which is induced by the exposure to high off-state bias. Catastrophic degradation may originate from the failure of dielectric submitted to high electric field, and/or of the III-N layer subject to extremely high voltages. In this section, we describe the two most relevant degradation mechanisms that may take place in GaN-based power MIS-HEMTs submitted to stress. The first process is the threshold voltage instability induced by off-state stress at high temperatures (high-temperature, reverse bias, HTRB), while the second one is the failure of the gate dielectric under positive gate bias.

In this session, we refer to HTRB, high temperature reverse bias, as the stress condition applied to induce the degradation of the devices. NBTI means negative bias temperature instability, a negative shift in threshold voltage induced by the exposure to high bias and temperature. Typically, the robustness of GaN transistors against HTRB is evaluated by exposing the devices to a constant voltage stress experiment. The gate is kept at negative values (for normally-on devices), in our case V_{GS} = −20 V, while the drain is at high voltage (V_{DS} > 520 V). Our system gives us the possibility of repeatedly interrupting the stress experiment to carry out quick I_D-V_{GS} and I_D-V_{DS} measurements. This allows us to monitor the main device parameters, and to investigate how/if the exposure to long-term off-state bias influences the threshold voltage and the on-resistance of the devices.

All the samples were stressed with V_{GS} = −30 V, and different drain voltages ranging from 0 V to 750 V. Fig. 13 reports the I_D-V_{GS} curves measured during a 1000 s stress experiment carried out at 150 °C, with a drain voltage of 520 V. Source was grounded during stress. As can be noticed, stress with V_{DS} = 0 V and negative gate voltage does not result in a significant threshold voltage shift. On the contrary, when a high drain bias is applied, threshold voltage shifts towards more negative values (negative bias temperature instability, NBTI). This effect is stronger at higher drain voltages, and only slowly recoverable. At V_{GS} = −30 V, V_{DS} = 520 V, T = 150 °C we measured a −5 V shift in threshold voltage (see Figs. 13 and 14). A significantly smaller variation (−1.5 V) was found at room temperature, by applying the same voltages to the devices (not shown for sake of brevity). Fig. 13(b) reports the threshold voltage variation measured during a recovery experiment, as can be noticed, the recovery of threshold voltage is very slow, even when the device is kept at zero bias and high temperature. The negative threshold shift originates from the presence of defects at the interface between the AlGaN barrier and the gate insulator and/or in the gate insulator (see the schematic drawing in

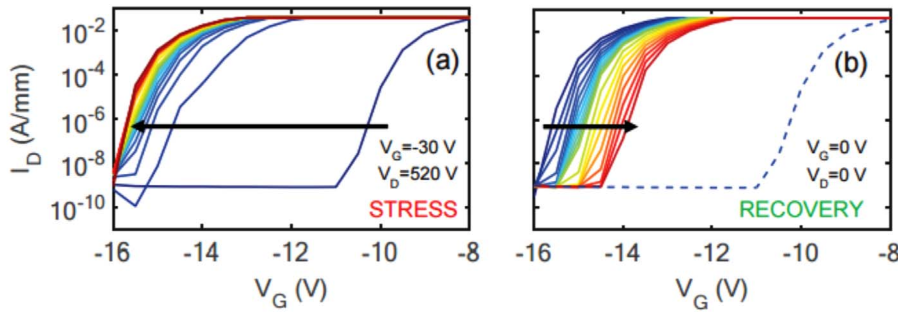

Fig. 13. I_D-V_{GS} curves measured repeatedly during a constant-voltage experiment, in off-state. The curves were taken during a stress having a total duration of 1000 s. To give a more accurate description of the variation of the main device parameters (V_{th} and R_{on}), in Figs. 14 and 16 we report the values of V_{th} and R_{on} extrapolated from these plots as a function of stress time (see the curves at V_{DS} = 520 V). ©2017 IEEE. Reprinted with permission from Dalcanale et al. [26].

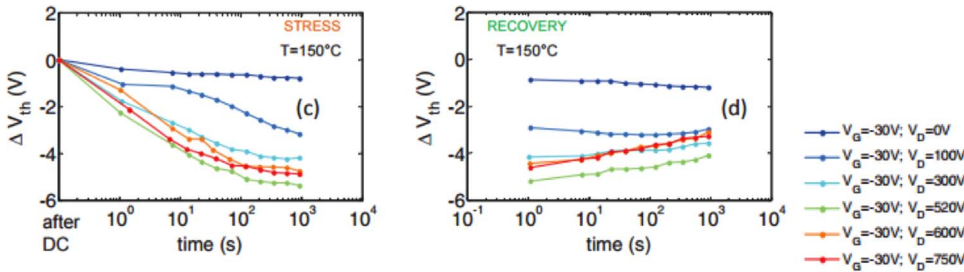

Fig. 14. Variation in threshold voltage during a set of constant voltage stress experiments, with different levels of V_{DS} (and the same value of V_{GS} = −30 V). The frame on the left shows the stress test, the one on the right the subsequent recovery at 0 V. ©2017 IEEE. Reprinted with permission from Dalcanale et al. [26].

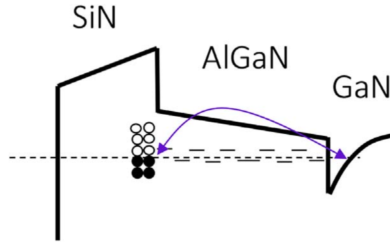

Fig. 15. Schematic representation of the process responsible for negative threshold voltage shift in GaN-based MIS-HEMTs.

Fig. 15, see also [16,24]). When a reverse bias is applied between gate and drain, the electrons trapped at these states are emitted and transferred to the channel. This results in a reduction of the net negative charge under the gate, and thus in a negative shift of the threshold voltage. During the recovery experiment, the electrons are transferred back towards the interface defects. Recovery is very slow, since the electrons have to move against the electric field. In addition, once the electrons are trapped back at the interface between SiN and AlGaN, they have a repulsive (electrostatic) action that limits the rate at which electrons are injected back from the channel to the interface. It is worth noticing that, in principle, also trapping in the buffer may affect the threshold voltage of the devices and induce NBTI/PBTI effects.

In most cases, GaN-based MIS-HEMTs are designed to be used in cascode configuration, and mounted in a double chip package along with a silicon MOSFET. The on/off-state of the cascoded ensemble is controlled by the silicon MOSFET, so a negative threshold voltage shift of the HEMT does not affect the performance of the GaN HEMT. The parameter which is very important for real-life applications is the on-resistance. For this reason, we evaluated the variation in on-resistance induced by HTRB stress in GaN-based MIS-HEMTs. As shown in Fig. 16, on-resistance is not affected by long-term HTRB stress. Fig. 17 reports the I_D-V_{DS} curves measured repeatedly during a stress test at V_{GS} = −30 V, V_{DS} = 750 V, T = 150 °C. No significant change is detected. This result indicates that currently available technologies have a high stability under high voltage/temperature stress. This is of high importance for the development of reliable power converters.

A permanent degradation of GaN-based MIS-HEMT may occur under positive gate voltage, when the gate bias is so high that the electric field in the silicon nitride insulator exceeds its breakdown field (typically higher than 6–7 MV/cm). The robustness of GaN-based MIS-HEMTs against positive gate bias can be evaluated by means of a step-stress experiment. An example is shown in Fig. 17: in this case, a GaN-based MIS-HEMT was submitted to stress at positive gate bias, with zero bias applied between drain and source. The stress voltage applied to the gate was increased by 0.5 V every 120 s, until failure was reached. The staircase line in Fig. 17 indicates the stress voltage at a given stress time, while the colored line shows the variation of device current during each step of the experiment. As can be noticed, the current flowing through the gate remains well below the measurement limit of the instrument until the stress voltage becomes higher than 22 V. This result indicates that the (thick) gate insulator can block the leakage current in a very efficient way. For higher stress voltages (22 V < V_{GS} < 37 V), a significant current starts flowing through the gate. As shown by the band diagram in Fig. 17, at positive gate voltages most of the potential drops on the SiN insulator, since the 2DEG – which is at zero volt – is formed at the AlGaN/GaN interface. At high stress

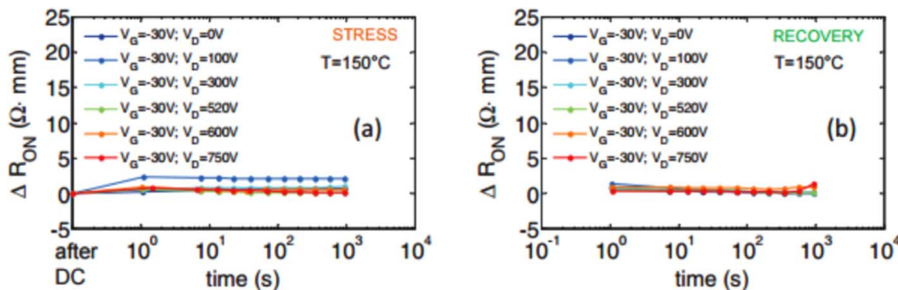

Fig. 16. Variation in on-resistance during a set of constant voltage stress experiments, with different levels of V_{DS} (and the same value of V_{GS} = −30 V). The frame on the left shows the stress test, the one on the right the subsequent recovery at 0 V. ©2017 IEEE. Reprinted with permission from Dalcanale et al. [26].

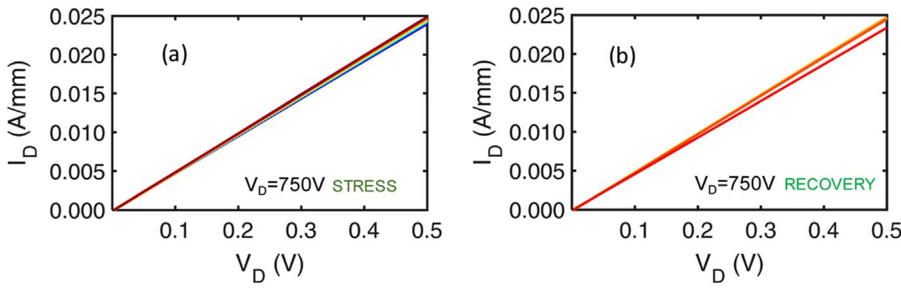

Fig. 17. I_D-V_{DS} curves measured during a 1000 s stress test at $V_{GS} = -30$ V, $V_{DS} = 750$ V, T = 150 °C. The frame on the left shows the stress test, the one on the right the subsequent recovery at 0 V. No significant variation is observed. (For interpretation of the references to color in this figure, the reader is referred to the web version of this article.)

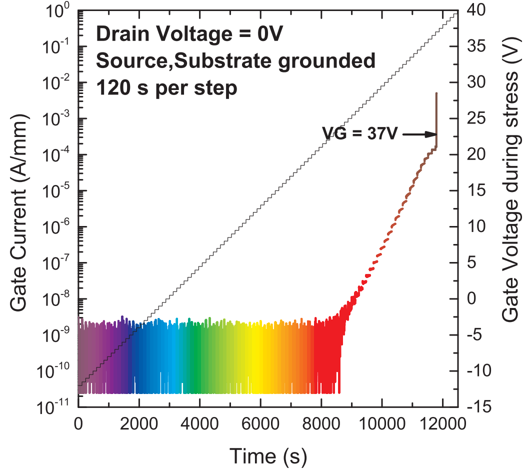

Fig. 18. Gate current measured during a gate-step stress. Gate voltage is increased every 120 s until failure is reached. The staircase line indicates the gate voltage, while the colored-line represents the gate current flowing through the structure during stress time. The stress temperature is 25 °C. (For interpretation of the references to color in this figure legend, the reader is referred to the web version of this article.)

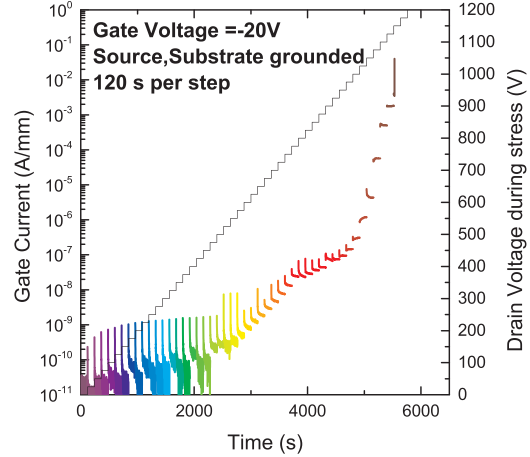

Fig. 20. Gate current measured during a drain-step stress, carried out in the off-state. Drain voltage is increased every 120 s until failure is reached. During stress time, the gate-source voltage is fixed at $V_{GS} = -20$ V. The staircase line indicates the drain voltage, while the colored-line represents the gate current flowing through the structure during stress time. Failure is reached at $V_{DS} = 1150$ V. (For interpretation of the references to color in this figure legend, the reader is referred to the web version of this article.)

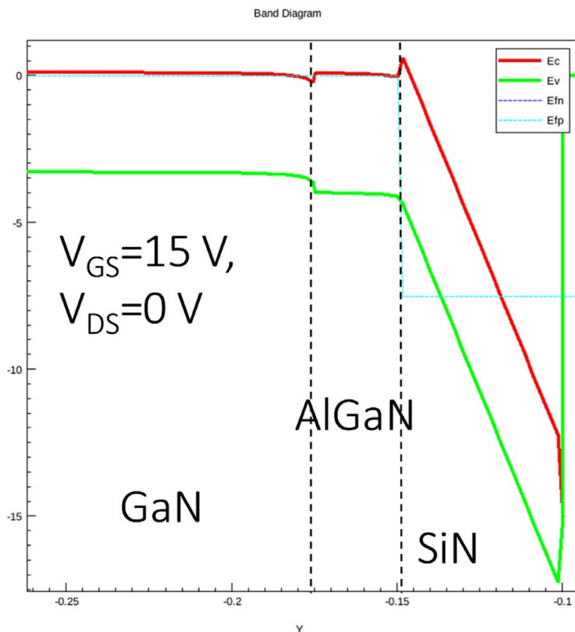

Fig. 19. Simulated band diagram under positive gate bias ($V_{GS} = 15$ V). The band diagram refers to a cut under the gate, and is simulated with $V_{DS} = 0$ V. The simulation refers to a device with a SiN thickness of 50 nm.

voltages, electrons from the 2DEG can be injected towards the gate insulator, and be collected by the gate metal. This results in a measurable gate current that, for extremely high gate voltages (36 V) – may reach the level of 100 µA/mm. The injected electrons are accelerated by the high electric field in the SiN, and this may generate a measurable electroluminescence signal due to the deceleration of these electrons at the gate metal. A catastrophic failure is reached at $V_{GS} = 37$ V, which on a 50 nm SiN layer, corresponds to an electric field of 7.4 MV/cm.

Evaluating the robustness of a MIS-HEMT at positive gate bias allows to study the breakdown limits of the gate insulator. In fact, at positive gate bias the electric field in the SiN is uniform, since the system can be assimilated to a 2-plates capacitor, where the positive plate is the gate metal, and the negative is the 2DEG. Under off-state/semi-on state conditions, the distribution of the electric field is significantly different, with the peak of the field being located at the edge of the gate on the drain side or at the drain contact [25], depending on the applied voltage. To evaluate the robustness of MIS-HEMTs in off-state conditions, we carried out a set of step-stress experiments in the off-state. The gate voltage was kept at $V_{GS} = -20$ V, while the drain voltage was increased until failure. State-of-the-art devices rated for 650 V operation showed a catastrophic failure only for $V_{DS} > 1150$ V (see a representative example in Fig. 17), indicating the good stability of the analyzed technology (Figs. 18–20).

4. Conclusions

In summary, with this paper we have presented an extensive overview of the main trapping and degradation processes that affect the performance and reliability of GaN-based HEMTs for power applications. In the first part of the paper, we have described the physical origin of dynamic-R_{on}, and its temperature dependence. In addition, we have discussed the different trapping mechanisms that may be triggered by off-state and semi-on state conditions. In the second part of the paper we have discussed both the gradual/recoverable and the permanent

degradation mechanisms of GaN-based MIS-HEMTs. The results described within this paper indicate that through careful growth and process optimization it is possible to fabricate devices with negligible dynamic-R_{on} at 600 V/150 °C, and with high robustness against HTRB stress and off-state step-stress. These devices are expected to find wide application in next generation power converters.

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