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Retraction

Retracted: A High-Efficiency, Low-Cost Solution for On-Board Power Converters

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This article has been retracted as it is essentially identical in content with a previously published paper titled "A Demagnetization Circuit for Forward Converters," by G. M. Ponzo, G. Capponi, P. Scalia, and V. Boscaino. This manuscript was published in the Proceedings of the 6th International Conference on Electrical Engineering/Electronics, Computer, Telecommunications and Information Technology, 2009 (ECTI-CON 2009) [1].

References

[1] V. Boscaino and G. Capponi, "A high-efficiency, low-cost solution for on-board power converters," *Advances in Power Electronics*, vol. 2012, Article ID 259756, 12 pages, 2012.

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Research Article

A High-Efficiency, Low-Cost Solution for On-Board Power Converters

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Wide-input, low-voltage, and high-current applications are addressed. A single-ended isolated topology which improves the power efficiency, reduces both switching and conduction losses, and heavily lowers the system cost is presented. During each switching cycle, the transformer core reset is provided. The traditional tradeoff between the maximum allowable duty-cycle and the reset voltage is avoided and the off-voltage of active switches is clamped to the input voltage. Therefore, the system cost is heavily reduced and the converter is well suited for wide-input applications. Zero-voltage switching is achieved for active switches, and the power efficiency is greatly improved. In the output mesh, an inductor is included making the converter suitable for high-current, low-voltage applications. Since the active clamp forward converter is the closest competitor of the proposed converter, a comparison is provided as well. In this paper, the steady-state and small-signal analysis of the proposed converter is presented. Design examples are provided for further applications. Simulation and experimental results are shown to validate the great advantages brought by the proposed topology.

1. Introduction

On-board power converter technology has extensively matured over the last two years. Until recently, the industry was manufacturing converters from 5 W of power to, at most, 30 W. Today, converter power levels are increasing to 50, 100, 300, and even 400 W in miniature sizes. These are rather dramatic improvements in a relatively short period of time. High-power converters are physically much smaller than their predecessors, achieving energy density levels of 50 W per cubic inch without the required external heat sink. Recently, distributed power architectures for telecommunications and data-computing systems have received a great deal of attention. With the spread of wide-input, low-voltage, and high-current applications, many topologies have been proposed to improve the efficiency, power density, and cost of the whole system.

The well-known forward converter is still the most suitable topology for medium power levels, well-suited for low-voltage and high-current applications [1, 2]. Yet, in forward converters an external circuit is required to achieve the core reset. By adding an auxiliary winding, the energy stored in the transformer could be recycled to the input rail but increasing the cost and complexity of the power supply. Otherwise, the energy is lost in the reset circuit, as in the Resistor-Capacitor-Diode (RCD) network [3–5]. The active clamp is actually the best-suited and most effective reset technique. A resonant path is provided and the transformer energy is firstly stored in the resonant path and then returned back to the transformer primary side [6, 7].

Despite several techniques have been proposed, reduced efficiency and increasing cost are unavoidable drawbacks of an external core reset. A tradeoff between the off-voltage of active switches and the maximum duty-cycle is introduced by each reset technique: if a wider duty-cycle range is required, the off-voltage of active switches will increase. Note that in a traditional forward topology widening the duty-cycle range is the only way to meet wide-input applications requirements. Since the cost of active switches is mainly determined by the off-voltage, at worst the forward converter

will not be suited for wide-input, low-voltage applications thus loosing the chance of a high-efficiency, inexpensive and low parts count solution.

This paper proposes a single-ended single-stage isolated converter which overcomes all drawbacks emphasizing all benefits of the traditional forward topology. The converter is a low-cost, high-performance solution for wide-input low-voltage applications. The converter features high-efficiency, high power density and low electromagnetic interference. The core reset is achieved without external circuits and the tradeoff between the duty-cycle range and the off-voltage is definitively avoided. Zero-voltage switching is achieved thus improving the power efficiency. The converter is intrinsically well-suited for wide-input applications. Since high-current applications are targeted, the continuous conduction mode is assumed. The steady-state and dynamic analysis are carried out and a comparison with the active clamp forward converter is provided as well. Simulation and experimental results are shown to test the efficiency of the proposed solution.

2. The Active Clamp Forward Converter

Figure 1 shows the well-known active clamp forward converter topology. A detailed analysis is provided in [8, 9]. Yet, for the sake of clarity main features are summed up in this section. The reset capacitor is connected in series with the auxiliary MOSFET in order to achieve the core reset. The auxiliary and the main MOSFETs are driven out of phase. The output capacitances of M1, D1, D2 and the transformer winding capacitance are collected in the C_{x1} capacitor, also called lump capacitor.

During the on-time, M1 is turned on and the magnetizing inductance stores energy from the input rail. During the off-time, the auxiliary MOSFET M2 is switched on to achieve the core reset. The magnetizing current is diverted in the reset path. A resonance occurs between the magnetizing inductor and the equivalent resonant capacitor which consists of the reset capacitor C_{cl} and the lump capacitor. The active clamp technique forces a "reverse" magnetizing current to flow through the transformer for a small portion of the timing period, storing energy in the primary inductance. When released, this energy is used to position the main switch voltage to zero by discharging the MOSFETs output capacitance just prior to it turning on. This alignment to zero drain voltage will automatically occur each switching cycle, provided that enough inductive energy is stored to overcome the opposing capacitive energy requirements of the circuit and power MOSFETs. Zero voltage transitions can be forced over a wide range of input voltage and load current values. The core reset is extended throughout the off-time, allowing self-driven synchronous rectification on the secondary-side. The voltage conversion ratio is given by

$$V_{\mathrm{out}} = NV_{\mathrm{in}}D, \tag{1}$$

where N is the transformer turns ratio (N_s/N_p), V_{in} the input voltage and the steady-state duty-cycle.

As highlighted by (1), if the input voltage range is doubled, the duty-cycle range will be doubled too to keep constant the output voltage. Therefore, extending the duty-cycle range of forward converters is the only way to meet wide-input, low-voltage applications. At steady-state, the output inductor current ripple is given by

$$\Delta I_{L_o} = \frac{V_{\mathrm{in}}ND(1-D)}{L_oF_{\mathrm{sw}}}, \tag{2}$$

where L_o is the output inductor and F_{sw} the switching frequency. The output voltage ripple is given by

$$\Delta V = \frac{\Delta I_{L_o}}{8C_oF_{\mathrm{sw}}}, \tag{3}$$

where C_o is the output capacitor. On the magnetizing inductance, the volts-second balance is expressed as

$$V_{\mathrm{in}}T_{\mathrm{on}} = V_{\mathrm{cl}}T_{\mathrm{off}}, \tag{4}$$

where T_{on} is the on-time and T_{off} the off-time. Introducing the duty-cycle D, the reset voltage V_{cl} across the reset capacitor C_{cl} is given by

$$V_{\mathrm{cl}} = \frac{V_{\mathrm{in}}D}{1-D}. \tag{5}$$

The off-voltage of both MOSFETs is given by

$$V_{\mathrm{off,main}} = V_{\mathrm{in}} + V_{\mathrm{cl}}. \tag{6}$$

Replacing the (5) in the (6), the (7) is given.

$$V_{\mathrm{off,main}} = \frac{V_{\mathrm{in}}}{1-\mathrm{D}}. \tag{7}$$

On the secondary-side, the off-voltage of D2 diode is given by

$$V_{\mathrm{off,D2}} = NV_{\mathrm{in}}. \tag{8}$$

The off-voltage of the D1 diode is given by

$$V_{\mathrm{off,D1}} = NV_{\mathrm{cl}} = NV_{\mathrm{in}}\frac{D}{1-D}. \tag{9}$$

If compared with existing demagnetization circuits, the active clamp technique extends the reset interval to the whole off-time. Therefore, a self-driven synchronous rectification on the secondary-side is allowed, as shown in Figure 2.

The power conversion efficiency is heavily improved by replacing diodes with active switches. Conduction losses are heavily lowered and drivers on the secondary-side are avoided by the self-driven configuration. Improved efficiency and zero-voltage switching are the most important advantages brought by the active clamp technique. Yet, if the duty-cycle approaches unity, the voltage stress on the reset capacitor as well as on active switches will increase to infinity. The cost of the power supply system is heavily affected by the cost of active switches and passive components. As a common rule, the duty cycle value of active clamp forward converters is usually limited to 70%. Therefore, wide-input low-voltage applications are really critical for a successful design of forward converters. At worst, the transformer, active switches, and then the whole power supply will be too expensive and the forward converter will not be suited any more. Designers aims at keeping all advantages brought by the forward topology such as low parts count, low cost and high efficiency, making the converter suitable for incoming applications as well.

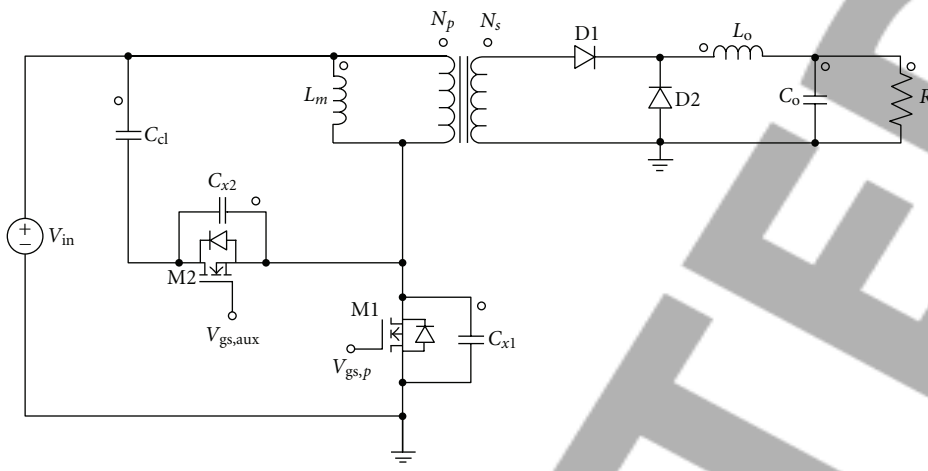

Figure 1: The active clamp forward converter.

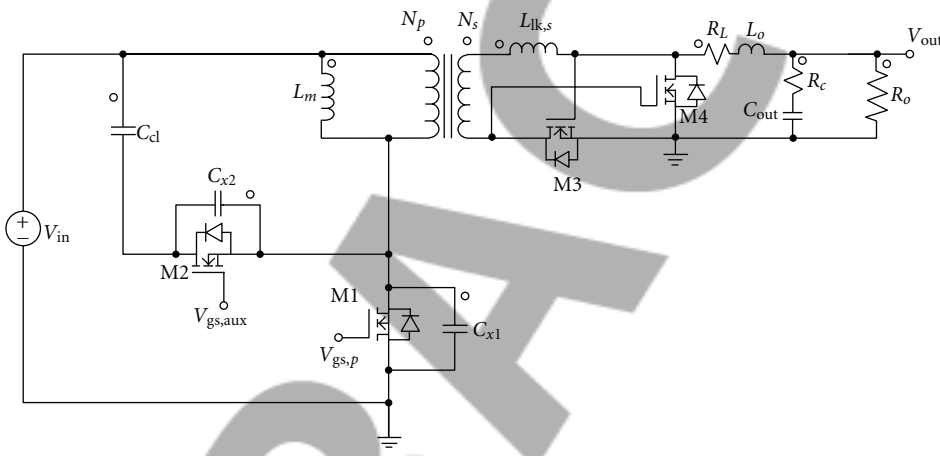

Figure 2: The active clamp forward converter with self-driven synchronous rectification on the secondary side.

3. The Proposed Single-Ended Topology

Figure 3 shows the proposed converter. Apparently, the proposed converter is just derived from the conventional active clamp forward converter by connecting the reset capacitor C_{cl} in series with the transformer primary windings. Really, the capacitor plays a quite different role in the proposed converter. The capacitor is not limited to the core reset function but is involved in the input-output energy transfer.

In the conventional active clamp forward converter, during the on-time the input-output energy transfer occurs while during the off-time the transformer is reset. In the active clamp forward converter, during the on-time the auxiliary net and thus the capacitor are disconnected from the primary windings. The series capacitor is not involved in the input-output energy transfer. In the proposed converter, the capacitor is always connected to the primary windings and the input-output energy transfer is heavily affected by the series capacitor. For these reasons, the proposed topology is presented as a new topology and not as a mere modification of existing converters. Several advantages are brought by moving the capacitor from the auxiliary to the primary net. The M2 drain terminal is tied to the input terminal. So, if M1 is switched on, the source terminal of the M2 is tied to ground. Therefore, the off-voltage of the auxiliary MOSFET is equal to the input voltage under any working condition. Vice versa, since the source terminal of M1 is tied to primary ground, if the auxiliary MOSFET is switched on, the drain terminal of M1 is tied to the input connections. Therefore, the off-voltage of M1 is equal to the input voltage under any working condition. After all, the off-voltage of both power switches is intrinsically limited by the input voltage rail. The cost of both power switches, which is mainly affected by the breakdown voltage value, is heavily reduced. The conventional tradeoff between the maximum allowable duty-cycle value and the power switches off-voltage is cancelled. Theoretically, the duty-cycle could be pushed up to unit value. As will be further discussed, the advantages brought by self-driven configuration are still preserved. The proposed topology is a low-cost, high performance solution which offers all the advantages of the conventional active clamp forward but still overcomes its drawbacks.

4. Steady-State Analysis

4.1. Voltage Conversion Ratio. Since high-current applications are addressed, a continuous conduction mode is assumed. The converter is firstly modelled by ideal elements. The main switch M1 is closed for a time T_{on} out of the switching period T_{sw}. The main and the auxiliary MOSFETs are synchronously driven out of phase. Dead-time intervals are actually introduced to avoid the simultaneous conduction of both primary MOSFETs. During the dead time, neither M1 nor M2 are on and the conduction is committed to body-diodes. Yet, dead-time intervals are neglected for the steady-state analysis thus assuming ideal gate drive signals. In order to perform the steady-state analysis, it is nearly always a good approximation to assume that the magnitude of the switching component is much smaller than the dc component of the output voltage and that the input voltage, the load current, and the voltage across the series capacitor are constant during the switching period T_{sw}.

If M1 is turned on, assuming positive polarity at V_{in} connections, the voltage drop across the primary windings during is given by

$$V_{L_m,on} = V_{in} - V_{cl}, \tag{10}$$

where V_{cl} is the voltage across the series capacitor, assuming positive polarity at primary windings connections. During T_{off}, M1 is off while M2 is driven into conduction. Therefore, the voltage across primary windings is equal to

$$V_{L_m,off} = -V_{cl}. \tag{11}$$

To avoid the magnetic core saturation, the volts-second balance should be met during each switching cycle. The volts-second applied to the magnetizing inductance during the on-time must equal the volt-second across the magnetizing inductance during the off-time, as highlighted by

$$V_{s1} + V_{s2} = 0, \tag{12}$$

where V_{s1} corresponds to the on-time volt-second product, whereas V_{s2} represents the off-time volt-second product. Since

$$V_{s1} = (V_{in} - V_{cl})T_{on} = (V_{in} - V_{cl})DT_{sw}, \tag{13}$$

$$V_{s2} = -V_{cl}T_{off} = -V_{cl}(1-D)T_{sw}, \tag{14}$$

the volts-second balance (15) is obtained:

$$(V_{in} - V_{cl})DT_{sw} - V_{cl}(1-D)T_{sw} = 0. \tag{15}$$

Rearranging, (15) and (16) is obtained

$$V_{cl} = V_{in}D, \tag{16}$$

V_{cl} is a positive voltage related to the input voltage by means of the system duty-cycle D and then lower than the input voltage.

Assuming positive polarity at diode connections, the on-time voltage across the output inductor L_o is given by

$$V_{L_o,on} = V_{sec,on} - V_{out} = (V_{in} - V_{cl})N - V_{out}, \tag{17}$$

where N is the power transformer turn-ratio N_{sec}/N_{pr}.

At steady-state, during the on-time the voltage across the output inductor is constant. The inductor current slope is constant and it is given by

$$S_{L_o,on} = \frac{V_{L_o,on}}{L_o} = \frac{[(V_{in} - V_{in}D)N - V_{in}ND(1-D)]}{L_o}. \tag{18}$$

Manipulating (18) and the (19) is obtained.

$$S_{L_o,on} = \frac{NV_{in}(1-D)^2}{L_o}. \tag{19}$$

On the falling edge of the gate drive signal, M1 is turned off. The voltage across the magnetizing inductance immediately reverses and the diode D1 is switched off. The output inductor opposes the current break trying to maintain the previously established current. The voltage polarity across it immediately reverses, forcing the diode D2 into conduction. The cathode node is thus clamped to the secondary ground. The output inductor voltage is now reversed and the inductor current is entirely carried on by the diode D2. Therefore, during the off-time the voltage across the output inductor is given by

$$V_{L_o,off} = -V_{out}, \tag{20}$$

where V_{out} is the output voltage.

At steady-state, during the off-time the voltage across the output inductor is constant. The inductor current slope is constant and it is given by

$$S_{L_o,off} = \frac{V_{L_o,off}}{L_o} = \frac{-V_{out}}{L_o}. \tag{21}$$

Manipulating (21),

$$S_{L_o,off} = \frac{-V_{in}ND(1-D)}{L_o}. \tag{22}$$

Applying the volt-second balance to the output inductor results in

$$[(V_{in} - V_{cl})N - V_{out}]DT_{sw} - V_{out}(1-D)T_{sw} = 0. \tag{23}$$

Rearranging the (23) and replacing V_{cl} by (16), (24) is obtained.

$$V_{out} = NV_{in}D(1-D). \tag{24}$$

The normalized voltage conversation ratio is given by

$$M = \frac{V_{out}}{NV_{in}} = D(1-D). \tag{25}$$

At steady-state the output inductor current ripple could be expressed as

$$\Delta I_{L_o} = S_{L_o,on}T_{on} = S_{L_o,on}DT_{sw}. \tag{26}$$

From (19) and (26),

$$\Delta I_{L_o} = \frac{NV_{in}D(1-D)^2}{L_oF_{sw}}. \tag{27}$$

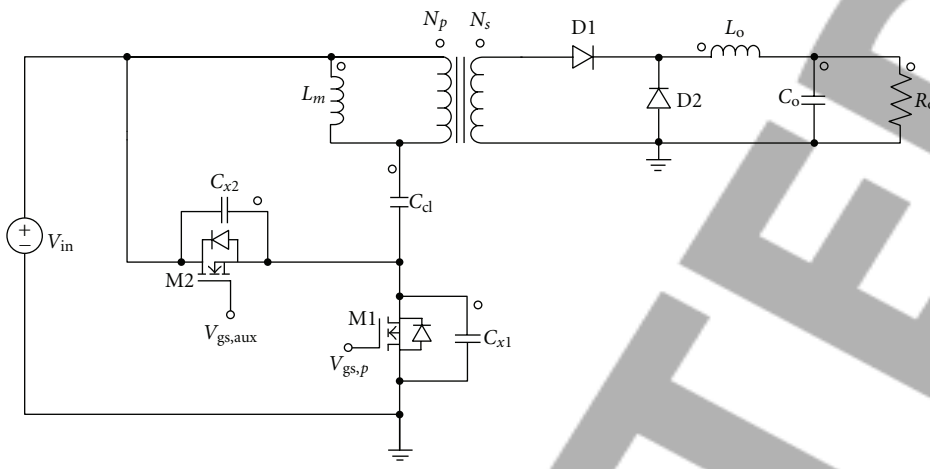

Figure 3: The proposed converter topology.

Note that in the traditional active clamp forward converter, the output inductor current ripple is given by (2). By comparing (27) and (2),

$$\Delta I_{L_o} = \Delta I_{L_o,\mathrm{ACF}}(1 - D). \tag{28}$$

Therefore, a decrease in the output inductor current is achieved. Being the same specifications, the cost of the output inductor as well as the volume of the entire power supply system could be easily reduced by the means of the proposed converter.

In traditional forward converters, if the input voltage range is doubled, the duty-cycle range is doubled too in order to keep constant the output voltage nominal value. Increasing the duty-cycle value leads to an increase of the off-voltage of active switches. Therefore, a practical limit for wide-input applications is fixed by the tradeoff between the cost of active switches and the maximum allowable duty-cycle value. In the proposed converter, during each switching cycle, the transformer core reset is achieved avoiding the traditional tradeoff between the off-voltage of active switches and the system duty-cycle. The cost of active switches is thus heavily reduced.

The normalized voltage conversion ratio M is a nonlinear function of the duty-cycle, as shown in Figure 3. The maximum value of the normalized voltage conversion ratio is equal to 0.25 corresponding to a duty-cycle $D = 50\%$. If compared with the conventional forward converter, equal N results in a lower conversion ratio making the converter suitable for low-voltage applications. By selecting the desired conversion ratio, two duty-cycle values which are symmetrical to 50% are obtained. In traditional forward converters, doubling the input range results in doubling the duty-cycle range as well. If a 36 V–72 V input voltage range is addressed, the maximum duty-cycle value is twice the minimum value. Since a 70% limit is fixed, at worst the forward converter will not be suited anymore. The proposed converter is well suited for wide-input applications since the duty-cycle range

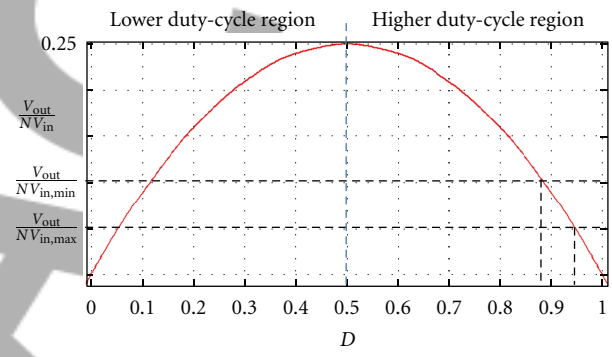

Figure 4: The normalized conversion ratio versus the system duty-cycle.

is narrowed and the tradeoff between the maximum duty-cycle and the system cost is avoided. For example, if a 36 V–72 V range is addressed and a 0.95 maximum duty-cycle value is set, a 0.89 minimum value is obtained by (16) keeping constant the output voltage, as shown in Figure 4. The minimum duty-cycle value is almost 93% of the maximum duty-cycle value. The advantage over the active clamp forward converter is emphasized if the steady-state duty-cycle is close to unity. If the steady state duty-cycle is less than 50%, increasing the duty-cycle leads to an increase of the voltage conversion ratio. Otherwise, increasing the system duty-cycle forces a decrease of the voltage conversion ratio. Therefore, two duty-cycle regions which are limited by 50% value are identified. The small-signal behaviour of the proposed system is heavily affected by the steady-state duty-cycle region, as will be further discussed.

Key waveforms of the proposed converter topology are plotted. Figure 5 shows, from top to bottom, the magnetizing inductance current, the ideal primary windings current, the effective primary current, the primary MOSFET current, the auxiliary MOSFET current, the output inductor current, the free-wheeling diode current, and the forward diode current.

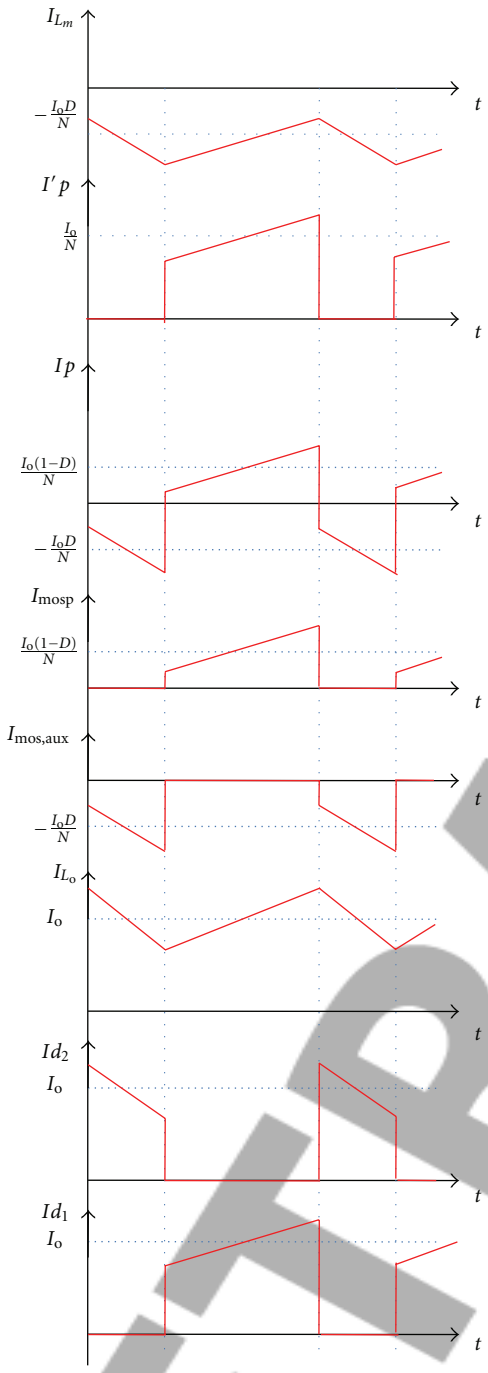

Figure 5: Key waveforms of the proposed converter topology.

4.2. Voltage and Current Stress. During the on-time, the voltage across the secondary windings is given by

$$V_{\text{sec,on}} = (V_{\text{in}} - V_{\text{cl}})N = NV_{\text{in}}(1-D), \tag{29}$$

where V_{cl} is the series capacitor voltage and N the transformer turns ratio.

Therefore, the diode D1 is turned on while the diode D2 is switched off. The output inductor current is entirely carried on by the diode D1. During the on-time, the load current is supplied by the primary windings and then by the input rail.

The voltage across the diode D2 is given by

$$V_{\text{D2,on}} = -V_{\text{sec,on}}. \tag{30}$$

Therefore, if the duty-cycle value approaches the unit value, the voltage stress across the freewheeling diode will be reduced.

On the primary side, during the off-time, the main MOSFET is off while the auxiliary MOSFET is turned on. The switching node is clamped at the input connections by the auxiliary MOSFET and the voltage across the main MOSFET is equal to the input voltage. The voltage across the primary windings is given by

$$V_{\text{pr,off}} = -V_{\text{cl}}. \tag{31}$$

During the off-time, the diode D1 is turned off and the freewheeling diode is forced into conduction and the switching node on the secondary side is thus clamped at ground connections.

The voltage across the diode D1 is given by

$$V_{\text{D1,off}} = NV_{\text{pr,off}} = -NV_{\text{cl}} = -NV_{\text{in}}D. \tag{32}$$

Therefore, if the duty-cycle value is lowered, the voltage stress across the diode D2 will be reduced.

If compared with traditional active clamp forward converters, the voltage stress on the secondary-side diodes is anyway reduced independently of the working duty-cycle region.

During the on-time, the series capacitor C_{cl} is charged by the primary current. Under steady-state conditions, during the off-time the series capacitor should be discharged. Since the secondary current is almost zero during the off-time, the capacitor is discharged by the magnetizing current only. By applying the charge balance to the series capacitance,

$$i_{C_{\text{cl}},\text{on}}D + i_{C_{\text{cl}},\text{off}}(1-D) = 0. \tag{33}$$

During the on-time, the capacitor current is given by

$$i_{\text{cl,on}} = i_{L_m,\text{on}} + i'_{\text{pr,on}}, \tag{34}$$

where I_{L_m} is the magnetizing current and i_{pr} is the secondary current reflected to the primary windings.

During the off-time the series capacitor current is thus given by

$$i_{C_{\text{cl}},\text{off}} = i_{L_m,\text{off}}. \tag{35}$$

By replacing (34) and (35) in (33), (36) is obtained.

$$i_{L_m} = -i'_{\text{pr,on}}D, \tag{36}$$

where $I'_{\text{pr,on}} = I_oN$.

Therefore, the average magnetizing current is given by

$$I_{L_m} = -I_o N D. \tag{37}$$

Since at steady-state the average current through the output capacitor is null, the average current through the output inductor is equal to the load current. The ac component of the inductor current flows through the parallel connection between load and capacitor. Commonly, the capacitor is large enough to assume that its impedance at the switching frequency is much smaller than the load resistance. Hence, nearly all the inductor current ripple flows through the capacitor. The ac-current flowing into the load could be reasonably neglected. A continuous conduction mode is preferred in high-current applications since lower and lower conduction power losses are involved. The inductor is thus sufficiently large to neglect the current ripple with respect to the average inductor current. The voltage ripple across the output capacitor is given by

$$\Delta V_{\text{out}} = \frac{q}{C_o} = \frac{\Delta I_L T_{\text{sw}}}{8 C_o}. \tag{38}$$

4.3. Zero-Voltage Switching. Zero-voltage switching (ZVS) of both primary switches is achieved by the energy stored in the leakage inductor. Therefore, the energy stored in the leakage inductor must discharge $C_{\text{ds,M1}}$ to zero-voltage level before switch M1 is turned on. In the other dead time, the energy stored in the leakage inductor must discharge $C_{\text{ds,M2}}$ before the switch M2 is turned on. At the beginning of the first dead-time, the capacitor $C_{\text{ds,M2}}$ is charged at V_{cl} voltage. Therefore, the energy required to achieve ZVS in the first dead-time is given by

$$E_{\text{req}} = \frac{1}{2} \cdot C_t \cdot (V_{\text{cl}})^2. \tag{39}$$

The energy stored in the leakage inductor, at the very beginning of the first dead-time, is given by

$$E_{\text{stored}} = \frac{1}{2} \cdot L_{\text{lk}} \cdot I^2{}_{pk,L_{\text{lk}}}, \tag{40}$$

where $I_{pk,L_{\text{lk}}}$ is the leakage inductor peak current value. At the beginning of the first dead-time, the leakage inductor current is given by the difference between the secondary current reflected to the primary and the magnetizing current. The peak value of the leakage inductor current is therefore given by

$$I_{pk,L_{\text{lk}}} = \frac{I_{pk,L_o} + \Delta I_{L_o}}{N} - \left(\left| \overline{I_{L_m}} \right| - \frac{\Delta I_{L_m}}{2} \right). \tag{41}$$

Condition (42) is required to achieve zero-voltage switching of M2 switch:

$$\frac{1}{2} \cdot L_{\text{lk}} \cdot I^2{}_{pk,L_{\text{lk}}} \geq \frac{1}{2} \cdot C_t \cdot (V_{\text{cl}})^2. \tag{42}$$

At the beginning of the second dead-time, the capacitor $C_{\text{ds,M1}}$ is charged at $(V_{\text{in}} - V_{\text{cl}})$. The energy required to achieve ZVS of M1 is therefore

$$E_{\text{req}} = \frac{1}{2} \cdot C_t \cdot (V_{\text{in}} - V_{\text{cl}})^2. \tag{43}$$

The energy stored in the leakage inductor is given by:

$$E_{\text{stored}} = \frac{1}{2} \cdot L_{\text{lk}} \cdot I^2{}_{pk,L_{\text{lk}}}. \tag{44}$$

At the beginning of the second dead-time, the leakage inductor current is be equal to the magnetizing inductor current since the diode D1 is not yet turned on. Therefore, the leakage inductor peak current is now given

$$\left| I_{pk,L_{\text{lk}}} \right| = \left| \overline{I_{L_m}} \right| + \frac{\Delta I_{L_m}}{2}. \tag{45}$$

Condition (46) is required to achieve zero-voltage switching of M1 switch:

$$\frac{1}{2} \cdot L_{\text{lk}} \cdot I^2{}_{pk,L_{\text{lk}}} \geq \frac{1}{2} \cdot C_t \cdot (V_{\text{cl}})^2. \tag{46}$$

In the traditional active clamp, the zero-voltage switching of the main Mosfet is achieved by the energy stored in the leakage inductor. By the same analysis, the condition to achieve ZVS of the main Mosfet is given by

$$L_{\text{lk}} \geq \frac{C_t \cdot (V_{\text{in}})^2}{(\Delta I_{L_m}/2)^2}. \tag{47}$$

4.4. Self-Driven Synchronous Rectification. The system efficiency could be heavily improved by self-driven synchronous rectification on the secondary-side. Both diodes could be replaced by two MOSFETs, as shown in Figure 6.

The free-wheeling diode is now replaced by M4 and appears in the return path. When the main MOSFET is turned on, the M4 gate jumps to $N(V_{\text{in}} - V_{\text{cl}})$ thus ensuring proper biasing during the on-time. When the on-time ends, M3 is forced into conduction as long as a voltage appears across its gate-source connection. As well as in the active clamp forward converter, the core demagnetization is extended to the whole off-time and the free-wheeling MOSFET V_{gs} exists for the whole off-time duration. The system efficiency is heavily improved by the proposed architecture.

5. Small-Signal Analysis

Parasitic components of passive elements are included in the small-signal analysis. The resistance r_{cl} is the equivalent series resistance of the primary-side capacitor, $r_{s,\text{trasf}}$ of the transformer, r_L of the output inductor, and r_c of the output capacitor.

The small-signal model of the proposed converter is derived assuming continuous conduction mode of operation. The small-signal model on the secondary side is shown in Figure 7. The G_{vo} transfer function is usually defined as

$$G_{\text{vo}} = \left(\frac{v_{\text{out}}}{d} \right)_{V_{\text{in}} = \cos t, I_{\text{out}} = \text{const}}. \tag{48}$$

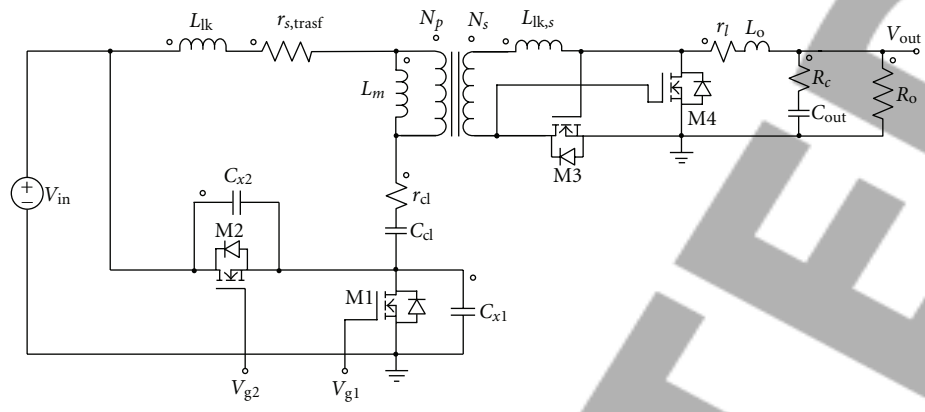

Figure 6: The proposed converter with secondary-side self-driven synchronous rectification.

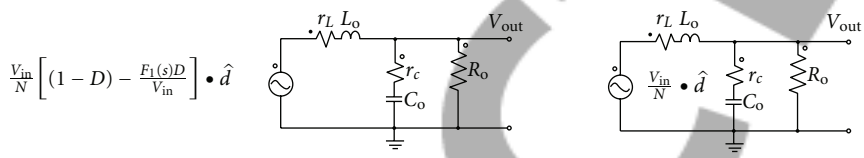

Figure 7: At the left, the small-signal model of the proposed converter. At the right, the traditional forward converter model.

During the on-time, the secondary voltage is equal to

$$v_{sec} = N(v_{in} - v_{cl}). \tag{49}$$

During the on-time, the V_{sec} voltage is applied to the output filter since D1 is forced into conduction. During the off-time, the free-wheeling diode is turned off and the switching node is clamped to ground connections. Therefore the v_s signal could be expressed as

$$v_{sec} = N(v_{in} - v_{cl})d. \tag{50}$$

According to the state-space averaging method, all variables are split with a dc term imposing the operating point, and an ac modulating signal which is sufficiently small in amplitude to keep the system linear. Hence,

$$\begin{aligned} d &= D + \hat{d} \\ v_{in} &= V_{in} + \hat{v}_{in}. \end{aligned} \tag{51}$$

Assuming V_{in} constant and perturbing the duty-cycle variable around the operating point,

$$\hat{v}_{L_o-C_o} = \left[(V_{in} - V_{cl}) \cdot \hat{d} - \hat{v}_{cl} \cdot D\right]N. \tag{52}$$

(52) could be expressed as

$$\hat{v}_{L_o-C_o} = NV_{in} \cdot \left[(1-D) - \frac{F_I(s) \cdot D}{V_{in}}\right] \cdot \hat{d}, \tag{53}$$

where $F_I(s)$ is defined as:

$$F_I(s) = \frac{\hat{v}_{cl}}{\hat{d}}. \tag{54}$$

Hence, the small-signal transfer function G_{vo} of the proposed converter is obtained by the small-signal model shown at the left in Figure 7 while the small-signal model of a traditional forward converter is shown at the right in Figure 7.

Hence,

$$\frac{\hat{v}_0}{\hat{d}} = \left[(1-D) - \frac{F_I(s)D}{V_{in}}\right] \cdot F_o(s), \tag{55}$$

where $F_o(s)$ is the output to duty-cycle transfer function of the traditional forward converter.

The $F_I(s)$ transfer function is obtained by the small-signal model of the primary side. Assuming constant the output current and assuming zero-ripple approximation, the ac term of the output inductor current could be neglected for the small-signal analysis.

During the on-time, the full load current flows through the secondary windings. During the off-time, since the diode D1 is turned-off, the load current flows through the free-wheeling diode D2 and no current flows through the secondary windings. The secondary windings current signal is given by

$$i_s = I_o \cdot d, \tag{56}$$

where d is the duty-cycle signal and I_o the load current. Splitting the duty-cycle variable with a dc and an ac term,

$$I_s + \hat{i}_s = I_o \cdot \left(D + \hat{d}\right). \tag{57}$$

According to the steady-state analysis

$$I_s = I_o \cdot D. \tag{58}$$

Therefore, from (57)

$$\hat{i}_s = I_o \cdot \hat{d}. \tag{59}$$

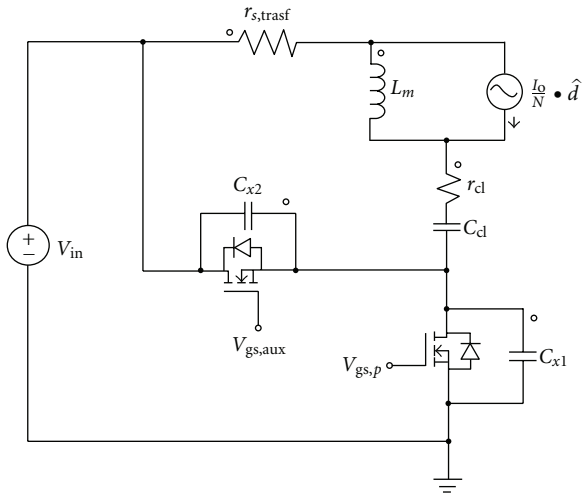

Figure 8: Primary-side small-signal model.

According to (59), the primary side small-signal model is shown in Figure 8. The secondary-side circuit is replaced by the current generator $\hat{i}_s$ and reflected to the primary side.

Note that the small-signal model shown in Figure 8 is the small-signal model of a buck converter whose output inductor is L_m and output capacitor is C_{cl}. Taking advantages by similarities, the $F_I(s)$ transfer function could be easily derived by the small-signal circuit. The model shown in Figure 8 is linear and the superposition principle could be applied. Neglecting the current source, (60) is obtained by circuit analysis:

$$\left(\frac{\hat{v}_{\text{cl}}}{\hat{d}}\right)_V = V_{\text{in}} \cdot \frac{(1 + s \cdot C_{\text{cl}} \cdot r_t)}{s^2 \cdot (L_m \cdot C_{\text{cl}}) + s \cdot (C_{\text{cl}} \cdot r_t) + 1}, \tag{60}$$

where r_t is defined as

$$r_t = r_{\text{cl}} + r_{s,\text{trasf}}. \tag{61}$$

Neglecting the voltage source, the system response is obtained:

$$\left(\frac{\hat{v}_{\text{cl}}}{\hat{d}}\right)_I = NI_{\text{o}} \cdot \frac{s \cdot L_m \cdot (1 + s \cdot C_{\text{cl}} \cdot r_t)}{s^2 \cdot (L_m \cdot C_{\text{cl}}) + s \cdot (C_{\text{cl}} \cdot r_t) + 1}. \tag{62}$$

The $F_I(s)$ is given by

$$F_I(s) = \frac{\hat{v}_{\text{cl}}}{\hat{d}} = \left(\frac{\hat{v}_{\text{cl}}}{\hat{d}}\right)_V + \left(\frac{\hat{v}_{\text{cl}}}{\hat{d}}\right)_I = V_{\text{in}} \cdot \frac{s^2 \cdot (C_{\text{cl}} \cdot I_{\text{o}} \cdot L_m \cdot r_t/N \cdot V_{\text{in}}) + s \cdot (C_{\text{cl}} \cdot r_t + I_{\text{o}} \cdot L_m/N \cdot V_{\text{in}}) + 1}{s^2 \cdot (L_m \cdot C_{\text{cl}}) + s \cdot (C_{\text{cl}} \cdot r_t) + 1}. \tag{63}$$

The $G_{\text{Vo},d}$ transfer function of the proposed converter is obtained by replacing (63) in (55)

$$G_{\text{Vo},d} = NV_{\text{in}} \cdot \frac{(s \cdot C_{\text{o}} \cdot r_c + 1)}{s^2 \cdot (C_{\text{o}} \cdot L_{\text{o}}) + s \cdot C_{\text{o}}(r_c + r_l) + 1} \cdot \frac{s^2 C_{\text{cl}} L_m (1 - D) + sC_{\text{cl}} r_t (1 - D)(I_{\text{o}} L_m D/NV_{\text{in}}) + (1 - 2D)}{(s^2 \cdot C_{\text{cl}} \cdot L_m + s \cdot C_{\text{cl}} \cdot r_t + 1)}. \tag{64}$$

The output filter introduces a zero and a complex pole, as given by

$$w_z = \frac{1}{r_c C_{\text{o}}}, \qquad w_p = \frac{1}{\sqrt{L_{\text{o}} C_{\text{o}}}}, \qquad \zeta_p = \frac{(r_c + r_L)}{2}\sqrt{\frac{C_{\text{o}}}{L_{\text{o}}}}. \tag{65}$$

The proposed architecture introduced an LC filter made up of the magnetizing inductance of the transformer and the series capacitor. The dynamic behaviour of the proposed converter is heavily affected by the input filter in different ways depending on the duty-cycle region. The analysis is carried on in both regions and criteria for region selection are provided for further applications. The input filter introduces a couple of complex poles:

$$w_{p,\text{in}} = \frac{1}{\sqrt{L_m C_{\text{cl}}}}, \qquad \zeta_p = \frac{r_t}{2}\sqrt{\frac{C_{\text{cl}}}{L_m}}. \tag{66}$$

Yet, a right half plane zero (RHPZ) is introduced by the input filter in the higher duty-cycle region. As highlighted by (64), the numerator constant term is given by $(1 - 2D)$ which is negative in the higher duty-cycle region, meaning that almost one root is located in the right-half s-plane. Depending on the converter design, the RHPZ lies within the frequency range of interest thus limiting the maximum achievable bandwidth. In the lower duty-cycle region, no RHPZ is introduced by the proposed topology.

6. Design Example

According to the proposed analysis, choosing the duty-cycle region is a critical step which heavily depends on the addressed application. The higher duty-cycle region is the most suitable for wide-input, low-voltage, high-current applications. If on-board applications are addressed, the higher duty-cycle region will be the most suitable.

Since no RHPZ is introduced, the lower duty-cycle region features the highest achievable bandwidth. The lower

region is the most suitable for wide-bandwidth, low-voltage, high-current applications. If point-of-load applications are addressed, the lower region will be the most suitable.

If wide-input, low-voltage, high-current applications are addressed, the proposed converter features higher performances than the traditional active clamp forward converter. Moreover, the cost of the whole power supply system is heavily reduced by the proposed architecture. Further improvements are provided by an accurate selection of the working duty-cycle region.

A laboratory prototype of the proposed converter for on-board applications has been designed and tested. The efficiency of the proposed architecture is shown by simulation and experimental results. Design criteria are discussed for further implementations. The telecom standard range of 36 V–72 V is the targeted input voltage range. A 50 W, 2.5 V, 20 A converter is designed and a PWM voltage-mode control at 250 kHz is implemented. Since on-board applications are addressed, the higher duty-cycle region is the most suitable. The transformer turns-ratio is designed by selecting the maximum duty-cycle value. By the proposed architecture, ideally the duty-cycle value could be pushed up to unit value. Yet, the off-time must be ensured to allow the core reset. A maximum duty-cycle of 0.9 is therefore a good selection. The maximum duty-cycle value corresponds to the maximum input voltage. Therefore, the turns ratio is designed according

$$N \geq \frac{N_s}{N_p} = \frac{V_o}{D_{\max} \cdot (1 - D_{\max}) \cdot V_{\text{in,max}}} = \frac{1}{2.59}. \quad (67)$$

An integer turns-ratio of 1 : 3 is chosen for the proposed application. The maximum and minimum duty-cycle values are 0.88 and 0.7, respectively. Since zero-ripple approximations were made on the magnetizing inductance value, the magnetizing inductor is designed to ensure that the magnetizing ripple current is lower than the average magnetizing current by a factor of 20%. By the transformer turns-ratio, magnetizing inductance and maximum magnetizing current, the transformer could be selected. In the proposed prototype, a Coiltronics VP5-0083R reconfigurable transformer is used.

The series capacitor value is designed according to the steady-state and dynamic analysis. At steady-state, during each switching cycle the voltage across the series capacitor should be rather constant to ensure proper core reset. Yet, the capacitor value should be as low as possible to ensure adequate bandwidth. The capacitor value has been designed to ensure a maximum ripple on the capacitor voltage of about the 10% of the minimum average series capacitor voltage.

On the secondary side, the output inductor is designed to ensure small-ripple approximation on the output mesh. The output capacitor value should be as high as possible to limit the over- and undershoots of the output voltage under load transients. Therefore, a unit damping factor for the output filter is designed. The system has been modeled in PSIM environment. The model is shown in Figure 9.

Three subsystems are highlighted: the converter, the control loop, and the driver model. Parasitic elements of passive components are included in the simulation model to improve the accuracy of simulation results. Self-driven synchronous rectification is implemented on the secondary-side. The driver section models are all available functions of the National Semiconductor LM5104 driver: high-side and low side MOSFETs are driven and adaptive time-delay is provided to prevent shoot-through.

In the feedback loop, galvanic isolation is provided by the optocoupler PS2701. Since low-voltage applications are addressed, the classical TL431 solution could not be adopted. The cathode node of the emitting diode is tied to ground. A common-emitter configuration is implemented and the optocoupler is driven by the error amplifier. The LED current is limited by the resistor R_k while the saturation current of the optocoupler bipolar transistor is limited by the resistor R_C. A type 3 compensation action is designed to achieve stability and adequate bandwidth. A 0.6 V reference voltage is obtained by MAX8515. The error to output voltage transfer function is given by

$$\frac{V_{\text{err}}}{V_{\text{out}}} = \frac{\text{CTR} \cdot R_C}{R_1 \cdot (R_k + R_D) \cdot (C_2 + C_3)} \cdot \frac{(1+s \cdot R_1 \cdot C_1) \cdot (1+s \cdot R_3 \cdot C_3)}{s \cdot (1+s \cdot R_c \cdot C_c) \cdot (1+s \cdot R_3 \cdot (C_2 \cdot C_3/(C_2+C_3)))}, \quad (68)$$

where CTR is the optocoupler current transfer ratio. The efficiency of the proposed architecture is shown by simulation and experimental results.

7. Simulation and Experimental Results

In Figure 10 steady-state waveforms are shown. A 36 V input voltage and 2 A load current are set. At the top gate drive signals, at the bottom drain-source voltages of primary-side switches under 36 V input voltage are shown. The leakage inductor is included in the PSIM model, according to the selected transformer ratings. ZVS is achieved for both MOSFETs.

In Figure 11, the input voltage is now set at 72 V and 20 A load current is drawn. At the top the drain-source voltages of both main (Vds1) and auxiliary (Vds2) MOSFETs, at the bottom gate voltages of both, Vgs1 and Vgs2, respectively, are shown. The off-voltage of both primary MOSFET is clamped at the input voltage, as shown by simulation results.

If a 36–72 V active clamp forward converter is designed, at least 150 V breakdown voltage will be required for power MOSFETs. By the proposed topology, 80 V breakdown voltages are required being the same input voltage range. The cost of active switches is heavily reduced.

Experimental results under steady state conditions are shown in Figure 12. The input voltage is fixed at 36 V and the load current is equal to 2 A. The drain voltage of the main switch Vsw is shown on Ch1 (10 V/div). The voltage at the transformer-capacitor connections V_{int} is shown on Ch2 (10 V/div). The transformer primary current is shown on Ch3 (2 A/div). Time base is set at 2 μsec/div. Note that the drain-source voltage of the auxiliary MOSFET M2 is obtained as the difference between the input voltage and the switching node voltage. The voltage across the series

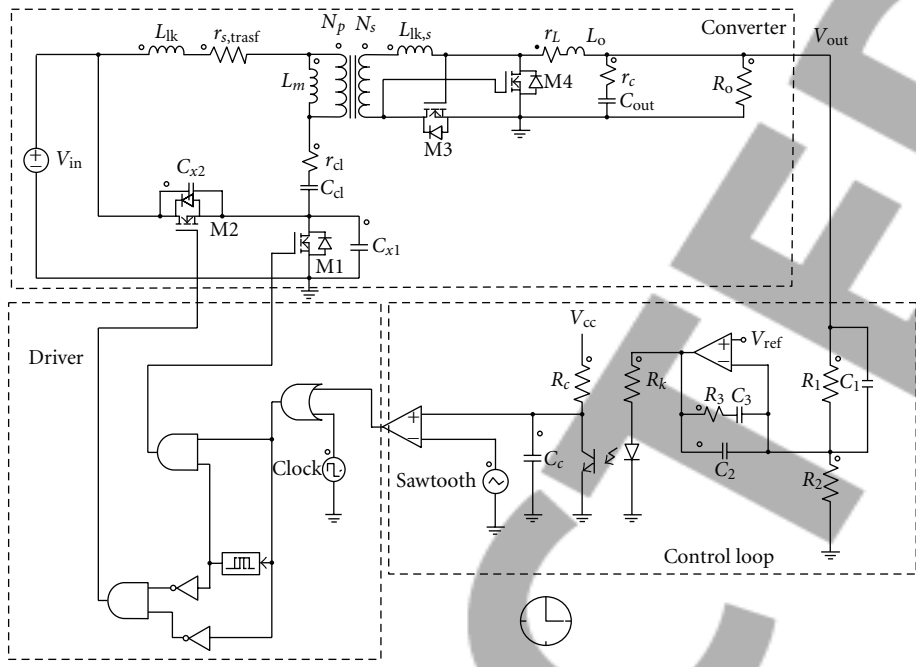

Figure 9: PSIM simulation model.

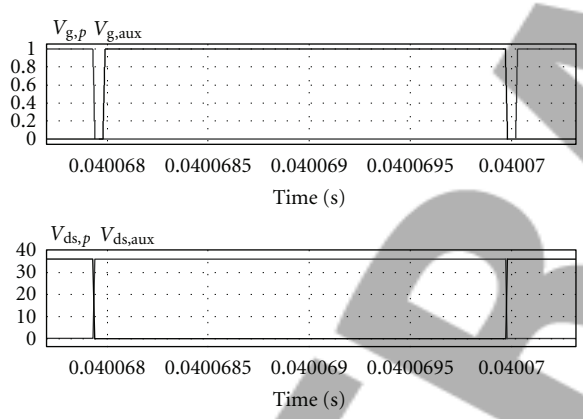

Figure 10: Primary-side steady-state waveforms under 36 V input voltage and 2 A load current.

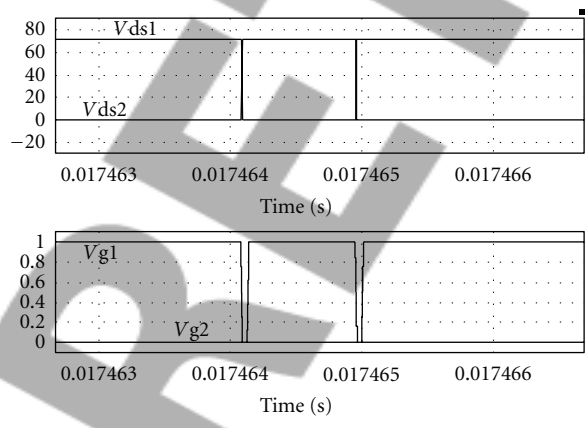

Figure 11: Primary-side waveforms under 72 V input voltage and 20 A load current.

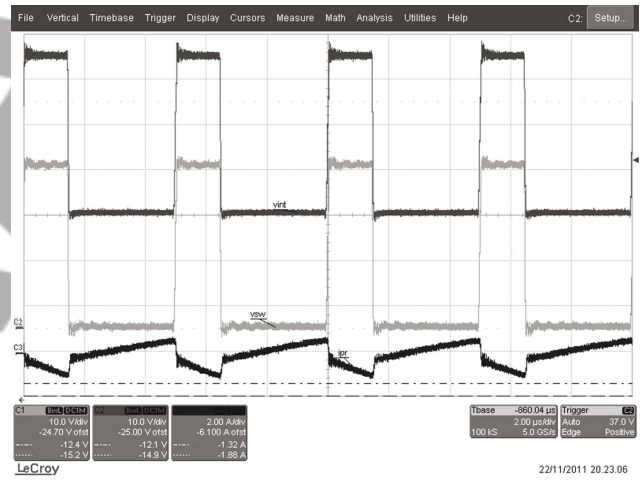

Figure 12: Experimental results on the primary side under 36 V input voltage and 2 A load current.

capacitor is obtained as the difference between Ch2 and Ch1 waveforms. As shown in Figure 12, the off-voltage of both active switches is clamped to the input voltage value, independently of the actual working conditions. According to (16), the measured average voltage across the series capacitor is equal to 25 V.

In Figure 13 secondary-side waveforms under 3 A load current are shown. On Ch1 (5 V/div) the secondary-side switching node voltage, on Ch2 (2 V/div) the output voltage, on Ch4 (2 A/div) the output inductor current waveforms are shown. Time base is set at 2 μsec/div. As shown by experimental results, system stability is achieved and the output voltage is regulated at the nominal value of 2.5 V.

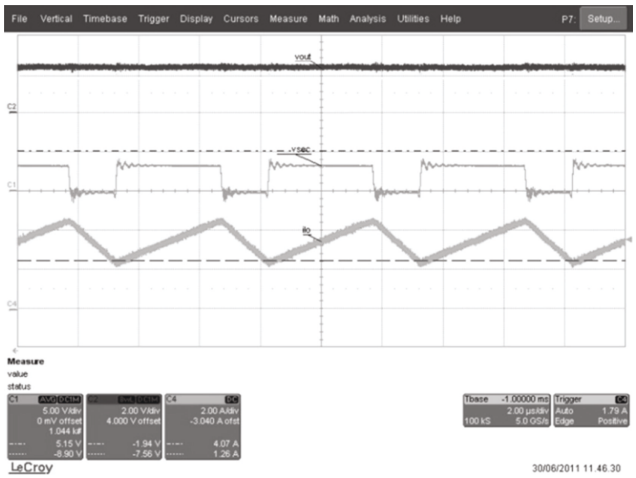

Figure 13: Secondary-side experimental waveforms at 36 V, 3 A.

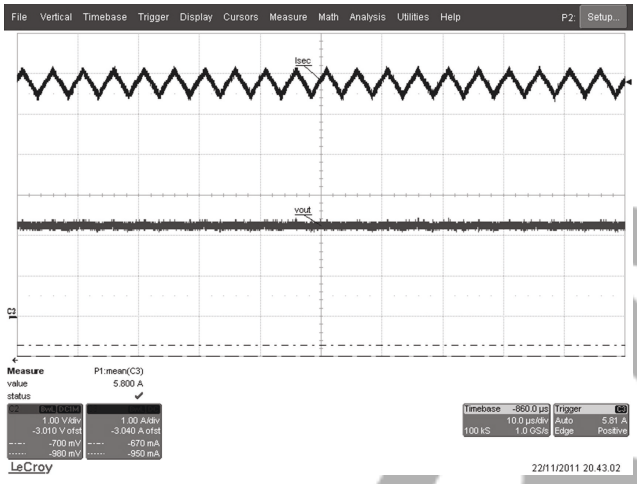

Figure 14: Experimental results at 26 V, 6 A.

In Figure 14 the output voltage (Ch2, 1 V/div) and the output inductor current (Ch3, 1 A/div) waveforms under 5.8 A load current are shown. Time base is set at 10 μsec/div. Stability is achieved under each working condition.

8. Conclusion

In this paper, a single-ended isolated topology for wide-input, low-voltage, and high-current applications has been proposed. The topology improves the power efficiency, reduces both switching and conduction losses, and heavily reduces the system cost. The transformer core reset is provided during each switching cycle not requiring additional circuits. The converter steady-state and dynamic analysis has been carried out and a comparison of the system performances in both allowable duty-cycle regions is extensively performed. A 50 W@2.5 V, 20 A converter has been realized and tested. The traditional tradeoff between the maximum allowable duty-cycle and the reset voltage is avoided. Independently of the actual working condition, the off-voltage of active switches is intrinsically clamped to the input voltage. Therefore, the cost of the whole system is heavily reduced. Zero-voltage switching is achieved for active switches and the power efficiency is greatly improved. As shown by simulation and experimental results, all advantages brought by the conventional active clamp forward converter are still preserved overcoming all its drawbacks. The converter is well suited for wide-input, low-voltage applications thus providing a cost-effective and high-performance solution.

References

[1] F. D. Tan, "The forward converter: from the classic to the contemporary," in *Proceedings of the 17th Annual IEEE Applied Power Electronics Conference and Expositions*, pp. 857–863, March 2002.

[2] Y. Gu, H. Chen, Z. Lu, Z. Qian, and K. Wei, "Investigation of candidate topologies for Brick DC-DC," in *Proceedings of the 20th Annual IEEEApplied Power ElectronicsConference and Exposition (APEC '05)*, pp. 1537–1540, March 2005.

[3] C. S. Leu, G. Hua, and F. C. Lee, "Comparison of forward topologies with various reset schemes," in *Proceedings of the 9th VPEC Annual Power Electronics Seminar*, pp. 101–108, 1991.

[4] N. Murakami and M. Yamasaki, "Analysis of a resonant reset condition for a single-ended forward converter," in *Proceedings of IEEE Power Electronics Specialists Conference*, vol. 2, pp. 1018–1023, 1988.

[5] J. A. Cobos, O. Garcia, J. Sebastian, and J. Uceda, "RCD clamp PWM forward converter with self driven synchronous rectification," in *Proceedings of the 19th International Conference on Industrial Electronics, Control and Instrumentation*, pp. 1336–1341, November 1993.

[6] P. Vinciarelli, "Optimal resetting of the transformer's core in single ended forward converters," U.S.Patent 4,441,146, 1984.

[7] B. R. Lin, K. Huang, and D. Wang, "Analysis, design, and implementation of an active clamp forward converter with synchronous rectifier," *IEEE Transactions on Circuits and Systems I*, vol. 53, no. 6, pp. 1310–1319, 2006.

[8] Q. M. Li and F. C. Lee, "Design consideration of the active-clamp forward converter with current mode control during large-signal transient," *IEEE Transactions on Power Electronics*, vol. 18, no. 4, pp. 958–965, 2003.

[9] Q. M. Li, F. C. Lee, and M. M. Jovanović, "Large-signal transient analysis of forward converter with active-clamp reset," *IEEE Transactions on Power Electronics*, vol. 17, no. 1, pp. 15–24, 2002.