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TOFPET2: a high-performance ASIC for time and amplitude measurements of SiPM signals in time-of-flight applications

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ABSTRACT: We present a readout and digitization ASIC featuring low-noise and low-power for time-of flight (TOF) applications using SiPMs. The circuit is designed in standard CMOS 110 nm technology, has 64 independent channels and is optimized for time-of-flight measurement in Positron Emission Tomography (TOF-PET). The input amplifier is a low impedance current conveyor based on a regulated common-gate topology. Each channel has quad-buffered analogue interpolation TDCs (time binning 20 ps) and charge integration ADCs with linear response at full scale (1500 pC). The signal amplitude can also be derived from the measurement of time-over-threshold (ToT). Simulation results show that for a single photo-electron signal with charge 200 (550) fC generated by a SiPM with 320 pF capacitance the circuit has 24 (30) dB SNR, 75 (39) ps r.m.s. resolution, and 4 (8) mW power consumption. The event rate is 600 kHz per channel, with up to 2 MHz dark counts rejection.

KEYWORDS: Analogue electronic circuits; Gamma camera, SPECT, PET PET/CT, coronary CT angiography (CTA); Data acquisition circuits; Front-end electronics for detector readout

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1 Introduction

Several applications require the measurement of light pulses detected by SiPMs with time resolution in the range 10 – 100 ps. Time-of-flight measurements are used in a number of nuclear and particle experiments as well as in PET medical imaging systems that require this performance.

The signal-to-background ratio of PET images can be improved by measuring the Time-of-Flight (TOF) of the two γ photons from positron electron annihilation. The required coincidence time resolution is below 200 ps (FWHM) [1]. Time resolution is strongly limited by the scintillating light yield and transport. For this reason the readout system must be sensitive to the first photo-electrons, as reported in [2]. This leads to the need of very high speed and low noise electronics, sensitive to the rising edge of the signal produced by the γ ray detector to obtain the temporal information [3].

Here we present a read out and digitization application-specific-integrate-circuit (ASIC) for TOF-PET applications, based on a regulated common-gate stage, operating as a low noise input current mirror.

The TOFPET2 is a 64-channel mixed-mode ASIC developed in standard CMOS 110 nm technology, which revises and add functionality to a previous chip version [4]. The proposed circuit is optimized for use with SiPMs with 320 pF total capacitance operating at gain of 1.25×10^6 . In such case, it provides r.m.s. time resolution below 100 ps for a single photo-electron (p.e). The circuit provides also linear amplitude measurement in the full dynamic range of input pulse charge (1500 pC). The maximum input charge corresponds to 2500 p.e. detected by devices with gain 3.5×10^6 .

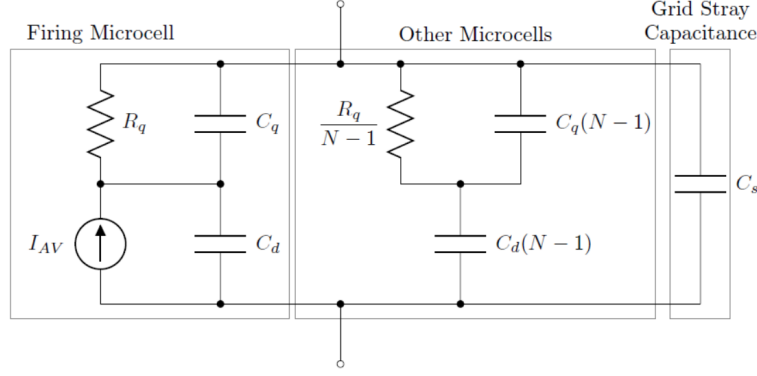


Figure 1. Electrical Model for the SiPM by [5].

Table 1. SiPM model parameters.

C_{TOT}	C_d	R_q	C_q	C_s	Q	N
320 pF	80 fF	160 k Ω	7 fF	6.8 pF	200 fC	3600

2 SiPM model

Electrical models for SiPMs were extensively described in [5], together with experimental setups to extract the relevant electrical parameters. The proposed model is depicted in figure 1. The dense array of the SiPM pixels has a total parallel capacitance C_{TOT} , which accounts not only for the grid capacitance C_g (due to the grid parallel interconnection) but also for the pixel capacitance $C_{cell} = C_d + C_q$, sum of the junction capacitance and the parasitic C_q . Therefore, $C_{TOT} = C_g + N(C_d + C_q)$ depends on the number of cells N in the array, thus on the active area, and may be in the range of 35 – 320 pF, respectively for 1 mm² and 9 mm² devices.

In order to extract these parameters, a test is performed on the SiPM biased at a voltage of few volts below the breakdown threshold to measure its impedance. A sinusoidal signal is injected across the device and the Bode diagram of the system is reconstructed by varying the frequency of the signal. The parameters of the model are reported in table 1.

The timing characteristics of the SiPM signals were measured with a pulsed laser, which generates light pulses of wavelength 375 nm and width of 50 ps. The corresponding SiPM signal is the result of several SiPM cells firing at about the same time. These data were compared to the transient simulations of one p.e. signal originated in one SiPM cell using the parameter in table 1. The good agreement between the data and the simulations shown in figure 2 confirms that this model is a sufficiently good approximation of the SiPM impedance and, thus, is suitable for ASIC frontend SPICE simulations.

3 ASIC architecture

The TOFPET2 ASIC general architecture is based on the previous chip version [4] but has significant differences. In particular, the new chip includes pulse amplitude measurement based on charge

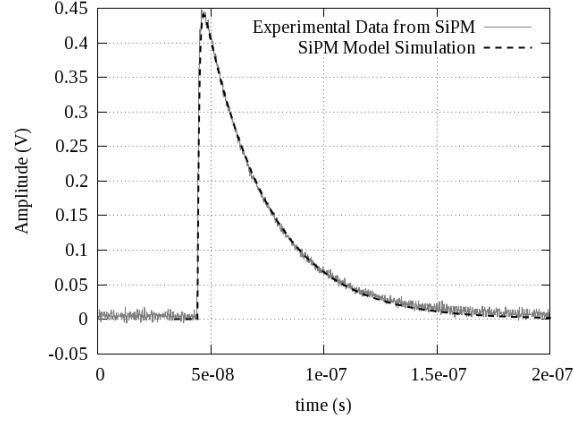


Figure 2. Output pulse for a SiPM activated by a pulsed laser compared to simulation results.

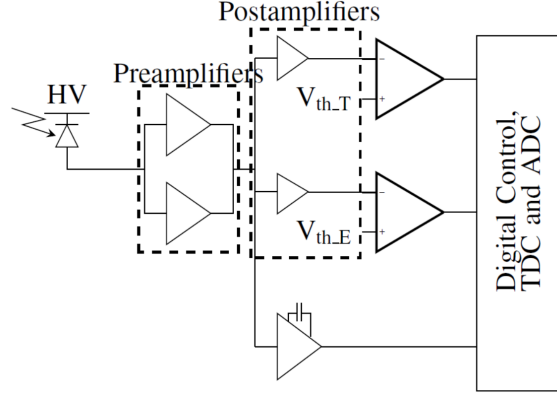


Figure 3. Top level scheme of the single channel.

integration and allows significant higher input and output data rates. The new requirements implied the redesign of the frontend amplifiers, the addition of a charge integrator and the full redesign of the digital logic.

The ASIC provides time and energy digitization of signals from 64 photo-sensor channels. While the circuit can operate with different photo-sensors, its performance was optimized for SiPMs. The ASIC has two selectable preamplifiers per channel allowing operation either with positive or negative polarity signals.

The readout scheme of one channel is depicted in figure 3. The selected preamplifier provides a signal to two post-amplifiers and a pulse-charge integrator. The post-amplifiers, separately specialized for time resolution and pulse triggering, have an adjustable transimpedance gain and provide voltage signals to two discriminators.

One discriminator is used for timing measurement with a programmable threshold down to a few photo-electrons. A second discriminator has higher threshold and is used for on chip rejection of low amplitude signals.

The signals from the discriminators are fed to a digital logic block, working at 200 MHz clock frequency, that controls two time-to-digital converters (TDC) and a charge integrator.

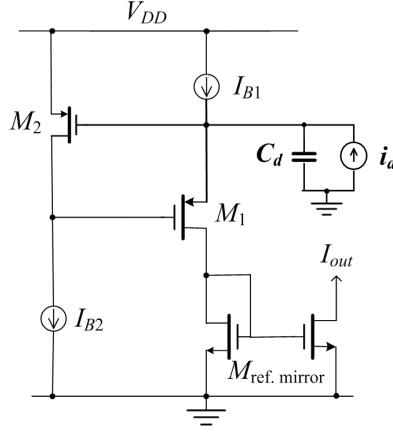


Figure 4. Simplified preamplifier circuit.

The first TDC measures the phase of the rising edge of the low threshold discriminator output with respect to the reference clock, while the second TDC measures the falling edge of the high threshold discriminator output. The mixed mode TDC block is based on four-fold time-to-analogue converter (TAC), for signal de-randomization and a 10 bit Wilkinson analogue-to-digital converter (ADC). The system is capable of 20 ps or 40 ps time binning (configurable).

The channel digital logic controls also the charge integration time interval, which can be configured with different options. The output of the charge integrator is digitized by a Wilkinson ADC. One out of two ADCs per channel is configured to measure either the charge amplitude (default mode) or the fine time of the falling edge of the high threshold discriminator. In the former case, the second time measurement has the resolution of the coarse time counter (200 MHz clock period). The time difference of the two measurements can be used to compute the time-over-threshold (ToT) which is dependent on the pulse amplitude. The digital data corresponding to each input pulse (event) is stored in local buffers waiting to be transferred to the global output FIFO. Each event is identified by the coarse time tag (clock counter) and by the channel identifier. The output data is transmitted by 1 to 4 LVDS links working at 400 or 800 Mbit/s each (configurable). The external clock is 400 MHz. The channel digital logic operates at half the main clock frequency.

4 Frontend amplifiers and discriminators

The preamplifiers are two selectable current conveyors, for positive and negative polarity signals, based on a modified version of the regulated common-gate transimpedance amplifier (TIA) [6]. The conveyors provide a low input impedance for the detector and a high impedance current output. The circuit for the positive signal version is showed in figure 4. It is an upgraded version of the preamplifier already proposed in [4], redesigned and optimized to extend the dynamic range while preserving timing performances. The negative signal version has the same topology, with the transistors, either NMOS or PMOS, switched to the complementary type.

With reference to figure 4, let us consider the regulator amplifier, consisting of the transistor M_2 , with gate-to-source transconductance g_{m2} and drain-to-source differential resistance r_{ds} , and the current source I_{B2} , with finite impedance r_{ib2} . The resulting output resistance of the amplifier

can be expressed as

$$R_{o2} = (r_{ds}^{-1} + r_{ib2}^{-1})^{-1}$$

The amplifier has a parasitic feedback capacitance C_{12} which is given by the parallel connection of the gate-to-drain capacitance C_{gd2} , concerning transistor M_2 , and the gate-to-source capacitance C_{gs1} , concerning transistor M_1 . Then, the transfer function of the regulator amplifier is given by

$$A(s) = -\frac{A_0}{1 + s \tau_a}$$

where

$$A_0 = g_{m2} R_{o2}$$

is the low-frequency amplification of the amplifier, and

$$\tau_a = R_{o2} C_{12}$$

is the time constant of the dominating pole. Following the analysis proposed in [7] for TIAs, the transfer function of the current conveyor can be expressed as

$$\frac{I_{Out}}{i_d} = \frac{1}{1 + s g_{m1}^{-1} C_d A_0^{-1} (1 + \frac{A_0 C_{12}}{C_d}) + s^2 A_0^{-1} g_{m1}^{-1} C_d \tau_a}$$

with g_{m1} the gate-to-source transconductance of transistor M_1 . The capacitance C_d represents the total capacitance of the SiPM, while i_d and I_{Out} are the input and output current signals of the preamplifier. With a power consumption of 2.5 mW in the preamplifier, a low-frequency amplification of 25 dB and pass-band of 330 MHz are achieved.

The post-processing is done by two transimpedance amplifiers and an integrator, which is described in the next session. The preamplifier is connected to the TIAs in AC mode. Each TIA is a PMOS current mirror replicating the AC part of the preamplifier current output on a 3 k Ω resistor.

The two TIAs feed discriminators. The first discriminator uses a low threshold at the level of one p.e., with resolution selectable between 0.5 and 0.1 p.e. The other discriminator has configurable threshold up to 1000 p.e. for on chip event selection.

5 Charge integrator

The charge integrator processes the output signal of the preamplifier within a time window that is generated by the digital logic, based on the discriminators output. In this scheme, four flipped capacitors sharing a single readout differential amplifier perform the signal integration, allowing de-randomization of the signals. The analogue signals are fed to a 10-bit analogue-to-digital converter (ADC) ADC for conversion. A simplified version of the integrator is depicted in figure 5.

The range of the integrator, specified in p.e. for a SiPM gain of 1.25×10^6 , can be selected among a set of possible ranges: 7.5 – 750 p.e., 15 – 1500 p.e., 30 – 3000 p.e. and 60 – 6000 p.e. These different ranges allow the use of the integrator in different schemes of PET crystals read-out, namely 1:1 coupling of crystal pixels to SiPM pixels and light sharing schemes, in which the light generated in a monolithic LYSO crystal is readout by several SiPMs pixels.

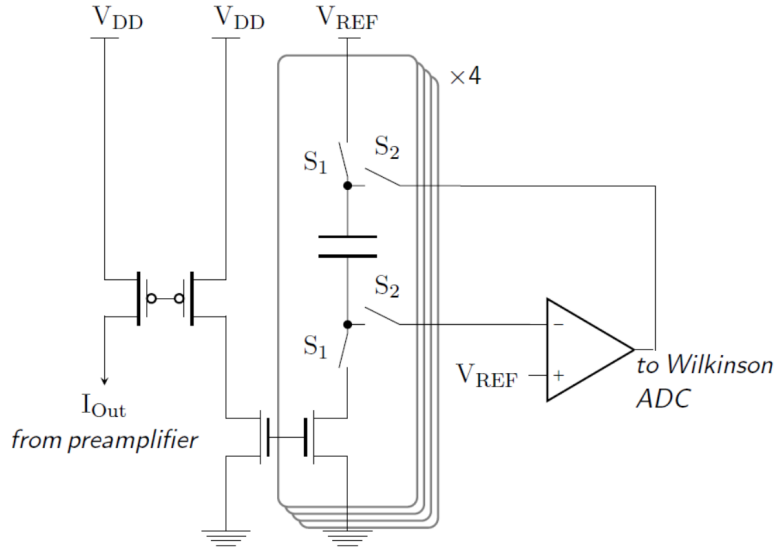


Figure 5. Simplified integrator scheme.

6 Back-end readout

The 64 channels data readout is handled by a global controller using an external clock up to 400 MHz, which builds-up the event data and runs the interface with the data acquisition back-end. The data above the trigger threshold are sent out in push mode. Each event consists of an event time tag, a channel identifier, and the time and amplitude measurements. Data transmission uses 64/66bit encoding to allow clock recovery and alignment of the data stream at the receiver. The ASIC has 4 output LVDS links working at 400 Mbit/s (SDR) or 800 Mbit/s (DDR). The performance in terms of output rate capability is 3.2 Gbit/s maximum rate, which allows 600 kHz average event rate per channel, and a dark counts rejection up to 2 MHz with negligible dead time.

7 Simulation results

In this section we present results of the chip simulations (schematics and post-layout). The simulations at schematic level were performed for the whole channel comprising all the blocks from the preamplifier to the digital control, including the integrator and the TDC/ADCs.

The results of the transient noise simulations of 1 p.e. input signals, assuming SiPM gain of 1.25×10^6 (3.5×10^6) and 320 pF total capacitance, show a time resolution of 75 ps (39 ps), with 4 mW (8 mW) power consumption per channel. These values were obtained from the time jitter of 100 simulated events at the discriminator output.

For post-layout verifications we compare the ratio between total integrated noise (N) at the output of the postamplifier and the slew rate (SR) for 1 p.e. input signals. In schematic level simulations this value is 102 ps, while in post-layout simulations the value of the ratio is 109 ps. The discrepancy between the noise-over-slew ratio for schematic level and post-layout simulations is less than 7%. Simulated 1 p.e. signal and noise at postamplifier output are shown in figure 6 [8].

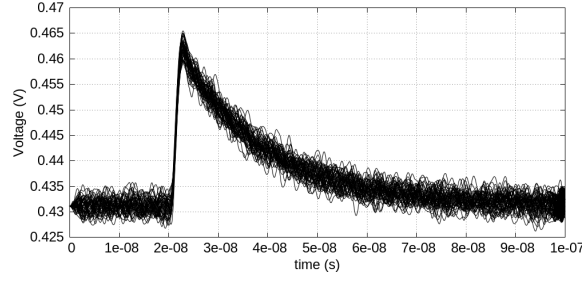


Figure 6. Transient noise simulation for a 1 p.e. (200fC) input signal, from a 320pF total capacitance SiPM. The waveform is kept at post-amplifier output.

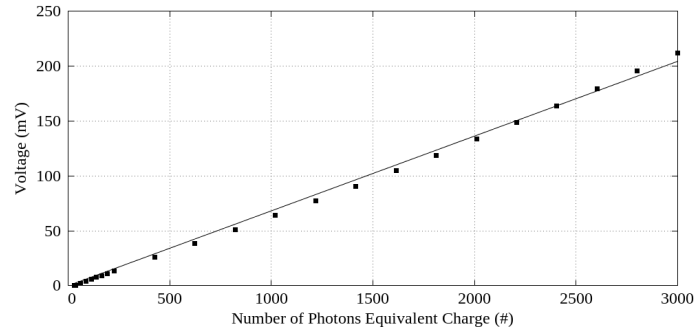


Figure 7. Simulated output linearity for the integrator in the range 30 – 3000 p.e.

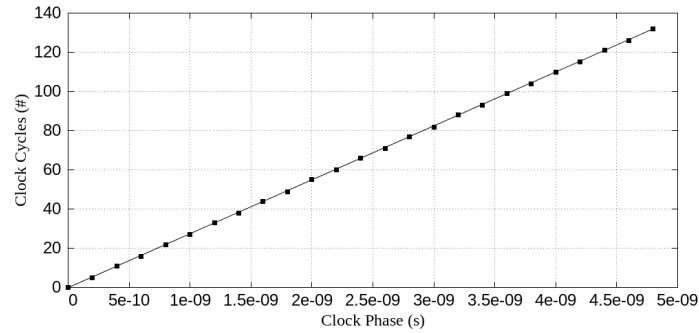


Figure 8. Simulated TDC conversion covering one clock period (5 ns) in steps of 200 ps and using TDC bin of 40 ps.

The linearity of the charge integrator for the setting 30 – 3000 p.e. is shown in figure 7. The maximum integral non linearity (INL) obtained at 3000 photo-electrons is 5% of the corresponding converted voltage, and it is adequate for the intended application. The analogue signals are fed to a 10 bit ADC for conversion.

The TDC linearity is depicted in figure 8, which shows simulated TDC conversions covering one clock period (5 ns) in steps of 200 ps and using a TDC bin of 40 ps. From these data we extract maximum INL 0.35 LSB.

8 Conclusions

The presented ASIC was designed to achieve a time resolution better than 100 ps for 1 p.e. signals generated by the considered SiPM, together with a linear amplitude response up to 3000 p.e. distributed in time according to the characteristic LYSO crystal light decay time. The design provides a wide range of configuration options, allowing for example to operate the ASIC in different PET light collection schemes like one-to-one coupling of LYSO crystals to SiPM pixels or light-sharing among several SiPM pixels. Additionally two different methods of pulse amplitude measurement are available, namely charge integration or ToT. The chip can operate with negligible dead time up to 600 kHz event rate per input channel, fulfilling the needs of all current or foreseen PET applications. The specified performances were achieved within the limited power budget of 5 mW per channel, in the case of SiPMs gain of 1.25×10^6 . The ASIC was submitted for production in early November 2015.

Acknowledgments

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