



International Workshop on Automobile, Power and Energy Engineering

A 130nm 1Mb Embedded Phase Change Memory with 500kb/s Single Channel Write Throughput

DING Sheng^{a*}, SONG Zhitang^a, CHEN Houpeng^a, CAI Daolin^a, WANG Qian^a,
CHEN Yifeng^a, CHEN Xiaogang^a, WU Guanpin^b, FENG Gaoming^a, XU Chen^a,
ZHONG Ming^a, XIE Zhifeng^b

^aState Key Laboratory of Functional Materials for Informatics, Laboratory of Nanotechnology, Shanghai Institute of Micro-system
and Information Technology, Chinese Academy of Sciences

^bSemiconductor Manufacturing International Corporation

Abstract

A 130nm 1Mb embedded phase change memory (PCM) has been achieved, requiring only three additional masks for phase change storage element, featuring 500kb/s single channel write throughput and $>10^8$ endurance. The prepare process has been optimized to reduce the cost and power. An 80nm heat electrode has been prepared with 130nm process. The optimal Read/Write circuit module is designed to realize the load/store function for PCM. The critical operation parameter is Reset/70ns/2.5mA and Set/1500ns/1mA, which means that the signal channel write throughput arrives to 500kb/s.

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Keywords: PCM, phase change memory, Reset, Set

1. Introduce

Phase Change Memory (PCM) is a promising technology to meet the growing need for a nonvolatile memory technology for high density and embedded CMOS applications with faster write speed and higher endurance than existing nonvolatile memories [1,2]. PCM is considered to be one of the most

* Corresponding author. Tel.: +86-021-62511070-8414; fax: +86-021-62134404

E-mail address: dinsh@mail.sim.ac.cn

promising candidates for the next-generation memory due to its advantages of non-volatility, high scalability, high speed, low power, and low cost [3]. Many companies and institutes have developed the large scale general PCM chip [4,5]. However, PCM is now challenged with the need of prove its cost effectiveness with providing the performances required by the system, with sufficient reliability. In this work we present a 1Mb embedded PCM chip with 130nm CMOS process, requiring only three additional masks for the storage element integration, featuring 500kb/s signal channel write throughput, and robust reliability results.

2. The cell structure and integration process

2.1. Cell Structure

The basic structure of PCM cell is shown in Fig. 1. This structure is called 1R1T, which is consisted of MOS (T) and phase change film (R). The advantage of 1R1T structure is low costs and low voltage drop in driving device which can ensure the voltage drop in phase change material exceed to the threshold value [6]. However, the problem of this structure is that the size of MOS is directly proportional to Reset current. Thus, to improve the density of memory array, Reset current should be reduced. Some researches show that the reset current is concerned with the contact area between heat electrode and phase change film [7]. The smaller contact area, the smaller reset current needed. Therefore the challenge of this structure is how to fabricate a tiny heat electrode in relative large size process. Next chapter will show our process results.

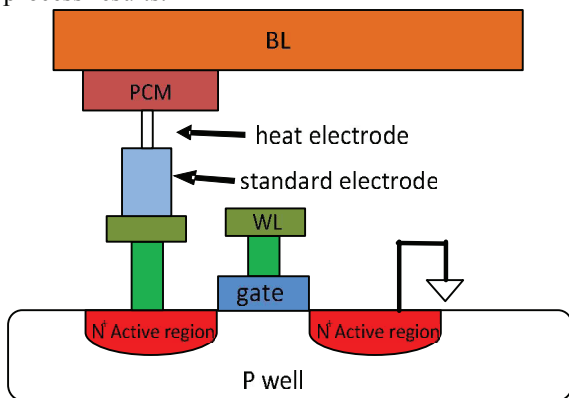


Fig. 1. The basic structure of PCM cell

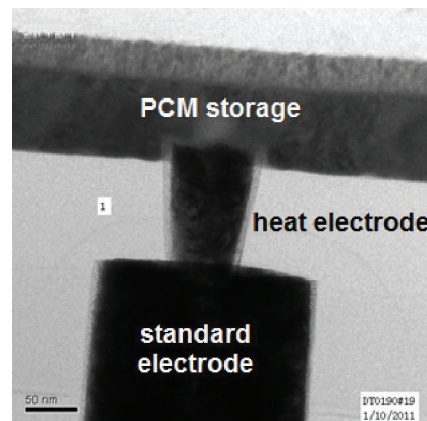


Fig.2. Transmission Electron Microscope (TEM) graph of the contact between electrode and phase change film

2.2. Integration Process

There are many ways to reduce the contact area [8]. In our embedded PCM chip, a self-alignment method is used to reduce the contact area [9]. We have successfully achieved the 80nm contact with 130nm CMOS process. Fig. 2 shows the Transmission Electron Microscope (TEM) graph of the contact between electrode and phase change film. From the graph, it is found that the standard contact is 130nm and the heat electrode is 80nm on the standard contact. For our self-alignment, the most advantage is that it only needs three additional masks to prepare PCM storage. So this process has low costs for preparing.

3. PERIPHERY CIRCUIT

3.1. Read Circuit

The function of read driving circuit is to distinguish between high resistance in the amorphous state and low resistance in the crystalline state. There exists the electrical switching effect (TSE) in PCM. If the read voltage exceeds the threshold, the resistance of PCM would change dramatically [10]. Thus, we have to use little enough read voltage. A cascade structure is used to realize this function, which is shown in Fig.3. *M1*, *M2*, *M3* and *M4* constitute a current mirror to supply the read current to PCM cell. If PCM cell is low resistance, the current in PCM cell is less than the current in *M3*&*M4*. The terminal *SDB* will be pull down. If PCM cell is high resistance, the current in PCM cell is larger than the current in *M3*&*M4*. The terminal *SDB* will be pull up. The comparator *X1* and latch *X2* can capture the voltage change of *SDB* during read operation. The gate of *M8* connects fixed voltage (*Vb*), which is a cascade structure and supplied by *M6* and *M7*. The terminal *BL* is connected to PCM cell. This structure ensures that read voltage in *BL* would not exceed *Vb*, which avoids the read damage. Fig.3(a) shows the schematic of our read circuit.

Fig.3(b) shows the simulation result of our read circuit. If PCM cell is high resistance, the *SDB* is pull up; if PCM cell is low resistance, the *SDB* is pull down. And during read operation, the voltage of *BL* is lower than the safe voltage.

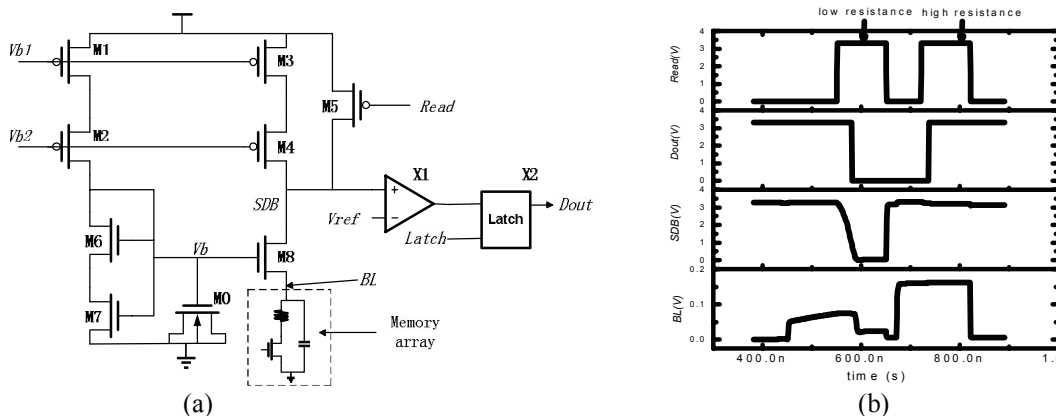


Fig.3.(a). The schematic of read circuit. (b) The simulation result of our read circuit.

3.2. Write Circuit

The function of write driving circuit is to operate the Reset/Set for PCM cell. The Reset/Set operation of PCM is based on current pulse. The heat generated by current pulse leads to reversible switching between high resistance in the amorphous state (Reset) and low resistance in the crystalline state (Set). The different pulse width and height cause different operation regardless of the initial state of cell. According to these theories, an easy current mirror for write driving circuit can satisfy our design request, which is shown in Fig.4.

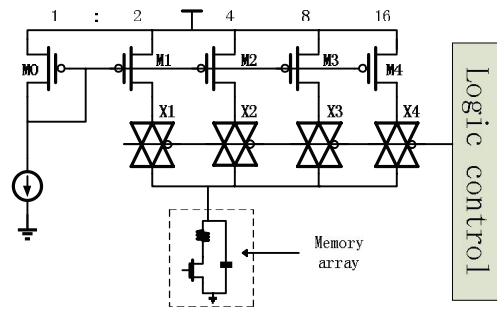


Fig.4. The schematic of write drive circuit

3.3. Full Chip

A full periphery circuit including read/write drive, decoder and PCM array has been successfully developed to realize the load/store function and improve the performance. Fig.5 shows the top schematic of our embedded IP core. And Fig.6 shows the micrograph of our embedded PCM chip.

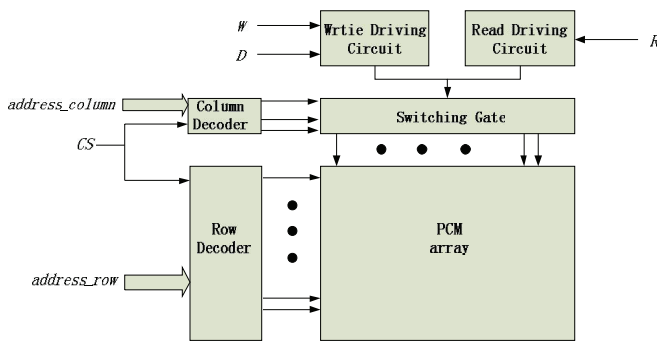


Fig.5. The framework of PCRAM chip

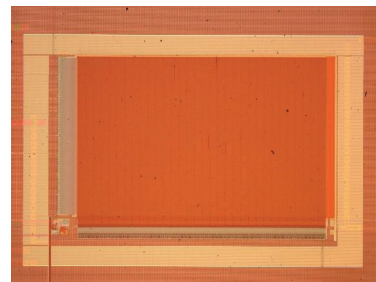


Fig.6. The micrograph of 1Mb PCRAM chip

4. Test Results

Fig.7 shows the write pulse current test result. We try different pulse width and height to operate PCM cell and measure the cell's resistance. This test can show the power cost and critical timing parameter for signal cell. Because of our tiny electrode, the reset current reduces, which means that the power cost reduces. It is found that the higher current corresponds to the faster timing. But there is a threshold value for timing, which means if the pulse width is lower than this threshold value, any current pulse cannot operate the cell. From this test, a group of optimal operation parameter is found: Reset/70ns/2.5mA and Set/1500ns/1mA. The signal channel write throughput arrives to 500kb/s.

Fig.8 shows the distribution of read-out resistance. Firstly, we measure the resistance of PCM cell. Then, we use our read module to read the PCM cell and record the read-out result. From fig.8, it is found that the cells whose resistance is larger than 18kohm is read-out "1" cell (which represents logic "0") and the cells whose resistance is lower than 15kohm is read-out "0" cell (which represents logic "1"). Thus, this test proves that our read module can distinguish between high resistance (18kohm) in the amorphous

state and low resistance (15kohm) in the crystalline state.

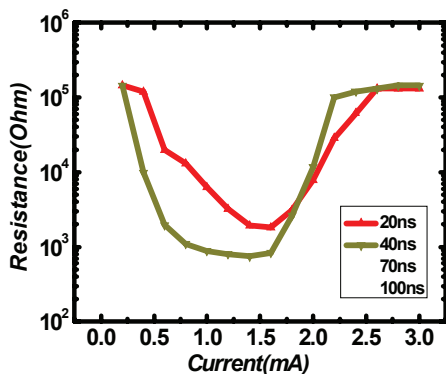


Fig.7. The write pulse current test results.

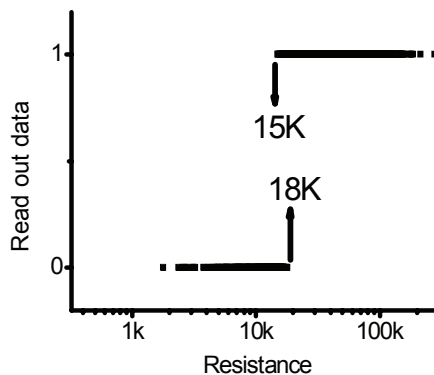


Fig. 8. The distribution of read-out resistance.

Figure 9 shows the resistance distribution. It is found that the proportion of cells which the resistance is <15kohm after Set operation is up to 99% and the proportion of cells which the resistance is >18kohm after Reset operation is up to 99%. This indicates the yield of full wafer. According to the more precise and harsher calculation, the yield of our PCM chip core is >99.99%.

Fig.10 shows the endurance result of our PCM cell. We operate one PCM cell repeat again and again, and then record the operation numbers. From the fig.10, it shows that the endurance is up to 10^8 which the typical endurance parameter for FLASH is about 10^6 .

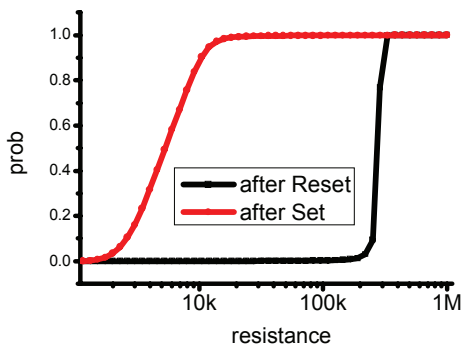


Fig.9. the distribution of PCM resistance

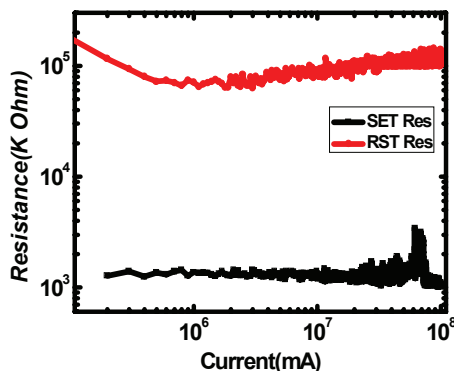


Fig.10. the endurance of PCM cell

5. Conclusion

1Mb embedded PCM chip with 130nm CMOS process has been successfully achieved. With only three additional masks for the PCM storage element integration, we reduce the cost and power. The full load/store function is realized with our periphery circuit. The write throughput arrives to 500kb/s and the

endurance of PCM cell is up to 10^8 .

Acknowledgements

Supported by National Integrate Circuit Research Program of China (2009ZX02023-003), National Basic Research Program of China (2007CB935400, 2010CB934300, 2011CB309602, 2011CB932800), National Natural Science Foundation of China (60906004, 60906003, 61006087, 61076121), Science and Technology Council of Shanghai (09QH1402600, 1052nm07000)

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