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Editorial

Selected Papers from the International Conference on Reconfigurable Computing and FPGAs (ReConFig'10)

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The sixth edition of the International Conference on Reconfigurable Computing and FPGAs (ReConFig'10) was held in Cancun, Mexico, from November 30 to December 2, 2010. This special issue covers actual and future trends on reconfigurable computing and FPGA technology given by academic and industrial specialists from all over the world. All articles in this special issue are extended versions of selected papers presented at ReConFig'10, for final publication they were peer reviewed to ensure that they are presented with the breadth and depth expected from this high quality journal.

There are a total of 16 articles in this issue. The following 8 papers correspond to the track titled general sessions. In "*Evaluation of Runtime Task Mapping Using the rSesame Framework*", K. Sigdel et al. present the rSesame framework to perform a thorough evaluation (at design time and at runtime) of various task mapping heuristics from the state of the art. The experimental results suggest that such an extensive evaluation can provide a useful insight both into the characteristics of the reconfigurable architecture and on the efficiency of the task mapping. In "*Exploration of Uninitialized Configuration Memory Space for Intrinsic Identification of Xilinx Virtex-5 FPGA Devices*", O. Sander et al. demonstrate an approach to utilize unused parts of configuration memory space for FPGA device identification. Based on a total of over 200,000 measurements on nine Xilinx Virtex-5 FPGAs, it is shown that the retrieved values have promising properties with respect to consistency on one device, variety between different devices, and stability considering temperature variation and aging. In "*Placing Multimode Streaming Applications on Dynamically Partially Reconfigurable Architectures*", S. Wildermann et al. discuss the architectural issues to design reconfigurable systems where parts of the hardware can be dynamically exchanged at runtime in order to allow streaming applications running in different modes of the systems to share resources. The authors propose a novel algorithm to aggregate several streaming applications into a single representation, called merge graph, in addition, they propose an algorithm to place streaming application at runtime which not only considers the placement and communication constraints, but also allows to place merge tasks. In "*On the Feasibility and Limitations of Just-in-Time Instruction Set Extension for FPGA-Based Reconfigurable Processors*", M. Grad and C. Plessl study the feasibility of moving the customization process to runtime and evaluate the relation of the expected speedups and the associated overheads. The authors present a tool flow that is tailored to the requirements of this just-in-time ASIP specialization scenario. The methods are evaluated by targeting a previously introduced Woolcano reconfigurable ASIP architecture for a set of applications from the SPEC2006, SPEC2000, MiBench, and SciMark2 benchmark suites. In "*A Fault Injection Analysis of Linux Operating on an FPGA-Embedded Platform*" J. S. Monson et al. present an FPGA-based Linux test bed for the purpose of measuring its sensitivity to single-event upsets. The test bed consists of two ML410 Xilinx development boards

connected using a 124-pin custom connector board. The Design Under Test (DUT) consists of the "hard core" PowerPC, running the Linux OS, and several peripherals implemented in "soft" (programmable) logic. In "*NCOR: An FPGA-Friendly Nonblocking Data Cache for Soft Processors with Runahead Execution*" K. Aasaraai and A. Moshovos propose an FPGA-friendly nonblocking cache that exploits the key properties of runahead execution. In "*A Dynamically Reconfigured Multi-FPGA Network Platform for High-Speed Malware Collection*", S. Mühlbach and A. Kock refine the base NetStage architecture for better management and scalability. By using dynamic partial reconfiguration it is possible to update the functionality of the honeypot during operation. The authors describe the technical aspects of these modifications and show results evaluating an implementation on a current quad-FPGA reconfigurable computing platform. In "*Exploring Many-Core Design Templates for FPGAs and ASICs*", I. Lebedev et al. present a highly productive approach to hardware design based on a many-core microarchitectural template used to implement compute-bound applications expressed in a high-level data-parallel language such as OpenCL. The template is customized on a per-application basis via a range of high-level parameters such as the interconnect topology or processing element architecture.

Two papers are within the area of security and cryptography. In "*Implementation of Ring-Oscillators-Based Physical Unclonable Functions with Independent Bits in the Response*", F. Bernard et al. analyze and propose some enhancements of Ring-Oscillators-based Physical Unclonable Functions (PUFs). PUFs are used to extract a unique signature of an integrated circuit in order to authenticate a device and/or to generate a key. The authors show that designers of RO PUFs implemented in FPGAs need a precise control of placement and routing and an appropriate selection of ROs pairs to get independent bits in the PUF response. In "*Blind Cartography for Side Channel Attacks: Cross-Correlation Cartography*", L. Sauvage et al. present a localisation method based on cross-correlation, which issues a list of areas of interest within the attacked device. It realizes an exhaustive analysis, since it may localise any module of the device and not only those which perform cryptographic operations. The method is experimentally validated using observations of the electromagnetic near field distribution over a Xilinx Virtex 5 FPGA.

Two papers are within the area of high performance reconfigurable computing. Nonuniform random numbers are key for many technical applications, and designing efficient hardware implementations of nonuniform random number generators is a very active research field. However, most state-of-the-art architectures are either tailored to specific distributions or use up a lot of hardware resources. At ReConFig'10, we have presented a new design that saves up to 48% of area compared to state-of-the-art inversion-based implementation, usable for arbitrary distributions and precision. In "*A Hardware Efficient Random Number Generator for Nonuniform Distributions with Arbitrary Precision*", C. de Schryver et al. introduce a more flexible version of a non-uniform random number generators presented at ReConFig'10.the authors introduce a refined segmentation scheme that allows to reduce the approximation error significantly.

Two papers are within the area of multiprocessor systems and networks on chip. In "*Redsharc: A Programming Model and On-Chip Network for Multi-Core Systems on a Programmable Chip*", W. V. Kritikos et al. document the API, describe the common infrastructure, and quantify the performance of a complete implementation of the reconfigurable data-stream hardware-software architecture (Redsharc). The authors also report the overhead, in terms of resource utilization, along with the ability to integrate hard and soft processor cores with purely hardware kernels being demonstrated. In "*Combining SDM-Based Circuit Switching with Packet Switching in a Router for On-Chip Networks*", A. Kuti Lusala and J. D. Legat present a hybrid router architecture for Networks-on-Chip "NoC". The architecture combines Spatial Division Multiplexing- "SDM-" based circuit switching and packet switching in order to efficiently and separately handle both streaming and best-effort traffic generated in real-time applications. Combining these two techniques allows mitigating the poor resource usage inherent to circuit switching.

Finally, two more papers are within the area of reconfiguration techniques. In "*Dynamic Circuit Specialisation for Key-Based Encryption Algorithms and DNA Alignment*", T. Davidson et al. explain the core principles behind the dynamic circuit specialization technique. Parameterised reconfiguration is a method for dynamic circuit specialization on FPGAs. The main advantage of this new concept is the high resource efficiency. Additionally, there is an automated tool flow, TMAP, that converts a hardware design into a more resource-efficient runtime reconfigurable design without a large design effort. In "*Using Partial Reconfiguration and Message Passing to Enable FPGA-Based Generic Computing Platforms*", M. Saldaña et al. introduce a new partition-based Xilinx PR flow to incorporate PR within the previously proposed MPI-based message-passing framework to allow hardware designers to create template bitstreams, which are predesigned, prerouted, and generic bitstreams that can be reused for multiple applications.

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