PHOTOVOLTAIC ENERGY HARVESTER WITH POWER MANAGEMENT SYSTEM

M. Ferri*, D. Pinna, E. Dallago, P. Malcovati

University of Pavia, Dept of Electrical Engineering, via Ferrata 1 - 27100 (PV), Italy

Abstract

The reduction trend of modern microsystem power consumption is balanced by the constant growth of complexity. Traditional batteries are, therefore, no longer sufficient for many applications, since they cannot guarantee a long enough life time [1]. By harvesting energy from the environment, such systems could work for nearly infinite time without the need of replacing batteries. In this paper we present a photovoltaic energy harvester system with a power management system to handle the collected energy. In the realized solution a couple of integrated miniaturized solar cells are used as energy source. The block diagram of the proposed system is shown in Fig.1



A 1 mm² integrated solar cell supplies an oscillator that provides the correct phase signals to eight Dickson charge pumps (only one charge pump is shown for simplicity). The storage capacitor C_S is external, thus allowing us to choose the proper capacitance according to the operating time-slot required to supply the load. In order to control the charge status of the capacitor, the voltage across C_S is monitored by an hysteresis comparator followed by a level shifter. This charge monitoring system is supplied by the second solar cell (auxiliary). When C_S is fully charged, the level shifter turns on the *p*-MOS switch M_S , thus connecting the load, discharging the capacitor and starting a new working cycle. In order to guarantee a stabilized voltage supply to the load we realized on-chip also a voltage regulator (LDO). The LDO, placed between the switch *p*-MOS switch M_S and the load, is supplied only when the load is connected.

The photovoltaic energy harvesting elements, implemented on-chip, are based on p-n junctions. Fig. 2 shows the cross-section and the equivalent circuit of the integrated micro solar cell [2].



The cell is realized with an *n*-well enclosing a *p*-diffusion, implemented with a particular geometry [3], in order to optimize the active area density and, hence, the efficiency. Fig. 3 shows the power curve of the realized cell, obtained with 300 W/m² illumination. As the substrate must be short-circuited with the n-well, the efficiency of the cell is, unfortunately, reduced by the recombination effect in the base of the parasitic *pnp* vertical transistor.



The proposed system has been realized in 0.35-µm CMOS technology. Fig. 4 shows the microphotograph of the chip. The chip area is 2.32 mm x 2.54 mm.





Fig. 5 shows the measured voltage V_S, acquired over a time-slot of 15 s, obtained for different values of C_S (47 nF, 100 nF and 147 nF). The system is illuminated with a light source, delivering about 300 W/m² and the load is a 10 MΩ resistor. Fig. 5 shows also the measured curent through the 10-MΩ resistive load over a time-slot of 30 s for different values of C_S (47 nF, 100 nF and 147 nF). The different peak values of the curves are due to the acquisition sampling frequency. Depending on the capacitance value, the energy available for the load and, hence, the operation duty-cycle changes. With $C_S = 147$ nF, for example, the system provides the same current value as with $C_S = 47$ nF, but for a longer time-slot.



REFERENCES

- 1. C. W. Seitz, "Industrial battery technologies and markets," IEEE Aerospace and Electronics Systems Magazine, vol. 9, no. 5, pp. 10–15, May 1994.
- 2. J. Ohsawa, K. Shono, and Y. Hiei, "High-voltage micro solar cell arrays of GaAs with output voltage up to 100 V" in IEEE/LEOS International Conference on Optical MEMS Conference Digest, 2002, pp. 103–104.
- M. Ferri, D. Pinna, E. Dallago and P. Malcovati, "Active area density optimization technique for harvester photodiodes efficiency maximization," in Sensors and Microsystems, P. Malcovati, A. Baschirotto, A. D'Amico, and C. Di Natale, Eds., Springer, The Netherlands, 2010, pp. 117–120.