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Research Article

Ka Band Phase Locked Loop Oscillator Dielectric Resonator Oscillator for Satellite EHF Band Receiver

S. Coco,[1] F. Di Maggio,[2] A. Laudani,[1] and I. Pomona[2]

[1] *DIEES, University of Catania, V. A. Doria 6, 95125 Catania, Italy*
[2] *Selex Communications, V. S. Sonnino 6, 95045 Misterbianco (CT), Italy*

Correspondence should be addressed to A. Laudani, alaudani@diees.unict.it

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This paper describes the design and fabrication of a Ka Band PLL DRO having a fundamental oscillation frequency of 19.250 GHz, used as local oscillator in the low-noise block of a down converter (LNB) for an EHF band receiver. Apposite circuital models have been created to describe the behaviour of the dielectric resonator and of the active component used in the oscillator core. The DRO characterization and measurements have shown very good agreement with simulation results. A good phase noise performance is obtained by using a very high Q dielectric resonator.

1. INTRODUCTION

In satellite network links, the phase noise performance and the required spectral purity of the local oscillator of the LNB receiver are very important issues [1–3]. In this case, a fundamental local oscillator locked to a very stable external reference can be the best architectural solution.

In this paper, we present the design and fabrication of a Ka band phase locked loop (PLL) dielectric resonator oscillator (DRO) used as local oscillator in the low-noise block of a down converter (LNB) for an EHF band receiver.

In order to obtain the best performance in terms of low-phase noise and output spurious the dielectric resonator oscillator architecture at the fundamental frequency (19250 GHz) has been chosen. A good phase noise performance is obtained by using a very high Q dielectric resonator. In order to analyze the behavior of the dielectric resonator and the active component used in the oscillator core, apposite circuital models have been created. The circuit simulations have been performed by using the harmonic balance solver available in advanced design system (ADS) simulation tool.

The oscillator circuit is fabricated by using SMT components mounted on a multilayer substrate: this represents a quite unusual realization for EHF applications. Two prototypes have been constructed and a full characterization has been carried out and the measurements show very good agreement with simulation results and then the PLL DRO has been integrated in a low-noise block down converter for EHF band satellite communication terminals.

The design, simulations, fabrication, and measurements have been carried out at Selex-Communications site of Misterbianco (CT), Italy.

2. OSCILLATOR DESIGN

The fundamental oscillation frequency is 19250 GHz. The architecture of the DRO circuit is based on a series feedback network, exhibiting a good performance in terms of a low drift of the oscillation frequency with respect to load variations [4–7]. A GaAs FET (Excelics EPB018A7) was chosen as active component both for its easy assembling and for its good gain and noise performance at working frequencies.

Because of the scarce information provided by the manufacturer for this component (only S parameters and gain at 1 dB compression point are given), it has been necessary to create an apposite nonlinear model to be used for the simulations. As starting point we used a Triquint own model available in the advance design system simulation tool

Table 1: LNB receiver performances.

Input frequency range	202 ÷ 21.2 GHz
Output frequency range	90 ÷ 1950 MHz
Gain	55 dB
Noise figure	1.6 dB
Gain flatness	
Any 500 MHz	3.5 dB
Any 40 MHz	1.6 dB
Spurious emission	>60 dBc
Phase noise	
@ 1 KHz	78 dBc/Hz
@ 10 KHz	84 dBc/Hz
@ 100 KHz	105 dBc/Hz
@ 1 MHz	120 dBc/Hz

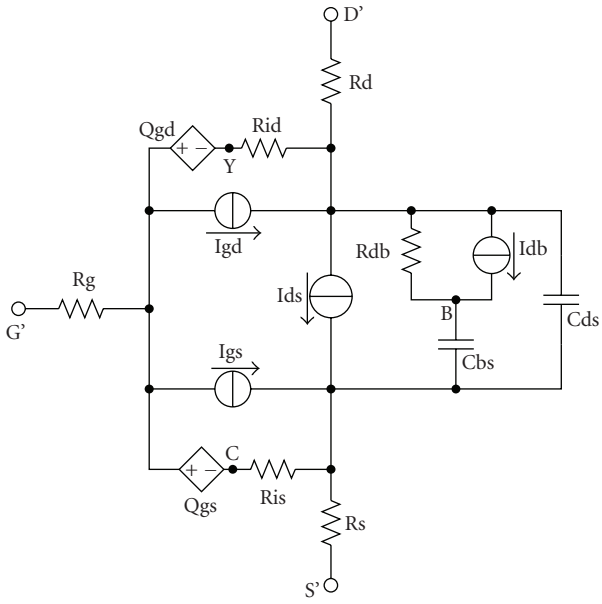


Figure 1: Triquint own model.

(Figure 1). This model has been improved by adding series inductances and resistances to the three device terminals and other capacitances in order to take into account the parasitic effects of the package (Figure 2).

Model parameters have been evaluated by using the information available from the manufacture. A dielectric resonator of high permittivity ceramic material has been chosen as resonant element; it is characterized by high temperature stability and a dielectric constant ranging between 30 and 40. In order to obtain high values of the quality factor (1000–40000), a metallic cover has been used. The desired phase noise characteristics are achieved thanks to the high-impedance path coupling the DRO to the other components. In order to simulate the behavior of the dielectric resonator within the oscillator circuit, an apposite *S* parameters model was created. This model foresees two microstrip lines placed in close proximity of the resonator and an apposite block describing the coupling effects between the dielectric resonator and the microstrip lines by using *S* parameters.

The simulation results for this model gives a resonant frequency of 19.250 GHz as expected.

To obtain good phase noise performance, the oscillator has been locked to an external reference by using a PLL architecture. The block diagram of the PLL is shown in Figure 3. The DRO output is compared with a 10 MHz reference in the main PLL circuit. The external reference signal is first filtered by another PLL circuit (cleaner) used to lock the output signal of a voltage controlled crystal oscillator (VCXO). The charge pump output is used to drive a varactor loaded with a microstrip stub inside the cavity in which the overall DRO is housed. The loop bandwidth is then optimized according to the phase noise specifications. A microcontroller shown in Figure 3 manages frequency assignment for the two PLLs.

3. TECHNOLOGY

Bare die devices mounted on the traditional hard substrate (Alumina) are generally used for EHF applications. On the other hand, in very complex circuits for low-frequency applications multilayer substrates and surface mounted technology are normally used. For the realization of this PLL DRO oscillator we made the choice of using a new ceramic multilayer substrate and packaged surface mounted devices (SMD), now available for high-frequency applications. In this way, all the complex oscillator circuit has been compactly fabricated in a small-size area employing easy mounting and low-cost materials. The multilayer substrate is composed by a ceramic layer (ε_r = 9.9), on which the microstrip lines have been realized, and four FR4 (ε_r = 4.4) layers used for the other interconnections. The final compact layout is shown in Figure 4. The dielectric resonator is visible inside the cavity. Even if at these frequencies distributed DC-blocks are generally used because of their low-insertion losses, in our case a more compact solution employing ceramic capacitances has been adopted. The prototype fabricated is shown in Figure 5. The board has been housed inside a metallic structure, closed by a cylindrical metallic waterproof cover (Figure 5).

4. SIMULATIONS AND MEASUREMENTS

The two circuital models have been used in the simulation of the complete oscillator circuit (Figure 6). Each lumped and distributed component has been optimized in order to reach the required phase noise and output power. The computed phase noise and output signal spectrum are shown in Figure 7. The phase noise and the output spectrum measured at the LNB output interface are shown in Figure 8. The CW input signal at 20700 MHz has been fed by a source generator. The measurements exhibit a very good

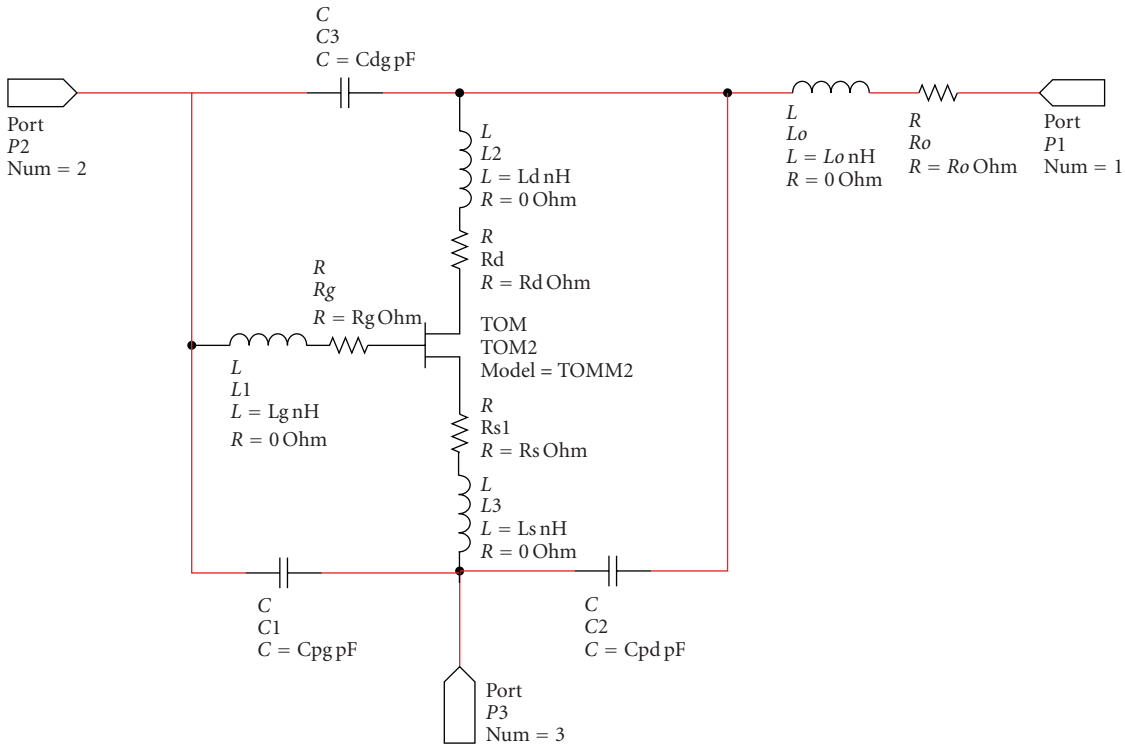


Figure 2: Improved model taking into account the parasitic effects of the package.

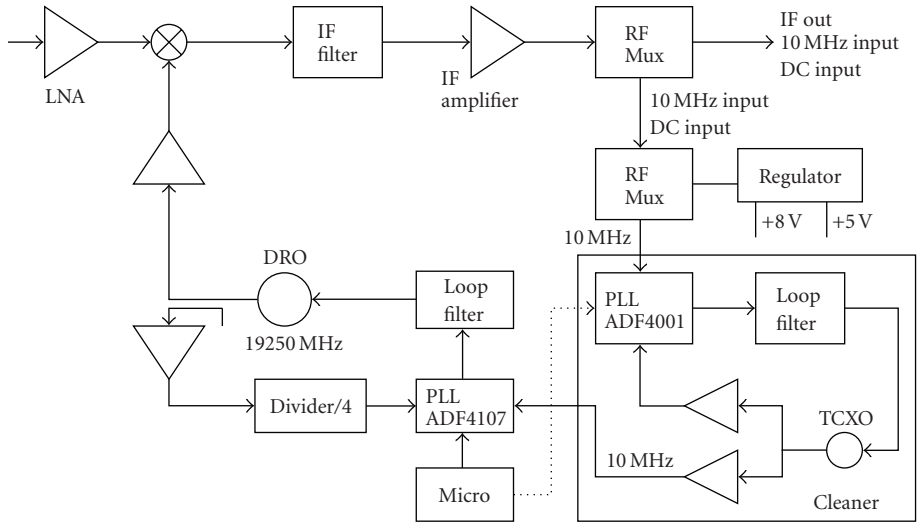


Figure 3: PLL block diagram.

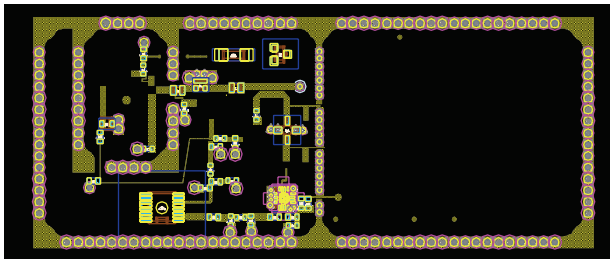


Figure 4: Final compact layout.

performance both in terms of phase noise and in terms of spectral purity.

5. LNB TEST RESULTS

The PLL DRO described above has been integrated in the low-noise block of the down converter for EHF band satellite communication terminals. The most significant performances obtained are summarized in Table 1.

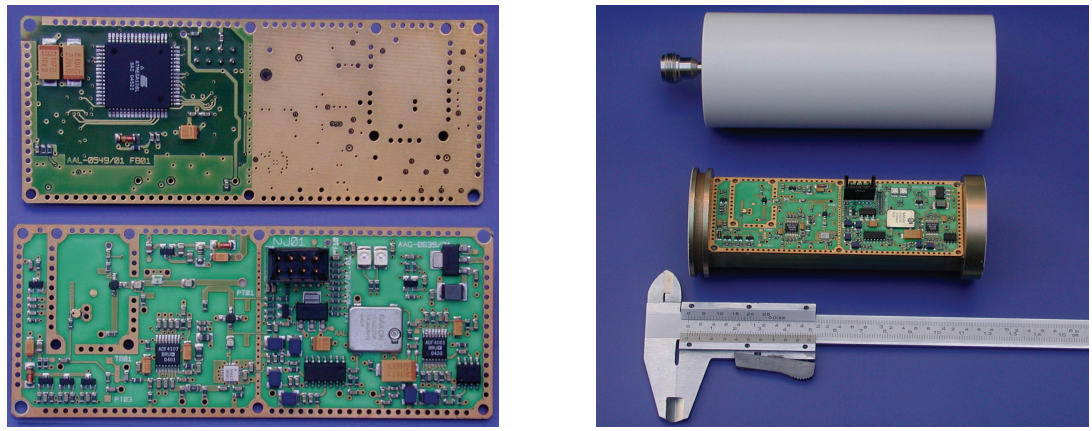


Figure 5: The prototype.

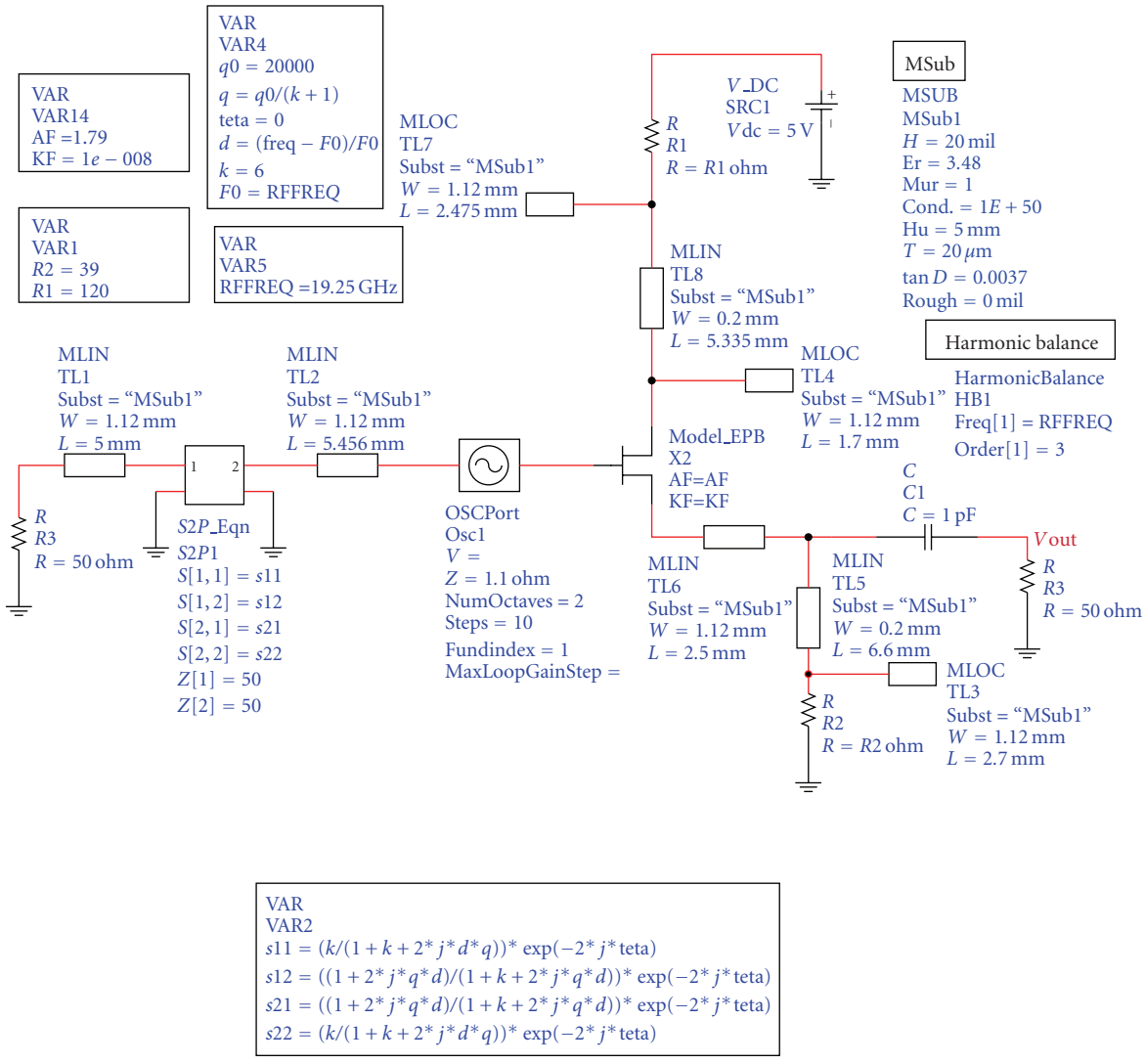
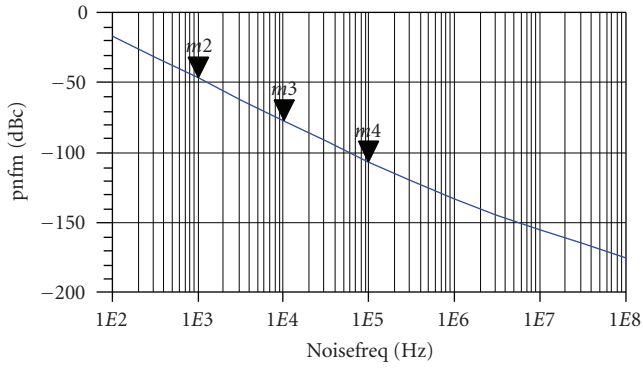
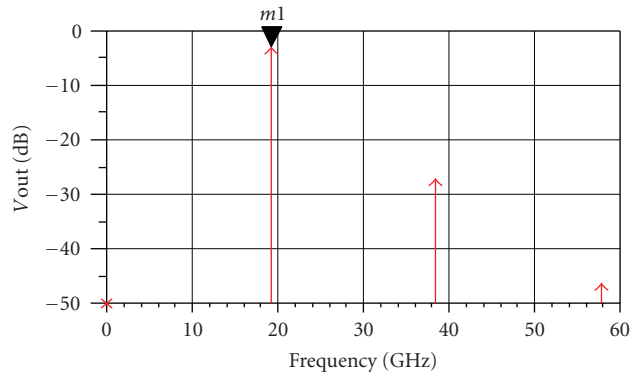


Figure 6: The complete oscillator circuit used for simulation.

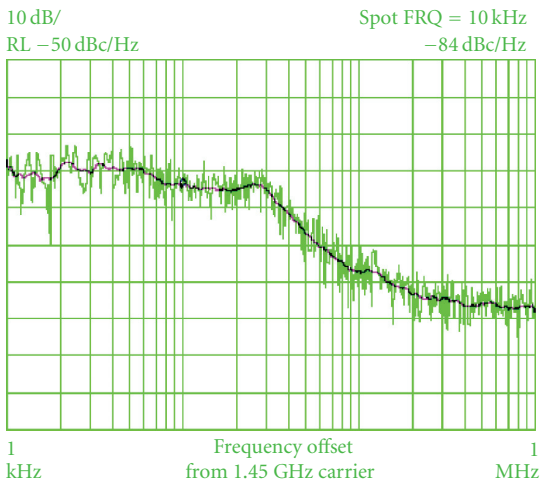




$m2$
Noisefreq = 1 kHz $m2 = -46.71$ dBc
$m3$
Noisefreq = 10 kHz $m3 = -76.65$ dBc
$m4$
Noisefreq = 100 kHz $m4 = -106.1$ dBc

$m1$
Frequency = 19.24 GHz $m1 = -3.017$

Figure 7: Simulation results.



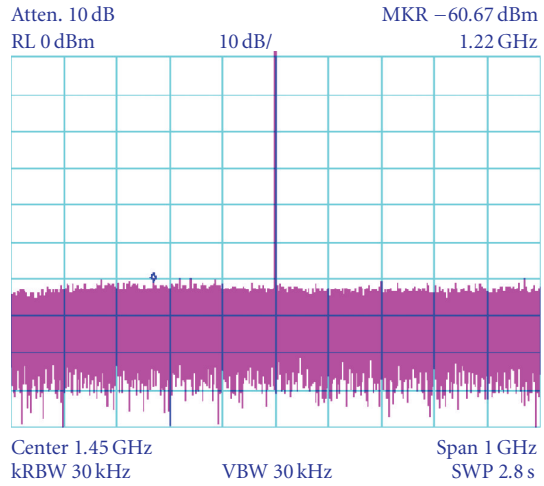


Figure 8: The phase noise and the output spectrum measured at the LNB output interface.

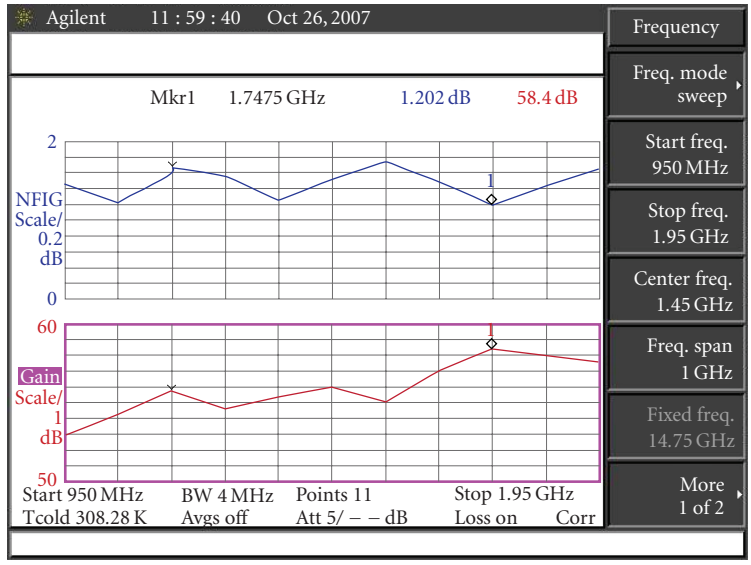


Figure 9: LNB gain and noise figure.

The phase noise measured is compatible with end-to-end forward performances as recommended in DVB-S2 standard. The LNB noise figure and gain are shown in Figure 9.

6. CONCLUSIONS

In this paper, a state-of-the-art phase locked DRO for an EHF low-noise block down converter is presented. The circuital models, appositely created to describe the behavior of the dielectric resonator and the active component used in the oscillator core, have provided a good methodology in order to speed the design process. The DRO has been used in a low-noise block down converter for EHF band satellite communication terminals. The phase noise obtained makes this LNB receiver particularly suitable for DVB-S2 applications.

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