Physical and Electrical Performance Limits of High-Speed SiGeC HBTs—Part II: Lateral Scaling

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***Abstract*—The overall purpose of this paper is the prediction of the ultimate electrical high-frequency performance potential for SiGeC HBTs under the constraints of practical applications. This goal is achieved by utilizing advanced device simulation tools with parameters calibrated to experimental results of most advanced existing technologies. In addition, detailed electrostatic and electrothermal simulations are performed for determining the parasitic capacitances, temperature increase, and safe operating area of aggressively scaled devices. The important figures of merit are then determined from circuit simulation employing an accurate compact model incorporating all relevant physical effects. Based on the vertical profile found in Part I, this paper focuses on achieving a balanced device design by lateral scaling. It is shown that the peak values of $(f_T, f_{\max})$ around (1, 1.5) THz may be achievable. Such a performance limit provides still significant headroom for further developing existing processes and makes SiGeC HBTs well-suitable for highly integrated millimeter-wave applications operating within the low-end of the terahertz gap.**

***Index Terms*—device simulation, high-performance bipolar technology, physical limits, SiGeC heterojunction bipolar transistor (HBT) device scaling.**

I. Introduction

AS OUTLINED IN detail in Part I [1] of this paper, SiGeC HBT technology has become a major contender for a large variety of applications ranging from consumer to emerging milimeter-wave electronics. In particular, the latter applications have moved into focus with the latest achievements in SiGeC HBT speed exhibiting $(f_T, f_{\max}) = (300, 500)$ GHz [2]. The overall goal of this paper is to explore the future prospects of SiGeC HBTs by investigating their ultimate electrical high-frequency (HF) performance potential using advanced device modeling tools. In [1], the vertical profile was aggressively scaled down to limits given by the constraints of practical applications. This results in 1-D isothermal device characteristics with the transit frequency f_T close to 1.5 THz at the open-base breakdown voltage $\mathrm{BV_{CEO}}$ well above 1 V.

In this paper, the 1-D structure is extended to a realistic 3-D device structure that includes all relevant parasitics, such as series resistances and capacitances, as well as the associated physical effects such as perimeter current injection, collector current spreading, and self-heating. 2-D and 3-D simulation tools are used to determine the parasitic capacitances and temperature increase along with the thermal impedance for aggressively scaled lateral dimensions. As outlined in the methodology description in Part I, the 1-D doping profile is kept unchanged during the lateral scaling procedure. Hence, the purpose of the latter is to determine the range of lateral dimensions yielding a balanced device design in which the ratio of $f_{\max}/f_T$ assumes reasonable values that are suitable for practical applications.

This paper is organized as follows. Section II details the lateral scaling approach and presents the obtained nonisothermal results. In Section III, the safe operating area (SOA) of the scaled devices is investigated, including self-heating, impact ionization, and tunneling effects. Finally, major issues associated with achieving the predicted ultimate HF performance and device fabrication are discussed in Section IV. The reader is referred to Part I for a list of often used acronyms and to [25] for supporting information on internal variables of the simulation and other relevant results.

II. Lateral Scaling

The lateral scaling analysis was performed for a complete 3-D transistor structure using a compact model with all relevant parasitic effects included. In the following, the determination of the model parameters is described. Then, the results of lateral scaling and possible tradeoffs are discussed.

A. Compact Model

For circuit simulations, the latest version 2.3 of the standard compact model HICUM/Level2 was employed [3]. From the electrical characteristics of the 1-D doping profile (cf. [1, Fig. 2]), the area-specific HICUM parameters for the internal transistor were extracted, which included those for the bias-dependent internal base sheet resistance. Fig. 1(a) shows the output characteristics of the Boltzmann transport equation (BTE) solution for different voltages V_{BE}. Since the BTE solver used does not include tunneling, the contributions to the base and collector current from trap-assisted and band-to-band tunneling as well as from impact ionization were calculated

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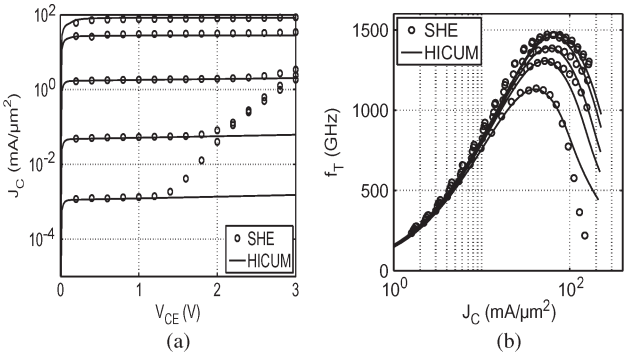

Fig. 1. Comparison between HICUM and 1-D BTE (SHE) results. (a) Output characteristics over a wide range of collector current densities at $V_{\rm BE} = [0.6, 0.7, 0.8, 0.9, 0.95]$ V. (b) Transit frequency versus collector current density for $V_{\rm BC} = [-1.0, -0.5, 0.0, 0.25, 0.5]$ V.

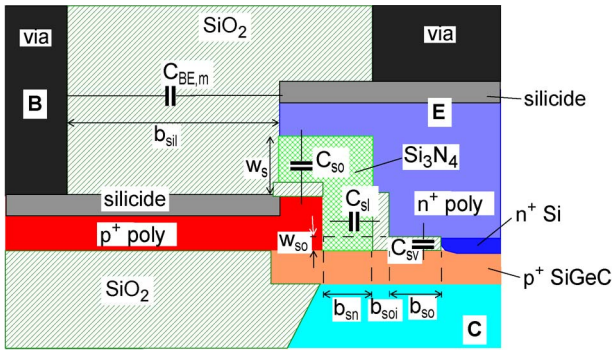

Fig. 2. Detailed schematic structure used for determining the parasitic BE spacer and metallization capacitances. The relevant dimensions were varied in the following ranges: $b_{\rm so} = [5 \ldots 30]$ nm, $w_{\rm so} = b_{\rm soi} = [2.5 \ldots 5]$ nm, $w_s = [5 \ldots 25]$ nm, $b_{\rm sn} = [10 \ldots 20]$ nm, and $b_{\rm sil} = [50 \ldots 250]$ nm.

consistently with HD simulation and then added to the BTE results. The 1-D compact model describes the BTE results very well. However, it does not include the effects of tunneling and (nonlocal) impact ionization in the base–collector region since sufficiently accurate model equations for these effects have not been implemented yet and since these effects have negligible influence on the small-signal figures of merit (FoMs) within the bias range of interest. Fig. 1(b) exhibits the transit frequency for different voltages $V_{\rm BC}$. The compact model captures the BTE results quite well up to current densities sufficiently beyond peak f_T and thus is well suited for the subsequent lateral scaling investigations.

The parameters for the elements describing the current and charge contributions of the emitter perimeter and external transistor regions were extracted from 2-D device simulation and then converted into parameters per length and per area. The values of these "process-specific" parameters remain constant during the lateral scaling procedure as long as the vertical doping profile remains unchanged. The concept of the effective junction width and area [4] has been used to include corner contributions. Electrostatic simulations were used to determine the parameters for the parasitic capacitances of the BE spacer and the contact metallization. The corresponding structure is shown in Fig. 2 along with the various capacitance contributions inserted. The electrostatic simulations were performed for a variety of dimensions covering a physically meaningful range down to extreme values. The results were converted to simple scaling equations using per unit length capacitance values. Regardless of the dimensions, the by far largest capacitance contributions are those of $C_{\rm sv}$ (ca. 70%) and $C_{\rm sl}$ (ca. 15%). Finally, the temperature coefficients of the compact model were determined directly from the bias-dependent BTE solution at 400 K for the 1-D case, from 2-D simulation for most of the external elements, and from existing experimental data for the contact resistances, which cannot be obtained from device simulation.

The complete set of specific parameters was then fed into the scaling tool TRADICA [5], which has been used for many years in the industry for production library and statistical model generation for existing SiGe HBT technologies. The scaling includes all relevant 2-D/3-D parasitic effects, such as emitter corner rounding and collector current spreading, as well as the detailed geometry dependence of series resistances (e.g., in [6] and [7]). Along with the design rules, the specific electrical parameters allow the generation of simulator model cards for a complete transistor structure based on given emitter dimensions and contact arrangement. The CBEBC configuration with $l_{E0} \gg b_{E0}$ (stripe structure) was selected since it generally yields the highest speed [8], whereas a short CEB structure with $l_{E0} = 3b_{E0}$ was selected due to its sensitivity to 3-D parasitic effects. All results shown below were obtained with the compact model and include all parasitic capacitances, self-heating, and 2-D/3-D effects; in addition, current densities are defined by normalizing the collector or base current to the actual emitter window area A_{E0}.

B. Scaling Results

The scaling considerations below were performed for the device structure shown in Fig. 3. The shallow vertical doping profile is completely contained within the shallow-trench thickness. The collector width hardly exceeds the emitter opening in the base polysilicon and, at its bottom, is assumed to be connected by a surrounding buried silicide or heavily doped silicon region. The structure shown in Fig. 3 assumes, e.g., a silicon-on-insulator (SOI) CMOS process, in which the HBT collector region has been opened to the bulk. However, results for an SOI HBT will also be presented since they are considered as a worst-case scenario from a thermal point of view.

The initial dimensions were based on the device structures and design rules of STMicroelectronics' most advanced BiCMOS process. The design rules allow, e.g., for a minimum emitter width of $b_{E0} = 50$ nm with a spacer width of $b_s = 45$ nm and define the initial scaling factor $s = 100\%$. The results for f_T and $f_{\rm max}$ are shown in Fig. 4 for the initial structure as well as for shrunk dimensions ($s < 100\%$). The values at 100% are already somewhat lower than those obtained from 1-D simulation (cf. Part I) due to the added parasitics of the complete 3-D structure. The spread in the FoMs indicates their sensitivity with respect to the most important uncertain parameters. Fundamentally, contact resistances are impossible to predict from device simulation; hence, estimated values based on existing state-of-the-art technology have been used. Among all contact resistivity values, the one of the emitter, i.e.,

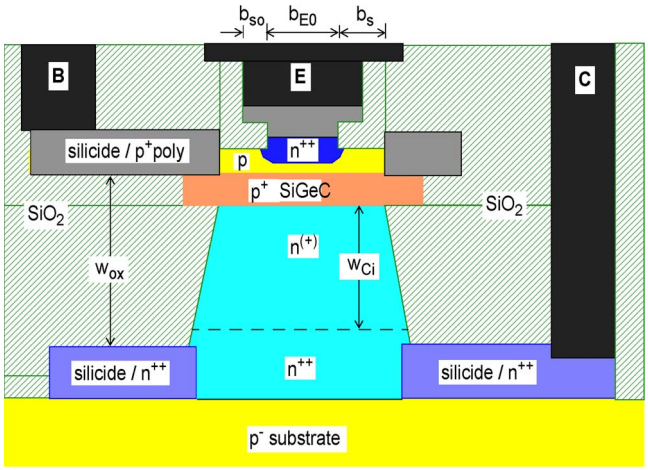

Fig. 3. Assumed schematic cross section of ultimately scaled bulk SiGeC HBT structure with important dimensions.

ρ_{KE}, has the largest impact on HF characteristics. In Fig. 4(a), ρ_{KE} was varied between the best existing value of 2 $\Omega\mu\mathrm{m}^2$ [2] and the theoretically best possible value of 0 $\Omega\mu\mathrm{m}^2$. The latter just serves as a reference indicating how much (or little) performance will be gained beyond more realistic values of $0.2 \ldots 0.5$ $\Omega\mu\mathrm{m}^2$ that may be achievable in future process technologies. Although the importance of contact resistances increases in downscaled technologies, the base contact resistance remains fairly small compared with the BE spacer and poly-to-monosilicon link resistance. However, for the external collector resistance, the contact (and possible sinker) resistance becomes dominant beyond $s = 50\%$.

For a given vertical structure, the biggest parasitic capacitance originates at the BE spacer. Although generally, this capacitance $C_{\mathrm{BE,par}} = (C_{\mathrm{sv}} + C_{\mathrm{sl}} + C_{\mathrm{so}} + C_{\mathrm{BE},m})$ increases with decreasing dimensions, innovative spacer concepts should not be excluded, which allow the thickness w_{so} (cf. Fig. 2) to be larger than in existing technologies. This would allow at least a partial compensation of the increase of the other components within $C_{\mathrm{BE,par}}$. As the theoretical upper boundary, the value for "0% $C_{\mathrm{BE,par}}$" (i.e., $C_{\mathrm{BE,par}} = 0$) has been inserted in Fig. 4(b). The other extreme case, i.e., "200% $C_{\mathrm{BE,par}}$," assumes an even larger capacitance increase than calculated from just shrinking the dimensions of the assumed spacer structure. The spacer width optimization may require a compromise between the respective capacitance and the external base resistance, depending on which capacitance component dominates and on the lateral outdiffusion of the emitter and external base doping.

Starting from the initial design rules, all lateral dimensions were then decreased simultaneously from their 100% values with the scaling factor s, resulting in a crossover of the f_T and $f_{\max}$ curves at a certain value of s. A balanced device design is roughly defined by the region between the crossover and the point where $f_{\max}$ reaches $1.5 f_T$. The corresponding region boundaries of s vary with the various transistor time constants, which in turn depend on specific electrical parameters and dimensions. For $\rho_{\mathrm{KE}} = 0.2\ \Omega\mu\mathrm{m}^2$ and straight scaling of $C_{\mathrm{BE,par}}$ (i.e., 100% curve in Fig. 4), the crossover point at $s \approx 80\%$ yields $f_{\max} \approx f_T \approx 1.2$ THz. This corresponds to an emitter window width of 40 nm. The upper boundary

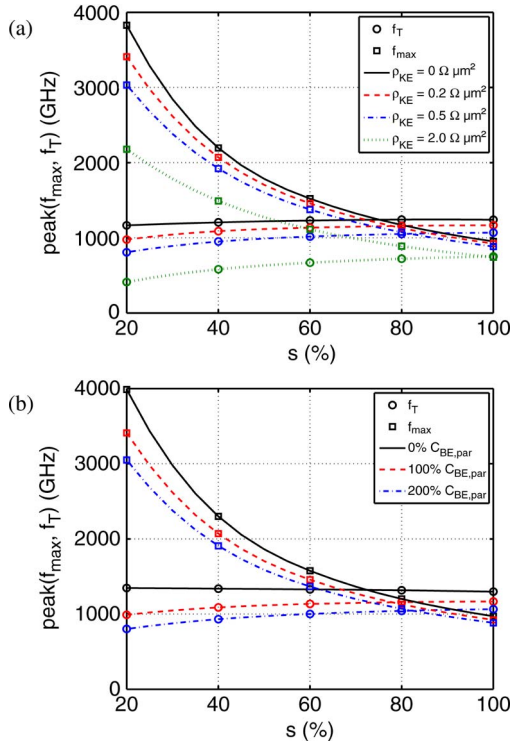

Fig. 4. Selected results of the lateral scaling analysis for the transit frequency and maximum oscillation frequency versus lateral scaling factor s of a long CBEBC bulk device ($l_{E0} = 10 b_{E0}$) at $V_{\mathrm{BC}} = 0$ V. Variation of (a) emitter contact resistance and (b) parasitic BE spacer capacitance (with $\rho_{\mathrm{KE}} = 0.2\ \Omega\mu\mathrm{m}^2$). At the crossover point of the curves with "$\rho_{\mathrm{KE}} = 0.2\ \Omega\mu\mathrm{m}^2$" and "100% $C_{\mathrm{BE,par}}$," $R_E \approx 5\ \Omega\mu$m and $C_{\mathrm{BE,par}} = 0.36$ fF/μm. Self-heating is included.

with $f_{\max} = 1.7$ THz and $f_T = 1.1$ THz is found at $s \approx 50\%$, which requires an emitter window width of 25 nm. With larger parasitic values, both the crossover point and the upper limit move to the right; i.e., less downscaling is required to reach a balanced design but at lower $f_{\max}$ and f_T values. The ultimate limit of SiGeC HBTS, which may still be acceptable for HF analog circuit design, appears to be around $f_{\max} = 2$ THz, with f_T dropping to 1 THz or possibly even below. These values are reached for $s \approx 40\%$ or an emitter window width of about 20 nm. The corresponding breakdown voltage $\mathrm{BV_{CEO}}$ is still expected to remain at its 1-D value since the peak electric field and transfer current density in the external transistor do not exceed those of the internal transistor. Further scaling, e.g., up to $s = 20\%$, may cause the BE perimeter depletion capacitance to increase stronger than what is assumed due to the highly uncertain lateral outdiffusion of the extrinsic base. However, at $s = 40\%$, the spacer width is 18 nm and appears to be still large enough for neglecting this effect.

For further discussion, three cases are defined by $s = (60, 50, 40)\%$. The corresponding FoMs and most important associated electrical parameters for the CBEBC and CEB structure are listed in Table I. The zero-bias internal base resistance R_{Bi0}; the total zero-bias BE, BC, and CS depletion capacitances C_{jE0}, C_{jC0}, and C_{jS0}, respectively; and the external series resistances R_{Bx}, R_E, and R_{Cx} were all calculated from analytical scaling equations in TRADICA. The thermal resistance was calculated directly from 3-D thermal simulations of the respective structure. The results of the 3-D

TABLE I
FOM AND IMPORTANT TRANSISTOR PARAMETERS OF COMPLETE 3-D BULK STRUCTURES (cf. FIG. 3) WITH THE ULTIMATE 1-D DOPING PROFILE FOR DIFFERENT LATERAL SCALING FACTORS s. THE UPPER VALUES WERE OBTAINED FOR A CBEBC CONTACT CONFIGURATION WITH $l_{E0} = 10b_{E0}$, WHEREAS THE LOWER VALUES ARE FOR A CEB LAYOUT WITH $l_{E0} = 3b_{E0}$. SELF-HEATING WAS INCLUDED IN THE BIAS-DEPENDENT RESULTS, WHEREAS THE PARAMETER VALUES ARE VALID FOR 300 K. R_E WAS CALCULATED FROM $\rho_{\mathrm{KE}} = 0.2\ \Omega\mu\mathrm{m}^2$ AND TAKING INTO ACCOUNT EMITTER WINDOW CORNER ROUNDING. FOR $C_{\mathrm{BE,par}}$, THE "100%" VALUE WAS USED. $V_{\mathrm{BC}} = 0$ V

scaling factor / electrical parameters	60%	50%	40%
b_{E0} (nm)	30	25	20
l_{E0} (nm)	300 90	250 75	200 60
R_{Bi0} (Ω)	25.8 64.2	25.2 63.8	24.5 63.5
R_{Bx} (Ω)	91.0 234	94.2 239	97.9 245
R_E (Ω)	22.4 76.5	32.5 112	51.1 180
R_{Cx} (Ω)	15.3 51	17.7 61	22 90
C_{jE0} (fF)	0.166 0.042	0.111 0.029	0.068 0.018
C_{jC0} (fF)	0.087 0.022	0.058 0.015	0.035 0.009
C_{jS0} (fF)	0.095 0.044	0.066 0.030	0.042 0.022
R_{TH} (K/mW)	16.7 44.1	21.2 56.2	28.8 76.6
f_{max} (THz) (@ J_C (mA/μm^2))	1.53 @ 100 1.41 @ 115	1.79 @ 111 1.65 @ 127	2.17 @ 123 1.98 @ 139
f_T (THz) (@ J_C (mA/μm^2))	1.19 @ 116 1.04 @ 141	1.17 @ 128 1.02 @ 155	1.13 @ 141 0.98 @ 168
τ_{CML} (ps) (@ J_C (mA/μm^2))	0.50 @ 248 0.56 @ 295	0.46 @ 284 0.55 @ 378	0.39 @ 280 0.50 @ 419

thermal calculations were verified with experimental data of various bulk and SOI device structures. In Fig. 4, the increasing $f_{\max}$ resulting from a lower base resistance and BC depletion capacitance comes at the cost of a decreasing f_T due to the increasing impact of parasitics and emitter perimeter minority charge storage. The CML delay time τ_{CML} has its minimum at $s = 50\%$ and slightly increases again for further scaling due to the relative increase in parasitic capacitances compared with the current carrying capability. It is also expected that the emitter width of 20 nm reached at 40% scaling will start to exhibit some level of quantum confinement. The resulting quantum pinch-in effect will further reduce the active emitter area, will increase the current density through the silicon portion of the emitter, and possibly will increase the emitter resistance somewhat.

III. THERMAL EFFECTS AND SOA

Real transistors exhibit significant self-heating, which may limit the operating conditions further beyond those imposed by electrical breakdown. In this section, the SOA in the ultimate limit is determined including thermal effects.

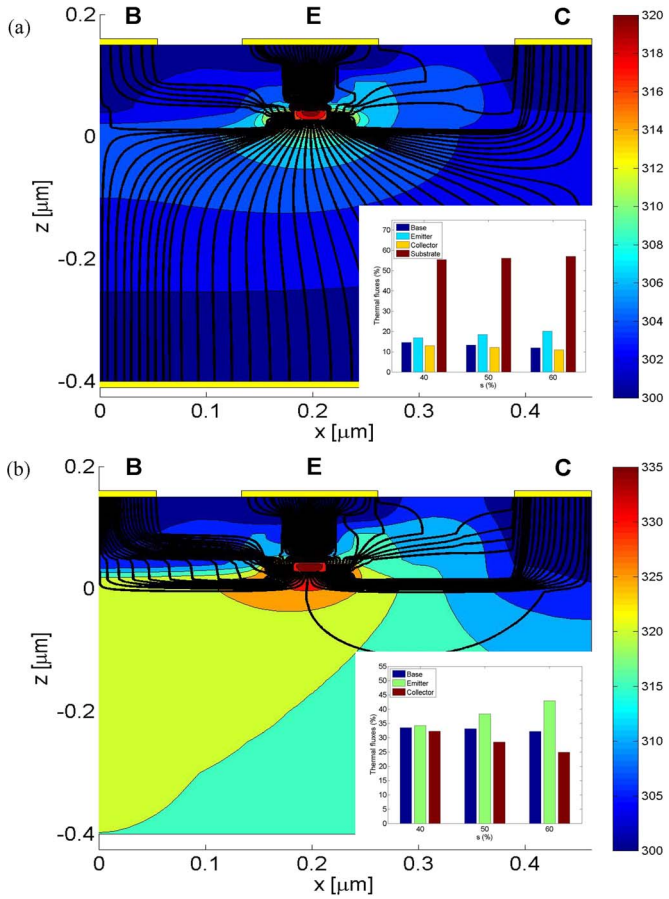

Fig. 5. Heat flux distribution and temperature contours in the 2-D cross section through the 3-D CEB structure with $s = 60\%$ used for thermal simulation: (a) bulk and (b) SOI. The inset shows the heat flux distribution between B, E, C, and S (bulk only) contact for different scaling factors. Power dissipation 0.4 mW, κ_{SiGe} from [14], $b_{E0} = 0.03$ μm, and $l_{E0} = 3b_{E0}$.

As the first step, 3-D thermal simulations have been performed for the CBEBC layout with a long emitter stripe, as well as for the CEB layout with short emitter length. From a thermal perspective, an SOI structure with 0.4 μm oxide underneath the buried layer corresponds to the worst-case scenario. For all materials, their finite thermal conductivity was included. Results for the heat flux and temperature contours are shown in Fig. 5 for the example of a scaled structure with $s = 60\%$. In the bulk structure [see Fig. 5(a)], both the wafer back side and the top contact metallization are assumed to be an ideal heat sink. The corresponding heat flow distribution (cf. inset) shows that the top contact contribution is relatively small. For the SOI structure [see Fig. 5(b)], only the surface contact heat sink is assumed since the heat flow through the substrate is negligible. According to these results and the quantitative evaluation in the figure inset, the heat flux is quite evenly distributed between the top contacts. With less aggressive scaling, the E contact starts acting as the main heat sink.

Fig. 6 exhibits electrical results obtained for a CEB layout with $s = 60\%$; in addition, $V_{\mathrm{BC}} = -1$ V has been chosen as the worst-case scenario for the temperature increase. Inserting the thermal resistance value obtained from 3-D simulation (cf. Table I) for the bulk structure yields, at peak f_T, a junction

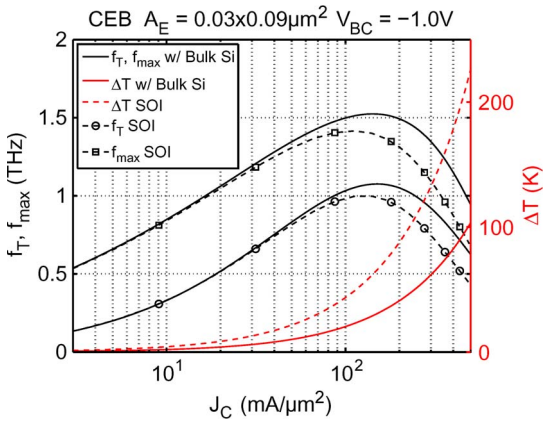

Fig. 6. Transit and maximum oscillation frequency versus collector current density under nonisothermal conditions for a bulk substrate and an SOI transistor. The right axis shows the temperature increase. The results are for a CEB contact configuration with $l_{E0} = 3b_{E0}$, $s = 60\%$, and $\rho_{\mathrm{KE}} = 0.2\ \Omega\mu\mathrm{m}^2$ and operated at $V_{\mathrm{BC}} = -1$ V.

TABLE II
FOMS (INCLUDING SELF-HEATING) AND IMPORTANT TRANSISTOR PARAMETERS (AT 300 K) OF THE COMPLETE 3-D CEB SOI STRUCTURE WITH THE ULTIMATE 1-D DOPING PROFILE FOR DIFFERENT LATERAL SCALING FACTORS s. THE SAME PROCESS-SPECIFIC PARAMETERS AS FOR TABLE I WERE USED. $V_{\mathrm{BC}} = 0\ V$

scaling factor / electrical parameters	60%	50%	40%
b_{E0} (nm)	30	25	20
l_{E0} (nm)	90	75	60
R_{Th} (K/mW)	84	105	142
f_{max} (THz) @ J_C (mA/µm²)	1.37 @ 106	1.60 @ 109	1.91 @ 119
peak f_T (THz) @ J_C (mA/µm²)	1.01 @ 131	0.99 @ 144	0.95 @ 155
τ_{CML} (ps) @ J_C (mA/µm²)	0.57 @ 280	0.52 @ 301	0.52 @ 419

temperature increase ΔT of about 28 °C (cf. right axis). This appears reasonable since, according to [9] for constant current scaling,[1] one expects in general only a marginal increase in device temperature compared with, e.g., a 350-GHz process with $\Delta T \approx 16$ °C at peak f_T. Compared with the isothermal case, self-heating causes the peak for both f_T and $f_{\max}$ as well as the corresponding current density to decrease by about 7%, mainly due to the mobility and carrier velocity reduction with temperature in the collector–base region. For an SOI structure, according to Fig. 6, the junction temperature roughly doubles to about 60 °C, whereas the peak values for f_T and $f_{\max}$ decrease further by about 10%. Note that peak $f_{\max}$ is reached at a lower current density compared with peak f_T, i.e., a trend that has already been observed in [2]. Information on relevant parameters and FoMs for the SOI structure is given in Table II.

It is well known that the operating limits of bipolar transistors are related to the drive conditions at the input port [10]. For instance, the widely cited FoM $\mathrm{BV_{CEO}}$ represents the maximum voltage under forced I_B conditions. However, this breakdown voltage does not fully describe the operating limits in practical cases since the base is usually not driven by a source with an infinite impedance. More relevant for practical applications are

[1]The emitter width b_{E0} is reduced proportional to the inverse of the current density at peak f_T.

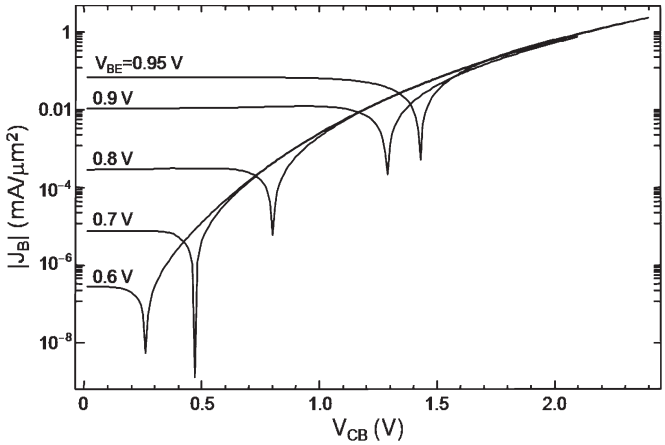

Fig. 7. Base-current density magnitude versus collector voltage of the CEB structure for different values of the base–emitter voltage. The dips correspond to the points of zero-base current. For higher values of V_{CB}, the base current becomes negative.

the operating limits under forced V_{BE} and forced I_E conditions. In the former case, the SOA is limited by a snapback behavior in the output $I_C(V_{\mathrm{CE}})$ characteristics [10]–[12], which is caused by the pinch-in effect that leads to collector current discontinuities in the common–base output characteristics [10]. The present analysis is performed for forced V_{BE} conditions since the related SOA is typically smaller than for the forced I_E case [10], [13]. Thus, in this analysis, the SOA is defined as the locus in the (V_{CE}, I_C) output plane that corresponds to the onset of the snapback under forced V_{BE} conditions given by $dI_C/dV_{\mathrm{CE}} \to \infty$ at constant V_{BE}.

In the following, instability phenomena resulting from the concurrent action of self-heating, impact ionization, and tunneling are investigated. As depicted in [1, Fig. 4], the tunneling current I_{BTB} flows from the collector to the base, thus providing a positive component to I_C and a negative component to I_B. Since I_{BTB} adds to the impact-ionization current I_{AVL}, the open-base breakdown voltage $\mathrm{BV_{CEO}}$ (corresponding to the condition $I_B = 0$) is reduced. Even if the effects of I_{BTB} and I_{AVL} are similar, the bias dependence is quite different. While I_{AVL} is proportional to the electron transport current I_T across the base and depends on the collector voltage V_{CB}, I_{BTB} depends solely on V_{CB}. This dependence can be approximated by the power law $I_{\mathrm{BTB}} \sim V_{\mathrm{CB}}^m$. As a result, the collector voltage $\mathrm{BV_{CEO}}$ corresponding to the open-base condition $I_B = 0$ is markedly dependent on the value of the base–emitter voltage. In fact, increasing V_{BE} yields an increase in the base-current component I_T/β so that a higher collector voltage is required to satisfy the condition $I_B = 0$. Therefore, $\mathrm{BV_{CEO}}$ increases with increasing V_{BE}. This behavior is depicted in Fig. 7, which shows the base-current density as a function of the collector voltage for different values of the base–emitter voltage V_{BE}. The bias points corresponding to condition $I_B = 0$ are clearly visible as dips.

The most critical instability effect limiting the SOA is the snapback behavior in the output characteristics. As discussed in previous work, this effect is due to the positive feedback induced by both impact ionization and self-heating (e.g., [10]–[12]). In fact, the impact-ionization current creates an ohmic voltage drop across the base resistance R_B, which tends to increase the base–emitter voltage in the internal region under

the emitter. This results in current crowding known as the pinch-in effect [10], [13]. As the collector voltage is increased, this positive feedback action leads to a snapback behavior in the output characteristics [10]–[12]. Since the tunneling current I_{BTB} adds to the impact-ionization current, it also contributes to instability mechanisms. Thus, it could be inferred that the snapback voltage would be reduced, resulting in a smaller SOA. However, this SOA reduction is less critical than expected because I_{BTB} is independent of the base–emitter voltage and, hence, is not subject to the positive feedback effect aforementioned. For investigating the limits of the SOA resulting from the above phenomena, the approach suggested in [11], which includes self-heating and the emitter and base related series resistances, has been extended here to include also the tunneling current. Model parameters were fitted by comparison with simulations. Assuming the impact-ionization current to be negligible with respect to I_{BTB} (cf. [1, Fig. 4]), the equation, which is shown at the bottom of the page, can be derived.

Here, V_{T0} is the thermal voltage at the reference temperature T_0 (e.g., 300 K), R_{TH} is the thermal resistance, m_C is the forward nonideality coefficient of the transfer current, Φ_{BE} (< 0) denotes the temperature coefficient of the base–emitter voltage at constant collector current, and β is the common–emitter small-signal current gain. R_E and R_B are the series resistances of the emitter–base calculated as function of dimensions according to [6]. The temperature dependence of I_{BTB} has been neglected.

The output characteristics obtained from the model are shown in Fig. 8. As can be seen, at a high collector voltage and low current densities, the SOA is limited by the tunneling current I_{BTB} (also shown as J_{BTB} in Fig. 8). At high currents, the SOA is limited by the occurrence of the snapback, which is caused by self-heating. The snapback current density J_{CF} calculated by (1), is shown in Fig. 8. For tracing the characteristics in Fig. 8, the dependence of the temperature coefficient Φ_{BE} on the collector current was taken into account, whereas a constant (average) value was assumed in (1). Note that, in Fig. 8, the instability induced by self-heating leads to a kink in the output characteristics rather than a snapback. This is due to the decrease in the magnitude of the temperature coefficient at high currents, which results in a reduction of the positive feedback induced by self-heating. The first term in (1) represents the snapback current due to self-heating alone [11]. This contribution is also shown in Fig. 8 (denoted as $J_{\mathrm{CF,SH}}$). As can be seen, the effect of I_{BTB} is to increase the snapback current density with respect to $J_{\mathrm{CF,SH}}$. The results shown in Fig. 8 indicate that the current density at which peak f_T is reached is well inside the estimated SOA. Also shown in Fig. 8 is the snapback locus calculated for an SOI device with a thermal resistance of 84 K/mW, which represents a worst-case scenario considering the assumed design rules and currently available information on the thermal conductivity of the SiGeC layer. For the latter, very different values can be found in the literature, which are all based on model calculations from the material composition. An experimental verification of the thermal conductivity of SiGeC layers is therefore desirable.[2] As can be seen, for such a scaled device, increasing the thermal resistance yields a significant reduction of the SOA, and in this case, self-heating also contributes to the onset of instability effects.

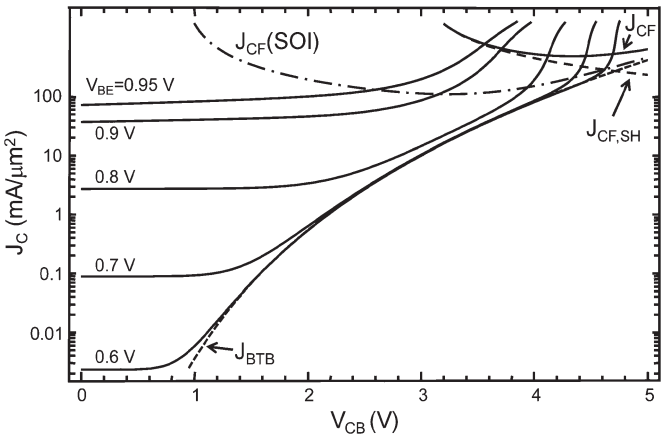

Fig. 8. Collector current density versus collector voltage of the CEB structure for different values of the base–emitter voltage. In addition, shown are the snapback current density J_{CF}, as calculated from (1); the snapback current density $J_{\mathrm{CF,SH}}$ due to self-heating alone; and the tunneling current density J_{BTB}. For comparison, the snapback current density of the corresponding SOI structure has been inserted as a dash-dotted line.

IV. Process Integration and Potential Issues

Since predictions of a process technology's ultimate limit have to be based on models, the results are typically met with a certain level of skepticism from process engineers. This skepticism is partially based on the lack of knowledge on how to obtain the assumed structures at the time of the prediction. Nevertheless, a reality check and risk analysis based on existing knowledge is certainly useful. Hence, a variety of issues concerning the realization of highly scaled SiGeC HBTs will be discussed below, starting with the 1-D profile and then moving to the 3-D structure. However, the reader should remember that the goal of this investigation was to determine the ultimate practically still useful SiGeC HBT structure and its electrical parameters. The currently unknown solutions for certain fabrication issues correspond to red marked areas in a SiGeC HBT roadmap that have been quite common in the International Technology Roadmap for Semiconductors tables for advanced CMOS nodes. Only proper research efforts will show in how far the ultimate limit can be realized.

[2]The thermal conductivity of the SiGeC layer does not have an impact on the junction temperature increase in the bulk structure. However, for the SOI structure, inserting instead of the value given in [14] a lower one that results from just a linear interpolation between the thermal conductivity of Si and Ge, leads to 36% change in junction temperature.

$$I_{\mathrm{CF}} \approx \frac{m_C V_{T0}}{|\Phi_{\mathrm{BE}}| R_{\mathrm{TH}} \left[V_{\mathrm{CB}} + V_{\mathrm{BE}} \left(1 + \frac{1}{\beta} \right) \right] - \left[\frac{r_B}{\beta} + r_E \left(1 + \frac{1}{\beta} \right) \right]} + I_{\mathrm{BTB}} \tag{1}$$

The narrow and highly doped base–collector (buried layer) profile in [1, Fig. 2] may possibly be fabricated using "millisecond annealing," as described in [15]. There (cf. Fig. 13), no indication of outdiffusion was observed for an as-grown B layer of 2 nm after a 1280 °C flash anneal even with a SiGe spacer of 3 nm at the collector side. In addition, a state-of-the-art spike anneal between 1000 °C and 1025 °C is not far from the target (cf. [15, Fig. 5]). In a different study [16], as-grown SiGeC base profiles with a concentration up to 3.5 10^{20} and a width down to 1.2 nm were demonstrated using selective epitaxy. Possible solutions for the collector may be an implanted buried layer and epitaxy at the beginning of the process flow of the bipolar module (after the primary steps of thermal treatment) or low-temperature epitaxy for both layers at a later stage.

Within a CMOS process flow with its present spike anneal for dopant activation, the integration may be more difficult. However, as the lateral scaling analysis shows (cf. Fig. 4), there is still some tradeoff possible between the vertical profile and the lateral dimensions depending on the electrical application and associated target FoMs. Another thought is that, for analog HF applications, 90-nm CMOS probably was the sweet spot for radio-frequency CMOS, whereas the electrical characteristics of MOSFETs with a gate length of 65 nm and below are becoming increasingly ill-suited[3] (e.g., in [17] and [18]). Therefore, other devices that enable HF front ends within a system-on-chip or system-in-package will eventually be required in any way. Since their fabrication volume will then be the same as for the digital CMOS chip, it may become of greater importance to adapt the CMOS process conditions for allowing better integration. This requires the consideration of the integration of HBTs during a sufficiently early phase of CMOS development. In addition, other (i.e., non-MOSFET) devices may be fabricated after or possibly on top of a finished digital CMOS wafer using the same fabrication facilities (e.g., in [19]). This would even allow for a stand-alone HBT process using a depreciated MOS production line (i.e., two to three generations back), which would still provide the necessary performance and cost advantage since lateral HBT scaling is much more relaxed than that of digital CMOS. Such HBT (BiCMOS or stand-alone) processes can always be used in system-in-package solutions, which may be in any way the future trend in communications and general milimeter-wave applications due to the difficulties of designing and flexibly realizing HF front ends for a multitude of desired frequency bands on a digital CMOS chip.

The probably most important problem regarding the limitations in a real (3-D) transistor structure is the high current density in the metal and the associated reliability issue caused by electromigration (EM). The current density at peaks f_T and $f_{\max}$ can exceed 100 mA/μm^2, which causes reliability concerns for the E and C metallization as well as possibly the poly- and monosilicon emitter contact region. Reducing both emitter width and length is typically attempted to maintain the same EM limits between process generations by keeping the ratio of the metal cross-sectional area A_M to the maximum emitter window area $A_{E0,\max}$ constant [9]. For the discussion below, a slot via and a first-metal (M1) layer, which are strongly recommended for ultra-HF applications, are assumed as well as W as contact material, with $J_{V,\max} = (16 \ldots 20)$ mA/μm^2, and Cu as M1 material.

Generally, the current through the slot via will flow both upwards to M1 and in parallel to the emitter window toward the end of the emitter finger. The exact distribution depends on the conductance of the via and the M1 layer. Surveying several technologies described in, e.g., [2], [20], and [21], reveals an emitter via width[4] $b_v \approx b_{E0,\min} + 2b_{\rm so} \approx (2 \ldots 4)b_{E0,\min}$ and height $h_v \approx (2 \ldots 6)b_{E0,\min}$ as well as an M1 layer width $b_{M1} \approx (2 \ldots 5)b_{E0,\min}$ and height $h_{M1} \approx (2 \ldots 4)b_{E0,\min}$. For the parallel current flow, this gives a cross section for the via of $A_v = (4 \ldots 8)b_{E0,\min}^2$ and for M1 of $A_{M1} = (4 \ldots 24)b_{E0,\min}^2$. Since the conductivity of W is about three times lower than that of Cu, only 30% at maximum (i.e., the most narrow M1 layer) of the current will flow through the via in parallel to the emitter window. Hence, one has to assume that most of the current first flows up to M1 and then parallel. As a consequence, the cross section of the via in series to the emitter window will be the limiting factor from an EM point of view. The current through the emitter window cannot exceed the maximum allowed current through the W via. This yields $J_{C,\max} = J_{v,\max} b_v / b_{E0,\min}$ for the maximum current density. Inserting the numbers given above gives $(32 \ldots 80)$ mA/μm^2, which is lower than the current density at peak f_T or $f_{\max}$. However, assuming that $J_{C,\max}$ is the operating point current at peak f_T or $f_{\max}$ corresponds to the worst-case scenario since a transistor in a circuit is usually not biased there but significantly below in order to account for process variations and large-signal swings without compression. In practical HF applications, the dynamic-current components are changing too rapidly to cause reliability issues. Nevertheless, the vias constitute a serious limitation that needs to be overcome in order to be able to reach the physical limit given by the semiconductor material.

One solution would be to widen the polysilicon and the via on the E window. For a CEB structure, this would come at the expense of a larger footprint and some increase in, mainly, the external base resistance, whereas for a double-base finger structure, the parasitic BC capacitance and the collector series resistance would also increase. Another option is to try to eliminate the via, i.e., deposit M1 directly on the polysilicon, which is challenging from a yield point of view. It is therefore necessary to search for via materials with better conductivity. By that time, the ultimate limit is reached, other materials with more favorable current carrying capability, such as carbon-nanotube (CNT) vias and even interconnect, may become manufacturable. CNTs would increase $J_{M,\max}$ by two to three orders of magnitude [22], [23]. A significant improvement in metal current density is most likely required in any way for future CMOS generations. However, if a maximum current density of 80 mA/μm^2 remains the limit, then the width of the lightly doped collector needs to be doubled, leading to a drop in peak f_T by about 25%.

[3]With each CMOS generation, the increasing output conductance significantly decreases the internal voltage gain (to about 6 at the 65-nm node and approaching 2 for 20 nm). As a consequence, the HF power gain and drive capability of these MOSFETs will become too small for most analog HF applications.

[4]For the definition of some of these dimensions, see Fig. 3. $b_{E0,\min}$ is the minimum allowed emitter width in a process generation.

The second concern in a real structure is self-heating and the associated temperature increase. Since a transistor in a circuit is usually not biased at peak $f_{\max}$ or f_T for the reasons mentioned before, the high-current region is typically only encountered for a very short period of time, which is by far too small to cause any significant self-heating. In an SOI CMOS process, the optimal thickness of the buried oxide (BOX) is still an open question since, for ultrahigh-speed operation, the often encountered oxide thicknesses in the range of 0.05 to 0.4 μm will be too thin to prevent significant HF substrate coupling. In addition, the silicon layer thickness in advanced FDSOI CMOS processes is too thin for accommodating the bipolar transistor integration so that the BOX has to be opened locally in any way unless a mesa-type structure is fabricated. As was observed in Fig. 6, removal of the BOX significantly reduces the self-heating impact and thus also relaxes the EM limit. An even better solution in terms of heat removal and electrical isolation would be silicon-on-diamond process technology [24].

Finally, the ultimate limit depends significantly on certain parasitics. Depending on the process architecture, the narrow 1-D base profile may cause a poor link to the external base region, which would result in a higher external base resistance than assumed here. A very important parasitic element is the emitter resistance, which is mostly determined by its semiconductor-to-metal contact portion. The predictions presented in this paper assume an improvement of the area-specific emitter (contact) resistance by about 4 to 10 over the best existing values of today. Improvements may possibly come from moving the metal contact very close to the highly doped bulk silicon or from other yet unknown changes in the material stack. Another important limitation will be the parasitic capacitances related to the contact stacks, which are getting very close to each other. Reducing the height of these stacks has to be balanced against the EM issues, at least for the E and C contacts.

Device simulation and lateral scaling investigations ignore the impact of material defects and inhomogenities, which will be expected to be of increasing importance in aggressively scaled technologies with extremely thin material layers. The reduction of imperfections is certainly another challenge that needs to be met by process engineers on the way to achieving the physical limits of any technology.

V. Conclusion

The overall purpose of this paper (Part I and Part II) is the prediction of the ultimate electrical HF performance potential for SiGeC HBTs under the constraints of practical applications. Compared with many other studies, this goal has been achieved by utilizing very advanced device simulation tools the parameters of which were calibrated to existing experimental results and, in case of DD and HD simulation, also to the results of the BTE. Furthermore, detailed 3-D electrostatic and thermal simulations were performed for the complete structure to determine the parasitic capacitances, temperature increase and thermal resistance of aggressively scaled devices. Finally, an accurate compact model was employed to incorporate the relevant physical effects and to determine important FoMs from circuit simulation. Since calibrated and sophisticated device simulation yields much more accurate and reliable results than simplified analytical estimates, only little use has been made of analytical scaling laws.

In case of the investigated SiGeC HBT technology, device operating frequencies beyond 1 THz with a well-balanced design appear to be possible while maintaining a still reasonable breakdown voltage and temperature increase. Depending on the available lithography for fabrication (or CMOS integration platform), $f_{\max}$ values up to 2 THz may be possible, albeit at a significant reduction of f_T. The exact scaling tradeoffs depend on the particular application and the advances that can be achieved in reducing parasitic effects such as the emitter contact resistance. Since lateral scaling requirements for HBTs are significantly relaxed compared with those for MOSFETs, vertical profile fabrication under the constraints of overall process integration appears to be the bigger challenge.

A very important issue that needs to be addressed for the ultimate device structure is EM in the contact vias. Another important aspect regarding the application of aggressively scaled devices are fabrication tolerances, which need to be addressed in future investigations. However, since the ultimate performance potential is still far above existing performance, there is considerable time left for solving the yet unknown issues. We estimate this time frame to be about 15 years.

Although this paper focuses on high-speed SiGeC HBTs, the limitations related to the vertical base–emitter region are also applicable to the class of high-voltage HBTs. However, their overall ultimate performance limit is determined by different constraints, such as the required breakdown voltage and, hence, collector thickness, which have not been considered here.

Obviously, as predictions are based on existing knowledge, there are always uncertainties on how to achieve them, and working process recipes can currently not be given. The corresponding questions can therefore only be answered by actually performing the necessary research work. The predicted performance potential provides information on, e.g., how a possible roadmap can be created with suitable steps that allow to reach the ultimate goal eventually, and enables estimates on how much return on investment may be expected from such a technology for future (sub)milimeter-wave applications. The investigations in this paper have focused entirely on finding the ultimate limits rather than analytical scaling laws. The latter can result from the next step, i.e., the creation of a realistic roadmap.

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