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FULL PAPER

Self-Aligned Megahertz Organic Transistors Solution-Processed on Plastic

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The processing of complex nanoscale electronic structures on plastic substrates is a significant challenge, requiring the combination of low temperature, nonaggressive, and high resolution methods. Here a scalable process flow on plastic is presented tbat enables the fabrication of flexible nanoimprinted organic field-effect transistors (OFETs) with self-aligned contacts and solution-processed semiconductor and dielectric layers, at processing temperatures ≤ 150 °C. OFETs are fabricated with device cutoff frequencies f > 1 MHz at low operating bias V_{DS} = −15 V. The technique allows the patterning of metal structures over four orders of magnitude from 375 nm to 1 mm without the need for a rigid carrier, and provides a fabrication pathway to high performance nanostructured organic circuitry.

1. Introduction

Plastic electronics encompasses devices fabricated either on plastic foils or with polymeric and solution-processed materials. These include organic field-effect transistors (OFETs),[1] sensing systems,[2–5] optoelectronics,[6–9] and more. They have the benefits of being flexible and compatible with technologies such as gravure and inkjet printing, but present a significant fabrication challenge. Techniques must feature low-temperatures and nonaggressive solvents, in order to allow processing on plastic and reduce costs. We focus here on OFETs as they form the building blocks of display backplanes, imaging and sensor arrays, and complex digital and analogue circuitry.[10,11]

While much of the reported literature on OFETs focuses on the static behavior and figures of merit such as field-effect mobility, very little explores the frequency response of devices. Only a handful of reports on OFET alternating current (AC) characterization use fabrication techniques that even partially fulfil the requirements set out above.[12–23] However to build functional flexible circuits it is important to understand how to reconcile device fabrication and performance.[24–26] This is a requirement if plastic electronics are to be implemented in applications such as radio frequency identification (RFID) tags which operate at megahertz frequencies.[27–29]

In our approach we reduce parasitic capacitances caused by overlapping electrodes, implement smaller device geometries, and gain a better understanding of the relationship between materials, processing, and architecture. We show that combining the strengths of multiple techniques allows the fabrication of high-performance OFET architectures on flexible foil, while maintaining the cited benefits of plastic electronics.

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2. Results and Discussion

2.1. Fabrication of Self-Aligned OFETs

Figure 1 illustrates the fabrication process: transistor channels are defined using ultraviolet nanoimprint lithography (UV-NIL) and bilayer liftoff processing; a thin dielectric layer is photopatterned; a second photolithographic bilayer liftoff process uses back exposure through the substrate to define the source and drain; and finally a semiconductor layer is solution-processed on top of the architecture. There is no requirement to prelaminate the flexible substrate onto a rigid carrier, a significant advantage over existing techniques.[30,31]

2.2. Bilayer Ultraviolet Nanoimprint Lithography

While the use of nanoimprint lithography in general is well reported as a nanostructuring technique,[32–35] and as a continuous process,[36] the combination with a bilayer resist stack

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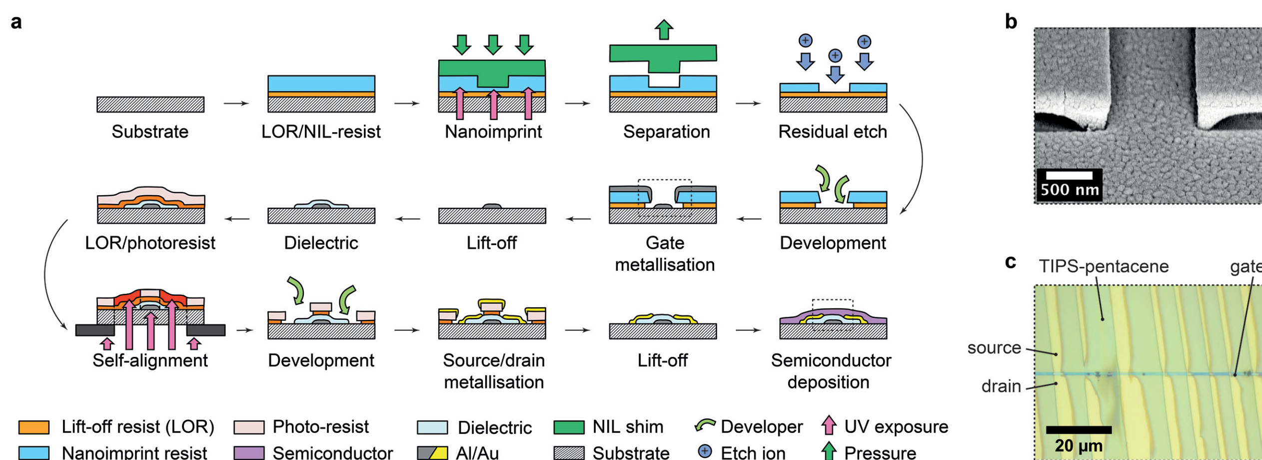

Figure 1. Bilayer UV-NIL self-aligned process flow. a) Illustration of OFET fabrication process (not to scale). b) SEM micrograph showing bilayer undercut of ≈750 nm UV-NIL patterned structure, metallised and pre-lift-off, image tilted at +52° to lens. c) Top-down optical micrograph showing zone-cast crystals of TIPS-pentacene on self-aligned architecture.

is uncommon, and as far as we are aware this approach has not been reported for OFET electrode formation on flexible foils. Our bilayer UV-NIL approach allows us to achieve homogeneous, nanoscale resolution of patterned features on plastic foils. The technique uses a sacrificial lift-off resist (LOR) layer under the UV-NIL resist (step "LOR/NIL resist" in Figure 1a). This offers a number of significant benefits over single layer processes,[15] allowing a well-controlled ≈500 nm undercut of the UV-NIL resist to facilitate lift-off (Figure 1b), as well as protecting the substrate from exposure to oxygen ion species during residual etch of the UV-NIL resist (Figure S1, Supporting Information). This allows the metallisation and lift-off of nano- to millimeter-long conductive features (lengths of 375 nm to >1 mm, of width 5 µm) with both Al and Au (Figure S2, Supporting Information). Structures show no increase in line edge roughness compared to the silicon imprint shim (Figure S3, Supporting Information); important for robust processing of circuit features such as bus lines. The short-channel lengths defined by this technique necessitate a thin gate dielectric to minimise deviation from ideal device behavior.[37] Here a t_D = 90 nm layer of highly cross-linked polymer dielectric is photopatterned on top of the gate structure (details described elsewhere).[38]

2.3. Bilayer Self-Aligned Lithography

Self-aligned lithography uses the OFET gate to define the source-drain electrodes.[15] As well as the benefit of minimised overlap, the technique relaxes the register tolerance for the corresponding patterning masks. Critical features are defined by self-alignment, whereas bus lines and interconnects are simultaneously defined by an intermediate photomask, avoiding additional exposures (see step "self-alignment" in Figure 1a). This approach can be integrated with semiconductor and dielectric deposition techniques such as printing, providing a solution to poor (>50 µm) gravure register tolerances.[39] Bilayer processing is implemented again to pattern source and drain electrodes with uniform, channel-length independent gate-electrode overlaps of $X_{OL} = 200 \pm 58$ nm. Overlaps are verified by focussed-ion beam scanning electron microscopy (FIB-SEM) and are symmetric for both source and drain (additional data in Figure S4, Supporting Information).

2.4. Semiconductor Deposition and DC Characterization

The organic semiconductor 6,13-bis(triisopropylsilylethynyl) pentacene (TIPS-pentacene) was solution-processed using spin-coating and zone-casting to form bottom-gate, bottom-contact OFETs with a range of channel length-to-width ratios ($25 < W/L < 320$). Zone-casting has recently been demonstrated as viable for large-area deposition of TIPS-pentacene with controlled crystal morphology.[40] A heated semiconductor solution is injected onto the moving OFET substrate; careful optimisation of both solution and substrate temperature, along with translation speed, allows the printing of uniaxially aligned TIPS-pentacene crystals parallel to the zone-casting direction. Charge transport in TIPS-pentacene is well correlated to its molecular packing motif, and increases with greater overlap of π–π bonds in adjacent molecules.[41–43] By aligning the casting direction parallel to the channel length (Figure 1c), we aim to maximise charge transport between source and drain.[44] **Figure 2** shows exemplary and summary characteristics for devices fabricated from both spin-coated (Figure 2a,b) and zone-cast TIPS-pentacene (Figure 2c,d). Although the spin-coated device in Figure 2a,b shows clear current saturation, a low off-current ($I_{DS}^{min} < 1$ pA) and a correspondingly high on/off ratio of ≈10^6 at low ($V_{DS} < 20$ V) operating bias, on average spin-coated devices are found to be limited by relatively low effective mobilities of $\mu_{sat} = 0.002$ cm^2 V^{-1} s^{-1} (summary normalised statistics in Figure 2e and supporting OFET data in Figures S5 and S6, Supporting Information). We attribute this variation to the disordered polycrystalline formation of TIPS-pentacene in the channel region during spin-coating.[45,46] Zone-cast devices were found to exhibit effective mobilities an order of magnitude greater than spin-coated devices of $\mu_{sat} = 0.03$ cm^2 V^{-1} s^{-1}.

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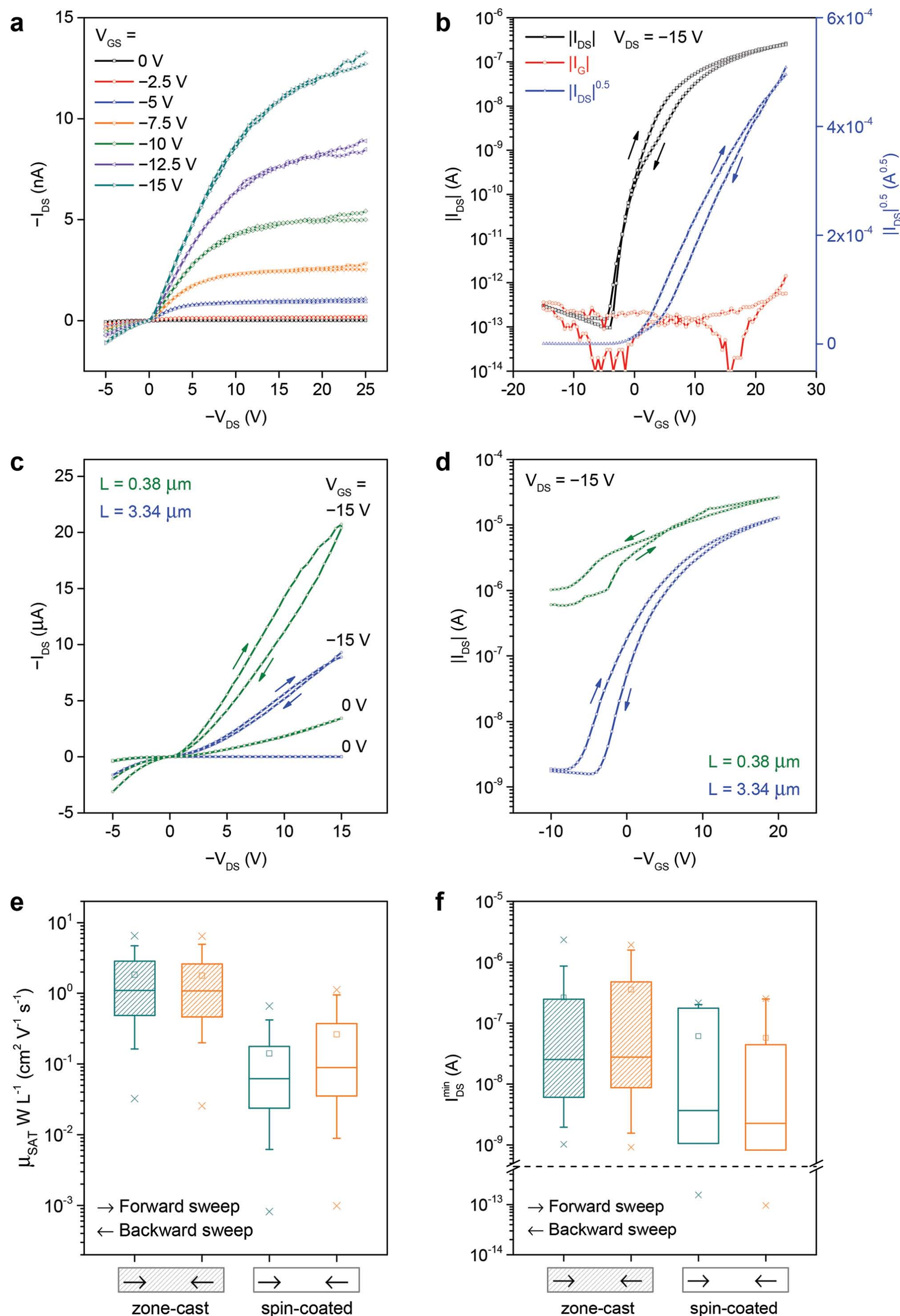

Figure 2. Quasi-static DC electrical characteristics of fabricated OFETs. a) Output and b) transfer characteristics of an $L = 3.53 \pm 0.06$ µm, $W = 128 \pm 1$ µm, OFET with spin-coated TIPS-pentacene, demonstrating current saturation and an on/off ratio of ≈10^6, where the plot of gate leakage $|I_G|$ follows the logarithmic current axis and demonstrates an exceptionally low leakage current <1 pA. c) Output and d) transfer characteristics of comparative OFETs with zone-cast TIPS-pentacene showing the influence of channel length on characteristics ($L = 3.53 \pm 0.06$ µm, $W = 128 \pm 1$ µm; and $L = 0.38 \pm 0.03$ µm, $W = 119 \pm 2$ µm). e) Box plots showing the statistics of the channel-dimension normalised saturation mobility and f) off-current I_{DS}^{min} for zone-cast (20 devices) and spin-coated TIPS-pentacene devices (13 devices). Box represents the limits of the 25th and 75th percentiles; whiskers represent 10th and 90th percentiles; squares represent arithmetic mean; horizontal lines inside boxes indicate median; crosses represent maximum/minimum. In the transfer and output characteristics, arrows denote transistor forward (off-to-on state, →) and backward (on-to-off, ←) voltage sweeps, allowing a direct comparison of the influence on hysteresis.

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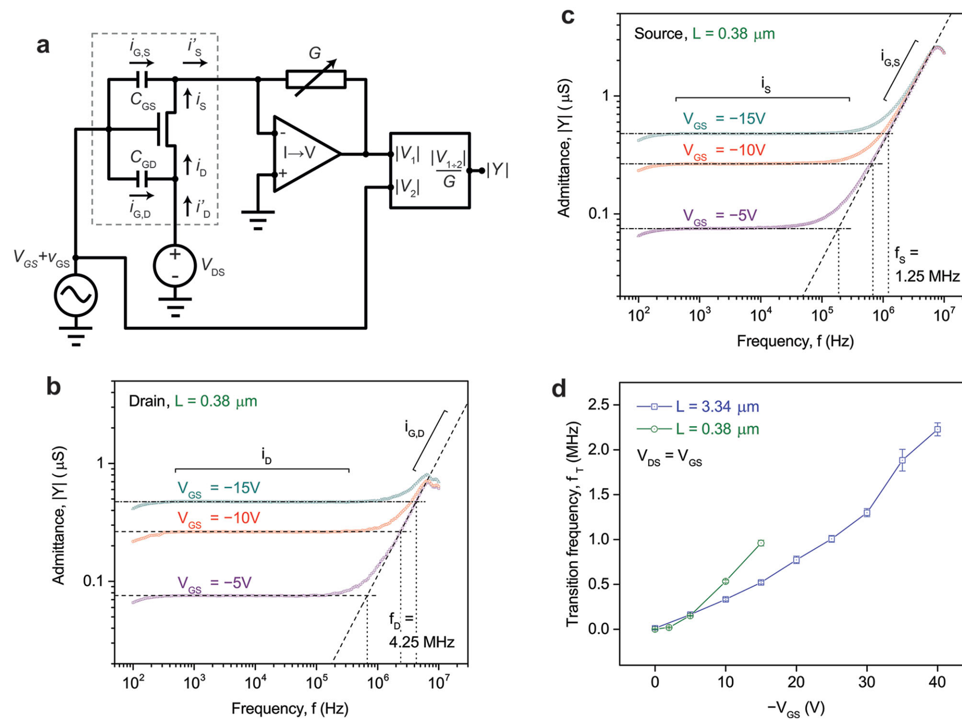

Figure 3. AC frequency measurements of zone-cast OFETs. a) Circuit schematic illustrating simplified measurement setup, the example here for source-gate admittance. The dashed box indicates the OFET under test, G represents the gain of the transimpedance amplifier, V_1 represents the response of the OFET, V_2 represents the stimulus, and $V_{1÷2}$ is the ratio of these two voltages; Y is the admittance. b) Measurement of drain-gate admittance, and c) source-gate admittance of short-channel zone-cast OFET as a function of stimulus frequency for different operating biases V_{GS}. The channel transconductance and overlap capacitance limited regimes are indicated by labelled braces, and the corresponding linear fits shown with dashed lines. Vertical dotted lines are guides to the eye indicating the approximate intercept with the frequency axis, indicating the values of f_D and f_S, respectively. d) Measured transition frequency f_T for long-channel and short-channel devices as a function of operating bias, where error bars represent the uncertainty in the fits of g_m, C_{GD}, and C_{GS}. Device geometry is as indicated in Figure 2.

2.5. AC Characterization of Self-Aligned Devices

Figure 3a illustrates the AC electrical characterization setup. We apply a DC gate bias superimposed with a small AC signal modulation to the device ($V_{GS} + v_{GS}$), while biasing it in the transdiode ($V_{DS} = V_{GS}$) regime. By monitoring the output at either the source or drain electrode we determine the magnitude of the admittance of the OFET, by taking the ratio of the magnitudes of the AC components of the drain current and gate voltage.

The AC component of the drain current i'_D of an OFET biased in the on-state can be approximated as the channel contribution i_D minus the parasitic displacement current $i_{G,D}$, as described in Equations (1) and (2), and illustrated in Figure 3a[47]

$$i'_D = i_D - i_{G,D} \tag{1}$$

$$i'_D = g_m v_{GS} - j2\pi f C_{GD} v_{GS} \tag{2}$$

$$g_m = \left.\frac{\partial I^*_D}{\partial V^*_{GS}}\right|_{v_{GS}=V_{GS}} \tag{3}$$

Where f is the gate modulation frequency, C_{GD} is the total gate-to-drain capacitance, v_{GS} is the modulated gate-source signal, C_i is the dielectric specific capacitance (C_i = 29 nF cm^{-2} in the devices presented here). Equation (3) defines the channel transconductance g_m in the limit of small v_{GS}, where $I^*_D \approx I_D + i_D$, $V^*_{GS} = V_{GS} + v_{GS}$, and V_{GS} is the DC gate bias. Note Equations (1) and (2) represent the complex current flow, ultimately we measure a voltage proportional to the magnitude of i'_D. Equation (2) describes two operating regimes: at low frequencies the drain current is dominated by the channel transconductance g_m; however, at high frequencies coupling through the overlap capacitance contributes an additional current flow, which increases proportionally with frequency. For large enough frequencies this capacitive current flow dominates, and the device output no longer switches properly in response to a change in the gate voltage.

We can define a cutoff frequency f_D by applying the condition $|i_D| = |i_{G,D}|$. This corresponds to the frequency where both the channel contribution and drain-gate capacitive current contribute equally to the frequency response, and beyond which device switching is inhibited. Considering the magnitude of Equation (2) in this limit yields the inverse relationship between frequency and drain-gate capacitance shown in Equation (4). A similar treatment is applied to the source-gate capacitance yielding the source cutoff frequency f_S shown in Equation (5)

$$f_D = \frac{g_m}{2\pi C_{GD}} \tag{4}$$

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$$f_S = \frac{g_m}{2\pi C_{GS}} \quad (5)$$

Figure 3b,c shows admittance measurements for both the drain and source electrodes of a zone-cast short-channel OFET biased in the transdiode regime (example corresponds to DC data in Figure 2c,d). The magnitude of the admittance is shown as a function of stimulus frequency, illustrating the flat channel dominated and sloping capacitance limited regimes. Features at f < 500 Hz and f > 7 MHz are artefacts of the maximum bandwidth of the characterization setup. The total overlap capacitances fitted from these plots are C_{GS} = 0.07 ± 0.02 pF and C_{GD} = 0.02 ± 0.003 pF, respectively, corresponding to very low channel-width normalised capacitances in the range C'_{OL} = 0.2–0.6 fF μm^{-1}. This highlights the significant advantage of the self-alignment process (further capacitance data in Figure S7, Supporting Information).

As a result of these low capacitances, very high maximum drain cutoff frequencies f_D = 4.25 ± 0.04 MHz and source cutoff frequencies f_S = 1.25 ± 0.01 MHz were measured at low operating bias (V_{GS} = –15 V) in the short-channel device. In the equivalent long-channel device, L = 3.34 ± 0.01 μm, values of f_D = 2.29 ± 0.02 MHz and f_S = 0.68 ± 0.004 MHz were measured under the same operating bias. Remarkably large peak cutoff frequencies f_S = 2.88 ± 0.02 MHz and f_D = 9.80 ± 0.10 MHz were measured at higher operating biases (data is summarised in **Table 1**; see Figure S8, Supporting Information, for corresponding long-channel admittance plots).

2.6. Source-Gate and Drain-Gate Capacitance

We observe the source-gate capacitance C_{GS} is consistently larger than the drain-gate capacitance C_{GD}, and as a result f_S is lower than f_D. Given the arbitrary assignment of source-drain to the architecture it is important to verify the origin of this behavior. Control experiments were performed by switching the electrodes (Figure S9, Supporting Information). The systematic shift was observed to follow the change in electrode assignment indicating it is not the result of asymmetry in the architecture, as verified by FIB-SEM. We therefore conclude the difference in capacitance is the result of the different relative bias at the two electrodes.

Table 1. Measured source-gate f_S and drain-gate f_D cutoff frequencies as a function of operating bias for short- and long-channel zone-cast TIPS-pentacene OFETs.

L [μm]	μ_{sat} [cm^2 V^{-1} s^{-1}]	$-V_{GS}$ [V]	f_S [MHz]	f_D [MHz]	f_T [MHz]
0.38 ± 0.03	0.03 ± 0.02	2	0.03	0.08	0.02
		5	0.19	0.68	0.15
		10	0.69	2.37	0.53
		15	1.25	4.25	0.96
3.34 ± 0.01	0.06 ± 0.05	5	0.22	0.69	0.16
		10	0.44	1.43	0.33
		15	0.68	2.29	0.52
		...	...	...	...
		40	2.88	9.80	2.23

For devices measured in the transdiode regime there is a large accumulation of charge carriers at the source, while a depletion region exists about the drain.[1,24] This accumulated charge contributes to the device channel capacitance at the source, but not at the drain.[47] Assuming that overlapping electrodes act as parallel plate capacitors, the overlap capacitance without channel contribution can be estimated using the Meyer capacitance model.[48,49] For the dielectric used, the expected drain-gate and source-gate overlap capacitance C_{OL} is equal to $WX_{OL}C_i \approx$ 0.01 pF, which is in good agreement with the measured average value of the drain-gate capacitance of C_{GD} = 0.02 pF. For a device biased in the transdiode regime (as measured here) the source-gate capacitance must also consider the contribution of the channel capacitance C_{CH} due to the accumulated charge adjacent to this electrode,[47] approximately $C_{CH} \approx 2/3WLC_i$ = 0.05 pF. The calculated source-gate capacitance $C_{GS} = C_{CH} + C_{OL}$ = 0.07 pF is therefore also in good agreement with the measured value of C_{GS} = 0.07 pF.

2.7. Maximum Device Switching Speed

It is important to consider the impact of both C_{GS} and C_{GD} on the switching performance of OFETs when applied to a circuit context. The transition frequency f_T, as described by Equation (6), is a more conservative figure of merit than either the source or drain frequency cutoffs, as it accounts for the capacitance of both electrodes. It gives the effective maximum switching speed of a transistor in a circuit, as limited by stray capacitance[24]

$$f_T = \frac{g_m}{2\pi(C_{GD} + C_{GS})} \quad (6)$$

It should be noted that f_T is dependent on g_m and hence the operating bias of the transistor (as demonstrated above for f_S and f_D). Figure 3d shows f_T as a function of V_{GS} (operating in the transdiode regime) for the short- and long-channel devices presented above. Even with this more conservative estimate, maximum transition frequencies of f_T = 0.96 ± 0.03 MHz and f_T = 0.52 ± 0.02 MHz at V_{DS} = –15 V are observed for short- and long-channel devices, respectively. Similarly a corresponding peak switching frequency of f_T = 2.23 ± 0.07 MHz is observed at V_{GS} = –40 V (Table 1). In the context of the reported literature these represent state-of-the-art values for solution-processed organic devices fabricated on plastic foil.[12–21] This is achieved without the need for a rigid substrate, using solution-processed dielectric and semiconductor, and is regardless of the relatively low effective mobility of these devices (μ_{sat} = 0.03–0.06 cm^2 V^{-1} s^{-1}), highlighting the impact and importance of self-aligned, low stray capacitance architecture on device performance.

2.8. Mobility in Short Channel Devices

We consider further the behavior of f_T as a function of device parameters. In the ideal case with no overlap capacitance, f_T

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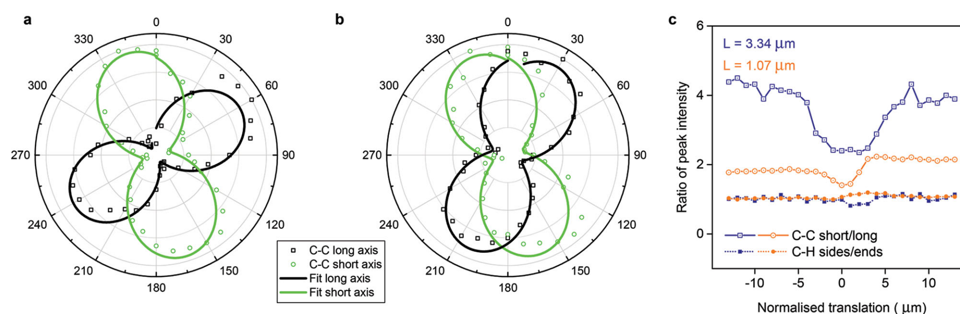

Figure 4. Anisotropy of TIPS-pentacene vibrational modes for different areas of OFET architecture. Polarized Raman spectroscopy of C–C long axis and C–C short axis vibrational mode ratios for a) TIPS-pentacene on top of drain electrode and b) TIPS-pentacene on top of channel for a $L = 1.07 \pm 0.01$ μm channel length device with fits, where 0° represents the casting direction. The greater the orthogonality of these modes, the more preferable the packing motif to charge transport. c) Shift in the ratio of C–C short and long-axis and C–H side and end modes of the TIPS-pentacene molecules as a function of substrate translation from source to drain, indicating the presence of a grain boundaries and a unfavourable change in packing behavior in the channel. The resolution of this measurement is limited by the Raman laser spot diameter (≈1 μm), hence a broadening of the apparent channel length.

scales with L^{-2}, and linearly with mobility.[18,47] Hence the reduction in channel length by approximately one order of magnitude might be expected to yield a factor of 100 increase in f_T, however we only observe a factor of ≈2 in our devices. This is due to the nonzero overlap capacitance of these devices (and hence a deviation from the ideal relation) and the relative scaling of the channel transconductances. The short channel device has a greater channel-width normalised transconductance ($g_m W^{-1} = 4.0$ mS m^{-1} compared to $g_m W^{-1} = 2.7$ mS m^{-1} for the long channel, both at 15 V bias) however this increase is lower than expected for the equivalent decrease in channel length. We attribute the difference to a decrease in the effective mobility of the short channel device, as a direct result of increased contact-resistance (as discussed below), as is common at shorter channel lengths.[18,20,37,50] This is despite the treatment of the gold source and drain with pentafluorobenzene thiol which forms a work-function lowering self-assembled monolayer on the electrodes.

In addition, we note that zone-cast devices exhibit effective mobilities of $\mu_{sat} = 0.03$ cm^2 V^{-1} s^{-1}, an order of magnitude below the value of $\mu_{sat} = 0.2$–0.5 cm^2 V^{-1} s^{-1} previously reported for the same zone-casting process carried out with TIPS-pentacene OFETs on interdigitated non-self-aligned Si/SiO_2 wafers.[44] In order to explore possible reasons for this reduced mobility, we examined the local molecular structure of the TIPS-pentacene molecules using angle dependent polarized Raman spectroscopy.[51,52] This technique allows the relative intensities of the C–C long and short-axis bond vibrational modes of the pentacene molecular core to be measured (Figure S10, Supporting Information, includes further details of this technique).[44] **Figure 4** shows the relative anisotropy of these modes for semiconductor on top of the drain electrode (Figure 4a) and on top of the dielectric within the channel (Figure 4b). We observed a systematic shift in the orientations of the long- and short-axis vibrational modes on top of the drain and channel regions, which was confirmed using translational scans across the device. Since these vibrational modes are orthogonal within the plane of the pentacene core, we deduce an upright packing motif on the drain compared to out-of-plane packing in the channel region. Hence, unfavourable packing in the channel and a domain boundary at the electrode-dielectric interface impairs charge transport and injection.

This result demonstrates the impact of architecture morphology on semiconductor crystal formation. Growing TIPS-pentacene crystals in a confined channel of depth ≈55 nm and separation ≤ 3 μm between two thiol self-assembled monolayer (SAM) coated Au contacts appears to result in an unfavourable structure and orientation. This is a critical issue as bottom-gate bottom-contact architectures facilitate self-alignment, and protect the semiconductor layer from UV radiation and solvent based photoresist developers and removers. While recent results have demonstrated that zone-cast TIPS-pentacene can yield OFET mobilities of $\mu_{sat} = 8.1 \pm 1.2$ cm^2 V^{-1} s^{-1} and greater,[40] this technique is based upon non-self-aligned, rigid silicon substrates with shadow-masked top-contacts. While this is preferable to achieve better molecular packing, this yields architectures with maximised electrode overlap, severely limiting the maximum theoretical frequency performance.

Our results here suggest that crystal growth techniques such as this require significant optimisation or redesign to be compatible with high-frequency flexible, self-aligned architectures. However, if achievable, they would have a direct impact on the operating frequency, potentially allowing access to hundreds of MHz and beyond.

2.9. Diode-Like Bulk Current

At very short channel lengths the OFET device dimensions approach the equivalent of those in vertically stacked organic diodes. The effective field drop across the channel $V_{DS}/L \approx 0.1$–0.5 MV cm^{-1} approaches that of a typical organic light emitting diode (OLED). As a result a DC bulk current I_{bulk} may form between source and drain, effectively contributing to the OFET off-current. We expect such a current to be related to the thickness of the semiconductor layer t_{osc}. A systematic increase in device off-current I_{DS}^{min} is observed in devices fabricated by both zone-casting, when compared to spin-coating (Figure 2f). Control measurements of the current–voltage characteristics of the I_{DS}, I_{GD}, and I_{GS} pathways were made before and after semiconductor deposition (data shown in Figure S11, Supporting Information). In zone-cast devices conduction pathways exist between the gate-source and gate-drain electrodes, which are not present in the corresponding spin-coated devices. Given prior knowledge of the robustness of the dielectric to semiconductor deposition methods,[38] we attribute this behavior to bulk current flow in the thick semiconductor film in zone-cast

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devices, compared to the thin spin-coated films. Further analysis of the normalised current voltage output characteristics indicates supra-linear behavior, indicating that high contact resistance at the injecting contact is also partly responsible for other nonidealities in the OFET characteristics (Figure S12, Supporting Information).

While further optimisation of the contacts will improve injection and reduce contact resistance effects, we note that it will also increase the bulk current flow. Hence reducing organic semiconductor film thickness is important in short channel devices to minimise off-current, which is particularly challenging in zone-casting and other solution deposition techniques where film thickness is strongly convoluted with crystal formation.

3. Conclusion

It is critical for the wider adoption of plastic electronics in circuits, that the fundamental challenges of fabricating high switching speed OFETs are addressed. We show here a complete fabrication platform on plastic foil, producing high-performance nanoscale OFETs, and the importance of considering electrical AC, DC, and structural domains. We note that while high mobility materials are valuable – they are only one of a number of factors to be considered when fabricating megahertz AC devices. Equal emphasis should be placed on reconciling these materials with the required architectures and fabrication techniques. Patterning self-aligned nanoscale features robustly on flexible plastic foil is a significant development in the move toward high performance processing of plastic electronics.

4. Experimental Section

Formation of Gate Electrode: A plastic foil was sonicated in ethanol for 10 min to remove contaminants and prebaked for 5 min at 150 °C on a hotplate to dehydrate and thermally stabilize the film. A 150 nm layer of lift-off resist (LOR1A, MicroChem Corporation) was spin-coated and prebaked for 5 min at 150 °C on a hotplate (2000 rpm, 45 s, 10 000 rpm s^{-1}). A 600 nm layer of UV-NIL resist (XNIL26, micro resist technology GmbH) was spin-coated as a second layer (3000 rpm, 30 s, 10 000 rpm s^{-1}). Imprint details are described in Note S1, Supporting Information. A residual layer of NIL resist is removed by an oxygen reactive ion etch (Surface Technology Systems) for 30 s at 10 W at 40 mTorr chamber pressure. A ≈ 500 nm bilayer undercut was developed by immersing the substrate for 30 s in developer (ma-D531, micro resist technology GmbH), followed by two 60 s stop washes in deionized water. A thermally evaporated 50 nm layer of aluminium was deposited at a rate ≤ 0.2 nm s^{-1} to ensure homogenous film coverage and adhesion. Substrates were immersed in photoresist remover (mr-REM 500, micro resist technology, GmbH) at room temperature for ≈3 h until residual material was observed to lift-off. The substrate was sonicated for 60 s to complete lift-off.

Formation of Thin-Film Dielectric: Substrates were thermally stabilized for 5 min at 150 °C on a hotplate. A 100 nm layer of photopatternable dielectric (GSID 938109–1, BASF) was spin-coated (3000 rpm, 60 s, 12 000 rpm s^{-1}). The dielectric was soft-baked for 5 min at 150 °C on a hotplate, before being exposed in a mask aligner at 365 nm for 180 s with a constant power of 10 mW. The layer was developed for 40 s in butyl acetate, and then cross-linked in a UV chamber (ELC-500, Electro Lite Corporation) at 365 nm under nitrogen for 10 min, resulting in a t_D = 90 nm dielectric layer.

Formation of Self-Aligned Source-Drain Electrodes: A 100 nm layer of lift-off resist (LOR1A, MicroChem Corporation) was spin-coated onto the substrate (4000 rpm, 45 s, 10 000 rpm s^{-1}), and soft-baked for 5 min at 150 °C. A 500 nm layer of positive photoresist (Microposit S1805 G2, Rohm and Haas) was spin-coated and soft-baked for 60 s at 115 °C (4000 rpm, 40 s, 12 000 rpm s^{-1}). The substrate was back-exposed at 365 nm for 5 s at 10 mW. A ≈ 300 nm bilayer undercut was developed for 15 s (MF-26A, Rohm and Haas). A 5 nm chromium adhesion layer was deposited (chrome plated tungsten rod, ≥ 99.5% purity, Testbourne Ltd) at ≤ 0.1 nm s^{-1}, followed by 50 nm of gold at a rate ≤ 0.2 nm s^{-1}, both by thermal evaporation. Lift-off was the same as for the gate electrode. FIB-SEM micrographs to verify the process are described in Note S2, Supporting Information.

Semiconductor Deposition: For both spin-coated and zone-cast devices a self-assembled monolayer of pentafluorobenzene thiol (Sigma-Aldrich) was deposited to improve charge injection by immersing the substrates in a 10 mM solution in ethanol for 15 min. For spin-coated devices a thin < 10 nm channel surface modification layer,[38,53] poly(alpha-methylstyrene) (PαMS, M_W = 632 000 g mol^{-1}, Polymer Source Inc) was prepared at 5 mg mL^{-1} in toluene, spin-coated, and annealed for 1 min at 100 °C on a hotplate (4000 rpm, 30 s, 12 000 rpm s^{-1}). A solution of 6,13-bis(triisopropylsilylethynyl)pentacene (TIPS-pentacene, High Force Research Ltd) was prepared at 10 mg mL^{-1} in anisole and spin-coated, with no subsequent annealing (2000 rpm, 60 s, 12 000 rpm s^{-1}). For zone-casting a 7 mg mL^{-1} solution of TIPS-pentacene in toluene was heated to 70 °C and the substrate to 60 °C. The substrate was translated at 500 µm s^{-1} perpendicular to the solution flow. Further details are described elsewhere.[44]

AC Electrical Characterization: Impedance measurements were performed in a nitrogen glovebox (H_2O < 1.5 ppm, O_2 < 8.4 ppm, M-Braun) using a network analyzer (Agilent 5061B) and transimpedance amplifier (Femto DHPCA-100). A sinusoidal stimulus is coupled into the OFET gate and network analyser (the latter as a reference). The device is relatively biased in the transdiode regime and the electrode under test (source or drain) is connected to the transimpedance amplifier (gain $G = 10^4$ V A^{-1}). The overlap capacitances are extracted from the linear slope of the admittance in the region 2 MHz < f < 5 MHz at V_{GS} = –5 V to obtain valid fits within the measurement bandwidth. Similarly, the transconductance is extracted from the plot at f = 1 kHz. See Note S3, Supporting Information, for details of DC characterization.

Raman Spectroscopy: Zone-cast crystal morphology was investigated using a Raman spectrometer (Renishaw microscope, Shimadzu UV-2550 spectrophotometer), probing at λ = 785 nm. For polarization measurements a half-wave plate was inserted into the beam and peak intensities were recorded as a function of polarization angle. Further details are covered in Figure S10, Supporting Information, and elsewhere.[44]

Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

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