A new physics-based model for TANOS memories program/erase

A. Mauri, C. Monzio Compagnoni[§], S. Amoroso[§], A. Maconi[§], F. Cattaneo,
A. Benvenuti, A. S. Spinelli[§†], and A. L. Lacaita[§†]
Numonyx, R&D - Technology Development, via C. Olivetti 2, 20041 Agrate Brianza (MI), Italy
[§] Dipartimento di Elettronica e Informazione, Politecnico di Milano, Milano, Italy and IU.NET
[†] also with IFN-CNR, Milano, Italy

Abstract

We present a new physics-based model able to reproduce the program/erase transients in TANOS memories, accurately describing the charge trapping/detrapping dynamics in the nitride layer. Modeling results are extensively validated against a large number of experimental data taken on samples with different gate stack compositions, considering a quite extended range of program/erase voltages and times. The good agreement between experimental and simulated results makes the developed model a useful tool for the assessment of the performance achievable by the TANOS technology.

Introduction

Due to the ever increasing constraints challenging the scaling of the floating-gate NAND Flash technology, TANOS memories have been proposed as a promising mass-storage solution for the 32 nm node and beyond [1, 2, 3]. Replacing the polysilicon floating-gate with a nitride layer for charge storage allows in fact a significant improvement in cell immunity to stress-induced leakage current (SILC) and cell-to-cell parasitic interference, enhancing the scaling perspectives of the technology from the reliability standpoint. However, a clear assessment of the program/erase (P/E) performance achievable by TANOS devices is still missing, as existing models either do not thoroughly describe the charge transport and trapping/detrapping in the nitride layer or are not validated with a large set of data.
In this work we present a new physics-based model able to describe the P/E transients in TANOS memories. The model carefully takes into account the trapping/detrapping dynamics in the nitride layer, including the energy relaxation of the injected electrons to the bottom of the nitride conduction band and the possibility for electrons to cross the nitride layer and escape from it without being trapped. This allows to explain the reduced sensitivity of the threshold voltage (V_T) shift on the P/E gate voltage reported for nitride with respect to floating-gate cells [4].

Experimental samples and results

Fig. 1 shows a schematics of the devices investigated in this work: TANOS capacitors comprising TaN metal gate, Al_2O_3 top dielectric, Si_3N_4 trapping layer and SiO_2 bottom oxide were fabricated on p-type substrate, including n^+-ring regions to assure channel inversion during program. Different thicknesses

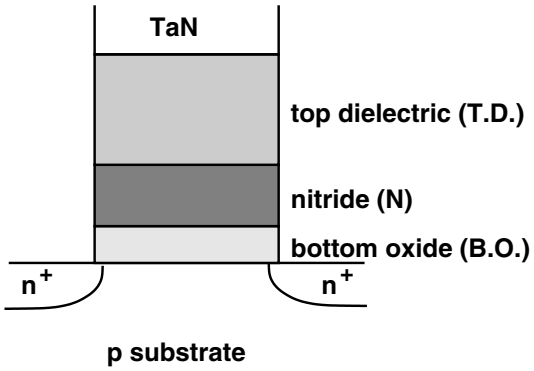

Figure 1: Schematic for the TANOS devices investigated in this work.

Sample	B.O.	N	T.D.
A	4.5 nm	6 nm	15 nm (Al_2O_3)
B	4.5 nm	6 nm	10 nm (Al_2O_3)
C	4.5 nm	4 nm	10 nm (Al_2O_3)
D	4.5 nm	6 nm	2 nm/15 nm (SiO_2/Al_2O_3)

Table 1: Gate stack composition for the investigated samples. B.O.=bottom oxide, N=nitride, T.D.=top dielectric.

of the gate stack layers were investigated, as reported in Table 1: a bottom oxide thickness of 4.5 nm was considered, to satisfy data retention and disturb requirements of non-volatile applications [5]. The nitride and Al_2O_3 thicknesses were varied in the range 4 to 6 nm and 10 to 15 nm, respectively. A dielectric stack including a 2 nm SiO_2 sealing layer between the nitride and the Al_2O_3 was also considered, in order to reduce the charge leakage from the nitride through the top dielectric during programming and data retention.
Fig. 2 shows the V_T transients achieved during Fowler-Nordheim programming on sample **A** at different gate voltages V_G ranging from 10 to 20 V (ring and bulk grounded). The curves clearly appear to be not vertically shifted by the difference in the adopted gate bias, as commonly observed on floating-gate cells: Fig. 3 shows that the threshold voltage shift (ΔV_T) at 10^{-3} s displays a 0.6 V/V dependence on V_G. This value is not unique and stricly depends on the nitride traps proprieties. Anyway TANOS memory reveals a reduced gate control over the programming transients with respect to the unit slope case valid for standard Flash cells.

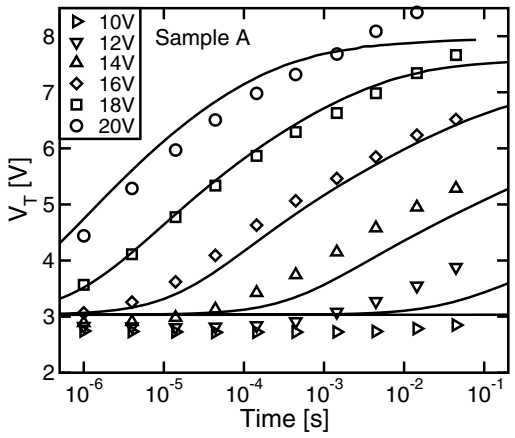

Figure 2: V_T programming transients for sample **A**. Symbols and lines are experimental and calculated results, respectively.

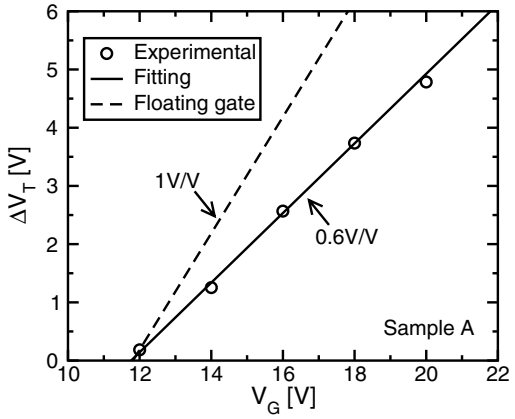

Figure 3: Gate dependence of ΔV_T for sample **A** extracted from Fig. 2 at 10^{-3} s.

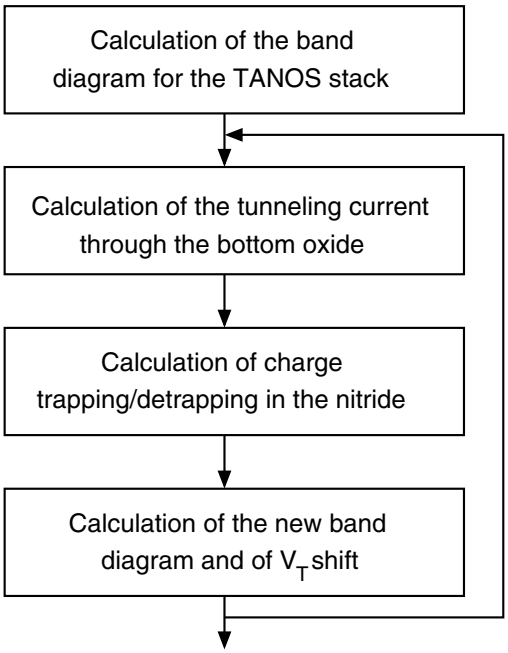

Figure 4: Flow-chart for the simulation procedure.

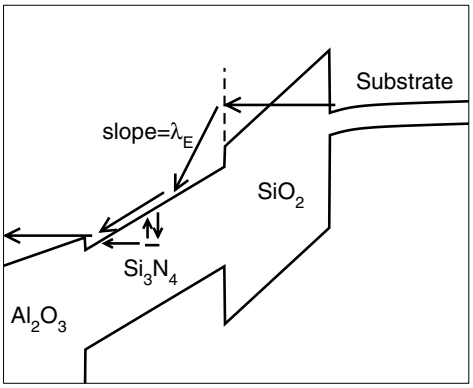

Figure 5: Energy band diagram for the TANOS structure, evidencing the electron fluxes involved in the program operation.

Physics-based model

In order to capture the programming transients of Fig. 2, we developed a new physics-based model able to describe the carrier trapping/detrapping dynamics inside the nitride layer. Fig. 4 shows the flow-chart of the simulation procedure: first, the initial potential profile along the 1D TANOS device is evaluated by solving the coupled Schroedinger-Poisson equations. Then, the V_T transient is obtained by iteratively solving the current continuity equation in the nitride, including trapping/detrapping processes, with the Poisson equation. The electron tunneling current through the bottom oxide is calculated using the WKB approximation and considering quasi-bound states in the substrate. As schematically depicted in Fig. 5, we considered a finite energy-relaxation length in the nitride for the injected electrons, ruled by the energy loss rate (eV per nm) parameter λ_E. This results in a thermalization length strictly dependent on the electrostatic potential profile in the nitride. In the tunnel oxide the electron relaxation can be neglected due the longer electron mean free path. Thermalized-electrons trapping in single-electron traps by means of a trapping cross-section σ_t and electron thermal and tunneling emission from the traps to the nitride conduction band are also accounted for. Trapping in the Al_2O_3 is neglected, considering this layer only as a tunneling barrier from the nitride to the gate and *vice versa* [6].

In order to deal with erasing transients, when a negative gate bias is applied three different charge flow processes are included: electron emission from previously charged nitride traps, hole and electron injection into the nitride from the substrate and the gate electrode, respectively.

Modeling results

Fig. 2 shows that our model correctly reproduces the programming V_T transients on sample **A**, including the reduced sensitivity to the programming bias. *This effect is due to the trapping mechanism and the finite number of traps available in the nitride for electron*. In fact, the limited number of available trapping centers gives the transients a saturating behavior to-

Parameter	Value
Nitride relative dielectric constant	6
Al_2O_3 relative dielectric constant	10.3
Nitride electron affinity	2.05 eV
Al_2O_3 electron affinity	1.25 eV
TaN work function	4.76 eV
Average traps energy depth	1.9 eV
Traps energy spread	0.12 eV
Traps cross-section	$8 \cdot 10^{-15}$ cm^2
Escape frequency from the traps	$2 \cdot 10^{10}$ Hz
Electron energy-loss rate	3.1 eV/nm

Table 2: Main parameters used for the simulations.

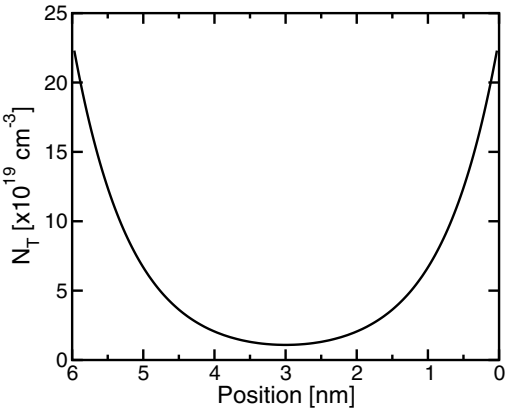

Figure 6: Spatial profile for the traps in the nitride layer.

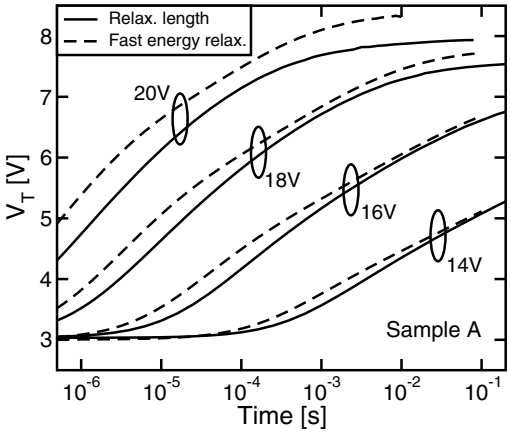

Figure 7: Programming ΔV_T for sample **A** assuming or neglecting the electron energy-relaxation length.

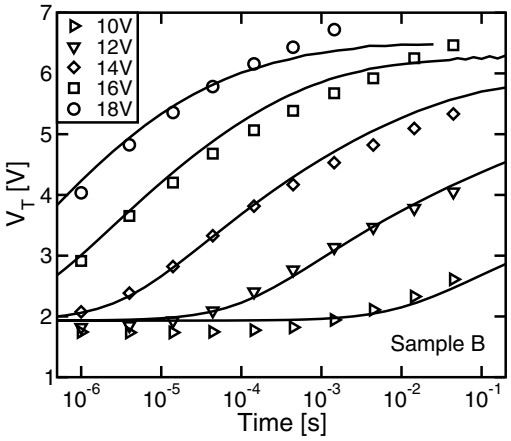

Figure 8: Same as in Fig. 2, but for sample **B**.

ward a maximum ΔV_T, which results from the balance of the input/output currents in the nitride layer. Therefore, for fixed programming time, the larger is the ΔV_T value and the lower is its growth rate, making the transients sensitivity to the gate bias lower than the expected 1 V/V. Moreover, the non-zero energy-relaxation length for electrons implies an initial trapping position which shifts deeper in the nitride as V_G is increased, slightly reducing the number of nitride traps that are actively involved in the trapping process. This further lowers the V_T curves as V_G increases, reducing the gate control over ΔV_T.

Table 2 reports the main parameter values used for the simulations: Al_2O_3 and Si_3N_4 parameters were chosen in accordance to the experimental results reported in [6]. A gaussian profile was assumed for the trap energy distribution, with average value $E_T = 1.9$ eV from the nitride conduction band edge and standard deviation $\sigma = 120$ meV. We assumed a larger trap density at the nitride edges, according to the hyperbolic cosine profile reported in Fig. 6. A trap cross-section of $8 \cdot 10^{-15}$ cm^2 was extracted, compatible with neutral traps [7].

Fig. 7 shows the impact of the non-zero energy-relaxation length on the V_T transients for sample **A**: a reduction of the achievable ΔV_T is clearly evident, which becomes larger as the programming voltage is increased. This reflects the lower nitride thickness contributing to charge trapping for large programming V_G, reducing the gate control over the ΔV_T shift.

Using the same set of parameters reported in Table 2, Fig. 8 shows that the model can quantitatively reproduce the V_T transients for sample **B**, having a thinner Al_2O_3 top dielectric layer. Moreover, modeling results are also in good agreement with experimental data when the nitride storage layer, and therefore the trapping process, is modified: Fig. 9 shows in fact that, keeping the same trap density at the nitride edges reported in Fig. 6, calculations well match the experimental results also on sample **C**. Finally, Fig. 10 shows that a good agreement between experimental and modeling results is obtained even in presence of the SiO_2 sealing layer on top of the nitride. All these results confirm the validity of the model on a quite extended range of programming biases and times, *making the model a reliable tool for the design of TANOS cells*.

Figs. 11 and 12 show experimental and calculated V_T erasing transients on samples **A** and **B** for negative gate biases in the -10 to -18 V range. Again, a very good agreement is found for all the investigated transients, confirming that the model correctly catches the basic physics involved in nitride charging/discharging. Finally, note that both the electron emission from the nitride traps and hole injection from the substrate contribute to the V_T reduction during the erase transient, while electron injection from the gate is negligible, as no saturation of the

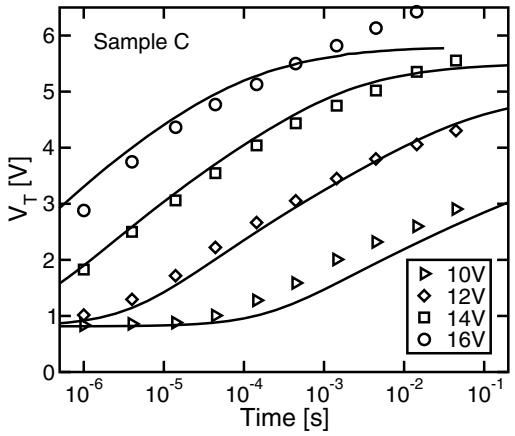

Figure 9: Same as in Fig. 2, but for sample **C**.

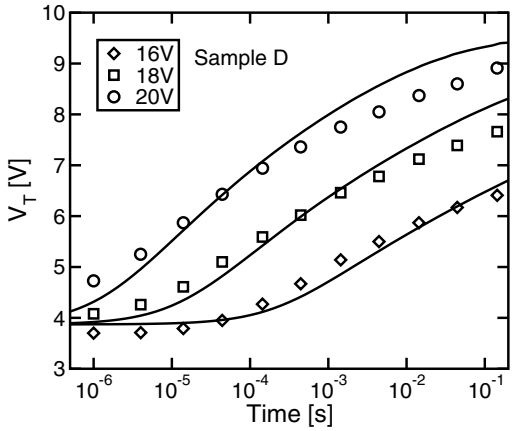

Figure 10: Same as in Fig. 2, but for sample **D**.

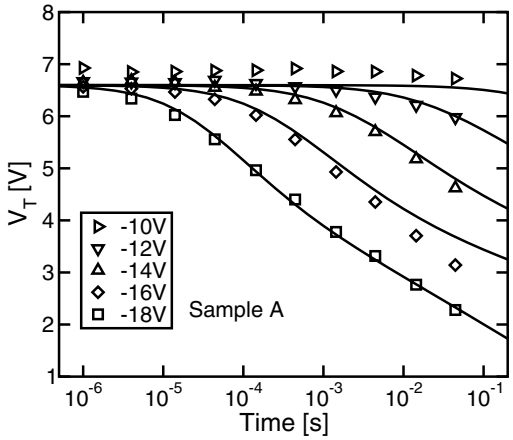

Figure 11: Erasing V_T transient for sample **A**. Symbols and lines are experimental and calculated results, respectively.

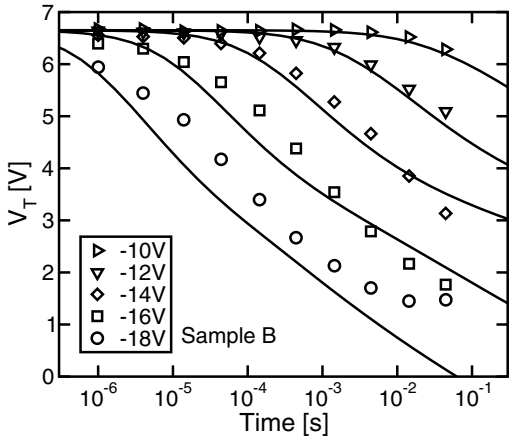

Figure 12: Same as in Fig. 11, but for sample **B**.

curves appears even for very long erasing times.

Conclusions

We presented a new physics-based model for the P/E transients in TANOS memories, extensively checking its validity on samples with different gate stack compositions and over extended ranges of P/E voltages and times. The model correctly reproduces the V_T transients in all cases and can be used to correctly assess the performance of the TANOS technology.

Acknowledgments

The authors would like to thank P. Cappelletti, E. Camerlenghi, R. Bez and L. Baldi from Numonyx for discussions and support. This work has been partially supported by the European Commission under the FP7 research contract 214431 "GOSSAMER" and by MIUR under the FIRB Project No. RBIP06YSJJ.

References

[1] C. H. Lee, *et al.*, "A novel SONOS structure of SiO_2/SiN/Al_2O_3 with TaN metal gate for multi-giga bit flash memories," in *IEDM Tech. Dig.*, pp. 613–616, 2003.

[2] Y. Park, *et al.*, "Highly manufacturable 32Gb Multi-Level NAND Flash memory with 0.0098 μm^2 cell size using TANOS (Si-Oxide-Al_2O_3-TaN) cell technology," in *IEDM Tech. Dig.*, pp. 29–32, 2006.

[3] J. S. Sim, *et al.*, "Self aligned trap-shallow trench isolation scheme for the reliability of TANOS (TaN/AlO/SiN/Oxide/Si) NAND Flash memory," in *Proc. Non-Volatile Semiconductor Memory Workshop*, pp. 110–111, 2007.

[4] A. Furnemont, *et al.*, "Physical understanding of SANOS disturbs and VARIOT engineered barrier as a solution," in *Proc. Non-Volatile Semiconductor Memory Workshop*, pp. 94–95, 2007.

[5] C.-H. Lee, *et al.*, "Charge trapping memory cell of TANOS (Si-Oxide-SiN-Al_2O_3-TaN) structure compatible to conventional NAND Flash memory," in *Proc. Non-Volatile Semiconductor Memory Workshop*, pp. 54–55, 2006.

[6] C. Scozzari, *et al.*, "Al_2O_3 optimization for charge trap memory application," in *Proc. ULIS*, pp. 191–194, 2008.

[7] D. Ielmini, *et al.*, "Modeling of SILC based on electron and hole tunneling – Part II: Steady-state," *IEEE Trans. Electron Devices*, vol. 47, pp. 1266–1272, June 2000.