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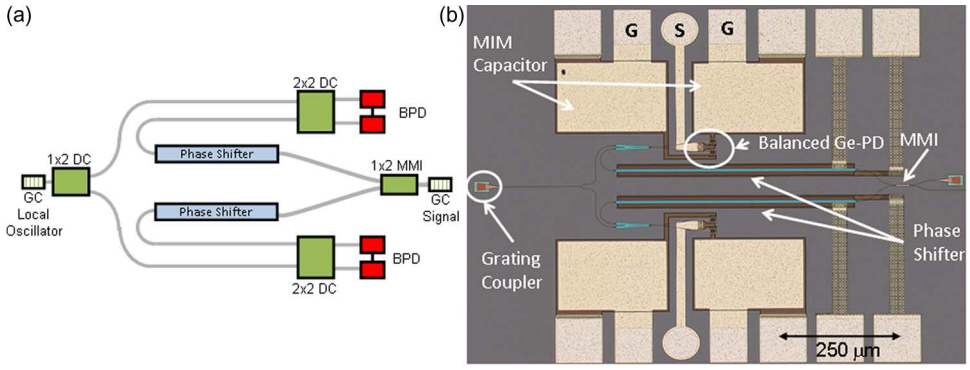

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A Compact Silicon Coherent Receiver Without Waveguide Crossing

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Abstract: A monolithically integrated silicon coherent receiver based on a novel scheme with a crossing-free 90° hybrid optical coupler and two balanced germanium photodetectors is reported. The integrated receiver is compact (footprint is 0.8×1.0 mm^2), and it is demonstrated by working with single-polarization 56-Gb/s quadrature phase-shift keying (QPSK) and 80-Gb/s 16-quadrature amplitude modulation (16-QAM) signals. In particular, QPSK transmission that is back-to-back at 28 Gbaud shows a bit-error rate (BER) below 10^{-4} for an optical signal-to-noise ratio (OSNR) lower than 17 dB, whereas 16-QAM at 20 Gbaud shows a BER not better than $3^{*}10^{-2}$ because of the nonideal behavior of the device. Reasons for the performance limitations are discussed.

Index Terms: Optical communications, silicon photonics, photonic integrated circuits (PICs), coherent receivers.

1. Introduction

Silicon photonics has become a viable technology platform for the development of high-speed and low-power consumption photonic integrated circuits (PICs). Differential quadrature phase shift keying (DQPSK) self-homodyne direct detection receivers have been recently demonstrated in Si photonics using Mach–Zehnder delay interferometers [1] and balanced photodetectors (BPD) based on germanium (Ge) [2] or hybrid Si/InGaAs [3]. However, coherent techniques can perform the more efficient signal detection of complex modulation formats with high spectral efficiency [4]. Optical coherent detection allows to access both phase and amplitude information, providing the best performance in terms of sensitivity. Moreover, owing to digital signal processing (DSP) [5], linear effects induced during the transmission can be completely compensated. Recently, a high performance hybrid integrated receiver for polarization multiplexed (PM)-QPSK signals was demonstrated operating up to 112 Gb/s [6]. The circuit exploited a silicon passive circuit for implementing the optical hybrid for coherent detection. More compact monolithically integrated Si receivers have been also demonstrated exploiting ad-hoc multi mode interference (MMI) combiners [7], [8]. A 10-channel integrated coherent receiver based on InP technology has been reported working up to 100 Gb/s per channel [9]. In all current schemes, either waveguide crossings or NxM MMIs must be used. In the first case, the receiver

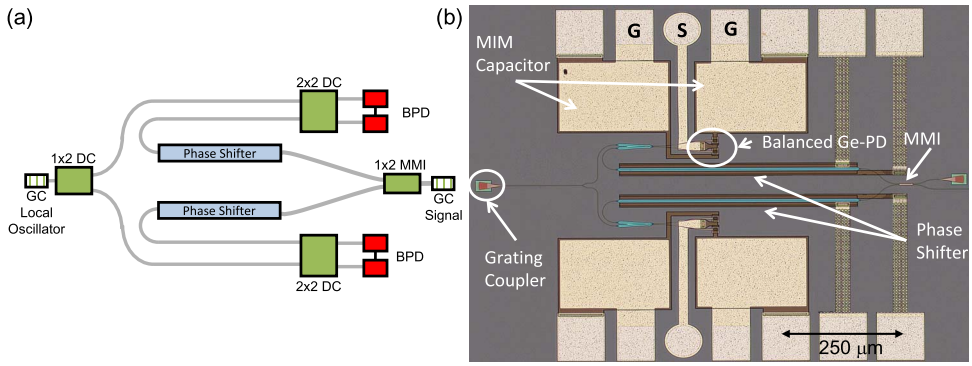

Fig. 1. Schematic diagram (a) and device photograph of the integrated silicon coherent receiver. (b) The footprint of the entire device is 0.8×1.0 mm^2. DC: directional coupler; GC: grating coupler; BPD: balanced photodetector.

could be prone to crosstalk interference [10], and in the second case, it could be prone to undesired back reflections from the MMIs, depending on fabrication accuracy.

In this paper, we report an integrated silicon coherent receiver with a novel design exploiting an alternative scheme of the optical hybrid which averts waveguide crossings [11], [12]. This mitigates, in principle, crosstalk and back-reflections. The device was manufactured at the Institute of Microelectronics (IME) through the OpSIS (Optoelectronic Systems Integration in Silicon) foundry service [13]. The PIC, described in detail in the following, in this first fabrication, works with single polarization signals only and is made by two grating couplers (GCs) for the input of the signal and local oscillator (LO), two thermally-tunable 500-μm long phase shifters, and two balanced Ge-photodiodes (PDs) with integrated decoupling capacitors. Preliminary results about the circuit were recently presented in a short conference paper [14]. We report the receiver experimental characterization through bit error rate (BER) measurements as a function of the optical signal-to-noise ratio (OSNR) together with examples of the recovered constellations after DSP. Device operation is proved with single polarization QPSK and 16-quadrature amplitude modulation (16-QAM) signals up to 56 Gb/s and 80 Gb/s, respectively. The experimental results show BER below 10^{-4} for the case of QPSK signal and a clearly visible received and demodulated constellation of the 16-QAM signals corresponding to a bit error rate of $3 * 10^{-2}$. Limitations to the performance of the device obtained in this first fabrication run are also discussed.

2. Coherent Receiver Architecture and Design

Fig. 1 shows the receiver architecture (a) and a picture (b) of the integrated coherent Si receiver.

Two single polarization grating couplers (GC) allow for coupling the received signal and the LO. The couplers have been designed to achieve a maximum coupled power at 1550 nm and show a 3-dB bandwidth of around 45 nm. Each grating coupler exhibits an insertion loss of 5.5 dB measured by GC test structures. A MMI 3-dB splitter separates the received signal in the in-phase (I) and quadrature (Q) arms of the receiver. The use of an MMI splitter instead of a directional splitter is only dictated by space constraints for the circuit on the chip.

The thermally-tunable 500-μm long phase shifters (PSs) integrated in the two arms enable precise control of the 90° differential phase shift between propagating signals so implementing in a simple controllable way the optical hybrid function. These PSs are realized with n-doped resistive Si heaters that exploit the thermo-optic effect. Fig. 2 reports the measured phase shift of the integrated PSs as a function of dissipated electrical power. Clearly, the in-phase and quadrature conditions must be optimized when changing the operation wavelength of the received signals and the device must be temperature controlled in order to avoid spurious phase drifts. On the LO input side of the receiver, a 3-dB directional coupler (DC) splits the LO power into the two arms. The LO and signal are combined with 3-dB directional couplers in each side of the

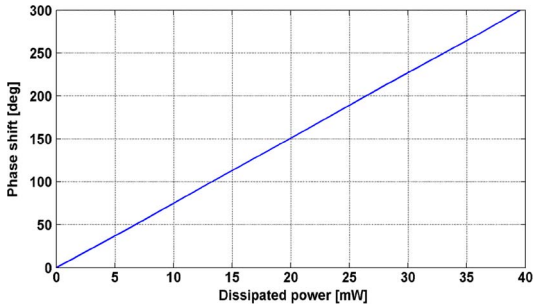

Fig. 2. A 500 μm long n-doped phase shifter response (phase shift vs. dissipated power).

TABLE 1

PIC insertion losses

	Insertion Losses
Grating Coupler	5.5 dB
Waveguide	3-4 dB/cm
Phase shifter	2 dB/mm
Path Insertion Loss: Local Oscillator	13 dB
Path Insertion Loss: Received Signal	14 dB

receiver (I and Q) and then converted to electrical signals with the integrated balanced photodetector made by two 11 μm-long Ge-PDs. The balanced detectors include 20-pF MIM capacitors for DC decoupling. Typical responsivity, dark current, and 3-dB bandwidth of single PD, per specifications of the OpSIS foundry [13], are 0.55 A/W, 5 μA (at 4 V reverse bias) and 20 GHz, respectively. High speed ground-signal-ground (GSG) probe pads are used to extract the data signals from the chip and additional pads are used for DC biasing and control of the phase shifters. The pads are arranged in a linear fashion near the edge of the circuit, so that a combined RF/DC multiprobe can be used to contact the chip. The device was fabricated on 220-nm silicon on insulator (SOI) wafers having a 2-μm thick buried oxide layer.

The single mode waveguide are 500-nm wide; the integrated receiver includes rib waveguides with a slab thickness of 90 nm for long straight sections and directional coupler, and single-mode strip waveguides which yield low bending loss for a minimum bending radius of 5 μm. Both strip and rib waveguides are utilized to limit optical losses and to reduce the footprint. Both waveguides propagate a single transverse electric (TE)-mode. Waveguide propagation loss is 3–4 dB/cm (OpSIS data) while propagation loss in the phase shifter is around 2 dB/mm (our estimation from measurement). Insertion loss values are summarized in Table 1, where also the estimated path insertion loss from the grating coupler to the PD is reported for the local oscillator and for the received signal (6 dB of losses are due to the two power splitters in the path).

Details of the mask of the balanced Ge-PDs are reported in Fig. 3 (on the left-hand side) where also the equivalent electrical circuit is schematized (on the right hand side). As it can be seen in the equivalent electrical circuit, and, as explained in detail in [15], the parasitic capacitance series $(C_{PD1} + C_{PD2})$ in balanced configuration reduces the photodiode bandwidth of around 3-dB in respect of the single PD case. The photodetector bandwidth reduction is confirmed by comparing the measured bandwidth of the balanced PD and of a single PD (which was in another part of the fabricated chip not shown in Fig. 1) reported on the right part of Fig. 3. The PD bandwidth was measured by means of a Network Analyzer for a reverse bias voltage of 3V for each photodiode. The measured 3-dB bandwidth reduces from around 16 GHz of the single PD case to around 10 GHz for the balanced detector.

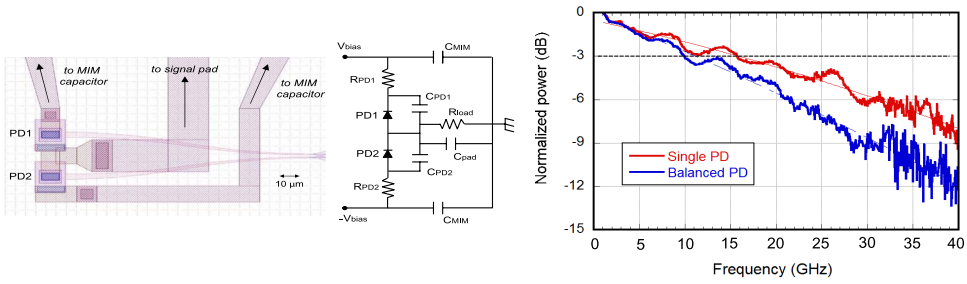

Fig. 3. (Left) Mask design of the balanced photodetectors with scheme of the equivalent electrical circuit. (Right) Bandwidth comparison of single and balanced photodetectors (at 3 V reverse voltage for each photodiode).

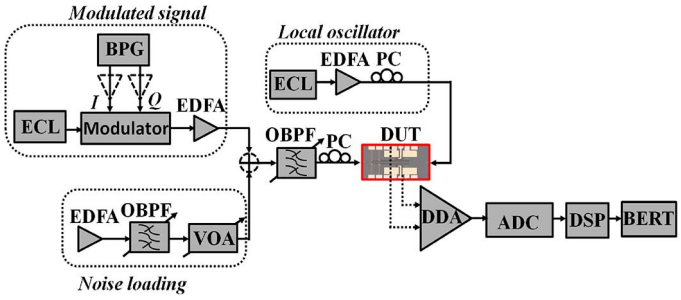

Fig. 4. Experimental setup. ECL: External cavity laser; BPG: Bit pattern generator; OBPF: Optical bandpass filter; EDFA: Erbium doped fiber amplifier; VOA: Variable optical attenuator; PC: Polarization controller; DDA: Dual driver amplifier; ADC: Analog-to-digital converter; DSP: Digital signal processing; BERT: Bit error rate tester.

The responsivity measured on a test single PD on the same chip was 0.5 A/W, while the dark current at -3 V was 9.2 μA. This value is actually larger than what expected from the specifications from the OpSIS platform.

3. Experimental Results

The experimental setup illustrated in Fig. 4 was employed to characterize the coherent receiver. Firstly, a QPSK signal was generated with a variable symbol rate by driving a nested Mach–Zehnder modulator with 2^7–1 pseudo random binary sequence (PRBS) for each arm (I and Q). An erbium-doped fiber amplifier (EDFA), an optical band-pass variable filter (OBPF) and a variable optical attenuator (VOA) were used for the noise loading stage, adding the filtered amplified spontaneous emission (ASE) noise to the modulated signal.

The resulting signal was then filtered using an OBPF and a polarization controller (PC) was employed in order to couple the light with a TE-polarization state to the device under test (DUT) through the grating coupler. The DUT is temperature controlled thanks to a Peltier cooler and operation temperature is 25 °C. The LO signal was generated using an external cavity laser (ECL) with a linewidth of 150 kHz and an EDFA. This source is then coupled to the DUT exploiting the second grating coupler. Two multiprobes, with both RF and DC probes, were used to collect the RF outputs from the balanced Ge-PDs, to control the phase shifters, and to bias the balanced Ge-PDs through integrated MIM capacitors.

As proper trans-impedance amplifiers (TIAs) were not available, the received signals were amplified with a dual-driver amplifier (DDA, small signal gain $=$ 20 dB, bandwidth $=$ 32 GHz) and then sampled by a 50-GS/s analog to digital converter (ADC). Finally, an off-line DSP recovered the output signal constellations and computed the BERs. The output constellation was optimized adjusting the phase shifters in the circuit in order to set proper quadrature condition.

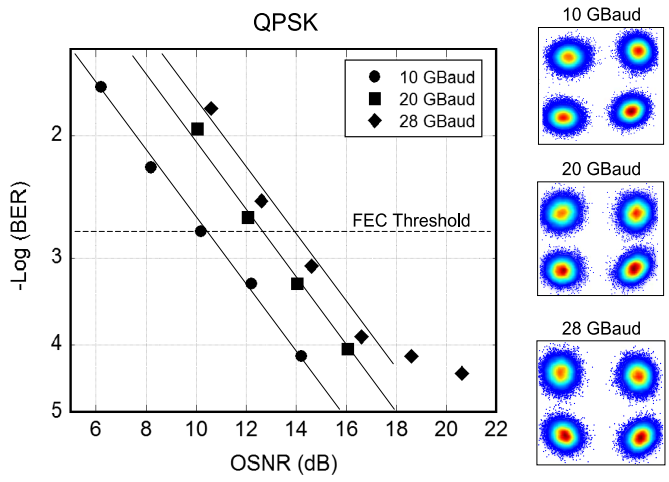

Fig. 5. BER versus OSNR (on 0.1 nm resolution bandwidth) for QPSK received signals at different baud rates and related constellations (at BER $= 10^{-4}$).

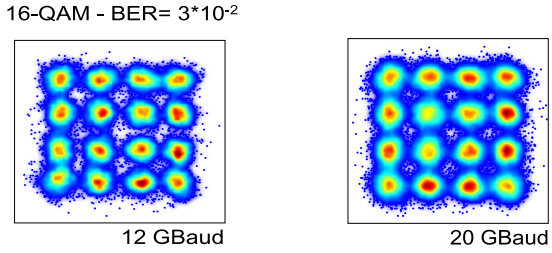

Fig. 6. A 16-QAM received signal with recovered constellations at 48 and 80 Gb/s.

Measurement results are summarized in Figs. 5 and 6. Fig. 5 reports the BER as a function of the OSNR (resolution bandwidth $= 0.1$ nm) for 10, 20 and 28 Gbaud QPSK signals, corresponding to 20, 40, and 56 Gb/s transmission, respectively. Measurements were performed at a -3 V reverse bias applied to each of the PD in the balanced receiver and using 3 and 20 dBm, for the signal and local oscillator off-chip optical power respectively. Considering the PIC path losses reported before, this means -11 dBm and 7 dBm power on the PDs for the signal and the local oscillator, respectively.

From Fig. 5 we have that the OSNR at a forward error correction (FEC) threshold of $2^{*}10^{-3}$ is 10, 12.8 and 14 dB for 10, 20 and 28 Gbaud respectively. QPSK constellations corresponding to the best BER value are reported in Fig. 5 insets. In a second experiment, a 16-QAM signal was generated using proper 4-level electrical signals at the transmitter and sent to the receiver in back-to-back. Constellations for the 12 and 20 Gbaud cases, corresponding to 48 and 80 Gb/s transmission respectively, are reported in Fig. 6. We have clearly visible symbols and moderate inter-symbol interference (ISI) even if noisy constellations. The 12 Gbaud constellation is slightly more defined, but, in both cases the best attainable BER by DSP was $3^{*}10^{-2}$. This happens because the quality of the received signals is close to the operating conditions of the DSP engine.

In addition, for both modulation formats, the length of maximum data sequences was limited to 2^{7}–1 in order to have reasonable BER values.

The limited performance of the receiver with 16 QAM signals can be addressed to two main reasons. The limited bandwidth in balanced configuration, as seen before, in combination with the lack of linear low noise TIAs for photocurrent amplification. Indeed, we used for electrical signal boosting driver amplifiers which were not optimized for low noise figure amplification of small current signals.

4. Conclusion

A novel integrated Si coherent receiver exploiting a new scheme without waveguide crossings, proposed in [11], [12], has been designed, fabricated, and tested back-to-back. The device consists of two single polarization grating couplers (for coupling of the received signal and of the LO), two 500-μm long phase shifters (for setting the quadrature condition), and two integrated balanced Ge-PDs. Despite performance degradation due to the combination of non-ideal electrical signal amplification and photodiode bandwidth limitation, experimental results show operation with single polarization 28 Gbaud QPSK (56 Gb/s) and 20 Gbaud 16-QAM (80 Gb/s) signals clearly demonstrating the feasibility of this novel receiver geometry.

In addition, even if the coherent receiver in the actual form is capable of receiving single polarization signals only; polarization multiplexed signals can be detected by a very similar architecture in which a 2-D grating for polarization splitting of the input signal is used [2], together with polarization diversity, i.e. using two parallel structures as reported in the present paper.

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