JVSTB Journal of Vacuum Science & Technology B

Evaluation of DyScO x as an alternative blocking dielectric in TANOS memories with Si 3 N 4 or Si-rich SiN charge trapping layers

G. Congedo, S. Spiga, U. Russo, A. Lamperti, O. Salicio, E. Cianci, and M. Fanciulli

Citation: Journal of Vacuum Science & Technology B **29**, 01AE04 (2011); doi: 10.1116/1.3533765
View online: http://dx.doi.org/10.1116/1.3533765
View Table of Contents: http://scitation.aip.org/content/avs/journal/jvstb/29/1?ver=pdfcov
Published by the AVS: Science & Technology of Materials, Interfaces, and Processing

Evaluation of $DyScO_x$ as an alternative blocking dielectric in TANOS memories with Si_3N_4 or Si-rich SiN charge trapping layers

G. Congedo,[a] S. Spiga,[b] U. Russo, A. Lamperti, O. Salicio, and E. Cianci
Laboratorio MDM, IMM-CNR, via C. Olivetti 2, 20864 Agrate Brianza (MB), Italy

M. Fanciulli
Laboratorio MDM, IMM-CNR, via C. Olivetti 2, 20864 Agrate Brianza (MB), Italy and Dipartimento di Scienza dei Materiali, Università Degli Studi di Milano Bicocca, Milano, Italy

(Received 11 August 2010; accepted 6 December 2010; published 26 January 2011)

Dysprosium scandate $DyScO_x$ with a κ value of ~20 has been investigated as blocking dielectric in charge trapping memory capacitors. $DyScO_x$ films with 28 and 18 nm thicknesses are deposited by atomic layer deposition on two different kinds of silicon nitride used as charge trapping layer, while SiO_2 is used as tunnel oxide and TaN is used as metal gate. Memory capacitors with Al_2O_3 as blocking layer with similar equivalent oxide thickness (EOT) to $DyScO_x$ are also characterized as benchmarks. $DyScO_x$ thermal stability on both Si_3N_4 and Si-rich SiN at annealing temperatures up to 900 °C demonstrates the complementary metal-oxide semiconductor process compatibility of the oxide. Especially when deposited on Si-rich SiN, comparable program and slightly better retention performance with Al_2O_3 are observed for $DyScO_x$, whereas erase still needs to be improved. Some variations in the electrical performance are found between the $DyScO_x$-based stacks with different charge trapping layer and have been discussed. Scaling the total stack EOT by reducing $DyScO_x$ thickness from 28 to 18 nm allows a large program/erase window, but with the penalty of an increased charge loss during retention. Our results suggest that the key factors in further improvement of $DyScO_x$ as blocking dielectric are the dielectric quality and leakage current.
 [DOI: 10.1116/1.3533765]

I. INTRODUCTION

The continuous demand for data storage in portable electronic devices has produced a very aggressive growth of NAND flash memories in the recent years. However, scaling the NAND flash technology, based on floating gate (FG) architectures, beyond the 2X technology node is extremely challenging due to the limitations related to the scaling of tunnel oxide (TO) below 7–8 nm, cell to cell interference and loss of control gate to FG coupling.[1]

Many evolutionary or revolutionary technologies have been proposed to eventually replace conventional FG memories. Among them, charge trap (CT) flash cell appears as the most technologically mature for NAND flash applications, because it is based on a fully complementary metal-oxide semiconductor compatible fabrication process and it is potentially compatible with a three-dimensional integration.[2] Moreover, in this technology the discrete nature of storage element (silicon nitride) allows more robustness to stress-induced leakage current and coupling interference issues. The most promising and investigated CT flash approach is the $TaN/Al_2O_3/Si_3N_4/SiO_2/Si$ (TANOS) cell, which is derived from the well known SONOS ($poly\text{-}Si/SiO_2/Si_3N_4/SiO_2/Si$) concept.[3] The key element of TANOS cell is the use of Al_2O_3 as blocking dielectric (BD) instead of SiO_2. Al_2O_3 allows a more efficient program/erase (P/E) operation due to the increased injecting field through the tunnel oxide with respect to the high-κ BD, while the SiO_2 TO can be kept thick enough to prevent direct tunneling during retention. Furthermore, a high work function metal gate such as TaN allows minimizing electron-back tunneling which causes erase saturation 3.

However, nitride scaling issues,[4] together with the moderate dielectric constant (κ) of Al_2O_3 (~9–10), represent a serious limitation in further improvements and scaling of the device. In this view, the use of a BD with κ value higher than Al_2O_3 is considered a viable solution. Indeed, in such a way, it is possible to reduce the electric field across the BD at fixed electric field through the SiO_2 tunnel oxide. The proper engineering of the dielectrics thickness and κ values within the stack can be therefore exploited for faster P/E operations and to minimize the electron leaking out toward the gate during retention. Besides a high κ value, materials suitable for BD application in TANOS memories must have sufficiently large energy band gap and band offsets with respect to the CT layer, thermal stability, low leakage current, low trap density, and high breakdown fields.[5]

Among the various high-κ candidates, rare-earth based scandates (i.e., $DyScO_x$ or $GdScO_x$) or aluminates ($GdAlO_x$, $LaAlO_x$) appear to fulfill the requirements for Al_2O_3 replacement as BD.[6] The case of scandates is of particular interest because with these ternary compounds it is possible to increase the κ value compared to the binary Sc_2O_3 without a large penalty in band gap or band offsets, which remain close to those of Sc_2O_3 [band gap of ~6.0 eV and conduction band offset of 2.0 eV with Si (Refs. 7 and 8)]. Previous papers have introduced $GdAlO_x$ (Ref. 9) and

[a]Author to whom correspondence should be addressed; electronic mail: gabriele.congedo@mdm.imm.cnr.it
[b]Electronic mail: sabina.spiga@mdm.imm.cnr.it

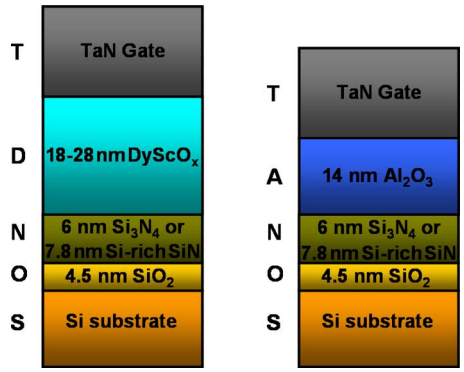

FIG. 1. (Color online) Schematic of the TDNOS and TANOS stacks analyzed in this work.

$LaAlO_x$ (Ref. 10) as BD, showing promising memory performance, but a large investigation on the electrical properties of rare-earth based scandates on top of silicon nitride in a TANOS cell has not yet been reported.

In this work, we show the electrical properties of TANOS-like memory capacitors incorporating ternary $DyScO_x$ as BD (TDNOS cell) upon two kinds of silicon nitrides as CT layer. We perform a comparison between program/erase and retention performance of $DyScO_x$ and Al_2O_3, first in the case of Si-rich SiN as CT layer, then in the case of Si_3N_4. Further, we analyze and discuss the impact of the different kind of nitride layer on the different memory performance of the devices. Finally, we check the effect of $DyScO_x$ thickness scaling on the overall performance of TDNOS stacks. A discussion on the issues to overcome for future integration of this material in charge trap memory devices is also provided.

II. EXPERIMENTAL DETAILS

Figure 1 shows the schematic of TANOS and TDNOS charge trapping memory capacitors characterized in this paper. The total EOT of the analyzed stacks is between 15 and 10 nm. For all stacks the tunnel oxide is 4.5 nm thick thermal SiO_2 tunnel oxide, while the charge trapping layer is 6 nm thick Si_3N_4 or 7.8 nm thick Si-rich SiN (with N/Si ratio of 1.05–1.15) made by low-pressure chemical vapor deposition. Finally either Al_2O_3 or $DyScO_x$ are integrated as blocking dielectrics, trying to compare the electrical performance of Al_2O_3 and $DyScO_x$ blocking dielectrics with same EOT and to address the scaling down of BD EOT. Table I provides the details of the samples, including physical thicknesses of the various layers measured by spectroscopic ellipsometry and EOT of memory capacitors extracted from the fitting of capacitance-voltage (*C-V*) curves at 1 MHz taking into account quantum mechanical corrections.[11]

TANOS cells are realized by atomic layer deposition (ALD) of Al_2O_3 on $Si_3N_4/SiO_2/Si$ (TANOS-1) and Si-rich/SiO_2/Si (TANOS-2) substrates. Al_2O_3 is deposited by ALD at 300 °C in the Savannah 200 reactor (Cambridge Nanotech Inc.) using $Al(CH_3)_3$ and O_3 as Al and oxygen source, respectively. After ALD process, rapid thermal annealing (RTA) is performed at 1030 °C in N_2 for 30 s to allow Al_2O_3 crystallization into the γ-phase,[5,12] which is known to improve the blocking dielectric quality due to reducing leakage current and trap density with respect to the amorphous phase.[6] The thickness of crystalline Al_2O_3 is around 14 nm and the measured κ value in the 9–10 range.

$DyScO_x$ films as BD are deposited by ALD at 350 °C in the F120 reactor (ASM Microchemistry Ltd.) using $Sc(C_{11}H_{19}O_2)_3$ and $Dy(C_{11}H_{19}O_2)_3$ as Sc and Dy precursors, respectively, and O_3 as oxygen source. Further details on the ALD growth are reported in Ref. 13. It is found from grazing incidence x-ray diffraction that as-deposited amorphous $DyScO_x$ layers develop polycrystallinity after RTA in N_2 at 600 °C for 30 s and reach the complete crystallization in the cubic solid solution phase at 900 °C.[13] The film composition measured by means of total reflection x-ray fluorescence is $Dy_{0.43}Sc_{0.57}O_x$. Time of flight-secondary ion mass spectrometry (ToF-SIMS) depth profiles reveal that the thermal stability of the DNOS stack is preserved for RTA temperatures up to 900 °C, temperature required for TaN crystallization. The κ value of $DyScO_x$ extracted from *C-V* measurements is ~18–20.[11,13] Consequently, two physical thicknesses are selected for $DyScO_x$: 28 nm to reach the same EOT of the 14 nm thick Al_2O_3 layer and 18 nm to analyze the memory performance of the stack when scaling its total EOT.

Capacitors are defined by 15 nm TaN/30 nm W deposition by reactive sputtering, device patterning by optical lithography, TaN/W wet etching or lift-off process and RTA at

TABLE I. Sample ID, RTA temperature, and EOT of the investigated stacks, along with the thickness of the different dielectrics measured by spectroscopic ellipsometry.

Stack	RTA (°C)	Physical thickness (nm)			Stack EOT (nm)
		Tunnel ox.	Trapping layer	Blocking dielectric	
TDNOS	900	4.5 nm SiO_2	7.8 nm Si-rich SiN	28 nm $DyScO_x$	15.3
TDNOS	900	4.5 nm SiO_2	7.8 nm Si-rich SiN	18 nm $DyScO_x$	12.7
TDNOS	900	4.5 nm SiO_2	6 nm Si_3N_4	33 nm $DyScO_x$	13.3
TDNOS	900	4.5 nm SiO_2	6 nm Si_3N_4	20 nm $DyScO_x$	10.1
TDNOS-1	1030	4.5 nm SiO_2	6 nm Si_3N_4	14 nm Al_2O_3	12.6
TDNOS-2	1030	4.5 nm SiO_2	7.8 nm Si-rich SiN	14 nm Al_2O_3	13.8

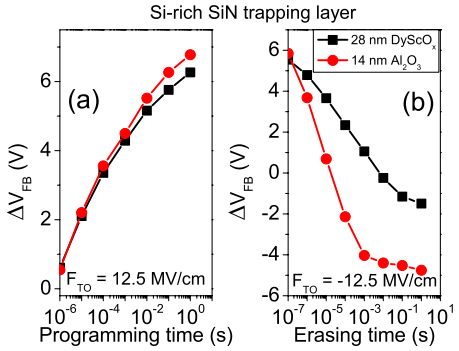

FIG. 2. (Color online) Comparison of (a) program and (b) erase transients at the same F_{TO} of TDNOS and TANOS-2 stacks with Si-rich SiN as charge trapping layer.

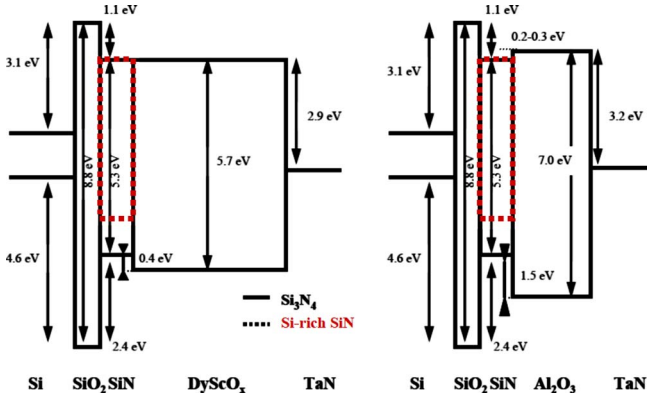

FIG. 3. (Color online) Schematic of the band diagrams of TDNOS and TANOS stacks.

900 °C for 30 s for TaN/W crystallization. Finally, memory capacitors were subjected to a forming gas annealing at 400 °C for 15 min.

Program characteristics are acquired by monitoring the flat band voltage shift ΔV_{FB} of the *C-V* curves of *n*-Si TANOS and TDNOS capacitors (ΔV_{FB} defined as the difference between the V_{FB} of the programmed state and the V_{FB} of the fresh cell) after each programming pulse, while the erase characteristics are assessed by monitoring the ΔV_{FB} after each erasing pulse on *p*-Si capacitors, starting from a programmed state of about 6 V. Finally, retention measurements are performed by evaluating the ΔV_{FB} loss (after programming each cell at $\Delta V_{FB} \approx 5$ V) at baking temperature in the 25–200 °C range.

III. RESULTS AND DISCUSSION

A. Memory performance of $DyScO_x$ on Si-rich SiN

Figures 2(a) and 2(b) show the P/E transients of TDNOS stack with Si-rich SiN as CT layer and the TANOS-2 benchmark. Considering the slight different EOT of the stacks (Table I) and the slight differences in V_{FB} values observed in the *C-V* curves of capacitors, the transients have been acquired by applying the same electric field across the SiO_2 tunnel oxide (F_{TO}), defined as: $F_{TO}=(V_G-V_{FB})/EOT$, where V_G is the voltage applied to the gate.

In this way, we ensure a fair comparison of the P/E characteristics of the stacks, and the influence of the different blocking dielectric is more clearly revealed. We have chosen F_{TO} values of ±12.5 MV/cm, allowing Fowhler-Nordheim (F-N) tunneling of the electrons through the TO. From Fig. 2(a) it can be observed that the initial steep ΔV_{FB} value is the same in the case of $DyScO_x$ and Al_2O_3, meaning that the program speed is the same. Only for pulse times above 1 ms the trapping rate is slightly reduced for $DyScO_x$-based stack. In the case of erase, shown in Fig. 2(b), faster speed is provided by Al_2O_3 even for short pulse times, and there is a clear difference in erase saturation level between the stacks.

In order to discuss the P/E behavior observed for TDNOS and TANOS-2 stacks, it is useful to look at their band diagrams (shown in Fig. 3), obtained using values taken from literature[8,14,15] and using the band diagram simulation software.[16] The slightly lower conduction band offset with Si of $DyScO_x$ film compared to Al_2O_3 [reported value of 2.0 ± 0.1 eV for $DyScO_x$ against 2.2 ± 0.1 eV for Al_2O_3 (Refs. 8 and 14)] could explain the slight reduction in program level for long pulse times in the case of TDNOS stack with respect to TANOS-2. Indeed, after being injected the high energy electrons which are traveling along the conduction band of nitride can see a low barrier (ϕ_B) between nitride and the blocking dielectric, thus flowing directly toward the gate instead of being trapped.[17] Moreover, the $DyScO_x$ layer could exhibit a higher leakage current than Al_2O_3, likely related to the presence of shallow traps. The different program behavior for high applied voltages and long programming pulses of charge trapping cells with different BD has been explained in other works[18] involving hole backtunneling from the gate through a BD with a low hole barrier height with the gate itself, as in our case (the hole barrier between $DyScO_x$ and TaN is reduced by 1 eV with respect to the case of Al_2O_3, see Fig. 3).

Concerning the poorer erase performance of TDNOS stack compared to TANOS-2 benchmark, the difference in band gap and band offset between $DyScO_x$ and Al_2O_3, as evidenced in Fig. 3, could have an important role. It is known that the electron barrier height ϕ_M between the blocking dielectric and the metal gate must be as high as possible to prevent electron backtunneling from the gate during erase. In the case of $DyScO_x$, the lower barrier with the TaN electrode determined by the different electron affinity compared to Al_2O_3 [reported electron affinity of 2.0 eV for $DyScO_x$ (Ref. 15) against 1.7 eV for Al_2O_3 (Ref. 19)] could promote more abundant electron current through the blocking dielectric toward the CT layer, which is known to limit erase saturation level.[3] A critical issue could also be a reduction in the effective TaN metal work function on top on $DyScO_x$, as was observed in literature[20,21] for TaN in contact with other oxides. This effect is not considered when building the energy band diagrams in Fig. 3, and a fixed TaN work function value of 4.9 eV is considered.[22] The different erase speed observed for the two stacks even for short erasing pulses could be also

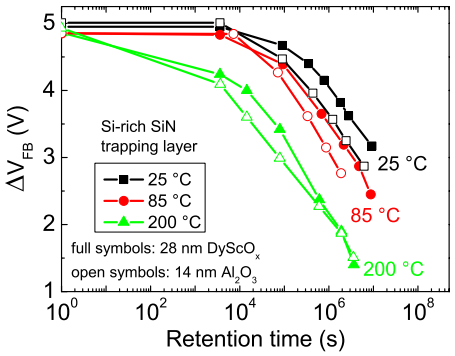

FIG. 4. (Color online) Retention characteristics at room temperature, 85 °C and at 200 °C, starting from a programmed state of 5 V, of TDNOS and TANOS-2 stacks with Si-rich SiN as CT layer.

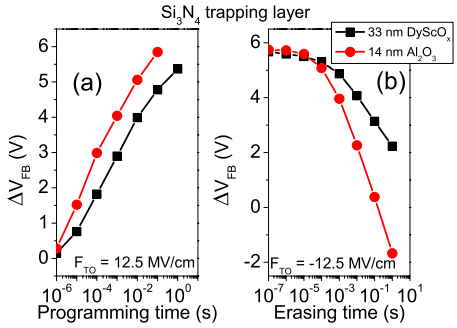

FIG. 5. (Color online) Comparison of (a) program and (b) erase transients at the same F_{TO} of TDNOS and TANOS-1 stacks with Si_3N_4 as charge trapping layer.

related to the presence of a trap-rich $DyScO_x$ blocking oxide, allowing trap-assisted tunneling of electrons from the gate toward the Si-rich nitride.

Figure 4 shows retention characteristics at 25, 85, and 200 °C for TDNOS and TANOS-2 stacks. At room temperature and at 85 °C, the larger physical thickness of $DyScO_x$ with respect to Al_2O_3 allows better retention due to an increased tunneling distance for electrons stored in the bulk of nitride. At 200 °C, TDNOS stack retains more charge than TANOS for baking times below 1×10^6 s, whereas the retention of the stacks becomes comparable for longer times. In order to explain the observed difference between Al_2O_3 and $DyScO_x$ we could consider that at 200 °C the thermionic emission of electrons from CT layer becomes a relevant charge loss mechanism, competing with trap to band tunneling.[10] Moreover, the effect of thermal excitation on charge loss becomes more important for long retention time.[23]Electrons which are thermally emitted from nitride trap to the conduction band, and subsequently migrated at the Si-rich SiN/$DyScO_x$ interface, can more easily escape in TDNOS than in TANOS stack due to the almost zero ϕ_B between DyScO and Si-rich SiN. It is worth noting that the testing temperature of 200 °C, although useful for physical understanding, is well beyond most of the final user temperature range (i.e., 85 °C for customer applications).

B. Memory performance of $DyScO_x$ on stoichiometric Si_3N_4

In Figs. 5(a) and 5(b) program and erase performance of TDNOS and TANOS-1 memory stacks with Si_3N_4 as CT layer are compared at a $F_{TO} = \pm 12.5$ MV/cm. As evident from Fig. 5(a), program speed of $DyScO_x$-based stack is sensibly reduced compared to Al_2O_3, with a ΔV_{FB} difference of 1–1.2 V even for short programming pulses. In the case of erase characteristics, shown in Fig. 5(b), poor erase is provided by TDNOS cell, which is not completely erased even for long erasing pulses.

Differently from what was observed for $DyScO_x$ on top on Si-rich SiN in the previous section, in this case the program efficiency of TDNOS stack with respect to TANOS-1 is evidently degraded, whereas erase speed of TDNOS and TANOS cells at short pulse times is the same. This findings could indicate differences in the dielectric quality of $DyScO_x$ and/or $DyScO_x$/nitride interface when grown on different starting surfaces (Si-rich SiN or stoichiometric Si_3N_4), as will be discussed in the next section. In particular, concerning erase operation, the most probable reason for the worse performance of $DyScO_x$ compared to Al_2O_3, is again the lower barrier between $DyScO_x$ and TaN gate with respect to Al_2O_3 (Fig. 3) and consequently an increased electron injection from the gate through the BD as the erasing pulse time increase.

Retention characteristics at room temperature are presented in Fig. 6(a). Higher charge loss in TDNOS stack than in TANOS-1 is observed already after 1 day at 25 °C, and the charge loss rate further increases for TDNOS stack with increasing times. This result could be a proof of the fast charge detrapping and leakage in $DyScO_x$. To confirm this hypothesis, field-accelerated retention measurements are performed on TDNOS stack at room temperature. When applying zero electric field across the tunnel oxide ($F_{TO} = 0$ MV/cm), the positive voltage applied to the gate would move the charge centroid toward the BD/CT layer interface, allowing charge loss by tunneling through the BD toward the gate. On the other hand, when zero electric field on the blocking dielectric ($F_{BD} = 0$ MV/cm) is applied, the negative applied voltage would push trapped electrons at the CT layer/TO interface, thus allowing tunneling through the TO toward the substrate. The results are shown in Fig. 6(b), starting from a high programmed level of ≈5 V in three

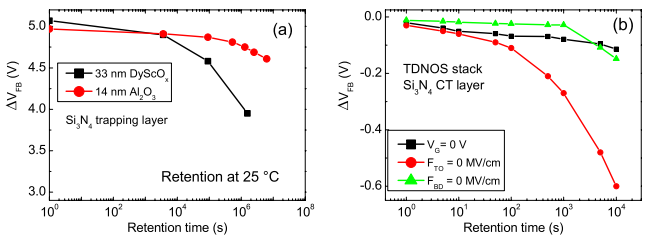

FIG. 6. (Color online) (a) Retention at 25 °C of TDNOS and TANOS-1 stack with Si_3N_4 as CT layer; (b) field-accelerated retention measurement (at room temperature) of TDNOS stack with Si_3N_4 as CT layer. $DyScO_x$ physical thickness is 33 nm.

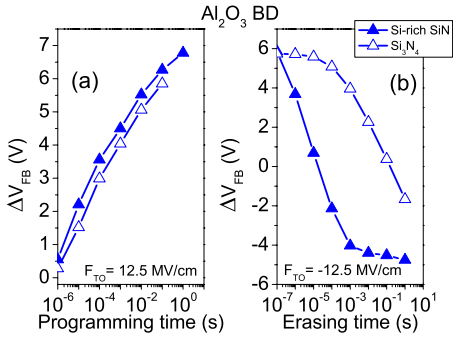

FIG. 7. (Color online) Comparison of (a) program and (b) erase transients at the same F_{TO} of TANOS-1 and TANOS-2 stacks.

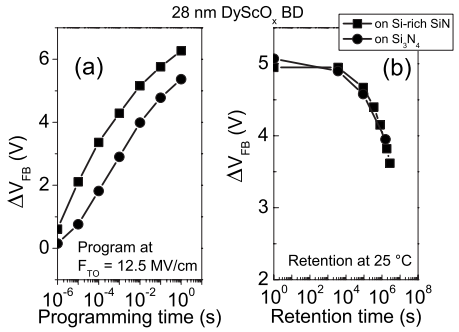

FIG. 9. TDNOS stacks with Si-rich SiN and Si_3N_4 as CT layer: (a) program transients at the same F_{TO}; (b) Retention at 25 °C. Squares: on Si-rich SiN; circles: on Si_3N_4. $DyScO_x$ nominal thickness is 28 nm.

different cases: F_{TO}=0 MV/cm, F_{BD}=0 MV/cm, V_G =0 V (the last case corresponds to pure retention measurement). The highest charge loss of 0.6 V after 10^4 s at room temperature is observed in the case of F_{TO}=0 MV/cm, whereas in the other two cases the charge loss rate and the charge loss values are comparable (0.1 V after 10^4 s). This result indicates that the main leakage path during retention is through $DyScO_x$, which exhibits fast charge detrapping from the programmed state. The observed behavior correlates with the poor program efficiency of TDNOS stack with Si_3N_4 as CT layer.

C. Effect of different charge trapping layer

The impact of different Si content in silicon nitride on memory performance of a TANOS cell has been extensively studied by several groups.[24–26] A common finding is that, in general, nitride engineering by increasing Si content slightly affects program characteristics,[24,26] but allows faster erase speed than Si_3N_4.[25,26] Retention is also hardly affected; charge loss is largely increased in Si-rich SiN with respect to Si_3N_4 not because of shallower trap energy levels but because of a higher electron occupation number in Si-rich SiN for the same charge state: defects which contribute to charge loss are Si-H bonds in Si_3N_4 and Si-H bonds and Si dangling bonds in Si-rich SiN.[24] Comparing P/E transients of TANOS-1 and TANOS-2 stacks, shown in Figs. 7(a) and 7(b), and their retention characteristics at 25 °C and 200 °C (Fig. 8), the trend observed in literature is confirmed in the better erase provided by TANOS-2 sample (Si-rich SiN) and at the same time its significant retention degradation.

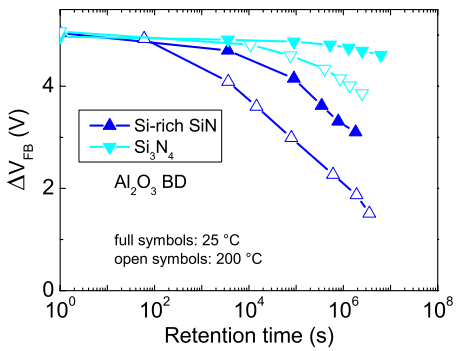

FIG. 8. (Color online) Retention at 25 °C (full symbols) and 200 °C (open symbols) of TANOS-1 and TANOS-2 benchmark samples.

Important differences in program and retention performance are instead found when comparing TDNOS stacks with $DyScO_x$ used as BD on top of Si-rich SiN and Si_3N_4. Figure 9(a) shows program transients at F_{TO}=12.5 MV/cm, and evidences that $DyScO_x$ on Si_3N_4 has lower program speed than $DyScO_x$ on Si-rich SiN. This strong difference was not observed in the case of Al_2O_3 on both kinds of nitride. Furthermore, from retention measurements at room temperature shown in Fig. 9(b), similar charge loss values are observed in both TDNOS stacks, while in principle the stack with Si-rich SiN would have worse retention than the stack with Si_3N_4 due to the well-known bad retention properties of a Si-rich nitride. All these features indicate a better dielectric quality, in terms of leakage properties and density of traps, of $DyScO_x$ film deposited on Si-rich SiN than when deposited on Si_3N_4, probably because of some modification close to the $DyScO_x$/nitride interface occurring during the ALD deposition or after the RTA step. ToF-SIMS profiles (data not shown) taken on DNOS stacks after RTA at 1030 °C, revealed that Si diffusion affects $DyScO_x$ layer: in the case of Si-rich SiN on bottom, the diffusion hardly affects the interface, whereas in the case of Si_3N_4 on bottom a broadening of the interface is revealed. It is possible to infer that, even at 900 °C, despite direct evidence is not seen, due to sensitivity, the considered interface is not perfectly identical in the two cases. Thus, an interface modification depending on the different nitride on bottom of $DyScO_x$ could be related to the observed different electrical behavior of the TDNOS stacks, i.e., in terms of increase in leakage current and different density of shallow traps in the blocking dielectric.

D. Effect of scaling $DyScO_x$ thickness on memory performance of TDNOS stacks

Capacitors featuring $DyScO_x$ films with nominal thickness of 18 nm are also fabricated to check the memory performance of TDNOS when scaling the total EOT of the stack. Figure 10(a) shows a set of programming transients acquired at different V_G values for TDNOS stacks with 28 and 18 nm $DyScO_x$ as blocking layer on Si-rich SiN. As

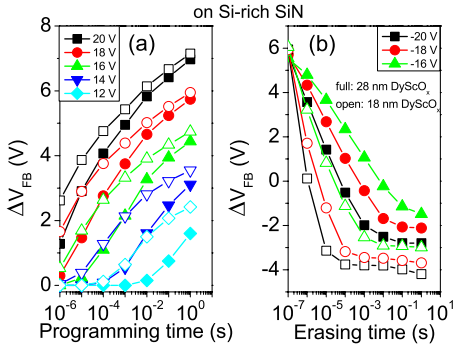

FIG. 10. (Color online) (a) program and (b) erase transients at different applied gate voltages for TDNOS stacks with Si-rich SiN as trapping layer and $DyScO_x$ as blocking dielectric with thickness of 28 nm (full symbols) and 18 nm (open symbols).

evident in the figure, the TDNOS stack can efficiently be programmed, with a V_{FB} shift in the range of 4–5 V at typical operating conditions (18–20 V, 100 μs–1 ms). Further, when decreasing the $DyScO_x$ thickness (or, equivalently, scaling the EOT of the cell), a given program level can be reached with a reduced V_G, especially for pulse times below 1 ms. The beneficial effect of the scaling of $DyScO_x$ thickness on erase performance is clearly visible in Fig. 10(b), where erase transients of TDNOS with different BD thickness (on Si-rich SiN) are shown: at the same negative V_G the cell can be completely erased for shorter pulse times in the case of $DyScO_x$ with nominal thickness of 18 nm. Similar results are obtained for TDNOS stacks with stoichiometric Si_3N_4 as trapping layer. Figure 11 shows the overall memory window (MW) as a function of the stack EOT for the TDNOS stacks with Si-rich SiN as CT layer, compared to the MW of TANOS-2 stack. Operating P/E conditions are ±20 V, 100 μs and ±18 V, 1 ms. The beneficial effect of scaling $DyScO_x$ thickness on the MW can clearly be observed, particularly in the case of erase. Large MW of about 9 V can be achieved when scaling EOT of the TDNOS stack from 15.3 nm down to 12.7 nm. Similar trend in MW improvement is also observed for the TDNOS stacks with Si_3N_4 as CT layer.

However, a worsening in retention of the TDNOS stacks is obtained when scaling $DyScO_x$ thickness from 28 down to 18 nm, whether the CT layer is Si_3N_4 or Si-rich SiN, at any

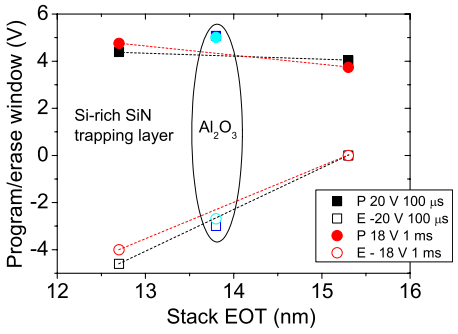

FIG. 11. (Color online) Plot of memory window of TDNOS capacitors with Si-rich SiN as CT layer, benchmarked with TANOS-2 stack. Operating conditions of P/E: ±20 V, 100 μs and ±18 V, 1 ms.

baking temperature. The most probable reason is that, when BD thickness is reduced, electrons stored in silicon nitride or in the shallow traps of $DyScO_x$ films see a reduced tunneling distance toward the gate electrode so that the probability of trap to trap or trap to band tunneling toward the gate is increased in the case of thin $DyScO_x$ film.

IV. CONCLUSIONS

In conclusion, TANOS-like capacitors incorporating $DyScO_x$ as BD are fabricated and their memory performance in terms of program/erase and retention are studied and benchmarked with correspondent TANOS cells. Despite the promising κ value and larger physical thickness compared to Al_2O_3, $DyScO_x$ overall performance as blocking dielectric is still insufficient to match the improvement required in a TANOS cell. The main reasons are related to the dielectric quality of the oxide especially in terms of current conduction and trap density, which require further optimization. Differences in electrical performance of $DyScO_x$-based stacks with different silicon nitrides on bottom are observed, indicating that a different charge trapping layer could affect the dielectric quality of $DyScO_x$ BD.

Scaling $DyScO_x$ thickness improves the overall memory window but leads to poor retention due to the reduced BD thickness. A solution to achieve memory stack improvement could be the use of an engineered blocking oxide composed of a sealing layer made of thin oxide with high band gap (i.e., SiO_2 or Al_2O_3) and a thick $DyScO_x$ layer on top. In this way, the presence of the high-quality sealing layer, in terms of leakage current and barrier height with the trapping layer, could improve the memory performance of the stack. In the case of $DyScO_x$, Al_2O_3 sealing layer could be the best choice due to the $DyScO_x$ thermal instability on SiO_2 for $T \geq 900$ °C.[13] Moreover the low κ value of SiO_2 compared to Al_2O_3 could compromise the overall κ value of the blocking oxide.

ACKNOWLEDGMENTS

This work was funded by the FP7 research Contract No. 214431 GOSSAMER. We are also grateful to Numonyx for supplying $SiN/SiO_2/Si$ substrates.

[1]K. Kim, *Proceeding of IEDM Technical Digest* (IEEE, Washington, 2005), p. 333.
[2]H. Aochi, *Proceeding of IMW* (IEEE, Monterey, 2009), p. 1.
[3]C. H. Lee, K. I. Choi, M. K. Cho, Y. H. Song, K. C. Park, and K. Kim, *Proceeding of IEDM Technical Digest* (IEEE, Washington, 2003), p. 613.
[4]T. Melde, M. F. Beug, L. Bach, S. Riedel, C. Ludwig, and T. Mikolaicjk, *Proceeding of NVSMW* (IEEE, Opio, 2008), p. 130.
[5]M. Alessandri, A. Del Vitto, R. Piagge, A. Sebastiani, C. Scozzari, C. Wiemer, L. Lamagna, M. Perego, G. Ghidini, and M. Fanciulli, Microelectron. Eng. **87**, 290 (2010).
[6]J. Kittl, K. Opsomer, M. Popovici, N. Menou, B. Kaczer, X. P. Wang, C. Adelmann, M. A. Pawlak, K. Tomida, A. Rothschild, B. Govoreanu, R. Degraeve, M. Schaekers, M. Zahid, A. Delabie, J. Meersschaut, W. Polspoel, S. Clima, G. Purtois, W. Knaepen, C. Detavernier, V. V. Afanas'ev, T. Blomberg, D. Pierreux, J. Swerts, P. Fischer, J. W. Maes, D. Manger, W. Vandervorst, T. Conard, A. Franquet, P. Favia, H. Bender, B. Brijs, S. Van Elschocht, M. Jurczak, J. Van Houdt, and D. J. Wouters, Microelectron. Eng. **86**, 1789 (2009).
[7]C. Zhao, T. Witters, B. Brijs, H. Bender, O. Richard, M. Caymax, T.

Heeg, J. Schubert, V. V. Afanas'ev, A. Stesmans, and D. G. Schlom, Appl. Phys. Lett. **86**, 132903 (2005).
[8]V. Afanas'ev, A. Stesmans, C. Zhao, M. Caymax, T. Heeg, J. Schubert, Y. Jia, D. G. Schlom, and G. Lukovsky, Appl. Phys. Lett. **85**, 5917 (2004).
[9]J. Pu, D. S. H. Chan, S.-J. Kim, and B. J. Cho, IEEE Trans. Electron Devices **56**, 2739 (2009).
[10]W. He, J. Pu, D. S. Chan, and B. J. Cho, IEEE Trans. Electron Devices **56**, 2746 (2009).
[11]G. Apostolopoulos, G. Vellianitis, A. Dimoulas, J. C. Hooker, and T. Conard, Appl. Phys. Lett. **84**, 260 (2004).
[12]M. Alessandri, R. Piagge, M. Caniatti, A. Del Vitto, C. Wiemer, G. Pavia, S. Alberici, E. Bellandi, and A. Nale, ECS Trans. **3**(3), 183 (2006).
[13]A. Lamperti, E. Cianci, U. Russo, O. Salicio, S. Spiga, G. Congedo, and M. Fanciulli, J. Vac. Sci. Technol. B **29**, 01AE03 (2011).
[14]V. V. Afanas'ev, A. Stesmans, M. Houssa, and M. M. Heyns, Appl. Phys. Lett. **78**, 3073 (2001).
[15]N. M. Murari, R. Thomas, S. P. Pavunny, J. R. Calzada, and R. S. Katiyar, Appl. Phys. Lett. **94**, 142907 (2009).
[16]R. G. Southwick and W. B. Knowlton, IEEE Trans. Device Mater. Reliab. **6**, 136 (2006).
[17]A. Suhane, A. Arreghini, G. Van den bosch, L. Breuil, A. Cacciato, A. Rothschild, M. Jurczak, J. Van Houdt, and K. De Meyer, *Proceeding of ESSDERC* (IEEE, Athens, 2009), p. 276.
[18]S. Jeon, J. H. Han, J. Lee, S. Choi, H. Hwang, and C. Kim, IEEE Electron Device Lett. **27**, 486 (2006).
[19]O. Blank, H. Reisinger, R. Stengl, M. Gutsche, F. Wiest, V. Capodieci, J. Schulze, and I. Eisele, J. Appl. Phys. **97**, 044107 (2005).
[20]Y. Sugimoto, M. Kajiwara, K. Yamamoto, Y. Suehiro, D. Wang, and H. Nakashima, Appl. Phys. Lett. **91**, 112105 (2007).
[21]A. Toriumi and T. Nabatame, ECS Trans. **25**(6), 3 (2009).
[22]S. Spiga, G. Congedo, U. Russo, A. Lamperti, O. Salicio, F. Driussi, and E. Vianello, *Proceeding of ESSDERC* (IEEE, Sevilla, 2010), p. 408.
[23]Y. Wang and M. H. White, Solid-State Electron. **49**, 97 (2005).
[24]E. Vianello, L. Perniola, P. Blaise, G. Molas, J. P. Colonna, F. Driussi, P. Palestri, D. Esseni, L. Selmi, N. Rochat, C. Licitra, R. Kies, G. Reimbold, B. De Salvo, and F. Boulanger, *Proceeding of IEDM Technical Digest* (IEEE, Washington, 2009), p. 83.
[25]C. Sandhya, A. B. Oak, N. Chattar, A. Joshi, U. Ganguly, C. Olsen, S. M. Seutter, L. Date, R. Hung, J. Vasi, and S. Mahapatra, IEEE Trans. Electron Devices **56**, 3123 (2009).
[26]G. Van den bosch, A. Furnémont, M. B. Zahid, R. Degraeve, L. Breuil, A. Cacciato, A. Rothschild, C. Olsen, U. Ganguly, and J. Van Houdt, *Proceeding of NVSMW* (IEEE, Opio, 2008), p. 128.