SFERA: An Integrated Circuit for the Readout of X and γ -Ray Detectors

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***Abstract*— In this work we present SFERA, a low-noise fully-programmable 16 channel readout ASIC designed for both X- and γ-ray spectroscopy and imaging applications. The chip is designed to process signals coming from solid-state detectors and CMOS preamplifiers. The design has been guided by the use of Silicon Drift Detectors (SDDs) and CUBE charge sensitive amplifiers (CSAs), although we consider the ASIC sufficiently versatile to be used with other types of detectors. Five different gains are implemented, namely 2800 e^-, 4400 e^-, 10000 e^-, 14000 e^- and 20000 e^-, considering the input connected to a 25 fF feedback capacitance CMOS preamplifier. Filter peaking times (t_P) are also programmable among 0.5, 1, 2, 3, 4 and 6 μs. Each readout channel is the cascade of a 9th order semi-Gaussian shaping-amplifier (SA) and a peak detector (PKS), followed by a dedicated pile-up rejection (PUR) digital logic. Three data multiplexing strategies are implemented: the so-called *polling X*, intended for high-rate X-ray applications, the *polling* γ, for scintillation light detection and the *sparse*, for signals derandomization. The spectroscopic characterization has shown an energy resolution of 122.1 eV FWHM on the Mn-K_α line of an ^{55}Fe X-ray source using a 10 mm^2 SDD cooled at -35 °C at 4 μs filter peaking time. The measured resolution is 130 eV at the peaking time of 500 ns. At 1 Mcps input count rate and 500 ns peaking time, we have measured 42% of processed events at the output of the ASIC after the PUR selection. Output data can be digitized on-chip by means of an embedded 12-bit successive-approximation ADC. The effective resolution of the data converter is 10.75-bit when operated at 4.5 MS/s. The chosen technology is the AMS 0.35 μm CMOS and the chip area occupancy is 5 × 5 mm^2.**

***Index Terms*— ASIC, gamma-ray detectors, high rate measurements, Silicon Drift Detectors, X-ray detectors, X-ray spectroscopy.**

I. Introduction

ONE of the main requirements in X- and γ-ray spectroscopy, nuclear physics experiments and medical imaging applications, is the optimization of the energy resolution of the overall detection system. Therefore, for a given application, given the incident photons energy and rate, design efforts are typically oriented to minimize the noise introduced by the acquisition chain, made of both detector and readout electronics. Thanks to the technological advances the microelectronics industry has encountered in the last fifteen years, readout front-ends are often implemented as multichannel application specific integrated circuits (ASICs) [1] so as to cope with the increasingly high number of units in the detection modules.

Under an architectural and operative perspective, monolithic crystal scintillator-based γ-ray readout electronics significantly differs from direct conversion X-ray electronics. A first difference might for example be represented by the data multiplexing strategy, which in the first case needs to take into account that all of the detectors of the matrix are hit by photons once a γ-ray is absorbed by the scintillator. This requires that all of the outputs of the analog channels are sequentially multiplexed after the event is detected by one channel of the ASIC or by another ASIC of the detection module. X-ray readout electronics could require instead sparsification of events, whereby only those channels that detected an event are multiplexed together with their digital address. Furthermore, for high throughput X-ray applications, an asynchronous, high-frequency sequential multiplexing may be preferable. Other important differences arising from the detector choice can imply a wide range of gain and shaping time. The gain range is associated with the different energy ranges to be accommodated (direct X-ray detection and γ-ray detection with scintillators). Short shaping times might be required in high-rate X-ray detection while longer shaping times may be needed for scintillators to minimize the ballistic deficit effect [2]. For scintillation detection, the optimization of the analog channel should indeed be done having regard to the decay time constants of the chosen scintillator. For example, the optimum shaper peaking time in case of γ-ray spectroscopy with a CsI:TI monolithic crystal, whose primary and secondary decay time constants are respectively about 0.8 and 3.5 μs, is a trade-off between the total noise, which depends on the number of detectors, and the ballistic deficit, which instead depends both on the detector size and on the scintillator behaviour with temperature [3]. All of these constraints are often met by designing specific ASICs which may lack the necessary versatility to be used in other applications. In addition, most readout ASICs designed so far do not provide on-chip analog-to-digital (A/D) conversion of the filters' output signals, making the analog transmission to the data acquisition system (DAQ) more susceptible to

Manuscript received February 8, 2016; revised April 20, 2016; accepted May 4, 2016. Date of publication May 9, 2016; date of current version June 21, 2016. This work was supported in part by INFN (SIDDHARTA experiment).

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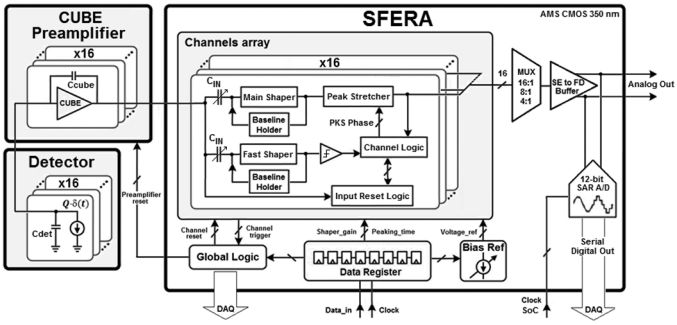

Fig. 1. SFERA simplified block diagram.

being corrupted by external interferences, as in the case of electromagnetically harsh experimental environments, such as nuclear physics experiments and synchrotron beam lines.

Aware of all of these impairments, in this work we have attempted to merge all the aforementioned requirements towards a more general-purpose ASIC approach, by designing a full-programmable circuit, with on-chip digitization, to be suitable for both X-ray and γ-ray detection modules. The reference device for this design is the Silicon Drift Detector (SDD) because of its excellent noise performance, thanks to which it has established itself as the state-of-the-art device for low-noise and high-rate X-ray detection in the typical range 0.2 to 30 keV, in X-ray spectroscopy applications, such as XRF (X-ray fluorescence). Thanks also to the high quantum efficiency, the SDD represents a competitive alternative to photomultiplier tubes (PMTs), PIN diodes and silicon photomultipliers (SiPMs) for scintillation light detection.

This paper is organized as follows. Section II deals with the design of SFERA, outlining the project specifications and describing the relevant circuit implementation details. In Section III the spectroscopic and high-throughput measurements are presented. Section IV introduces the 12-bit A/D converter integrated on the ASIC while the conclusions are drawn in Section V.

II. Circuit Implementation

A. ASIC Architecture

The circuit is designed to process signals coming from pulsed-reset CMOS charge-preamplifiers, such as CUBE [4], coupled to different kinds of detectors, as shown from the block diagram of Fig. 1. Apart from the SDDs, mentioned in the introduction, other examples of feasible devices may include small area PIN diodes and Germanium detectors [5]–[8]. The decision to use monolithic CMOS preamplifiers instead of integrating them directly into the ASIC is a consequence of the outlined applications and detector dimensions. Whereas employing detector-arrays whose single units feature an area of few tens of square millimeters, an independent CSA gives more flexibility since it can more easily be mounted in close proximity to the detector anode. This guarantees a lower electronic noise because the stray capacitance associated to the anode-to-preamplifier wire bonding connection is minimized.

The analog section of SFERA is made of a bank of 16 readout channels, organized in 4 independent subsets of 4 each for data multiplexing purposes. Each analog channel integrates two distinct SAs with the same architecture: the main one, optimized for noise and connected to the output multiplexer and the fast shaper, that is used to generate the internal triggers employed by the PUR logic to discard piled-up events. The output voltage baselines of the shaping amplifiers are kept reasonably constant with the input photons rate by means of baseline-holder (BLH) circuits. The BLH consists of a slew-rate-limited nonlinear buffer, a low pass filter and a transconductor in series [9]. SFERA offers full programmability of the main shaping amplifier filter parameters. The peaking time may be set among 0.5, 1, 2, 3, 4 and 6 μs while a fixed value of 200 ns has been chosen for the fast shaper. By tuning the input coupling capacitance (C_{IN}) the filter's gain changes to accommodate a dynamic range respectively of 2800 e^-, 4400 e^-, 10000 e^-, 14000 e^- and 20000 e^-, considering the input connected to a 25 fF feedback capacitance CUBE preamplifier. This allows to cover a wide energy range for both X- and γ-ray detection with monolithic crystal scintillators. In particular, the first three gain settings correspond to a dynamic range of 10 keV, 16 keV and 36 keV using a SDD. The main shaper is followed by two additional blocks that operate jointly: the peak detector and the PUR logic. In particular, the task of the latter is to synchronize the PKS phases and to reject piled-up events [10].

SFERA digital global logic is responsible for driving the output multiplexer (MUX) in different operational modes according to the target application. Static programming bits are stored in an internal memory (SRAM) programmable via serial protocol interface (SPI). Output multiplexed data are buffered by two single-ended to fully-differential output buffers. As an alternative to external converters, the IC also integrates a 12-bit successive-approximation ADC, discussed in detail in Section IV, so as to eventually digitize the data before communicating them to the DAQ, an interesting solution for low-power and compact detection modules or in the case of strong electromagnetic interference environment (e.g., at synchrotron facilities).

The chip is implemented in AMS 0.35 μm CMOS technology and occupies an area of 5×5 mm^2. The physical layout is shown in the die photograph of Fig. 2.

Below, a few relevant circuit implementation details are presented, namely the shaping amplifier, peak detector and MUX digital control logic.

B. Shaping Amplifier

The topology that has been chosen for SFERA shaping amplifiers is the semi-Gaussian, a very widespread choice in nuclear electronics. The choice of the optimum order of the filter and its implementation (real vs. complex conjugate poles) have been made according to design guidelines of time-continuous unipolar SAs, as the ones reported in [11]. The design relies on a trade-off between ballistic deficit (BD), high-throughput capability and energy resolution, which all influence the ENC of the system. For this reason, the order

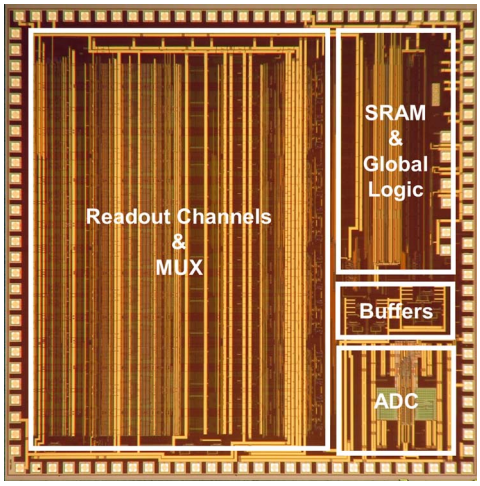

Fig. 2. SFERA physical layout implementation and main building blocks. The technology is AMS CMOS 0.35 μm C35B4 and the die size 5 × 5 mm^2.

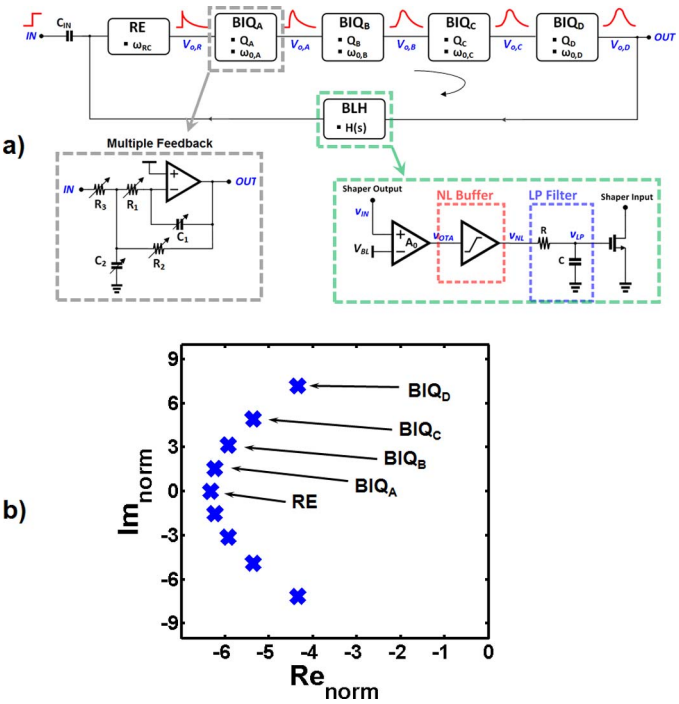

Fig. 3. Block diagram of the unipolar 9th order complex-conjugate poles SA, designed by cascading a real pole stage and four biquadratic cells (a) and filter poles constellation normalized by the peaking time (b).

of the filter has been chosen to be the 9th. The shaper block diagram is illustrated in Fig. 3(a), which also shows the circuit implementation, consisting of the cascade of an RC stage, responsible for the real pole of the transfer function, and four biquadratic multiple-feedback (MFB) cells, which provide 4 complex-conjugate poles pairs. These are shown in the poles constellation of Fig. 3(b).

Since the filter peaking times depend on the poles' position in the complex plane and given that the natural frequency and quality factor of each complex-conjugate pole pair are a function of the MFB circuit parameters, the SA peaking times are selectable by tuning the resistances and capacitances of each stage. Considering a single multiple-feedback cell, it is worth noting that the same circuit parameter, whether a resistance or a capacitance, may affect different characteristics, such as the stage frequency response, peak-gain, input-referred noise, area occupancy and DC operating points. Even more complex is tuning all of the passives of all of the cells such that all these requirements are simultaneously met. Each MFB stage provides for 5 parameters (3 resistances and 2 capacitances) while the real stage provides for one resistance (having fixed its capacitance). Furthermore, the input coupling capacitance C_{IN} is involved in the SA peak gain calculation thus it must also be parametrized. A total of 22 circuit parameters must be therefore computed in order to satisfy all of the aforementioned specifications. A viable way to do this is by designing one stage at a time by means of parametric SPICE simulations in Cadence®. A more straightforward and rigorous approach has instead been chosen for the design, which exploits Matlab™ modelling simulations to obtain, for each filter peaking time, the best set of circuit parameters $[C_{IN}, R_0, R_{1A}, R_{2A}, R_{3A}, C_{1A}, C_{2A} \ldots C_{1D}, C_{2D}]_i$, where i is the peaking time index, ranging from 1 to 6.

In addition to the semi-Gaussian analog filter, the shaping amplifier also integrates four comparators, not shown in Fig. 3(a), to generate the digital triggers employed by the peak detectors, the channel logic and the global digital section of the chip for both data multiplexing and event rejection purposes. The first comparator generates the preamplifiers reset pulse once the voltage of the input node (IN), which increases in a ramp-like fashion because of the detector leakage current integration, has surpassed a given threshold (i.e., 3 V). The second, sensing the output of the RC stage, produces the triggers (called TR_HT, where "HT" stands for "high threshold trigger") used to reject events outside of the selected input energy range. The third and fourth discriminator are connected to the output of the main and fast shaper respectively, generating the trigger signals needed to synchronize the multiplexer digital logic and to discard piled-up events, namely TR_{MAIN} and TR_{FAST}, respectively.

C. Peak Stretcher

The PKS has a 3-phase topology [12], as shown in the schematic diagram of Fig. 4, where a first *track* phase, in which the circuit operates in a closed-loop buffer fashion with all switches named TRK and WR closed, is followed by the *write* phase, opening instead the TRK switch as soon as a photon hits the detector and the fast SA output comparator generates a trigger. In this latter phase the PKS still operates in closed-loop but only following the positive derivative of the semi-Gaussian SA output voltage pulse. Once its peak has been reached and no pile-up has occurred, the TR_{mirror} signal triggers the third phase (*read*) by opening all WR switches and closing RD ones. The loop is now open and the analog peak value, made available at the multiplexer input, is stored by the capacitor C_H. Such a PKS topology has an inherent offset subtraction property, that allows to get rid of the operational amplifier offset [13]. The latter is indeed first stored on C_H during *track* and *write* and then subtracted from the output at the *write*-to-*read* switchover.

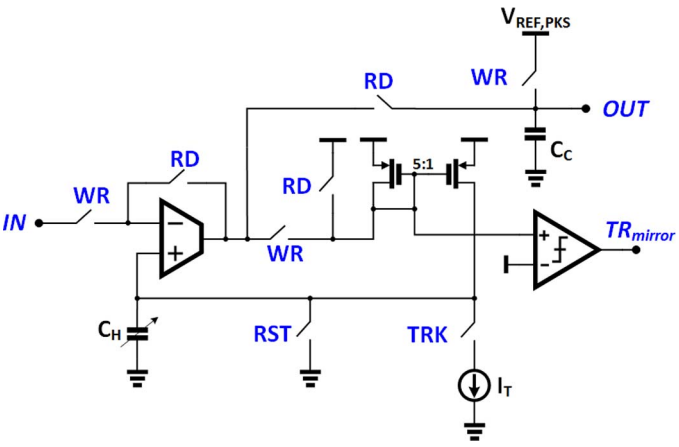

Fig. 4. 3-phase PKS circuit implementation with control signals.

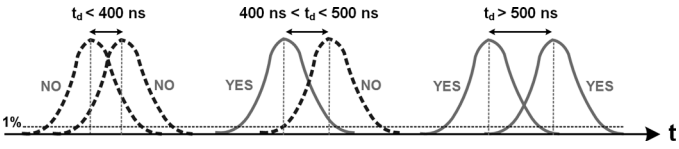

Fig. 5. Example of PUR logic operation for the 500 ns peaking time. If the time shift (t_d) between two incoming photons is shorter than 400 ns (left) both detected events are discarded, while if t_d falls between 400 and 500 ns (center) only the second is discarded. For time shifts longer than 500 ns (right) both the events are correctly acquired.

The peak detection mechanism operates jointly with a high-efficiency PUR logic [10], whose task is to discard partly overlapped semi-Gaussian pulses, but only if the amount of overlap significantly affects the amplitude of the adjacent pulses. If the distance shift between two incoming photons is lower than the peaking time of the filter then one, or even both pulses, will not spur any peak detection at the PKS level because the SA output pulses amplitudes would more likely be mutually corrupted. Fig. 5 shows an example of the pile-up rejection strategy in the case of the shortest 500 ns peaking time.

D. Output Multiplexing Protocols

Three different data multiplexing strategies have been implemented in SFERA: *polling-X*, *polling-*γ and *sparse*. In the *polling-X* readout, targeting high-rate X-ray applications, data are sequentially output multiplexed at a fixed frequency of 10 MHz, asynchronously with respect to the occurrence of input photons. In the *polling-*γ, for scintillation light detection with detector-arrays and monolithic crystal scintillators, the data are sequentially multiplexed after a global trigger is generated by one channel (typically the one with the largest amplitude). Finally, the *sparse* readout is employed to accomplish event sparsification.

In the *polling-X* multiplexing strategy the MUX operates a fast sequential readout of the PKS outputs, which is asynchronous and uncorrelated from any peak detection and pile-up rejection operation taking place upstream. The MUX digital logic comprises a shift-register (SR) made of 16 flip-flops, whose outputs work as the selection lines (sel) of the multiplexer switches, as shown in the descriptive block diagram of Fig. 6.

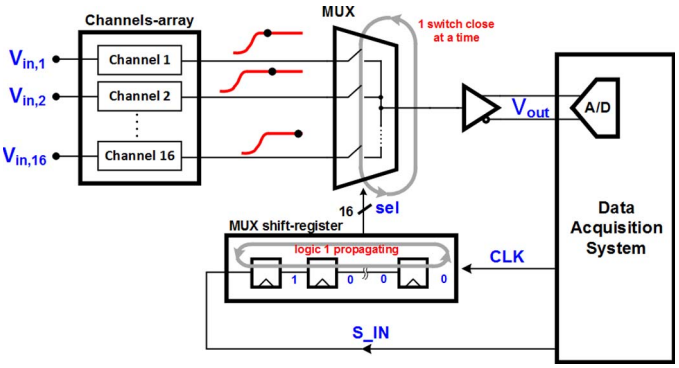

Fig. 6. Polling-X output multiplexing protocol descriptive diagram and interface with the DAQ.

A logic 1 is right-shifted in the SR on each rising edge of the clock signal CLK provided by the data acquisition system (DAQ). The S_IN signal, also generated by the external DAQ, is provided to the shift-register input after a number of clock pulses equal to the number of channels being multiplexed and is sampled on the CLK rising edge. In this way a new logic 1 is loaded in the first position of the SR, giving rise to a new readout sequence starting from the first channel. It is worth mentioning that the analog output MUX can also be programmed to operate in a 16:1, 8:2, 8:1, 4:2 or 4:1 fashion, depending on the format of the detector array to be readout and the foreseen input photon rate. The advantage of this modality is to facilitate the DAQ management of the output events, considering also the fact that the channel address does not need to be transmitted. Such readout protocol can exhibit good efficiency also at high throughput rates, once the polling frequency is sufficiently large with respect to the average event rate, which may be limited by the PUR in each channel.

The *polling-*γ multiplexing protocol is intended for the use of SFERA in γ-ray spectroscopy and imaging applications, where several detection modules, made of arrayed detectors coupled to monolithic crystal scintillators, need to be readout by multiple ASICs. This operational mode also exploits a sequential readout of all the ASIC 16 channels, as shown in the block diagram of Fig. 7, that this time is instead synchronous with the event detection. When a γ-ray photon is absorbed by the crystal, the visible light emitted is spread with a certain distribution over the detection units. Thus, all of the electronic readout channels have to be processed to properly reconstruct the γ-ray photon energy.

The first SA among all of the channels of all of the ICs employed in the system that detects a valid event, will generate a TR_OUT_LT pulse, where "LT" stands for "low threshold trigger", transmitted to the DAQ. In response to such a trigger, representing the logic OR of all the TR_{MAIN} signals (see Section II-B), the data acquisition system communicates to all of the chips a TR_IN_ACK so as to enable all of the peak stretchers to switch from the *write* to the *read* phase, which means that after a period equal to the semi-Gaussian

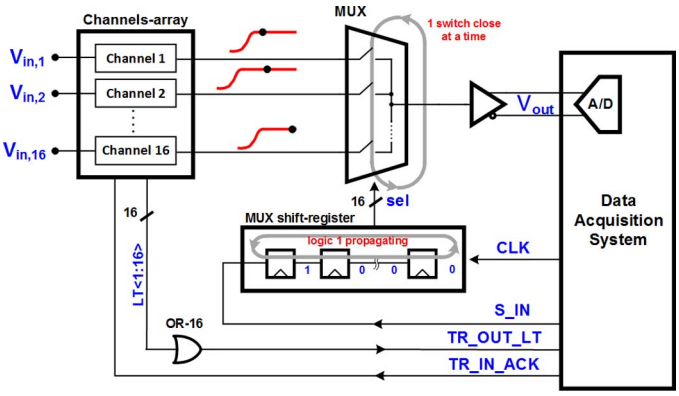

Fig. 7. Polling-γ output multiplexing protocol descriptive diagram and interface with the DAQ.

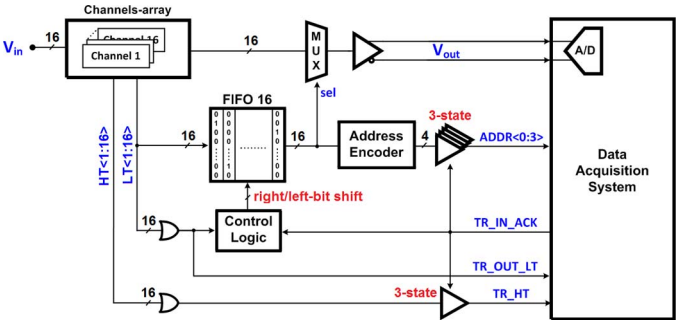

Fig. 8. Sparse digital logic block diagram and interface with the DAQ.

pulse rise-time, they will have reasonably held the SA peak-amplitudes. The S_IN and CLK signals accomplish the same operation described for the polling-X multiplexing, with the difference that only a single train of clock pulses (16, 8 or 4 depending on the MUX mode) is provided for each detected event. As well as the previous modality, the polling-γ also does not need the channel address to be communicated to the DAQ.

Finally, the *sparse* multiplexing protocol has been implemented to accomplish the requirements of the SIDDHARTA project [14], in which only those channels detecting an event need to be output multiplexed. A simplified block diagram of the digital logic used to do this is shown in Fig. 8. Its task is to manage the data transfer to the DAQ, synchronously providing to it both the firing channels' addresses and the related stretched pulse-peaks in the same time order that the events are detected. In this operational mode, once a photon hits the detector, the arrival timestamp is communicated to the data acquisition system by the TR_OUT_LT signal, which in this case is the logic OR of all the TR_{mirror} triggers coming from the channels' peak-stretchers and indicated with $LT < 1 : 16 >$ in the picture. On the rising edge of the TR_OUT_LT trigger, the instantaneous values of all 16 of the LT signals are clocked in the first free position of a 16-bit first-in-first-out (FIFO) memory, thus storing the one-hot-encoded address of the channel that generated the trigger.

The use of a FIFO multi-bit register accomplishes a dual purpose. The first is to implement the sparsification of events by simultaneously providing the channel address

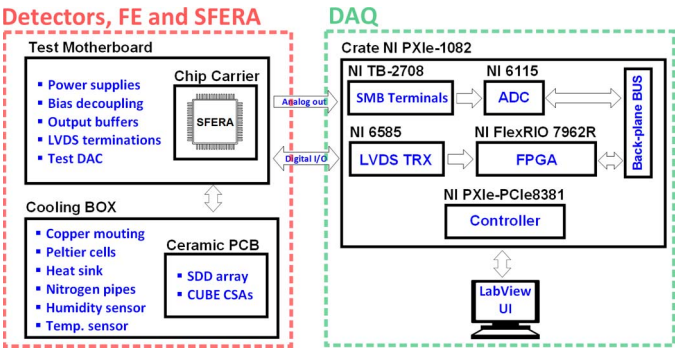

Fig. 9. Block diagram of the complete acquisition system comprising detectors, front-end and back-end electronics.

both to the external DAQ and to the analog MUX (using it as selection line). This ensures the synchronism with the associated analog output value. The second function is to manage high-rate event bursts. In fact, when photons which are less distant in time than the TR_IN_ACK clock period are detected on different channels, each PKS will still hold a proper analog peak voltage while the addresses are sequentially stored in the FIFO. The latter are then shifted-out at a lower speed, allowing the DAQ to properly digitize the related MUX outputs one after the other. This operation occurs at a specific request from the DAQ by means of the TR_IN_ACK pulse, which triggers a right-bit shift of the elements in the FIFO and whose duration is lower bounded by the analog-to-digital conversion time. It is therefore evident that the number of TR_OUT_LT and TR_IN_ACK pulses have to be equal to properly readout all the FIFO queue. Prior to their transfer to the data acquisition system, the one-hot-encoded addresses are converted into a 4-bit binary format ($ADDR\langle 0 : 3\rangle$) and buffered by tri-state drivers. A TR_HT trigger, which is the logic OR of the TR_HT signals of the single channels (indicated with $HT\langle 1 : 16\rangle$ in Fig. 8), is also provided to inform the DAQ about events exceeding the energy range, that are typically associated to the X-ray background foreseen in SIDDHARTA and which can then be conveniently discarded. The use of tri-state buffers for both $ADDR\langle 0 : 3\rangle$ and TR_HT signals, which are enabled during the on-time of TR_IN_ACK, is due to the multi-ASIC hardware apparatus of the experiment, in which 24 ICs will be required to readout 48 SDD-arrays of 8 units each. To minimize the number of lines and connections between the readout electronics and DAQ, which can definitely represent an issue in terms of size, cost and design complexity, $ADDR$ and TR_HT signals are shared on two common buses. The *sparse* modality is inherently more efficient than the *polling-X* but it requires a more complicated management on the DAQ side and the transmission of the channel address.

III. Measured Results

A. Experimental Set-Up

The experimental measurements have been performed to characterize both the spectroscopic performance and the throughput capabilities of SFERA. The experimental set-up, whose architecture is presented in the block diagram of Fig. 9,

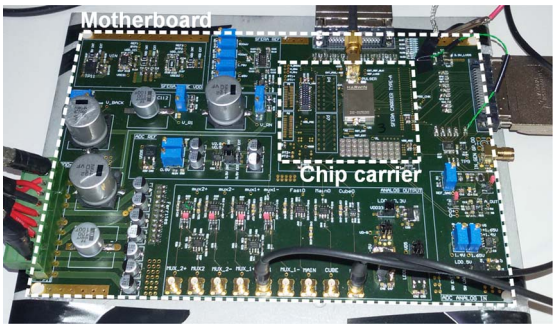

Fig. 10. Experimental set-up test PCBs: motherboard and chip carrier plugged on it.

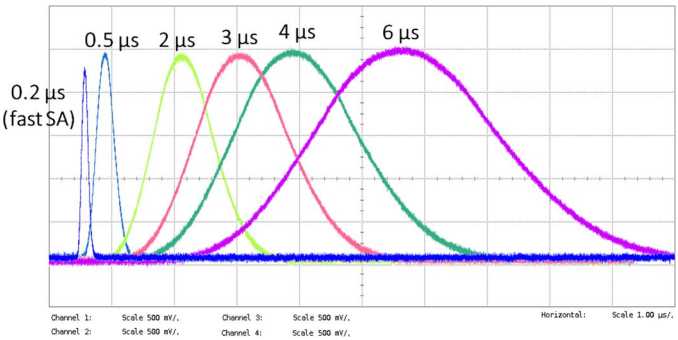

Fig. 11. Shaping amplifiers output semi-Gaussian pulses at 0.2, 0.5, 2, 3, 4 and 6 μs peaking time.

comprises three main subsystems: the cooling box, two printed circuit boards (PCBs) and the DAQ.

The former consists of an aluminium box hosting the detectors, charge preamplifiers, Peltier-cells, copper heat sink and water pipes. Two custom PCBs, namely the *motherboard* and the *chip carrier* depicted in Fig. 10, have been designed to provide power supplies, bias decoupling capacitors, LVDS terminations for the on-chip transceivers and a 16-bit D/A converter to characterize the embedded SAR ADC. Finally, the DAQ is made of commercial National Instruments^{TM} hardware. In particular, a NI-6115 12-bit ADC board is employed to digitize SFERA output multiplexed data while a FlexRIO 7962R FPGA module manages all control signals to and from the chip.

An example of the main and fast shaper output pulses at different peaking times and at the maximum filter gain of 2800 e^- is presented in Fig. 11, as measured with an oscilloscope. No undershoot has been observed for any of the possible configurations of gain and peaking time, resulting in almost ideal semi-Gaussian output waveforms, as expected from simulations.

B. X-Ray Spectroscopy Measurements With ^{55}Fe

The first set of experimental measurements that has been performed is X-ray spectroscopy using ^{55}Fe sources and FBK [15] silicon drift detectors, both in a single circular format and in a 3×3 matrix format with square-shaped single units.

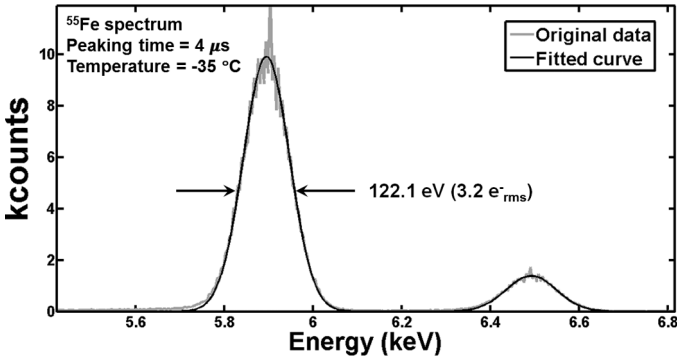

Fig. 12. Energy spectrum of a ^{55}Fe source measured with a 10 mm^2 area single SDD at -35 °C and 4 μs peaking time. The SDD measured current density leakage at room temperature is lower than 50 pA/cm^2.

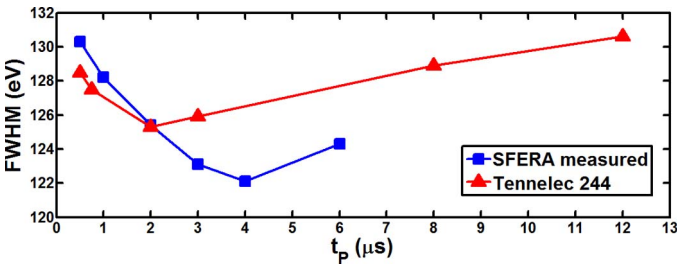

Fig. 13. SFERA energy resolution for all the implemented peaking times compared with the commercial SA Tennelec TC 244 performance.

1) Single Small-Area SDD: The single SDD employed for the measurement is a circular 10 mm^2 area detector, whose leakage current density is about 36 pA/cm^2 at room temperature. Fig. 12 presents the ^{55}Fe energy spectrum measured at 4 μs shaping time, showing an energy resolution of 122.1 eV FWHM on the Mn-K$_\alpha$ emission line, equivalent to an ENC of 3.2 e^-_{rms}, which is among the best results reported so far with a SDD. Although the nonlinearity characteristics of the 12-bit NI-6115 ADC employed for the measurements give rise to the slight indentations visible at the top of both peaks K$_\alpha$ and K$_\beta$, the energy resolution obtained from the fitting is not affected, considering the perfect overlap between the side walls of the spectral energy lines and the fitted curve. An energy resolution of 130.3 eV FWHM on the Mn-K$_\alpha$ line (ENC of 6.2 e^-_{rms}) has been measured at the shortest 500 ns SFERA peaking time.

The noise characterization at different peaking times is instead presented in Fig. 13, and moreover compared to the curves obtained with a commercial 7th order semi-Gaussian Tennelec Tc244 shaping amplifier. For the same detector and set-up, better performance has been measured with SFERA compared to the commercial shaper. It is worth noting that the slightly better performance of the Tennelec SA at short shaping times (below 2 μs in this case) is due to the semi-Gaussian 7th order filter response, which indeed exhibits a better noise filtering behaviour at short t_P.

2) 3×3 SDD-Array: The 3×3 SDD-arrays employed for the measurements have already been successfully integrated in a monolithic scintillator-based γ-ray detection module targeting astronomy applications [16], as well as in preliminary X-ray spectroscopy measurements in view of the SIDDHARTA experiment [17]. Their single units feature

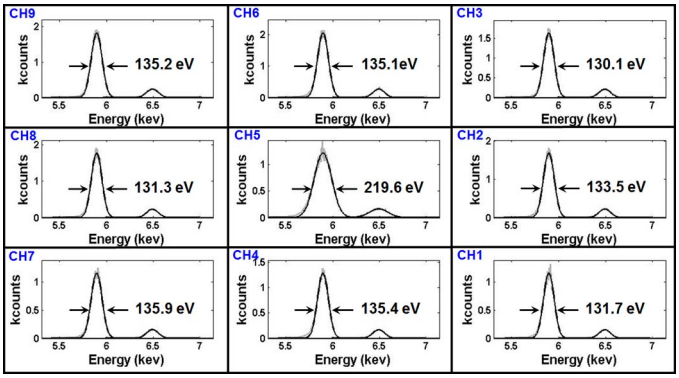

Fig. 14. Energy spectra of a 3×3 SDD matrix at -35 °C and 4 μs peaking time.

TABLE I

ENERGY RESOLUTIONS, EXPRESSED IN TERMS OF eV FWHM ON THE ^{55}Fe MN-K$_\alpha$ SPECTRAL LINE, OF THE 3×3 SDD MATRIX AT -35 °C FOR 3,4 AND 6 μs PEAKING TIME

Channel	Leakage current [pA]	Mn-K$_\alpha$ FWHM		
		t_P = 3 μs	t_P = 4 μs	t_P = 6 μs
1	0.27	134.3	131.7	134.6
2	0.39	134.3	133.5	134.7
3	0.27	132.5	130.1	132.1
4	0.25	139.1	135.4	138.6
5	20.3	205.8	219.6	205.7
6	0.3	130.3	135.1	130.8
7	0.94	131.3	135.9	131.3
8	0.6	133.8	131.3	132.4
9	1.7	138.9	135.2	136.9

an area of 8×8 mm^2 and a leakage current approximately between 1 and 2 nA/cm^2 at room temperature. These experimental measurements had the dual purpose of validating the ASIC proper operation with a fully functional matrix and verifying any possible improvement compared to the previous electronic solutions reading out such arrays [17]. Good spectroscopic results have been obtained from a fully functional matrix, which are presented in Fig. 14 for the 4 μs peaking time and summarized in Table I for the 3, 4 and 6 μs t_P, together with the measured leakage currents for each single unit.

Because of the higher leakage technology, the energy resolutions of these detectors are not as low as the ones measured with the low-leakage single SDD presented above (different area as well), although these results are, to date, the best achieved with such matrices [16].

Seven-on-nine channels exhibit a leakage current well below 1 pA, deduced from the CUBE output voltage slope with no incoming photons. These values are consistent with the theoretical estimations at -35 °C, also below 1 pA (with the exception of channel 5), obtained from the measured leakage at ambient temperature. *CH*5 presented instead a leakage current which did not properly scale down as the temperature was reduced. It indeed settled to 20 pA at -35 °C, that is more than an order of magnitude higher than that of the other channels, resulting in an energy resolution slightly above 200 eV FWHM for the measured peaking times.

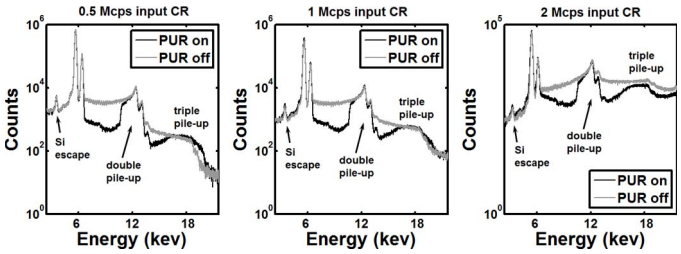

Fig. 15. Output energy spectrum with and without pile-up rejection in the case of pulsing the ASIC, operated at the shortest 500 ns peaking time, with the emulated signals of an ^{55}Fe X-ray source, at 0.5 (left), 1 (center) and 2 Mcps input count-rate (right).

The optimum t_P for the matrix under test and at -35 °C is 4 μs, with the best energy resolution of 130.1 eV FWHM on the Mn-K$_\alpha$ energy line (ENC of 6.2 e^-_{rms}) measured on array channel 3.

Finally, although SFERA has achieved the goal of processing the signals coming from a fully functional matrix, even better performance have been achieved with these FBK 3×3 SDD-arrays, in a matrix with eight out of nine working channels. Indeed, energy resolutions of 127.2 and 127.9 eV FWHM on the Mn-K$_\alpha$ line have been measured on two different units at 6 μs peaking time, confirming the excellent noise performance achievable with SFERA coupled to CUBE and to SDD matrices.

C. High-Throughput Measurements

The proper operation and efficiency of the PUR logic have been specifically addressed. The maximum input photons rate achievable with ^{55}Fe X-ray sources available in the laboratory was limited to 250 kcps, not sufficient to explore the maximum throughput available with SFERA. For this reason, a digital detector emulator (DDE) DT5800D by Nuclear Instruments [18] has been employed. This instrument allowed SFERA to be pulsed with an emulated ^{55}Fe X-ray spectrum as provided directly at the output of the preamplifier, with a rate up to 2 Mcps, and therefore represented a useful tool for the PUR experimental characterization. Fig. 15 shows the spectra acquired with SFERA operated at the shortest 500 ns peaking time with and without the PUR logic enabled and pulsing the input node with the emulated ^{55}Fe signals at 0.5, 1 and 2 Mcps respectively. For the sake of graphical representation, in order to visualize also double and triple pile-up lines, the chosen gain is the 10000 e^-. The spurious lines at double and triple the Mn-K$_\alpha$ and K$_\beta$ energies are still present in the spectrum and, in particular, the ones associated to the double pile-up are made of three different peaks, that occur approximately at 11.8 keV (K$_\alpha$ + K$_\alpha$, which is the most likely one), 12.4 keV (K$_\alpha$ + K$_\beta$) and 13 keV (K$_\beta$ + K$_\beta$, the less likely, thus with less counts). The effect of the PUR action is rather evident at the three counting rate conditions. Out of these pile-up spectral regions, the PUR mechanism efficiency is still evident, despite its slight worsening at 2 Mcps input count-rate.

Using the same emulator, the throughput capabilities of the ASIC have been measured at different input count rates, always with the PUR active. Fig. 16 shows the input-output count-rate characteristic of SFERA for each of the different

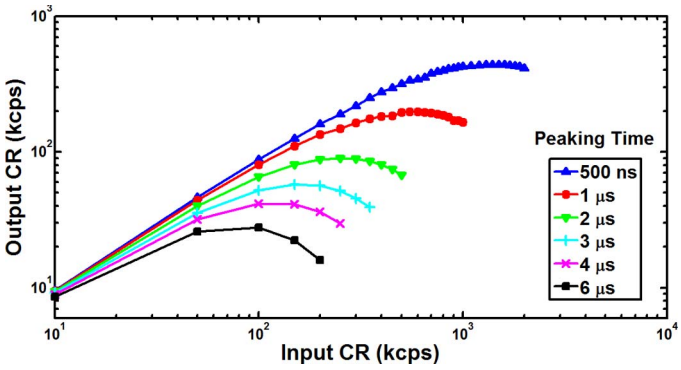

Fig. 16. Output versus input count-rate pulsing the ASIC with the emulated signals of an ^{55}Fe source for all the different peaking times.

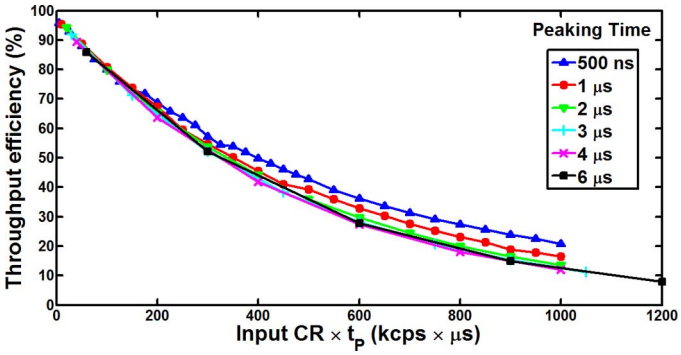

Fig. 17. Throughput efficiency for all the different peaking times.

peaking times, where the input rate is programmed through the DDE and the output rate is estimated by normalizing the spectrum integral count with respect to the acquisition time. The maximum output count-rate SFERA is able to provide at 0.5 μs peaking time is about 438 kcps at 1.5 Mcps input count-rate.

From these characteristic curves, a figure-of-merit that quantifies the ASIC throughput logic efficiency can be conveniently defined as the ratio between output and input count-rates, and its trend is presented in Fig. 17, where the input count-rate is normalized by multiplying for the peaking time. A very good efficiency, for an analog processing circuit, of 42% has been measured at 1 Mcps for the shortest 500 ns peaking time, which is approximately halved up to 2 Mcps.

Due to the significantly high output noise power of the DDE, which did not allow us to perform energy resolution measurements, a specific high-rate spectroscopic characterization of SFERA must be made in the future by making use of more active ^{55}Fe X-ray sources or an X-ray tube. Nonetheless, the use of the DDE still has provided some important preliminary information about the enlargement of the emulated spectral lines when increasing the input count-rate. A FWHM increase of the ^{55}Fe Mn-K$_\alpha$ line of about 3.5% from 10 kcps to 1 Mcps and 9% from 10 kcps to 2 Mcps have been measured.

IV. The On-Chip 12-Bit SAR ADC

A. Introduction

A 12-bit successive-approximation-register ADC has been integrated in SFERA. It is a revision of the work presented

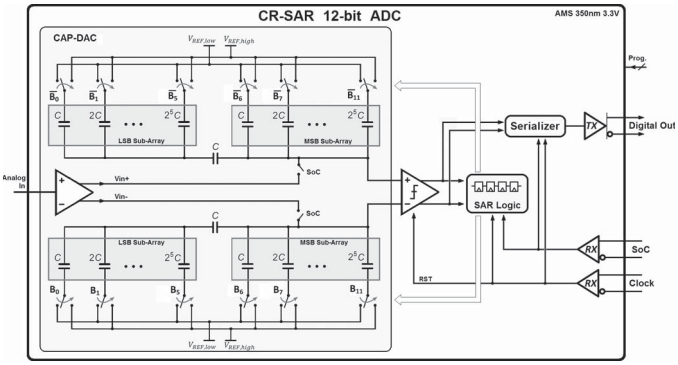

Fig. 18. Schematic diagram of the implemented 12-bit charge-redistribution BCA-based SAR ADC.

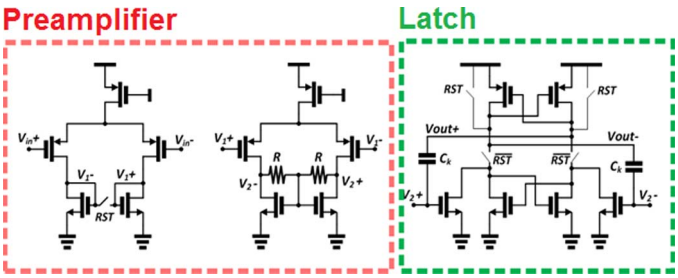

Fig. 19. Comparator simplified schematic diagram.

in [19], where modifications in the digital output serializer have been made to ease the communication with the external DAQ. When implemented in a multichannel readout ASIC, as in this work, such an ADC might represent a valid alternative to external data converters when designing low-power and compact detection modules or when operating in environments with strong electromagnetic interference, such as for instance synchrotron facilities. The block diagram of the circuit is shown in Fig. 18, which highlights the three main sub-circuits of any SAR ADC, namely the comparator, SAR logic and feedback DAC.

The chosen architecture is the charge-redistribution with bridge-capacitor-array (BCA) [20], being the one that features the smallest input capacitance for the same capacitive DAC (CAP-DAC) area. The bottom-plate switching algorithm employed is the *monotonic* because it simplifies the SAR logic design and exhibits the highest power efficiency [21]. A fully-differential topology has been adopted to minimize the influence of common-mode noise and disturbances from the power supply.

B. Comparator

The comparator architecture is presented in the schematic diagram of Fig. 19.

Given that the power consumption does not represent a stringent design constraint and, in contrast to the vast majority of SAR ADCs, whose comparators typically comprise a single dynamic-latch only, the latch stage of the proposed implementation is preceded by two time-continuous low-gain, low-offset preamplifiers. The latter are realized as simple single-stage amplifiers with a p-type input MOS pair to accommodate the

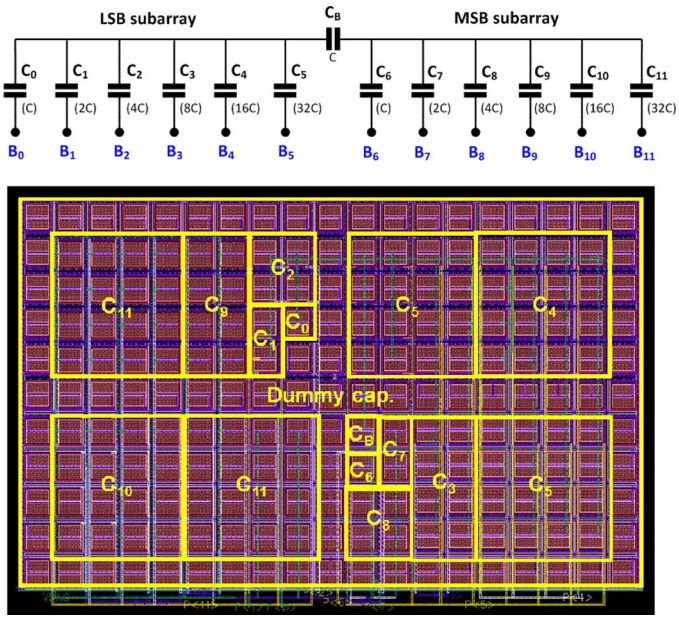

Fig. 20. Schematic diagram of the 12-bit bridge-capacitor capacitive DAC and physical layout implementation.

decrease of the common-mode voltage along the conversion. Their DC gain and GBWP are approximately 20 dB and 620 kHz respectively. The dual task they accomplish is to mitigate the dynamic-latch offset, of about 20 mV_{rms} for this implementation, and to prevent any kick-back noise injection on the CAP-DAC top-plates without significantly sacrificing the comparison delay. The latter effect is further reduced by using a couple of cross-capacitors connected between the input and the output with the same polarity of the latch [22]. Simulated performance of the comparator shows an input-referred offset of 4.5 mV_{rms} and a maximum comparison delay of 3.5 ns.

C. Capacitive DAC

Ultimately, the most critical block of the overall ADC is undoubtedly the capacitive feedback DAC, since the nonlinearities of the whole converter depend mainly on this block. For this reason, in the absence of any digital calibration algorithm, particular care must be devoted both to properly sizing the unit capacitance (to ensure monotonicity of the input-output static characteristic), which has been set to 140 fF, and to the design of the physical layout. The geometrical arrangement adopted for the latter is a common-centroid configuration so as to cope in principle with process oxide spreads. Fig. 20 shows the schematic diagram of the implemented 12-bit BCA-based CAP-DAC as well as the physical layout.

Apart from the arrangement of the individual capacitors, considerable efforts have been spent on making negligible (tens of aF) all of the stray capacitances between the bottom plates of the capacitors of one sub-array and the top-plate of the other (sometimes referred in literature as *cross-parasitics*), mainly arising from metal path overlaps and fringe effects, because of the strong impact they have on the CAP-DAC linearity.

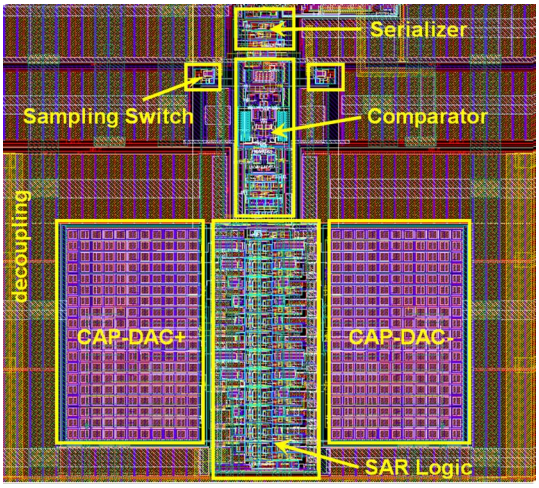

Fig. 21. Layout of the implemented 12-bit SAR ADC.

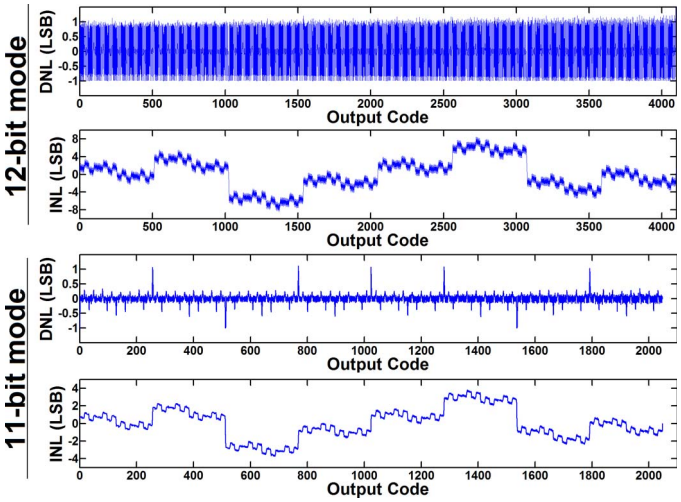

Fig. 22. Differential (DNL) and integral (INL) nonlinearity characteristics.

Finally, the layout of the complete SAR ADC is presented in Fig. 21. A bank of CMOS capacitors, surrounding the converter, has also been implemented to provide enough bias decoupling for the voltage references and power supply. The ADC area occupancy is 0.42 mm^2, which almost doubles when the decoupling capacitors are also taken into accounts.

D. Measured Results

For what concerns the electrical measurements, both static and dynamic parameters have been characterized with the aid of a 16-bit D/A converter which is hosted on a dedicated section of the motherboard PCB. While controlled by the NI-FlexRIO FPGA module of the DAQ, such a DAC allows the application of custom analog signals at the input pin of the SAR ADC.

The static parameters, namely differential (DNL) and integral nonlinearity (INL), are presented in Fig. 22 for both 12 and 11-bit operation, showing a DNL of $-1/+1.1$ LSB and $-0.8/+1$ LSB when operating the converter at 12 and 11-bit respectively while an INL of $-8/+8$ LSB and $-3.9/+4$ has

TABLE II
PERFORMANCE COMPARISON WITH OTHER STATE-OF-THE-ART ADCS IN NUCLEAR ELECTRONICS APPLICATIONS

	[23]	[24]	[25]	[26]	[27]	[28]	[29]	[30]	[31]	[32]	**This work**
Architecture	Wilkinson	Wilkinson	Wilkinson	Pipeline	Pipeline	Pipeline	Pipeline	SAR	SAR	SAR	SAR
Process	0.35 μm	0.35 μm	130 nm	0.35 μm	0.35 μm	130 nm	65 nm	0.25 μm	40 nm	65 nm	0.35 μm
Resolution	10-bit	12-bit	8-bit	10-bit	12-bit	12-bit	10-bit	10-bit	12-bit	10-bit	12-bit
Speed [MS/s]	$>$ 0.005	1.28	6.25	0.4	25	40	50	1	160	2	4.5
DNL [LSB]	+0.5/-0.5	+0.75/-0.75	+0.4/-0.4	+1.2/-1.2	+1.2/-1	-	-	+0.6/-0.6	-	+0.7/-1	+0.9/-0.8
INL [LSB]	+0.6/-0.6	+0.5/-0.5	+0.5/-0.5	+2.5/-2.5	+8/-8	-	-	+0.6/-0.3	-	+2.5/-3.2	+3.9/-3.9
ENOB [bit]	-	9	-	8.9	9.1	9	8	-	10.9	9.05	10.75
Power [mW]	0.4	3	0.6	14	37	15	12	-	6.1	0.09	19
Area [mm^2]	0.25×0.25	-	0.13×0.14	2.24	1.7×0.6	-	0.8	0.4×0.4	-	0.0072	0.7×0.6

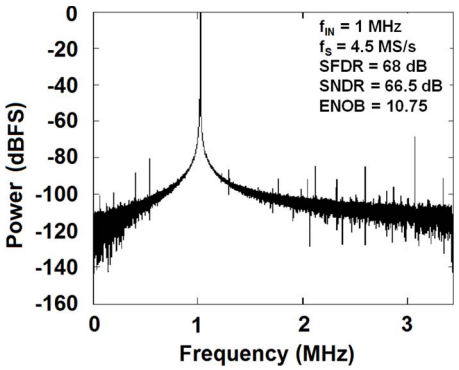

Fig. 23. Output spectrum of a 2 V_{pp} amplitude 1.02 MHz input sinusoid sampled at 4.5 MS/s.

been measured at 12 and 11-bit operation. Dynamic parameters are summarized in the graph of Fig. 23, showing the frequency spectrum of a converted 1 MHz input full-scale sine wave sampled at 4.5 MS/s.

Although the ENOB specification has been satisfied, achieving an effective resolution of 10.75-bit, it is worth noting that the circuit presents a few impairments (in the form of missing codes in the 12-bit operation). They arise from residual cross parasitics, inducing deterministic errors, and from a possible radial oxide gradient against which the common-centroid CAP-DAC layout would not be immune (statistical mismatch). Both of these causes of nonlinearity can be addressed in a further revision of the converter at the physical layout level. However, while the former can easily be corrected by means of a better routing and shielding of the metal traces connected to the top and bottom of the CAP-DAC capacitors, the latter would require deeper changes, such as a novel design of the single capacitive array.

A performance comparison among the state-of-the-art A/D converters employed in nuclear electronics applications is presented in Table II. Despite the aforementioned linearity impairments, the proposed SAR ADC still achieves a competitive resolution compared to the other published ADCs, thus spurring the interest in a future revision of the circuit.

Concerning the digital crosstalk between the ADC and SFERA analog channels, which is potentially harmful for the spectroscopic performance of the ASIC, the switching noise coming from the converter has been addressed from a physical layout perspective, with the aim of reducing the parasitic coupling of disturbances through the substrate. Several isolation guard rings have indeed been used and, moreover, the power and ground domains of ADC and readout channels are properly split. Analog and digital signals and power lines never overlap throughout the chip while almost 1 nF of decoupling capacitance has been integrated to provide enough filtering of the ADC voltage references. During the spectroscopic measurements, we have not observed any performance degradation due to the switching activity of the on-chip A/D converter.

In conclusion, the described quantizer therefore represents a good candidate as the digitizer to be integrated in multichannel readout ASICs for applications requiring less that 11-bit resolution up to 5 MS/s sampling speed. We recall that the purpose of the ADC in our ASIC is the direct digitization of the multiplexed analog data.

V. CONCLUSIONS

This work presented SFERA, a fully-programmable multichannel readout IC for solid state detectors intended to be coupled to CMOS preamplifiers. Thanks to its state-of-the-art noise performance, the SDD has been outlined as the reference device for the design and characterization, although the use of the chip can be extended to other types of detectors. SFERA features 6 different peaking times, ranging from 0.5 to 6 μs and 5 gains to accommodate a wide input energy range. It integrates a 9th order analog semi-Gaussian shaper and high-efficiency pile-up rejection logic. Depending on the target application, whether it is X- or γ -ray detection, three different data multiplexing protocols may be employed. Data can be on-chip digitized by the embedded 12-bit SAR ADC, which exhibits an effective resolution of 10.75-bit. The spectroscopic characterization of the ASIC has shown an excellent energy resolution of 122.1 eV FWHM on the Mn-K_α line of an ^{55}Fe X-ray source, equivalent to 3.2 e^-_{rms}, using a 10 mm^2 SDD cooled at -35 °C. Good spectroscopy performances, in comparison with previous ASICs, have also been achieved with 3×3 SDD-arrays (8×8 mm^2 single units). High-rate measurements have highlighted the adequacy of SFERA also in high-rate applications, showing a PUR throughput efficiency of 42% at 500 ns peaking time and 1 Mcps input count rate, without a significant deterioration in resolution.

The ASIC presented in this work, thanks to its full programmability and performance, may represent a versatile solution

for the readout of both X- and γ-ray spectroscopy and imaging detectors.

ACKNOWLEDGMENT

The authors would like to thank C. Piemonte and N. Zorzi from Fondazione Bruno Kessler for providing the SDDs used in the experimental measurements. The authors would also like to thank Dr. A. D. Butt and Dr. I. Mulholland for their technical support.

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