The read-out and data transmission for the MAGNEX focal plane detector for the NUMEN project

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The read-out and data transmission for the MAGNEX focal plane detector for the NUMEN project.

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Abstract. The main task of the read-out electronics for the new NUMEN focal plane detector (FPD) is the real-time data collection from the front-end ASICs and the high bandwidth transmission to data acquisition, in addition to the slow control of the front-end electronics and the synchronization of the whole detector. The read-out electronics architecture, designed to be modular and expandable to the final size of the detectors, is based on System On Module (SOM). This very versatile device couples high performance FPGA to powerful processor architecture and allows a graphical approach to the programming and interfacing. A detailed description of the architecture and the specifications of the read-out electronics are presented.

1. Introduction

With the ongoing upgrades of the cyclotron accelerator [1] at INFN Laboratori Nazionali del Sud (LNS) foreseen for the NUMEN project [2, 3, 4], an upgrade of the FPD [5] of the MAGNEX spectrometer [6, 7, 8] will be necessary. It includes the design of new front-end (FE) and read-out (RO) electronics, able to couple with the increased event rate (up to 10MHz in the NUMEN experiments). The Segmented anode and the FE electronics were totally redesigned with a solution that includes the VMM3 chip [9]. This solution led to the development of a totally digital RO based on System On Module (SOM) by National Instruments [10].

2. FE-RO Architecture

The main idea for the design of the electronics of the new FPD is the use of the same architecture of FE and RO (Figure 1) both for the tracker and the Particles Identification Detector (PID) wall. This choice allows an easier syncronization of the detectors, the uniformity of the data format, a contained software development as well as the reduction of the costs. The requirements for such system are: readout of about 1400 channels for the tracker and 4000 channels for the PID-wall, capability to handle a foreseen event rate of 100 kHz/cm, modularity, scalability, and radiation hardness. The architecture is based on a replica of the same module shown in Figure 2. Each module is equipped with a variable number of VMM3 chips according to the number of

the corresponding channels to be read-out. These chips are read-out by an FPGA based system manufactured by National Instruments (SOM). A single SOM has 160 General Purpose Input Output pin (GPIO) that could be used, appropriately configured, for data read-out, slow control and communication ports. Taking into account the GPIOs required for slow control and for an additional Gigabit Ethernet connection, a SOM would be able to manage and read-out the data of 10 VMM chips. In particular for the tracker, if we keep in mind that the pitch of the strip of the segmented anode is 0.75 mm, and that a VMM reads 64 strip, each SOM should transfer data with a bandwidth of about 3 Gb/s, at the highest event-rate foreseen for the experiment. So the final number of VMM chips coupled to a SOM will be a compromise between the best bandwidth used by two Gigabit Ethernet connections, available in the SOM, and the possibility to design an unique kind of board for the front-end of each detector in the experiment.

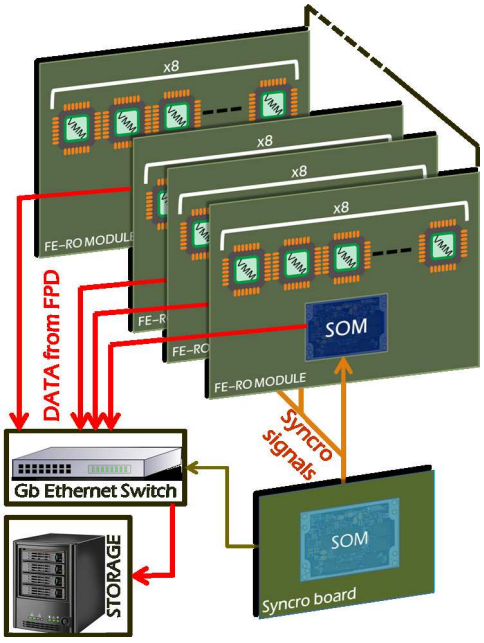

Figure 1. FE-RO architecture.

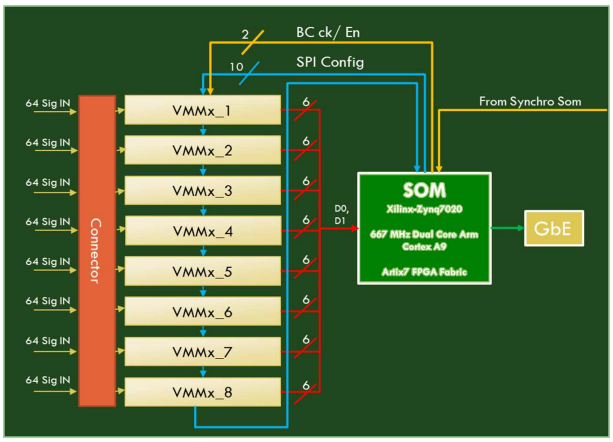

Figure 2. FE-RO module.

3. System on Module (SOM)

The System on Module (SOM) is a very compact, flexible, reliable, high-performance, industrial-grade, deployment-ready embedded computer. It combines a 667 MHz Dual-Core ARM Cortex-A9 processor, NI Linux Real-Time OS and an Artix-7 programmable Xilinx FPGA. A functional block diagram of the SOM is presented in figure 3. Both the real-time processor, whose main functions are communication and signal processing, and the FPGA, usefull to implement high-speed controls, custom timings and triggering, can be programmed with LabVIEW, allowing a very short development time, and a high debugging capacity [11]. In addition, the processor allows to run any application developed for linux-based operative system. Through a single high-density connector, it is possible to access lines dedicated to the main communication standards managed by the processor, as well as 160 digital I / O lines managed directly at the FPGA level: 16 Single-Ended 3.3 V and 144 configurable also as 72 differentials. This powerful combination of resources in a single system allows the management of the slow control of front-end ASICs, the read-out of data and their transfer, through a standard ethernet protocol, towards the system of storage. The SOM is also able to generate and distribute, with a very low skew, all the clock signals necessary for the correct functioning of the apparatus. The computational resources of

this system would also allow to implement triggering and filtering strategies in the case it is necessary to reduce the data bandwidth at larger event rate. Radiation tolerance tests were also conducted at the University of Sao Paulo, in the Nuclear and Energy Research Institute (IPEN) reactor. Although data analysis is still in progress, the tests have demostrated that the SOM, exposed to a neutron flux (from 10^4 to 10^6 n/cm^2*s) well above that estimated by the simulations for the NUMEN experiment, at maximum beam intensity, is subject to some effects (single event upset) recoverable by a system reset operation. Due to the flexibility of the system and its described features, its application as read-out electronics for all the spectrometer detectors is promising and reliable.

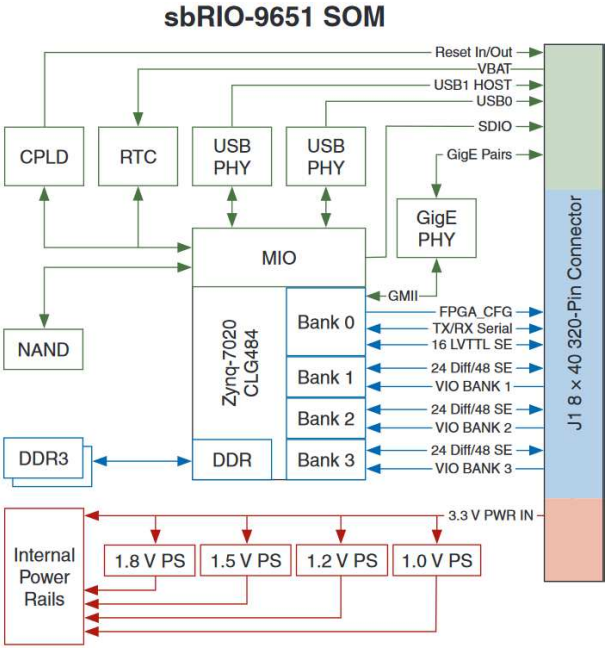

Figure 3. Functional block diagram of the SOM (Courtesy by National Instruments).

4. Status

The developers of the chip sent us a complete system to testing and studying the second version of the chip (VMM2). When all the features that could be of interest for the experiment were investigated and verified, was developed a new read-out board equipped with a SOM that allowed, coupled with the original front-end board, to test the control and the communication between the SOM and the chip. Then was developed a front-end board with VMM2 useful to study the coupling between the whole acquisition system (composed by front-end and read-out custom boards) and some detector prototypes intended to use in the experiment. Meanwhile a new version of the chip (VMM3) was available and the front-end board was upgraded with a new design that is now under construction.

References

[1] Calabretta L *et al.* 2017 *Modern Physics Letters A* **32** 1740009
[2] Cappuzzello F *et al.* 2015 *Journal of Physics: Conference Series* **630** 012018
[3] Agodi C *et al.* 2015 *Nuclear and Particle Physics Proceedings* **265-266** 28 – 30 ISSN 2405-6014 proceedings of the Neutrino Oscillation Workshop
[4] Cappuzzello F *et al.* 2018 *The European Physical Journal A* **54** 72

[5] Cavallaro M *et al.* 2012 *The European Physical Journal A* **48** 59 ISSN 1434-601X
[6] Cappuzzello F *et al.* 2016 *The European Physical Journal A* **52** 167 ISSN 1434-601X
[7] Cappuzzello F *et al.* 2014 *Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment* **763** 314 – 319 ISSN 0168-9002
[8] Cunsolo A *et al.* 2007 *The European Physical Journal Special Topics* **150** 343–346
[9] De Geronimo *et al.* 2013 *IEEE Trans.Nucl.Sci.* **60** 2314–2321
[10] URL `http://www.ni.com/pdf/manuals/376962c.pdf`
[11] URL `http://www.ni.com/white-paper/6983/en/`