Available online at www.sciencedirect.com

ScienceDirect

Materials Today: Proceedings 4 (2017) 5045–5052

materialstoday: PROCEEDINGS

www.elsevier.com/locate/procedia

13th International Conference on Nanosciences & Nanotechnologies & 9th International Symposium on Flexible Organic Electronics

# Interface Trap State Characterization of Metal-Insulator-Semiconductor Structures Based on Photosensitive Organic Materials☆

E. Bezzeccheri[a,*], A. Femia[a], R. Liguori[a], A. Rubino[a]

[a]*Department of Industrial Engineering, University of Salerno, Via Giovanni Paolo II 132, 84084, Fisciano (SA), Italy*

**Abstract**

Flexible organic and printed electronics has led in the last years to exciting applications, especially for what concerns devices incorporating photosensitive materials. Among the latter, organic field-effect phototransistors are a promising technology because of the high light-sensitivity and the possibility of being integrated within more complex systems. Nevertheless, their optimization has not been thoroughly investigated and considerable variations are often observed in their behavior. In this framework, the most critical aspect is represented by the interface formed between the organic semiconductor and the employed dielectric layer. In our contribution, we have fabricated metal-insulator-semiconductor (MIS) structures based on the archetypal photosensitive organic materials poly(3-hexylthiophene) (P3HT) and [6,6]-phenyl C61-butyric acid methyl ester ($PC_{61}BM$) on Silicon/$SiO_2$ substrates, exploiting their blend in a bulk heterojunction configuration. The MIS structures have been characterized by means of admittance spectroscopy to study the properties of the trap distribution at the interface between the organic semiconductors and the silicon oxide insulating layer. The complex behavior of the capacitance and loss diagrams has been interpreted with a simple electrical model to extract the density of the traps at the interface between the insulator and the semiconductor. It is shown that in the blend-based MIS device several peaks arise in the loss diagram with respect to the only P3HT MIS device. This could be attributed to a different interaction between the single species in the bulk heterojunction and the silicon oxide layer. Furthermore, the reported values of trap densities result in the range of those determined for analogous structures and materials.

*Keywords:* organic electronics; phototransistor; P3HT; PCBM; bulk heterojunction; admittance spectroscopy.



* Corresponding author. Tel.: +39089964453

*E-mail address:* ebezzeccheri@unisa.it



Selection and peer-review under responsibility of the Conference Committee Members of NANOTEXNOLOGY2016 (13th International Conference on Nanosciences & Nanotechnologies & 9th International Symposium on Flexible Organic Electronics).

## 1. Introduction

Over the last decade, organic electronics has shifted its focus from the study of basic material properties to the exploitation of complex system architectures. In this regard, one promising technology concerns the realization of optoelectronic devices, with particular consideration to the solution processing of the materials [1-5]. Focusing on light-sensitive detectors [6], exciting applications have been successfully demonstrated exploiting the conformal features and biocompatibility of photosensitive organic semiconductors, as the realization of near infrared detectors [7] and of prosthetic apparel to restore sensitivity in the retina of blind rats [8]. Such multifaceted systems rely on the exploitation of organic photodiodes and phototransistors, among which the latter have been proven to possess high light-sensitivity and the design flexibility to be employed in a number of applications. For instance, organic phototransistors with performance comparable or superior with respect to the conventional planar structures can be realized in vertical fashion [9], which provides better process integration with other organic electronics devices.

Nevertheless, the realization of reliable systems to be employed in commercial applications is subordinate to a full device optimization. In this regard, in organic field-effect phototransistors it is crucial to study the properties of the insulator/semiconductor interface, since trap levels at this particular device site are often responsible for transport degradation [10], which in turn negatively affects the photogenerated charge extraction [11-13]. In the characterization of trap states and carrier lifetimes several transient and frequency domain techniques have been employed, such as Open Circuit Voltage Decay (OCVD) [14], Deep Level Transient Spectroscopy (DLTS) [15] and admittance spectroscopy [26-28].

In this work, the admittance spectroscopy method has been applied to investigate the interface properties of organic field-effect phototransistors based on poly(3-hexylthiophene) (P3HT) and [6,6]-phenyl C61-butyric acid methyl ester ($PC_{61}BM$), comparing a bulk heterojunction device [16,17] to a neat P3HT device. An analogous technique have been applied in [18] to probe the increased photoresponse of P3HT:$PC_{61}BM$ with respect to P3HT. However, this method has not been applied to our knowledge to characterize the interface traps of bulk heterojunction organic field-effect phototransistors.

In particular, we have measured the admittance of the devices at various electrical biases, for frequencies between 20 Hz and 2 MHz. The behavior of the real and imaginary part diagrams has been described with a simple electrical model relying on a resistor-capacitor (RC) equivalent circuit. The interface behavior has been associated to a Fermi level pinning regime and trap densities have been extracted, resulting in the order of $10^{10}$ $cm^{-2}$ $eV^{-1}$. Moreover, the loss diagram of the P3HT:$PC_{61}BM$ device shows an additional peak with respect to the neat P3HT device, which could be allegedly associated to a different interaction between the single species in the bulk heterojunction and the silicon oxide layer. These considerations are further supported by comparison with the admittance spectrum of a plain $PC_{61}BM$ device, as discussed at the end of section 3.

## 2. Materials and methods

The phototransistors were realized in a bottom-gate top-contact configuration on thermally oxidized p-type Silicon substrates (electrical resistivity of 0.001 Ω cm), with nominal Silicon Oxide thickness of 300 nm (Ossila). The substrates, onto which the semiconductors were spin-coated, served as gate contact and insulator. The source and drain electrodes were realized in Au by thermal evaporation deposition through a shadow mask. The channel geometry was interdigitated with form factor *W/L* of 360 and the total contact area (source plus drain) was of 2.5 $mm^2$.

The device processing was performed in a class 100 clean room. Prior to semiconductor deposition, the substrates were cleaned with a standard procedure comprising ultrasonic cleaning in Isopropyl alcohol and Acetone. In addition, an UV-$O_3$ sterilization was performed before the last Isopropyl alcohol cleansing step. The P3HT and P3HT:$PC_{61}BM$ (Sigma-Aldrich) solutions were prepared in ortho-Dichlorobenzene with concentrations of 1:100 %wt and 1:1:100 %wt, respectively. The solutions were stirred for 2 hours on a hot plate at 60° C and filtered before utilization. The deposition of the semiconductors occurred on the cleaned substrates at 2000 rpm for 60 seconds, with an acceleration ramp of 5 seconds.

Morphology analysis of the resulting films were performed with a stylus profilometer (KLA-Tencor P-6). The resultant thicknesses were of 30±3 nm for P3HT and 69±6 nm for P3HT:$PC_{61}BM$ bulk heterojunction. In addition,

the average roughness and waviness were around 27±5 Å and 6±2 Å respectively, as measured on a scan domain of 400 µm. The devices were completed by the deposition of the source and drain contacts from a base pressure of $4 \cdot 10^{-7}$ mbar at an evaporation rate of 0.15 nm $s^{-1}$. The resulting Au thickness was of 46 nm. The samples were held in vacuum until the electrical characterization was performed.

The admittance of the metal-insulator-semiconductor (MIS) diode formed between the gate and the source contacts was evaluated with an LCR meter (Agilent 4980A) for gate biases between -40 V and 40 V, considering a sinusoidal excitation of 100 mV. All measurements were performed at ambient temperature, in ambient air and under dark conditions.

## 3. Results and discussion

Admittance spectroscopy consists in measuring the small-signal steady-state parallel admittance of a given device varying the excitation frequency. The admittance $Y_P$ is often expressed in terms of the capacitance $C_P$ and loss $L_P$ functions, as in Equation (1), where $\omega$ is the angular frequency ($2\pi f$) and $i$ is the imaginary unit. The capacitance and loss functions for a Maxwell-Wagner relaxation process with time constant $\tau_0$ are reported in Equation (2) [19], where $q$ is the elementary charge, $A$ the device area and $D_S$ is the involved density of states per unit area and energy.

$$Y_P(\omega) = \omega L_P(\omega) + i\omega C_P(\omega) \tag{1}$$

$$C_P(\omega) = qAD_S \frac{1}{1+\left(\omega\tau_0\right)^2},\ L_P(\omega) = qAD_S \frac{\omega\tau_0}{1+\left(\omega\tau_0\right)^2} \tag{2}$$

According to Equation (2), the loss function appears to possess a peak located at $\omega\tau_0=1$ with magnitude $L_{max}$, which coincides with the capacitance value at the same radial frequency. In addition, the capacitance is subject to an inflection point at the frequency in which loss has its maximum.

The admittance spectra as measured in the P3HT and P3HT:$PC_{61}BM$ MIS diodes are shown in Figure 1 (scatter). A multiple peak behavior can be observed in the loss diagrams, where each peak can be associated to a particular relaxation process. The first peak of the P3HT diode is shown to depend in both frequency and magnitude on the applied gate bias, while the second possesses a voltage independent frequency and a magnitude with minor polarization effects.

The latter peak has been attributed to the parasitic contact resistance arising from the measurement setup and will not be taken into further consideration in the analysis of the device. Similarly, in the P3HT:$PC_{61}BM$ diode two peaks and a weak shoulder (peak #3) are visible. The low and middle frequencies peaks show a similar frequency and magnitude behavior on gate bias, while the shoulder moves below the middle peak for voltage going from positive to negative.

The admittance behavior of the two devices has been modeled with simple equivalent electrical circuits formed by RC branches, as shown in the insets of Figure 1c and Figure 1d. Each RC branch is associated to a peak in the loss diagram and the circuit time constant is chosen to match with the considered peak frequency ($RC=\tau_0$). In this context, the dispersion relations for the capacitance and loss spectra reported in Equation (2) arise from a series-parallel transformation of the RC branch. The admittance model curves are also visible in Figure 1 (solid lines) and the values of the electrical parameters used in their generation are listed in Table 1, for the various gate biases.

The parameters have been chosen to fit the peaks occurring in the loss diagrams and some discrepancies arise due to the model simplification. In particular, the low frequency dispersion of the curves is believed to be originated by parasitic effects due to a non-structured semiconductor layer [20]. Furthermore, the peak fit in the loss diagrams is inaccurate between consecutive peaks. This can be associated to a multiple time constant relaxation process, which is failed to be described by a Maxwell-Wagner relationship due to the broadening of the peaks [19].

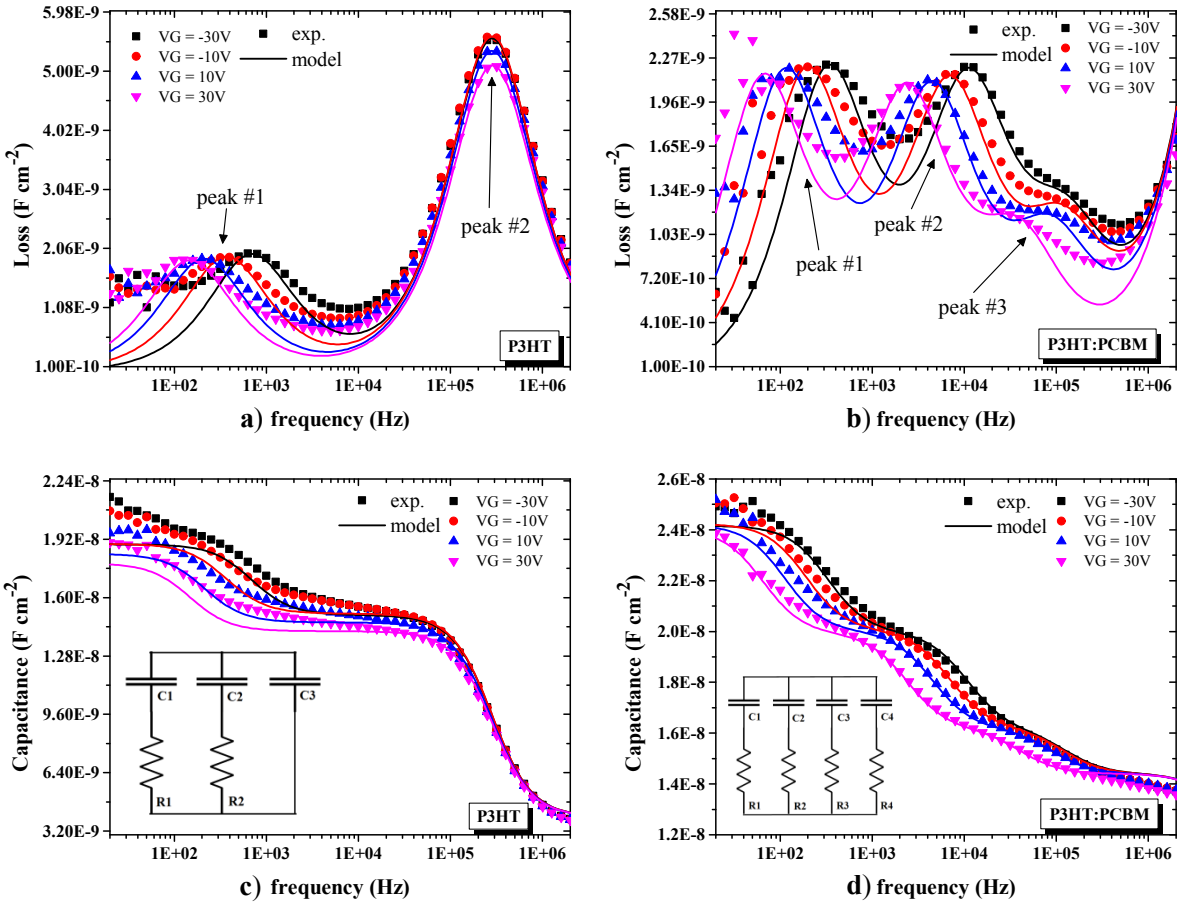


Fig. 1. Loss spectra of the (a) P3HT device and (b) P3HT:$PC_{61}BM$ device; capacitance spectra of the (c) P3HT device and (d) P3HT:$PC_{61}BM$ device, with the equivalent circuit reported in the inset. The data are normalized over a pad area of 1.25 $mm^2$, with both experimental (scatter) and electrical model (solid) curves shown. The different peaks are also highlighted in the loss spectra.

Table 1. The values of electrical parameters employed in the generation of the electrical model curves. The parameters not reported in the table have been considered constants. In particular, for P3HT $C_3$ has been fixed to 50 pF (base capacitance at high frequencies), while for the bulk heterojunction values of $R_4$ = 56.2 Ω and $C_4$ = 177 pF (base capacitance at high frequencies) have been employed.

| $V_G$ [V] | P3HT | | | | P3HT:$PC_{61}BM$ | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| | $R_1$ [MΩ] | $C_1$ [pF] | $R_2$ [kΩ] | $C_2$ [pF] | $R_1$ [MΩ] | $C_1$ [pF] | $R_2$ [MΩ] | $C_2$ [pF] | $R_3$ [kΩ] | $C_3$ [pF] |
| -30 | 4.8 | 48.5 | 4.1 | 138 | 9.2 | 52.5 | 0.30 | 48.0 | 56.9 | 21.5 |
| -10 | 9.0 | 47.8 | 4.0 | 139 | 15.8 | 52.5 | 0.47 | 48.0 | 58.9 | 22.5 |
| +10 | 1.6 | 47.0 | 4.2 | 133 | 27.1 | 52.5 | 0.74 | 47.8 | 79.7 | 22.2 |
| +30 | 2.3 | 46.5 | 4.4 | 127 | 47.2 | 51.3 | 1.41 | 47.0 | 176.4 | 22.0 |

Despite its simplicity, the RC circuit approach allows the estimation of some important material-related parameters. To this extent, the model has been used to extract the relaxation times $\tau_0$ for each peak in both devices. The results are reported against gate bias in (natural) logarithmic scale in Figure 2 (left axis). The peak #3 in the bulk heterojunction device can be attributed to the capacitance associated with the bulk of the semiconducting region [25], and will be of no further consideration in the insulator/semiconductor interface properties analysis. An

analogous peak is likely to occur in the P3HT device, but it does not appear in the loss spectrum due to the screening from the parasitic peak #2. On the other hand, the first peak of the P3HT MIS, as well as the first and second peaks of the P3HT:$PC_{61}BM$, are shown to follow an exponential law. This is likely to be related to a thermalization process such as charge trapping in energy gap states [21].

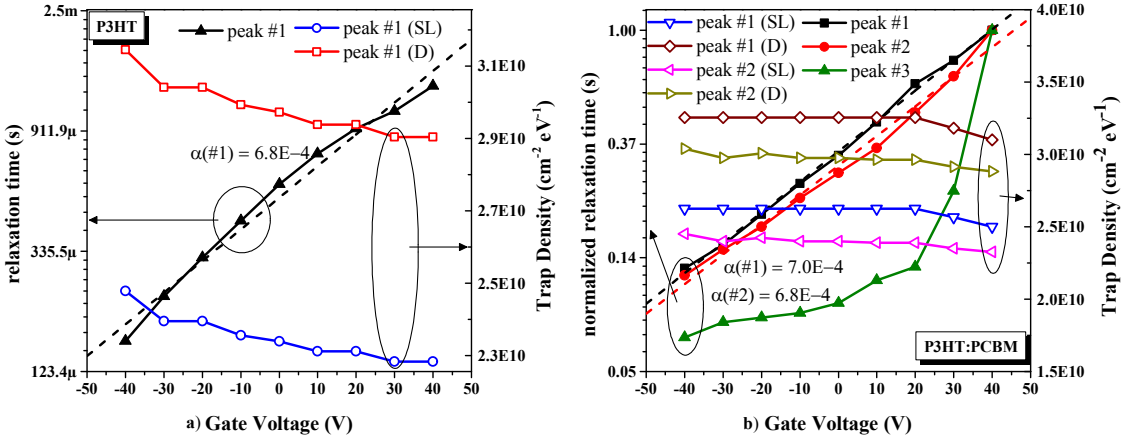


Fig. 2. Trap parameters for the (a) P3HT device and (b) P3HT:$PC_{61}BM$ device. The relaxation times (ln scale) are calculated as the inverse of the peak angular frequency. Except for peak #3, the peaks exponential relation upon voltage can be associated to a thermalization process. The relaxation times of the P3HT:$PC_{61}BM$ device are normalized to 3.2 ms (#1), 99.5 µs (#2) and 15.9 µs (#3). Trap density are reported for both single level (SL) and distribution (D), resulting in the order of $10^{10}$ $cm^{-2}$ $eV^{-1}$.

In this regard, it is worth noting that the slope of the $\tau_0$ curves is positive, indicating that the distance from the trap level to the conduction level is increasing with voltage. This is consistent to the picture of a valence band shifting down with respect to the Fermi level at the interface consequently to the application of a positive gate polarization (Figure 3). A fitting parameter $\alpha$ has been considered when taking into account the relationship between the band bending at the interface and the applied voltage ($\Delta E=\alpha V_{GS}$), since only part of the gate bias is responsible for the shift of the relative Fermi level position. The resulting values of $\alpha$ are very small (in the order of $10^{-3}$), indicating that only a minor part of the gate voltage is applied to the semiconductor interface, with a relative shift in the Fermi level energy in the order of meV. This could be ascribable to a Fermi level pinning regime, which is likely to be originated from the trapping effect at the interface [22,23].

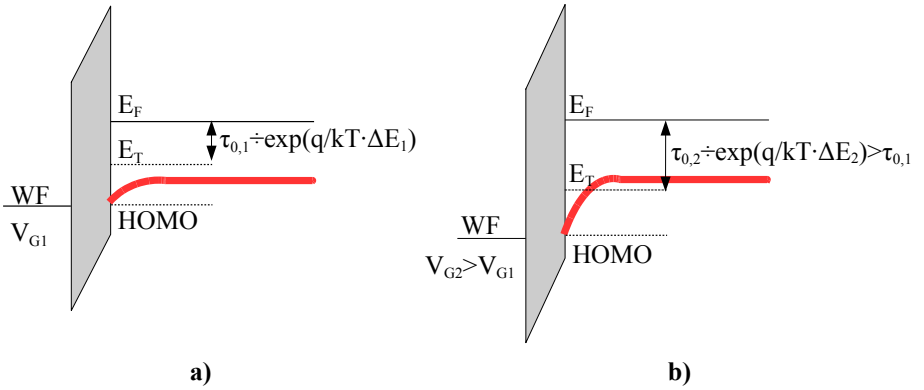


Fig. 3. The energy diagram at the insulator/semiconductor interface. In b) a higher gate voltage is applied with respect to a), which results in a higher relaxation lifetime. Here, $E_F$ is the Fermi level, $E_T$ the interface trap level (donor states) and $WF$ is the gate workfunction. The conduction level is the HOMO (red line), of which the interface level has been quoted.

The interface trap densities related to the first peak of the P3HT device and the first and second peaks of the P3HT:$PC_{61}BM$ device are also reported in Figure 2. These have been inferred after Nicollian and co-workers [24,25], who have given a thorough discussion on how to employ admittance spectroscopy to probe interface trap states in MIS structures. They show that in the case of a trap states energy distribution, the Maxwell-Wagner relationship of Equation (2) are modified as in Equation (3), where $L_{max}$ is located at $\omega\tau_0=1.98$.

$$C_P(\omega) = q^2 A D_S \frac{\tan^{-1}(\omega\tau_0)}{\omega\tau_0},\ L_P(\omega) = \frac{q^2 A D_S}{2} \frac{\ln\left[1+(\omega\tau_0)^2\right]}{\omega\tau_0} \tag{3}$$

$$D_S = \frac{2\beta L_{\max}}{q^2 A} \tag{4}$$

For both single level and distribution, the loss peak can be directly related to the trap density as in Equation (4), where the $\beta$ factor is equal to 1 for a single trap level and 1.24 for an energy distribution. In both cases, the values reported in Figure 2 have been calculated using the latter relationship. The trap state density have resulted in the order of $10^{10}$ $cm^{-2}$ $eV^{-1}$, which is consistent with the range reported in literature for several organic/organic and inorganic/organic interfaces [26-30]. In addition, it can be observed that trap densities are approximately constant with gate bias, which can be a further evidence of a Fermi level pinning regime, i.e. the trap distribution is probed only in a very thin interval of energies.

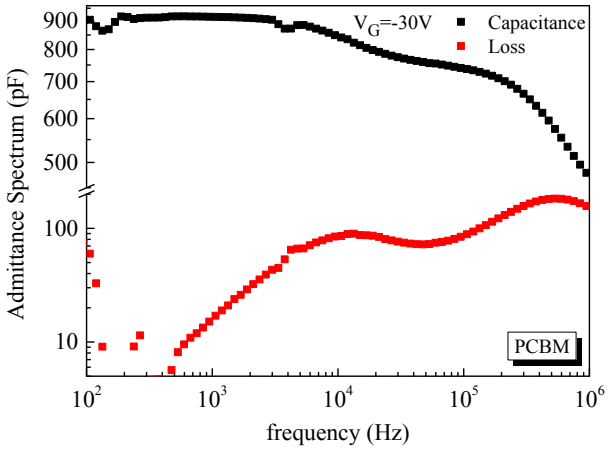


Fig. 4. Admittance spectrum of $PC_{61}BM$ devices. The peak arising at $10^4$ Hz can be considered of the same nature of peak #3 in the bulk heterojunction device.

The results previously reported show that an additional trap distribution is arising in the bulk heterojunction device with respect to the neat P3HT device, with trap states density comparable with that of the latter. This consideration is further supported by the admittance measurement of a plain $PC_{61}BM$, which is reported in Figure 4. As can be seen, a peak in the loss spectrum arise around $10^4$ Hz, similarly to peak #2 in the P3HT:$PC_{61}BM$ device, further confirming the presence of an additional trap distribution at the interface. The latter could be attributed to a different chemical interaction between the single species in the blend and the silicon oxide layer. Schafferans et al. [31] have experimentally reported that in P3HT:$PC_{61}BM$ solar cells an additional deep trap distribution arises with respect to the only-P3HT case. Furthermore, the P3HT:$PC_{61}BM$ traps are shown to increase in concentration upon oxygen exposure much faster than in neat P3HT. Their results can be explained considering that trap states

introduced by fullerene derivatives are preferential site for oxygen reactions to happen, as proposed recently [32]. The same mechanisms can be operative in devices such as bulk heterojunction phototransistors, considering the interface as preferential reaction site.

## 4. Conclusions

In this work, the admittance spectroscopy method has been applied to investigate the interface properties of organic field-effect phototransistors based on P3HT and $PC_{61}BM$. A comparison has been made between a bulk heterojunction device and an only-P3HT device. The admittance of the phototransistors has been characterized at various electrical biases and the behavior of the real and imaginary part diagrams has been described with an equivalent RC circuit. From the analysis of the peaks in the loss diagrams, the interface behavior has been associated to a Fermi level pinning regime and trap densities have been extracted, resulting in the order of $10^{10}$ $cm^{-2}$ $eV^{-1}$. The additional low-frequency peak arising in the loss diagram of the bulk heterojunction device has been associated to a different interaction between the single species in the bulk heterojunction and the silicon oxide layer. In particular, the trap states introduced by $PC_{61}BM$ could be preferential sites to oxygen reactions to happen, which is consistent with other reports on the subject.

## Acknowledgements

This work was partially supported by the SMARTAGS project (PON02_00556_3420580), financed by the Ministero dell'Istruzione, dell'Università e della Ricerca (MIUR) in the ambit of the National Operational Programme for Research and Competitiveness 2007-2013. The authors are also grateful to Aniello Falco (Technische Universität München) for the precious technological advices on the preparation and processing of the P3HT:$PC_{61}BM$ blend.

## References

[1] A. Abdellah, B. Fabel, P. Lugli, G. Scarpa, Org. Electron. 11 (2010) 1031–1038.
[2] A. Reale, L. La Notte, L. Salamandra, G. Polino, G. Susanna, T. M. Brown, F. Brunetti, A. Di Carlo, Energy Technol. 3 (2015) 385–406.
[3] D. Acierno, E. Amendola, S. Bellone, S. Concilio, L. Ferrara, P. Iannelli, H.-C. Neitzert, et al., J. Non-Cryst. Solids 338 (2004) 278–282.
[4] P. Vacca, M. G. Maglione, C. Minarini, G. Salzillo, E. Amendola, D. Della Sala, A. Rubino, Macromolecular Symp. 228 (2005) 263–272.
[5] H. Neitzert, M. Ferrara, A. Rubino, S. Concilio, P. Iannelli, P. Vacca, L. Ferrara, C. Minarini, J. Non-Cryst. Solids 352 (2006) 1695–1699.
[6] K.-J. Baeg, M. Binda, D. Natali, M. Caironi, Y.-Y. Noh, Adv. Mater. 25 (2013) 4267–4295.
[7] T. Rauch, M. Böberl, S. F. Tedde, J. Fürst, M. V. Kovalenko, G. Hesser, U. Lemmer, W. Heiss, O. Hayden, Nat. Photonics 3 (2009) 332–336.
[8] D. Ghezzi, M. R. Antognazza, R. Maccarone, S. Bellani, E. Lanzarini, N. Martino, M. Mete, et al., Nat. Photonics 7 (2013) 400–406.
[9] E. Bezzeccheri, S. Colasanti, A. Falco, R. Liguori, A. Rubino, P. Lugli, AIP Conf. Proc. 1736 (2016) 020084.
[10] H. Ma, H.-L. Yip, F. Huang, A. K.-Y. Jen, Adv. Funct. Mater. 20 (2010) 1371–1388.
[11] R. Liguori, A. Rubino, Org. Electron. 15 (2014) 1928–1935.
[12] R. Liguori, W. Sheets, A. Facchetti, A. Rubino, Org. Electron. 28 (2016) 147–154.
[13] R. Miscioscia, F. Loffredo, G. Nenna, F. Villani, C. Minarini, M. Petrosino, A. Rubino, et al., Org. Electron. 30 (2016) 83–91.
[14] S. Bellone, G. D. Licciardo, IEEE T. Instrum. Meas. 6 (2008) 1112–1117.
[15] Y. S. Yang, S. H. Kim, J.-I. Lee, H. Y. Chu, L.-M. Do, H. Lee, J. Oh, T. Zyung, et al., Appl. Phys. Lett. 80 (2002) 1595–1597.
[16] M. A. Ruderer, P. Müller-Buschbaum, Soft Matter 7 (2011) 5482–5493.
[17] M. A. Brady, G. M. Su, M. L. Chabinyc, Soft Matter 7 (2011) 11065–11077.
[18] M. Devynck, B. Rostirolla, C. P. Watson, and D. M. Taylor, Appl. Phys. Lett. 105 (2014) 183301
[19] P. Stallinga, Electrical Characterization of Organic Electronic Materials and Devices, Wiley, 2009.
[20] S. Nowy, W. Ren, A. Elschner, W. Lövenich, W. Brütting, J. Appl. Phys. 107 (2010) 054501.
[21] D. K. Schroder, IEEE T. Electron Dev. 44 (1997) 160–170.
[22] C. Tengstedt, W. Osikowicz, W. R. Salaneck, I. D. Parker, C.-H. Hsu, M. Fahlman, Appl. Phys. Lett. 88 (2006) 053502.
[23] Z. Liu, M. Kobayashi, B. C. Paul, Z. Bao, Y. Nishi, Phys. Rev. B 82 (2010) 035311.
[24] E. Nicollian, A. Goetzberger, Bell Syst. Tech. J. 46 (1967) 1055–1133.
[25] E. H. Nicollian, J. R. Brews, MOS (Metal Oxide Semiconductor) Physics and Technology, Wiley, 1982.

[26] M. Petrosino, A. Rubino, J. Appl. Phys. 109 (2011) 114504.
[27] M. Petrosino, A. Rubino, Org. Electron. 12 (2011) 1159–1165.
[28] M. Petrosino, A. Rubino, Synthetic Met. 161 (2012) 2714–2717.
[29] H. Hirwa, S. Pittner, V. Wagner, Org. Electron. 24 (2015) 303–314.
[30] A. Bolognesi, M. Berliocchi, M. Manenti, A. Di Carlo, P. Lugli, K. Lmimouni, C. Dufour, IEEE T. Electron Dev. 51 (2004) 1997–2003.
[31] J. Schafferhans, A. Baumann, A. Wagenpfahl, C. Deibel, V. Dyakonov, Org. Electron. 11 (2010) 1693–1700.
[32] A. Distler, T. Sauermann, H.-J. Egelhaaf, S. Rodman, D. Waller, K.-S. Cheon, M. Lee, D. M. Guldi, Adv. Energy Mater. 4 (2014) 1300693.