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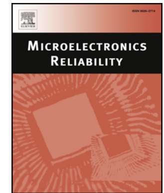

Impact of sidewall etching on the dynamic performance of GaN-on-Si E-mode transistors

A. Tajalli[a], E. Canato[a,*], A. Nardo[a], M. Meneghini[a], A. Stockman[b,c], P. Moens[b], E. Zanoni[a], G. Meneghesso[a]

[a] Department of Information Engineering, University of Padova, Italy
[b] ON Semiconductor, Oudenaarde, Belgium
[c] CMST, University of Ghent, Belgium

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ABSTRACT

The aim of this paper is to investigate the role of the etching of the sidewalls of p-GaN on the dynamic performance of normally-off GaN HEMTs with p-type gate. We analyze two wafers having identical epitaxy but with different recipes for the sidewall etching, referred to as "Etch A" (non-optimized) and "Etch B" (optimized). We demonstrate the following relevant results: (i) the devices with non-optimized etching (Etch A), when submitted to positive gate bias, show a negative threshold voltage shift and a decrease in Ron, which are ascribed to hole injection under the gate and/or in the access regions; (ii) transient characterization indicates the existence of two trap states, with activation energies of 0.84 eV (C_N defects) and 0.30 eV. The latter (with time-constants in the ms range) is indicative of the hole de-trapping process, possibly related to trap states in the AlGaN barrier or at the passivation/AlGaN interface; (iii) by optimizing the p-GaN sidewall etching (for the same epitaxy) it is possible to completely eliminate the threshold voltage shift. This indicates that hole injection mostly takes place along the sidewalls.

1. Introduction

The renovation of traditional power systems by using Gallium Nitride (GaN) high-electron-mobility transistors (HEMTs) has become a challenging topic [1]. Some recent advances may change what is possible today in power electronics. In fact, wide band gap semiconductors not only enable higher power densities than conventional silicon based devices do, but can also convert between DC and AC at higher temperatures, using higher switching frequencies and with greater efficiency [2].

Depletion-mode transistors have excellent performance, owing to the inherent high sheet carrier density at AlGaN/GaN hetero-interface caused by the material's unique polarization-induced electric field; on the other hand, obtaining enhancement-mode has been relatively difficult, and several optimization steps are still underway [3–6]. In order to obtain an enhancement mode device, a p-type doped GaN cap layer is introduced under the gate metal. GaN HEMTs with a p-type gate can show threshold voltage instabilities, as reported by preliminary reports [7–10].

In this article, we present a detailed study of the trapping process induced by positive gate bias in GaN HEMTs with p-type gate. By analyzing two different gate processes, we study the kinetics of the threshold voltage variation, and we demonstrate that etching of the sidewalls of p-GaN can significantly influence device stability. The original results described within this paper demonstrate that: (i) the exposure to a positive gate bias induces a dynamic increase of the drain current, ascribed to a negative shift of the threshold voltage and to a decrease in on-resistance, in the devices with non-optimized etching ("Etch A"). (ii) Two dominant trapping mechanisms occur. The first one is associated with charge-state transition of carbon impurities in nitrogen substitutional position (C_N). The second mechanism is indicative of the hole de-trapping process from traps at the AlGaN barrier and/or at the passivation/AlGaN interface. (iii) The negative threshold voltage variation can be suppressed by an optimized p-GaN sidewall etching process for the same epitaxy.

2. Experimental details

Enhancement-mode AlGaN/GaN power HEMTs with p-type gate fabricated on Si substrate are considered in this paper. A schematic cross-section of the gate region in a p-GaN gated HEMT is depicted in Fig. 1.

* Corresponding author.
E-mail address: eleonora.canato@dei.unipd.it (E. Canato).

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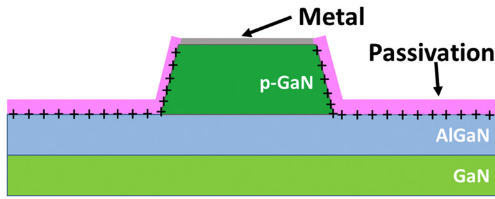
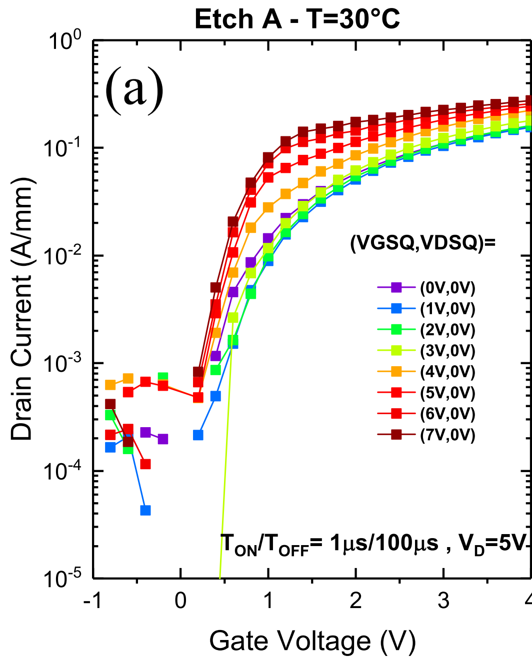


Fig. 1. Schematic representation of the p-GaN gate in the AlGaN/GaN HEMT.



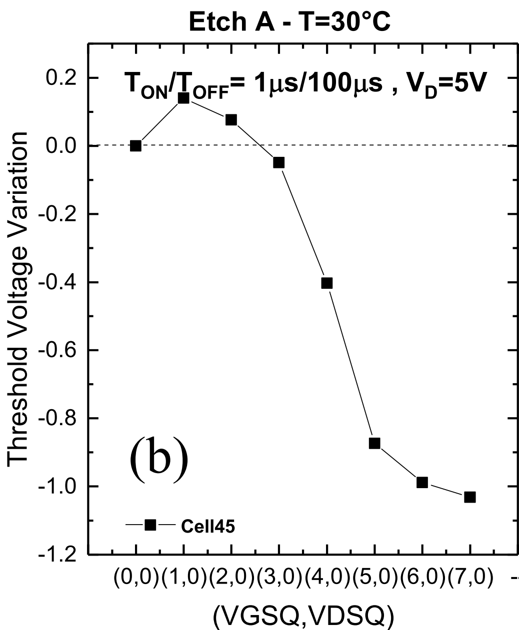


Fig. 2. (a) Sidewall process A: drain current versus gate voltage after different forward gate voltage stress. (b) Pinch-off voltage variation versus forward gate voltage stress for sidewall process A.

Two wafers are studied. The devices have identical epitaxy but the untreated ones have undergone a reference process without improvements, referred to as "Etch A", while the devices "Etch B" are fabricated

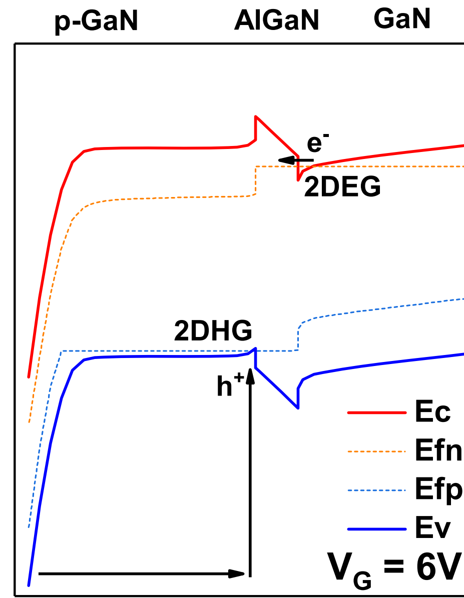


Fig. 3. Band diagram under the region at $V_G = 6$ V (simulated with Sentaurus provided by Synopsys). Two mechanisms are reported: 1) injection of electrons from the 2DEG towards the AlGaN barrier; 2) accumulation of positive charges (holes), injected from the gate metal.

with a process variation, resulting in higher quality of the p-GaN sidewall and access regions (different etch chemistries were used for case "A" and "B").

It is shown that the same process reduces the reverse and forward gate leakage current significantly [11].

The devices under test feature a single finger with a gate width of 200 µm. The device analysis has been carried out on-wafer.

3. Results

3.1. Pulsed characterization of reference devices

Double-pulse measurements are carried out (using a custom built system), starting from several quiescent (V_{GS}, V_{DS}) bias point with a positive V_{GS} value (up to 7 V) and zero volt on the drain. This induces significant trapping under the gate and in the access regions, resulting in threshold voltage instability. I_DV_D and I_DV_G curves were tested at room temperature, by adopting a duty cycle of 1% (pulse width = 1 µs, pulse period = 100 µs).

The transfer characteristics are measured at a drain potential of 5 V and are plotted in Fig. 2(a) for process A.

Through pulsed measurement it is possible to compare different devices in terms of charge trapping [12]. The results for the device fabricated with process A demonstrate that a positive gate bias induces a dynamic increase of the drain current, ascribed to a variation of the pinch-off voltage (see the region around 10^{-3} A/mm in Fig. 2(a)) and a decrease in on-resistance (see the high current region in Fig. 2(a)). The pinch-off voltage variation is calculated and plotted as function of quiescent bias applied to the gate in Fig. 2(b).

The device shows a slight positive pinch-off voltage shift after stressing at 1 V, followed by significant negative shift for positive gate trapping level. The small positive shift is ascribed to the injection of electrons from the 2DEG towards the AlGaN barrier (Fig. 3), which only occurs after electrons have accumulated in the channel. On the other hand, the physical mechanisms behind the negative shift and the decrease in Ron is the accumulation of positive charges (holes), injected from the gate metal. These holes can be trapped at/in the AlGaN barrier (thus inducing a negative Vth shift, Fig. 3) and/or at the passivation/AlGaN interface (inducing a decrease in Ron).

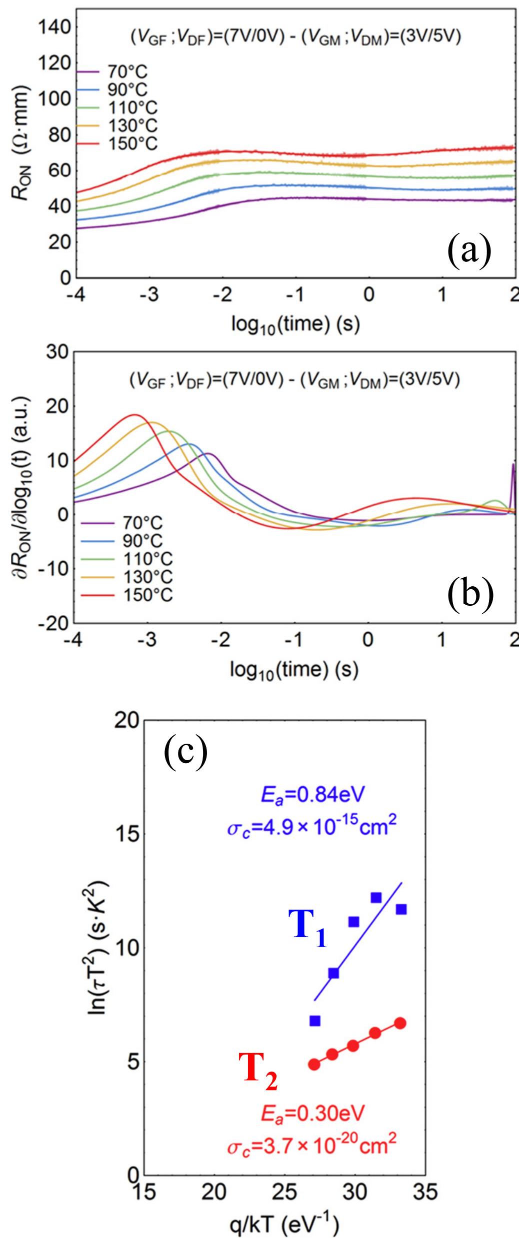


Fig. 4. Sidewall process A: analysis of de-trapping kinetics reveals two traps (one is carbon, the second represents the hole-de-trapping).

3.2. Transient characterization of reference devices

The characterization of trapping phenomena was carried out by drain-current deep-level transient spectroscopy (I-DLTS), which is based on the analysis of drain current transients (i.e. drain current variation with time) as a function of the channel temperature. This technique can provide very accurate information on the activation energy and cross section of the trap levels that limit the performance of GaN-based transistors [12].

The measurements were carried out by analyzing the charge de-trapping transients in the saturation region at several temperature levels. The results of this investigation are summarized in Fig. 4 and were obtained by carrying out the set of transient measurements with filling bias condition (V_{GF}; V_{DF}) = (7 V; 0 V) and de-trapping condition (V_{GM}; V_{DM}) = (3 V; 5 V). Several ambient temperatures were considered compatibly with the time constant (from 70 °C to 150 °C, 20 °C/steps).

For a better understanding of the properties of the trap levels responsible for negative threshold voltage shift, it is necessary to extrapolate the Arrhenius plots of the traps and their signature in terms of activation energies and capture cross-sections.

The results reveal two traps summarized in Fig. 4(c): the signatures of T_1, T_2 correspond to apparent activation energies and apparent capture-cross sections of 0.84 ± 0.24 eV/4.9 × 10^{-15} cm^2 for T_1 and 0.30 eV/3.7 × 10^{-20} cm^2 for T_2.

Level T_1 is similar to the other literature as possible charge-state transition of carbon impurities in nitrogen substitutional position (C_N).

The signatures of T_2 is related to hole-de-trapping responsible for the threshold voltage and Ron instabilities, and the activation energy Ea = 0.30 eV is indicative of relatively fast traps (~ms range), located in the AlGaN barrier and/or at the passivation/AlGaN layer.

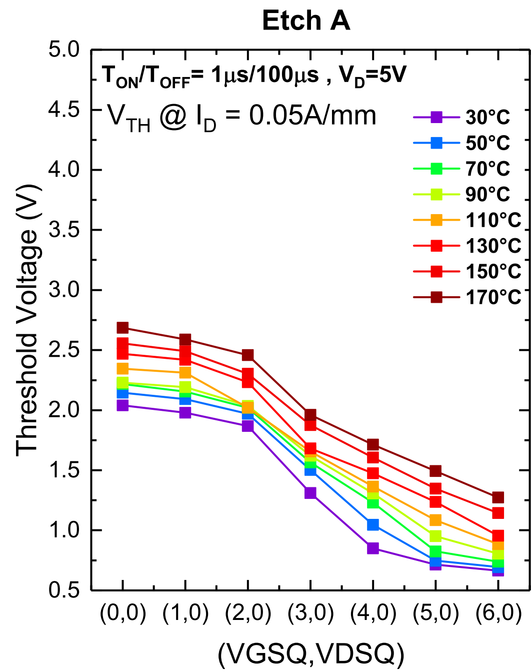


Fig. 5. Sidewall process A: V_{th} at different temperatures.

3.3. Temperature dependent characterization of reference devices

Fig. 5 shows the threshold voltage (for I_D = 50 mA/mm) extracted from pulsed forward gate measurements at different temperatures (from 30 °C to 170 °C, 10 °C/steps), aimed at further investigating the trapping mechanisms underlying the negative threshold voltage shift. High temperature does not strongly increase the threshold voltage shift of the reference structure transistor.

3.4. Characterization of devices with improved p-GaN sidewall

In this section we present the same experimental analysis performed on the devices with the same epitaxy as the reference devices but fabricated with an optimized process for p-GaN sidewall etching, referred to as “Etch B”.

By optimizing the sidewall surface quality and changing the etch tool, we found that the exposure to positive gate has no effect on the threshold voltage. This demonstrates that the threshold voltage instability has been solved, as can be seen in Fig. 6, only through optimization of the sidewall treatment. We therefore conclude that the Vth/Ron shift reported for Etch A samples mostly takes place as a result of injection of holes through interface states along the p-GaN sidewalls, rather than in the “bulk” p-GaN layer. These holes, once injected along the sidewall/passivation interface, can reach the access region thus additionally favoring a decrease in Ron. A careful optimization of

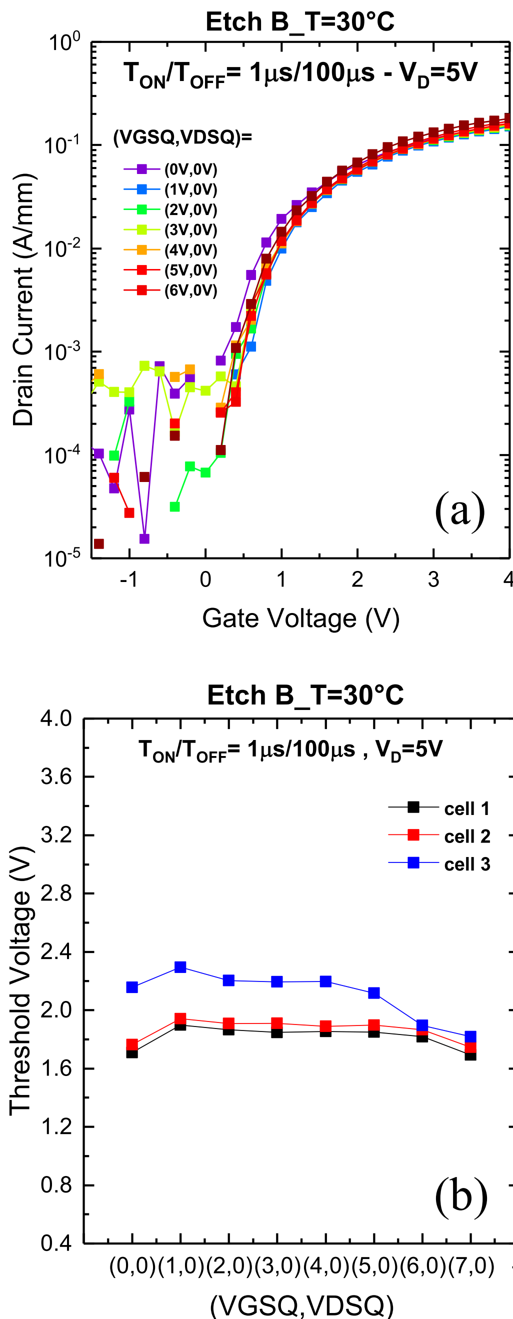


Fig. 6. Sidewall process B: (a) drain current versus gate voltage after different forward gate voltage stress and (b) pinch-off voltage versus forward gate voltage stress.

sidewall etching is therefore a necessary step towards the fabrication of devices with stable Vth/Ron under high positive gate bias.

Fig. 7 shows that the improvement of the p-GaN sidewall quality implies excellent threshold voltage stability even at high temperature.

4. Conclusion

In summary, the threshold voltage instability induced by pulsed gate forward stress has been investigated in p-GaN gated AlGaN/GaN-on-Si HEMTs. The role of the etching of the sidewalls of p-GaN on the the dynamic threshold voltage behaviour has been analyzed.

In particular, under double pulse testing an untreated device shows a negative threshold voltage shift at positive gate voltage, which is explained by hole injection under the gate and/or the gate-source region.

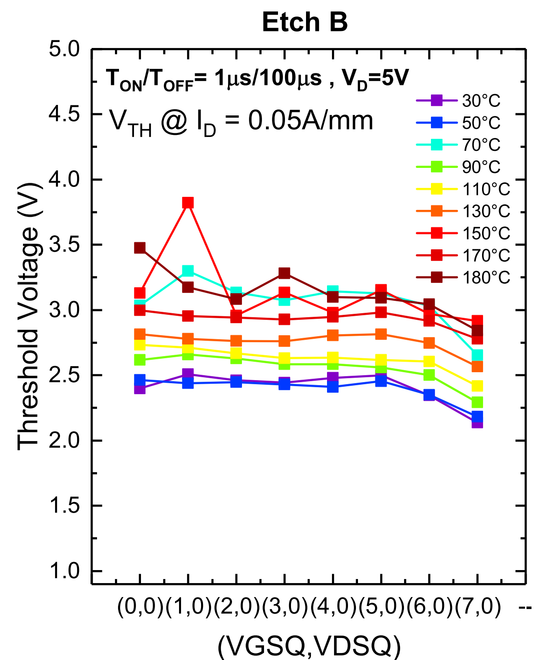


Fig. 7. Sidewall process B: Vth is stable at high temperatures.

Transient measurements indicate that two trapping mechanisms take place, with activation energies of 0.84 eV (C_N defects) and 0.30 eV (hole de-trapping process).

Overall, we have demonstrated in this paper the suppression of threshold voltage instability by optimized passivation of the p-GaN sidewall. The improved stability of “Etch B” highlights that hole trapping mostly takes place along the sidewalls.

Acknowledgements

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References

[1] H. Amano, et al., The 2018 GaN power electronics roadmap, J. Phys. D. Appl. Phys. 51 (2018) 163001 (48 pp.).
[2] M. Meneghini, G. Meneghesso, E. Zanoni (Eds.), GaN Power Devices Materials, Applications and Reliability, Springer, 2017.
[3] M. Meneghini, I. Rossetto, C. De Santi, F. Rampazzo, A. Tajalli, A. Barbato, M. Ruzzarin, M. Borga, E. Canato, E. Zanoni, G. Meneghesso, Reliability and failure analysis in power GaN-HEMTs: an overview, 2017 IEEE International Reliability Physics Symposium (IRPS), Monterey, CA, 2017 (pp. 3B-2.1–3B-2.8).
[4] M. Meneghini, I. Rossetto, M. Borga, E. Canato, C. De Santi, F. Rampazzo, G. Meneghesso, E. Zanoni, S. Stoffels, M. Van Hove, N. Posthuma, S. Decoutere, Degradation of GaN-HEMTs with p-GaN Gate: dependence on temperature and on geometry, 2017 IEEE International Reliability Physics Symposium (IRPS), Monterey, CA, 2017 (pp. 4B-5.1–4B-5.5).
[5] F. Lee, L.-Y. Su, C.-H. Wang, Y.-R. Wu, J. Huang, Impact of gate metal on the performance of p-GaN/AlGaN/GaN high electron mobility transistors, IEEE Electron Device Lett. 36 (3) (Mar. 2015) 232–234.
[6] M. Ťapajna, O. Hilt, E. Bahat-Treidel, J. Würfl, J. Kuzmík, Gate reliability investigation in normally-off p-type-GaN cap/AlGaN/GaN HEMTs under forward bias stress, IEEE Electron Device Lett. 37 (4) (Apr. 2016) 385–388.
[7] G. Meneghesso, M. Meneghini, I. Rossetto, E. Canato, J. Bartholomeus, C. De Santi, N. Trivellin, E. Zanoni, GaN HEMTs with p-GaN gate: field- and time-dependent degradation, Proc. SPIE 10104, Gallium Nitride Materials and Devices XII (2017) 1010419.
[8] M. Meneghini, O. Hilt, J. Wuerfl, G. Meneghesso, Technology and reliability of normally-off GaN HEMTs with p-type gate, Energies 10 (2) (2017) 153.
[9] A.N. Tallarico, S. Stoffels, N. Posthuma, P. Magnone, D. Marcon, S. Decoutere,

E. Sangiorgi, C. Fiegna, PBTI in GaN-HEMTs with p-type gate: role of the aluminum content on DeltaV_TH and underlying degradation mechanisms, IEEE Trans. Electron Devices 65 (1) (Jan. 2018) 38–44.
[10] L. Sayadi, G. Iannaccone, S. Sicre, O. Häberlen, G. Curatola, Threshold voltage instability in p-GaN Gate AlGaN/GaN HFETs, IEEE Trans. Electron Devices vol. 65, (6) (June 2018).
[11] A. Stockman, E. Canato, A. Tajalli, M. Meneghini, G. Meneghesso, E. Zanoni, P. Moens, B. Bakeroot, On the origin of the leakage current in p-gate AlGaN/GaN HEMTs, 2018 IEEE International Reliability Physics Symposium (IRPS), Burlingame, CA, 2018 (pp. 4B.5-1–4B.5-4).
[12] M. Meneghini, A. Tajalli, P. Moens, A. Banerjee, E. Zanoni, G. Meneghesso, Trapping phenomena and degradation mechanisms in GaN-based power HEMTs, Mater. Sci. Semicond. Process. 78 (May 2018) 118–126.