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Influence of block copolymer feature size on reactive ion etching pattern transfer into silicon

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Abstract

A successful realisation of sub-20 nm features on silicon (Si) is becoming the focus of many technological studies, strongly influencing the future performance of modern integrated circuits. Although reactive ion etching (RIE), at both micrometric and nanometric scale has already been the target of many studies, a better understanding of the different mechanisms involved at sub-20 nm size etching is still required. In this work, we investigated the influence of the feature size on the etch rate of Si, performed by a cryogenic RIE process through cylinder-forming polystyrene-block-polymethylmethacrylate (PS-*b*-PMMA) diblock copolymer (DBC) masks with diameter ranging between 19–13 nm. A sensible decrease of the etch depth and etch rate was observed in the mask with the smallest feature size. For all the DBCs under investigation, we determined the process window useful for the correct transfer of the nanometric cylindrical pattern into a Si substrate. A structural and physicochemical investigation of the resulting nanostructured Si is reported in order to delineate the influence of various RIE pattern effects. Feature-size-dependent etch, or RIE-lag, is proved to significantly affect the obtained results.

Supplementary material for this article is available online

Keywords: block copolymers, reactive ion etching, self-assembly, cryogenic RIE, holey silicon

(Some figures may appear in colour only in the online journal)

1. Introduction

The continuous technological progress pervading the various scientific fields composing nanotechnology leads to the demand for an increasingly high degree of control in the fabrication of nanometric features. The milestone of this progress is the capability to control, with high accuracy and precision, both dimensional and lateral positioning of small features with typical size at sub-20 nm level. The achievement of this capability is a mandatory step in the development of applied science such as microelectronics [1], photonics [2], and nano-metrology [3].

It is thus clear that there is a need to develop fabrication techniques allowing the control of regular structures on a large scale with nanometric accuracy. In this context, a possible solution able to fit all the mentioned requirements is represented by the use of the diblock copolymers (DBCs). DBCs represent a particular class of macromolecules composed by two chemical distinct and thermodynamically

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incompatible polymeric blocks. When DBCs are heated over their glass transition temperature, they phase-separate and self-assemble into regular patterns on a large scale with different morphologies [4]. Among all the different accessible morphologies, hexagonally packed cylinders perpendicularly oriented with respect to the underlying substrate are particularly attractive for pattern transfer application. By selective removal of one of the two blocks followed by additive or subtractive processes it is possible to fabricate pillars or holes with tunable characteristic dimensions ranging between 40–10 nm [5]. Due to this capability, DBCs have been indicated as a good candidate to overcome some peculiar limitations of current lithography techniques in different industrial applications, including the contact hole (CH) patterning to shrink, repair, and multiply the CH [6]. Besides the DBC mask formation, the pattern transfer process to the underneath substrate should be carefully addressed and a variety of issues regarding the etch process at nanometric scale should be resolved.

Several studies were reported in the literature regarding sub-20 nm pattern transfer into the silicon (Si) substrate by using a sacrificial hard mask, which provides a high etch selectivity during the pattern transfer processes [7]. These hard masks can be fabricated both in positive and negative configurations by using intermediate steps involving the deposition of an oxide or a metal (usually SiO_2, Al_2O_3, and Cr) [8], or through a sequential infiltration synthesis technique into the DBC template [9]. However, in applications requiring a low etch rate, the use of hard DBC masks is detrimental. Indeed, the introduction of some additive materials and extra steps into the fabrication process can alter the geometrical parameters of the original DBC mask, while increasing the complexity of the overall process. Alternatively, employing a simple soft mask combined with a highly selective reactive ion etching (RIE) process is a simple and viable strategy to finely control the pattern transfer process, embracing a variety of low aspect ratio applications.

RIE pattern transfer at micrometric and sub-micrometric level has been widely investigated. Nevertheless, the extension of the RIE processes to the nanometric level requires us to account for specific effects related to the small dimension of the structures of interest. In particular, the influence of feature size on apparent etch depth (RIE-lag), the aspect ratio dependence etch (ARDE), and the influence of pattern density (micro-loading) are still largely unknown when operating in the sub-20 nm scale. Furthermore, the improvement of sidewall characteristics is needed for recent applications in sub-20 nm scale such as FinFet fabrication [10].

Among the several types of RIE processes, deep reactive ion etching (DRIE) is the most industrially robust and effective technique to gain high aspect ratio anisotropic etching [11]. Different types of plasmas are used in DRIE of Si, including Cl, Br, and F-based plasmas. However, F-based plasmas and in particular SF_6 are commonly used and widely studied plasmas due to their non-hazardous nature offering higher safety levels compared to Cl- and Br-based plasmas. More specifically, SF_6-based DRIE processes such as the Bosch process, fluorocarbon mixing mode process (often referred to as the pseudo Bosch process) [12], and cryogenic process are currently used in Si etching technology.

The Bosch process or gas-chopping process was first introduced by Lärmer [13]. The main drawback of this process is the scalloping of sidewalls, i.e. sidewalls having a saw-tooth form, which arises from the alternating nature of this process. Therefore, the realisation of nanostructures by the Bosch process requires accurate fine-tuning of each process step to attain smooth sidewalls. This condition becomes challenging in the case of sub-20 nm features. The mixing mode process [12] is based on the same chemistry as the Bosch process, but in this case the etch gas and passivation gas are simultaneously injected, resulting in smooth and controllable sidewalls. However, this process involves relatively high milling (physical etch), which results in low selectivity between Si and the polymeric mask. Although the good sidewall finishing makes this process a viable candidate for nanoscale Si etching [14], the low selectivity with respect to the polymeric mask requires the introduction of hard masks during the fabrication process to guarantee efficient pattern transfer on the underlying substrate. Finally, the cryogenic etch process of Si utilises SF_6-O_2 chemistry to passivate and etch the Si substrate [15]. Similar to fluorocarbon-based etch recipes, the cryogenic etch of Si could be utilised in both mixing and pulsing mode [16]. However, the latter is not commonly employed in the literature. In the cryogenic mixing mode of SF_6-O_2, both gases are injected into the RIE chamber at the same time, resulting in a simultaneous passivation and etch process [15]. A very thin SiO_xF_y passivation layer is formed by holding the wafer at temperature ranging from -100 °C to -140 °C, providing very smooth and vertical sidewalls during the etch process. This process is predominantly a chemical etching and only a low-energy ion bombardment is required to remove the thin passivation layer from the horizontal surfaces and maintain a constant Si etch rate [17]. The low milling rate allows a soft mask to be used with very high etch mask selectivity. Selectivity greater than 100:1 was reported for optical photoresist on Si substrate [18]. Such a high selectivity combined with smooth sidewalls and thin passivation layer make this process extremely appealing for nanoscale Si etching even at sub-20 nm nanopatterns [19].

In this work, we investigate the possibility to use a cryogenic etch process to assure propagation of a nanoporous polymeric template into the underlying Si substrate. Some 30 nm-thick polystyrene-block-polymethylmethacrylate (PS-*b*-PMMA) thin films with perpendicular-oriented hexagonally packed PMMA cylinders embedded in a PS matrix were synthesised by spin coating and subsequent high-temperature thermal treatment. After removal of the PMMA cylinders, nanoporous PS templates with different pore diameters ranging from 19–13 nm were obtained by tuning the DBC's molar mass (M_n). The narrow diameter of the DBC cylinders imposes an extra limitation on selectivity through reducing the Si etch rate even in very low aspect ratio structures. A direct pattern transfer from the DBC mask into a Si substrate was performed by RIE using a cryogenic mixing mode of

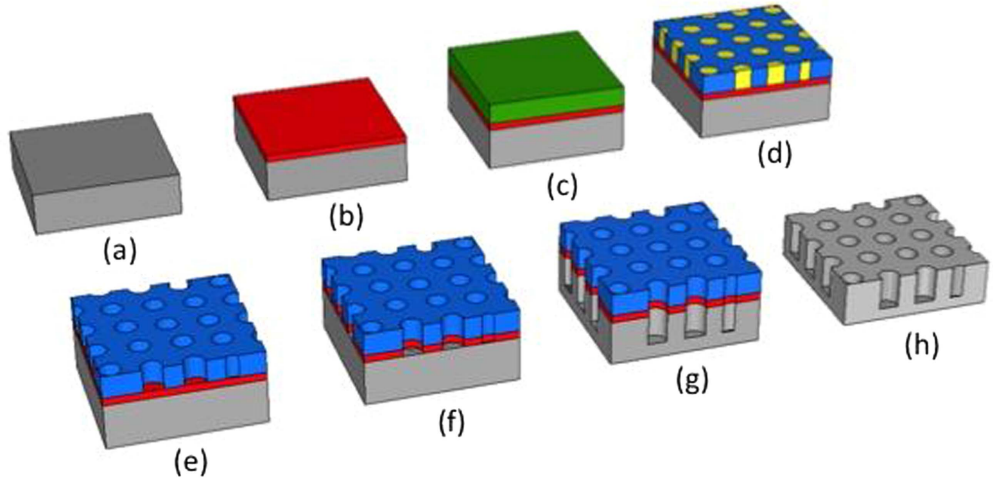

Figure 1. Sketch of experimental procedure: (a) Cleaning and surface functionalization of Si substrate. (b) Deposition and grafting of random copolymer. (c) Deposition of block copolymer. (d) Phase separation between PS and PMMA in vertically aligned cylindrical configuration. (e) Selective removal of PMMA with respect to PS. (f) Removal of PS thin layer from bottom of cylinders. (g) Pattern transfer to the Si substrate. (h) Removal of the mask residuals.

Table 1. Morphological characterisation of the DBC masks: DBC molar mass (M_n), PS block molar mass (M_n styrene), PS volume fraction (f), polydispersity index, average cylinder diameter (d), and average lattice spacing (L_0). The values for d and L_0 were taken from [5].

Sample	M_n [kg/mol]	M_n Styrene [kg/mol]	f	PDI	Diameter [nm]	L_0 [nm]	*Thickness* [nm]	*Aspect Ratio*	*Porosity* [%]
B54	53.8	37.0	0.71419	1.07	13.0 ± 1.0	28.8 ± 0.5	30	2.3	18.5
B67	67.1	46.1	0.71353	1.09	17.0 ± 1.0	35.0 ± 1.0	30	1.8	21.4
B82	82.0	57.0	0.72121	1.07	19.0 ± 1.0	42.9 ± 0.7	30	1.6	17.7

SF_6-O_2. Finally, the electronic properties of the holey silicon were investigated by x-ray photoelectron spectroscopy (XPS).

2. Experimental details

The experimental procedure of this work is briefly depicted in figure 1. Several steps are necessary to clean (a) and neutralise the substrate (b), self-assemble the polymeric film (c–d) and remove the PMMA cylinder to create the nanoporous polymeric film (e–f) that is used as a soft mask for subsequent pattern transfer to the underlying Si substrate (g–h). All experimental details are reported and widely discussed in the following sections.

2.1. Surface neutralisation

A (100) Si substrate with native oxide was selected for fabrication of all samples, in 1 × 1 cm^2 dimension. To entirely clean the surface from organic residues and to maximise the concentration of hydroxyl groups, we performed a bath in piranha solution for bare substrates (H_2SO_4/H_2O_2 with 3:1 vol. ratio at 80 °C for 40 min). The samples were then rinsed in deionized H_2O, dried under N_2 flow, cleaned in isopropanol ultrasonic bath and again dried under N_2 flow. The perpendicular orientation of the cylinders was promoted by a surface neutralisation using a P(S-r-MMA) random copolymer (RCP). According to the standard procedures described in previous studies [20], an RCP solution (9 mg in 1 ml toluene) was spun on the substrates at 3000 rpm for 30 s, to obtain a 30 nm-thick film. After RCP deposition, samples were annealed using a rapid thermal processing (RTP) (250 °C for 300 s in N_2 atmosphere) to allow the grafting of the RCP chains to the substrate. Finally, the non-grafted RCP chains were removed in an ultrasonic bath of toluene. As a result of this process, a 3.3 nm-thick RCP layer was grafted on top of the substrates, assuring proper surface neutralisation of the substrate [21, 22].

2.2. DBC mask preparation

Three asymmetric PS-*b*-PMMA DBCs with different molar mass (M_n = 54, 67, 82 Kg mol^{-1}) were considered. The DBC characteristics are described in table 1, in which for simplicity the DBCs are labelled, based on their molecular weight, as B54, B67, and B82. For each type of PS-*b*-PMMA, the solution of 9 mg of DBC in 1 ml toluene was spun onto the grafted RCP later at 3000 rpm for 30 s, resulting in films with thickness of h = 30 nm. This factor has to be carefully taken into account, since tuning the diameter of the pores while maintaining constant the film thickness, implies a different aspect ratio for each DBC mask. In order to explore the possible dependence of the etch depth as a function of the mask's aspect ratio, thicker DBC masks (h = 40 nm) were

prepared using the DBC with narrower pore diameter (i.e. B54). All the samples were processed in an RTP machine under N_2 atmosphere, by varying the annealing conditions [5, 23].

The PMMA removal was obtained by exposing the samples to UV radiation and the excess PMMA was removed completely in an acetic acid bath and a subsequent rinse in deionized water. Finally, an oxygen plasma treatment was performed to cross-link the PS chains and remove the RCP at the bottom of the pores. During the RCP removal from the bottom of the cylinders in the mask, by isotropic O_2 plasma, the mask's pore diameters are enlarging about 0.05 nm s^{-1} [24]. To minimise this enlarging during the RCP removal step, a thin RCP layer, about 3 nm, has been adopted for all the samples.

2.3. Propagation to the Si substrate

Pattern transfer into the Si substrate was performed by Plasmalab 100 RIE, employing the cryogenic mixing mode of SF_6/O_2 gases. The RIE parameters were: SF_6 flow = 28 sccm, O_2 flow = 1 sccm, RF power = 12 W, ICP power = 550 W, P = 20 mTorr and $T = -120$ °C. After the RIE process, residuals of the polymeric mask were removed in a piranha solution (H_2SO_4/H_2O_2 with 3/1 vol. ratio at 80 °C for 40 min).

2.4. Morphological analysis

In-plane morphological characterisation of both the DBC mask (orientation and ordering) and nanopatterned Si was performed by a scanning electron microscope (SEM) analysis (Zeiss Supra 40 SEM). The film thickness and superficial porosity of the DBC mask were measured by a M-200U spectroscopic ellipsometer at 70° with a one-layer model (PS plus void). The etch depth and porosity estimation of the HS substrate was also performed by ellipsometry and using a one-layer model (Si plus voids). Finally, the measured thickness of the HS layer was validated by x-ray reflectivity measurement and the results are discussed in the supplementary document, which is available online at stacks.iop.org/NANO/28/404001/mmedia. The surface roughness of the HS samples was measured by intermittent contact atomic force microscope (IC-AFM, NT-MDT NTEGRA Spectra) averaging on different areas (250 nm^2, 512 × 512 pixels). In order to enable more trustworthy comparisons, the same tip (NT-MDT NSG10) was used for all the samples, scanning it at 0.5 Hz rate and modulating the amplitude of its oscillation in the few nanometre regime. All the images were subjected to surface and line-flatten corrections and a fast Fourier transform filtering. XPS measurements were performed on a PHI 5600 instrument equipped with a monochromatic Al Kα x-ray source (1486.6 eV) and a concentric hemispherical analyser. The spectra were collected at a take-off angle of 80° with a bandpass energy filter at 11.75 eV.

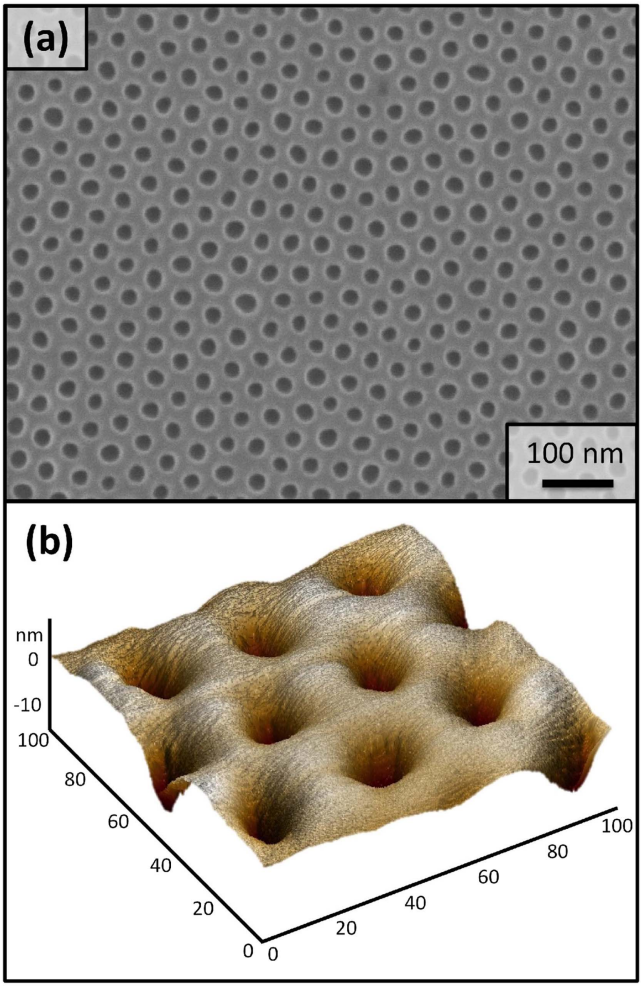

Figure 2. (a) SEM image of a nanometric mask obtained by the self-assembly of B82. (b) AFM height map of the B82 polymeric mask before the RIE process.

3. Results

The first part of this study compared the Si etch rates when operating on a bare Si substrate or on a Si wafer covered with a nanostructured polymeric mask. The pattern transfer to Si was carried out through the B82 DBC mask, i.e. the one with the largest pore diameter. In order to evaluate the quality of the pattern transfer through nanometric templates, we carefully analysed the morphology of the pristine DBC mask by systematic SEM and AFM analysis. The SEM micrograph shown in figure 2(a) was taken before removal of the PMMA phase and confirms the formation of hexagonally packed nanometre-sized cylinders, perpendicularly oriented with respect to the substrate. The AFM micrograph reported in figure 2(b) indicates the surface morphology of the B82 mask after removal of the PMMA cylinders. The sample exhibits an arithmetic average surface roughness (R_a) of about 2 nm with a good homogeneity over a large scale.

The extraction of the etch rate on bare Si for the selected RIE recipe was performed by processing bare Si substrates, half masked by a commercial optical resist. The bare samples were RIE processed for different times (t_{RIE}) ranging between

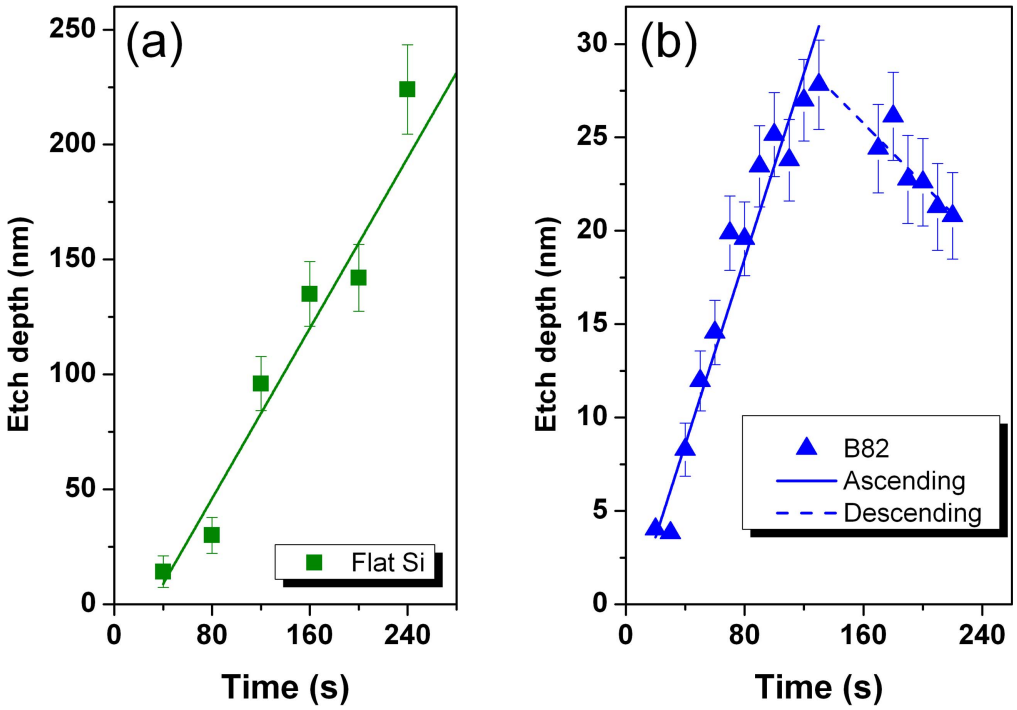

Figure 3. Evolution of the etch depth as a function of time (t_{RIE}) during RIE processing in the case of bare Si (a) and through DBC mask B82 having pores of 19 nm diameter (b).

40–240 s and finally, the etch depth was measured using a stylus profilometer (Tencor P10 profilometer). Conversely, the depth of the pores was determined from ellipsometric data following the procedure described in the experimental section.

The evolution of the etch depth as a function of time is reported in figure 3 in the two cases. Several differences emerged between the pattern transfer performed on the bare surface and through a nanostructured mask. In the case of the bare substrate (figure 3(a)), we observed a linear trend of the etch depth as a function of t_{RIE}, corresponding to an etch rate of about 60.2 nm min^{-1} and a maximum depth of about 225 nm at $t_{RIE} = 240$ s. Conversely, the RIE processes performed through the B82 mask (figure 3(b)) indicates a dual behaviour: in the temporal range of $20 \leqslant t_{RIE} \leqslant 120$ s, the etch depth increases linearly resulting in an etch rate of 14.9 nm min^{-1}, reaching a maximum value of 27 nm. Under our experimental conditions the etch rate on bare Si is about four times higher than the one obtained through a nanometric template.

Beyond $t_{RIE} = 120$ s we observed a linearly descending trend with a lower slope than in the ascending region. In order to better understand the ongoing etch behaviour through the nanostructured mask, the surface morphology after the RIE process has been analysed by AFM. As indicated in figure 4, for $20 \leqslant t_{RIE} \leqslant 120$ s the Si surface is smooth with a roughness value comparable to the unprocessed Si wafer ($R_a = 0.2$ nm). In case of the samples treated for $t_{RIE} = 170$ s, an increase of the surface roughness (up to $R_a = 0.6$ nm) is evident in the flat zone between two adjacent pores, where it was supposed to be masked during the etch process. Finally, for $t_{RIE} \geqslant 200$ s a certain amount of waviness (corresponding to $R_a > 3$ nm) appears on the surface, indicating the complete degradation of the DBC mask and the loss of the original nanometric pattern. It is worth noting that the narrow diameter of cylinders in the DBC mask does not permit the AFM tip to completely penetrate the pores, thus the depth values extracted from AFM measurement cannot be used to analyse the overall depth.

Although etch selectivity between PS film and bare Si, for the adopted RIE process, was about 1:15 (PS film to Si), the apparent selectivity between the DBC mask and Si was much lower than the expected value (about 1:1). Indeed, based on the selectivity value of PS film, at $t_{RIE} = 170$ s only about 9 nm of mask should be degraded and the Si substrate is supposed to be still covered by about 21 nm of PS mask, while the AFM result indicates an increase in surface roughness of Si, in the zones which were supposed to be masked, corresponding to full degradation of the mask.

According to the previous considerations, we explored the behaviour of the etching process through the DBC masks with smaller pore diameters, only in the restricted range of t_{RIE} between 20–120 s, where the linear behaviour was observed. The results of the etching processes through all the DBCs are reported in figure 5(a), in which a clear influence of the pore diameter on the final etch depth is evident. For a given t_{RIE}, the depth of the nanometric pores created through the B82 masks is always higher than the one in B67 and in turn higher than in B54. It is worth noting that in all the samples treated at $t_{RIE} \leqslant 30$ s, pattern transfer into Si was not completed and the pores in the Si were not fully opened (we will discuss it later in figure 7). For the same reason, the measured depth by ellipsometer for those samples did not match well with the employed one-layer model. Consequently, the obtained etch depth may

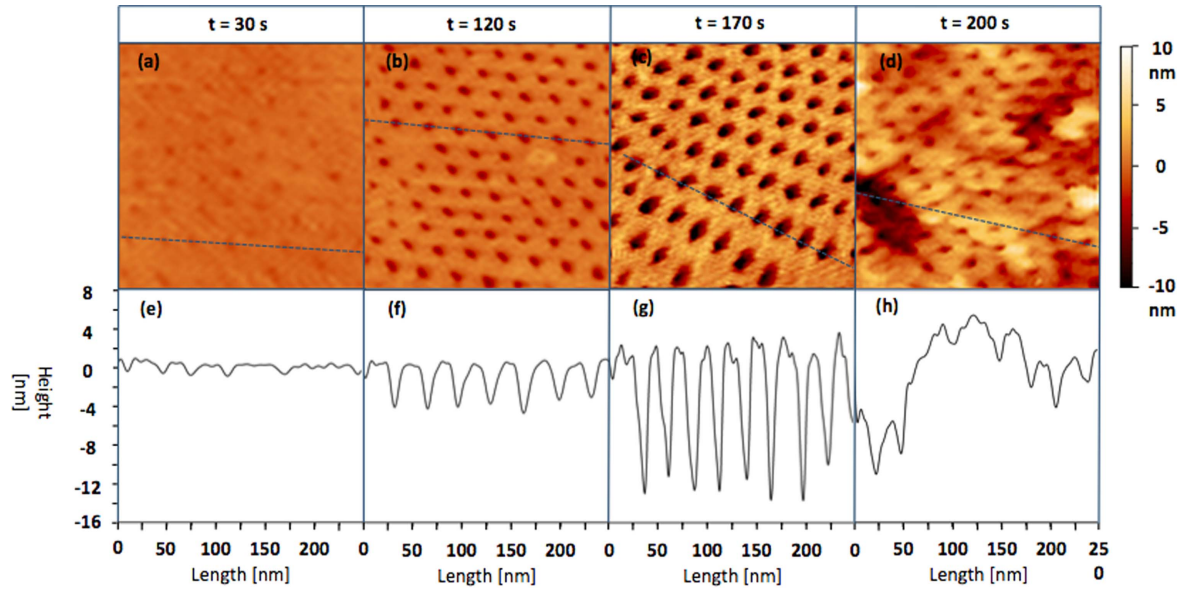

Figure 4. (a)–(d) AFM micrographs and (e)–(h) transversal AFM profiles of B82 transferred pattern in Si. The mapped area is a square 250 × 250 nm^2. Since the AFM tip could not fully penetrate the small pores, the depth information is not the real value.

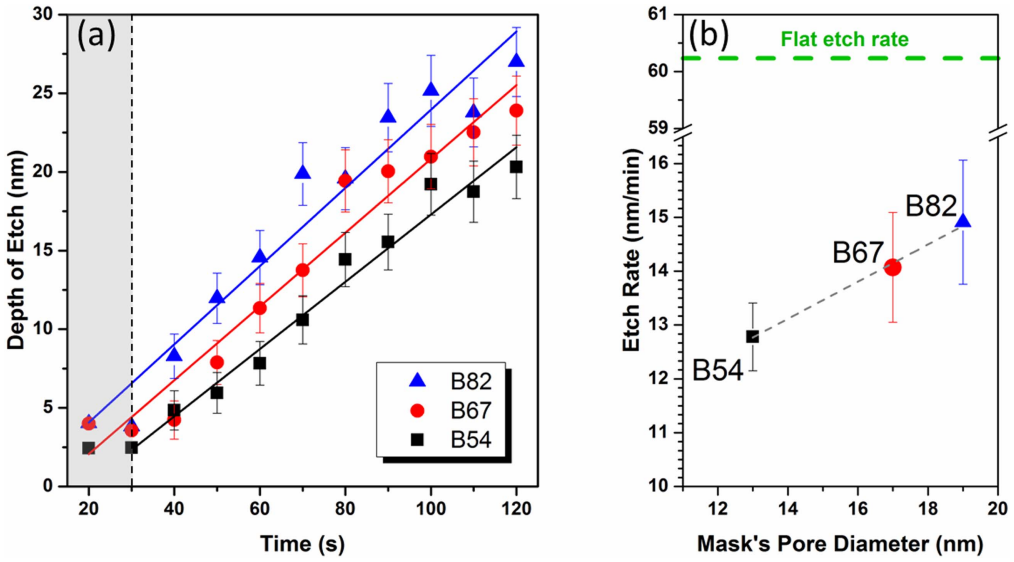

Figure 5. Etch depth in Si versus RIE etch time (t_{RIE}), using different DBC masks (a). Etch rate as a function of nominal mask pore diameter and etch rate on bare Si (b).

drift from the original value. In figure 5(a), the measured depths for $t_{RIE} \leqslant 30$ s are marked in a grey box and indeed they could be considered as a negligible etch depth. Irrespective of the characteristic of the polymeric mask, in the range between 40–120 s, the etching depth presents a linear behaviour corresponding to etch rates of 12.8 (B54), 14.1 (B67), and 14.9 (B82) nm/min, respectively.

These slopes are plotted in figure 5(b) as a function of pore diameters in the polymeric mask. In the same figure, the etch rate on the bare surface is indicated by a green dashed line. The etch rates through all types of DBC masks are markedly lower than the etch rate on the bare surface. As already discussed in the case of the largest pore diameter (B82), the etch rate is about 25% of that of bare Si. Further reduction of the etch rate is observed reducing the pore diameter of the polymeric mask.

In order to compare the transferred pattern in Si with the original mask, pore diameter (d) has been calculated for the three types of samples, in the range of $t_{RIE} < 120$ s, using ImageJ software based on SEM images on a large area and the results are indicated in figure 6. As can be seen, the pore diameter in Si, for the three groups of samples, was enlarged as the RIE etch time increased with a trend similar to that of the etch depth. For B82 with $t_{RIE} < 55$ s and for B67 with $t_{RIE} < 70$ s, the pore diameter of nanopatterned Si is less than the nominal diameter of the mask, which may be a sign of incomplete pattern transfer. Regarding B54, the pore diameter of the nanopatterned Si is mostly less than the nominal value

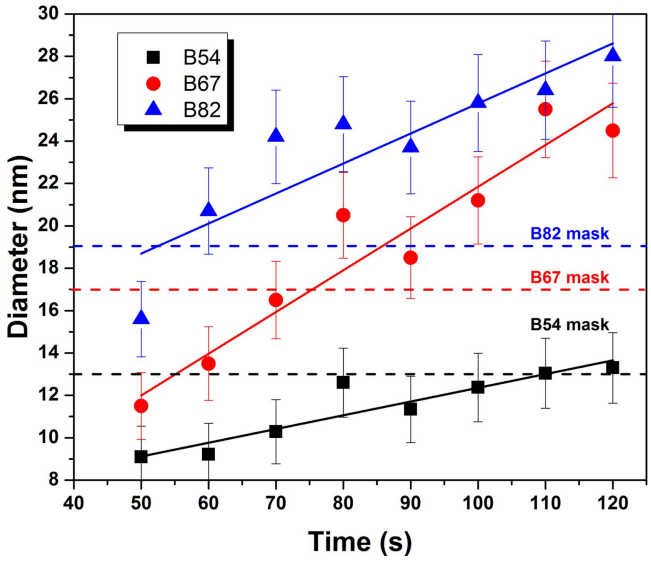

Figure 6. Pore diameter as a function of RIE etching time for three groups of masks. Pore diameter of samples in the range of $t_{RIE} < 50$ was impossible to obtain due to insufficient SEM image contrast or equivalent low etching depth.

of the mask and only for $t_{RIE} > 110$ s does it reach the original mask value.

By correlating the SEM images with the AFM results obtained after the pattern transfer processes performed at different t_{RIE}, it is possible to identify for the three DBC masks four different working windows corresponding to a particular configuration of the superficial morphology. These working windows, reported in figure 7, can be classified by an incomplete pattern transfer (A), a good pattern transfer (B1), the appearance of a non-negligible surface roughness (B2), and finally the appearance of a distorted Si surface (C). For RIE processes with duration up to $t_{RIE} = 30$ s (working window A in figure 7), the SEM micrographs revealed the absence of any cylinders in the transferred hexagonal pattern, thus the etching process cannot be considered to have been completed. The etch depth measured by ellipsometer for short t_{RIE} corresponds to working window A, and presents a high uncertainty value (figure 5(a)).

The working window classified as $B1$, defines the range of t_{RIE} where the pattern transfer of the hexagonally arranged cylinders is achieved without altering the surface roughness of the Si substrate. For all the DBCs the $B1$ zone is defined up to $t_{RIE} = 120$ s. For RIE times longer than $t_{RIE} = 120$ s, although the hexagonal disposition of the cylinders is not altered, the surface roughness between the pores starts to increase gradually. This surface roughness is employed as a signal to set the starting point of the degraded mask. Simultaneously, we observed a slight decrease in the etch depth. This behaviour is classified as zone $B2$, which has been identified mostly based on the AFM results. Although both $B1$ and $B2$ working windows could be considered as the pattern transfer zone, the existence of the surface roughness in the $B2$ zone could be problematic for final application. By further increase of RIE time, $t_{RIE} > 150$ s for B54, $t_{RIE} > 170$ s for B67, and $t_{RIE} > 200$ s for B82, SEM images indicate a sort of distortion on the surface, where the pores are joined together and the original pattern is completely lost. This zone C is called the surface-distorted zone.

The results reported so far point out that the main limitation on the maximum achievable etch depth, is the apparent selectivity between the soft mask and the Si. One possible solution, to reach a higher etch depth in Si, might be by using a thicker mask. Therefore, the etch behaviour through the thicker B54 mask (40 nm thick corresponding to mask aspect ratio of 3.1) was also investigated and the results are compared to those obtained in the case of the 30 nm-thick mask in figure 8. It is worth mentioning that the porosity of the 40 nm-thick B54 mask, or equivalently average cylinder diameter (d) and average lattice spacing (L_0), was similar to the thin one. As can be implied, there is no gain from using the thicker mask and indeed pattern transfer was started with a short delay of 50 s and then continued with an etch rate about 40% lower (7.6 nm min^{-1}) than that of 30 nm-thick mask (12.8 nm min^{-1}). Finally, the maximum obtained etch depth using the thicker mask is about 13.1 nm, which indeed is about 35% lower than the one of the 30 nm-thick mask.

In order to probe the electronic characteristics of the HS samples as a function of the periodicity and size of the nanopores, XPS measurements were performed on the samples fabricated using the different DBC masks and dry etched for $t_{RIE} = 120$ s. Considering the specific experimental conditions during the XPS analysis, the sampling depth is smaller than the thickness of the HS layer. Consequently, the acquired XPS spectra correspond to photoelectrons generated in the HS region, with negligible contribution from the underlying Si bulk. Figure 9 reports the high-resolution spectra of the Si 2p and valence band regions for the HS samples obtained using the different DBCs. The same spectra were acquired on a bare Si sample that was used as a reference (figure 9(a)). The analysis of the Si 2p high-resolution spectra highlights the presence of two main components centred at ~100 and ~103 eV, respectively, and corresponding to Si^{0+} and Si^{4+} valence states. The component at ~103 eV is related to the formation of a native oxide layer on the Si surface during air exposure. Interestingly, the intensity of the Si^{4+} component in the HS samples is higher than in the reference one, consistent with the higher surface/volume ratio of the nanostructured samples. The component at ~100 eV is attributed to the Si in the bulk of the HS samples. The position of the Si^{0+} components in the different HS samples is roughly constant, irrespective of their characteristic dimensions. The valence band edge in the valence band region is determined by means of a linear extrapolation procedure [10]. The energy difference between the Si^{0+} component of the Si 2p spectrum and the valence band edge is ($\Delta E = 98.72 \pm 0.06$ eV) within the experimental, indicating that no modifications of the electronic structure of Si have been introduced by the nanostructures at the surface.

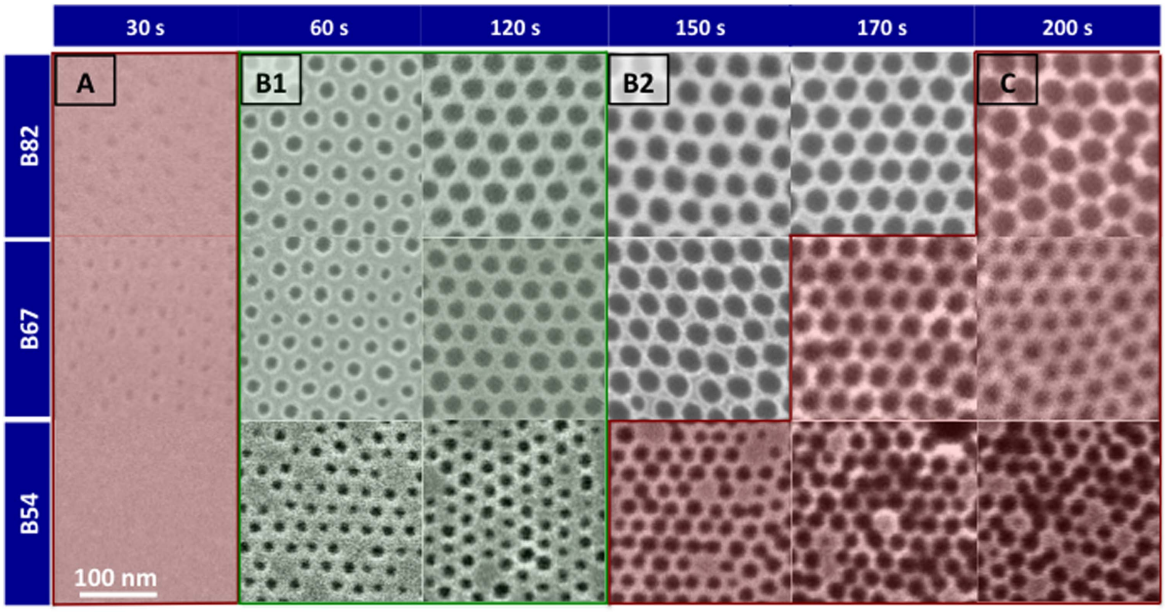

Figure 7. SEM images of transferred pattern into the Si for three different types of DBC masks in various etching times (t_{RIE}). Incomplete pattern transfer (A), good pattern transfer (B1), appearance of a non-negligible surface roughness (B2), and distorted Si surface (C).

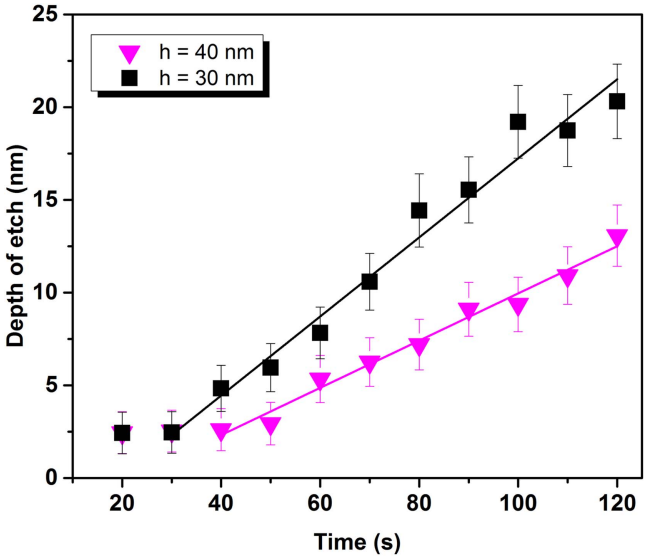

Figure 8. Etch depth in Si versus RIE etch time (t_{RIE}) for the B54 mask type with two different thicknesses: 30 and 40 nm.

4. Discussion

The presented results pointed out that the etch rate on bare Si is roughly 4–5 times higher than the obtained results though all the DBC masks. Moreover, by reducing the pore diameter from 19 to 13 nm, we observed a 14% decrease in the etch rate. Although the maximum achievable etch depth is limited due to the apparent selectivity between the soft mask and the Si substrate, an increase in mask thickness has a negative impact on the maximum achievable etch depth and obtained etch rate.

By considering the apparent selectivity of DBC masks and the selectivity of PS thin film with respect to the Si, about

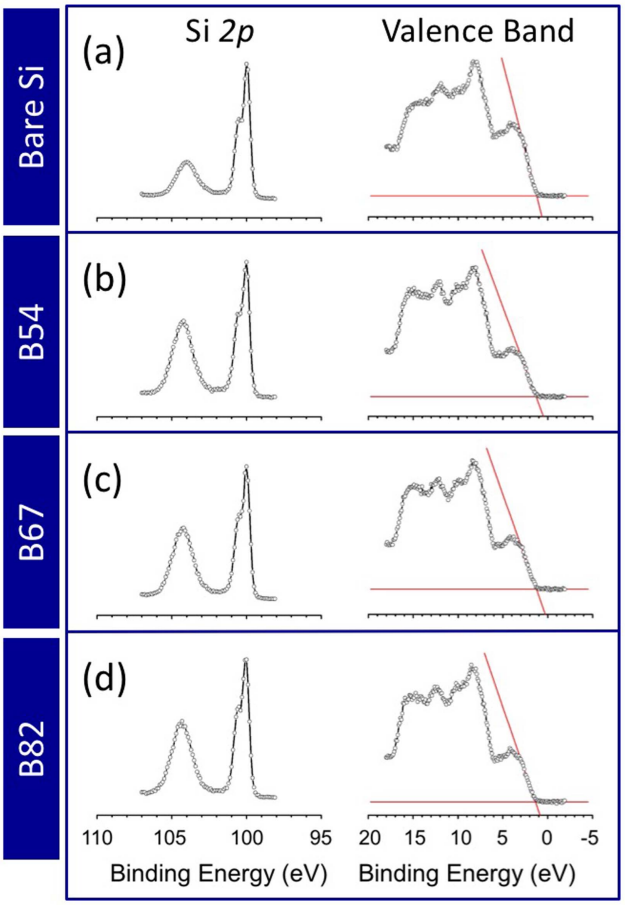

Figure 9. High-resolution XPS spectra of the Si 2*p* and valence band region for a bare Si (a) and for HS samples prepared by RIE (t_{RIE} = 120 s) through nanoporous PS templates obtained using self-assembled films of DBC with M_n = 54 kg mol^{-1} (b), M_n = 67 kg mol^{-1} (c), and M_n = 82 kg mol^{-1} (d).

1:1 and 1:15, respectively, one can extract that the DBC mask degrades five times faster with respect to the PS thin film. This could be due to the porosity of the DBC masks, which provides a lateral window for isotropic degradation (in both the vertical and horizontal direction), in the presence of oxygen ions during the low-bias RIE process. While in the case of the PS thin film (non-patterned), the mask degradation is just in the vertical direction resulting in a more durable mask (selectivity of 1:15). Future investigation is required to better understand the origin of this observation.

In order to disclose the origin of such behaviour, different processes must be considered. Some limited studies have already been reported in the literature on RIE processes performed through masks with minimum features up to 50 nm [17–26], while the influence of smaller features was still not classified. In that range, the influence of the mask feature size on the final etch depth at micrometric scale is generally called RIE-lag [27]. The main difference between the aforementioned studies and the present case, apart for the minimum feature size, is that the DBC masks are homogeneously distributed over the entire surface of the samples, while micro- and sub-micro-patterning by electron beam lithography, reported in the literature, covered only a small area of samples [17–26]. This pattern density mismatch can possibly lead to sensibly different results in the final etch depth due to the existence of other RIE effects such as the micro-loading effect [28].

Indeed, the etch rate and etch depth obtained by the RIE process could be influenced by the total amount of exposed Si or unmasked Si. This etch behaviour is called macro-loading and it commonly leads to a decrease in the etch rate due to the high consumption of fluorine radicals for a higher amount of Si loading [16]. In order to avoid the macro-loading effect, all the samples have been prepared on substrates having the same dimension and they were loaded on a 6 inch Si support wafer (polished Si (100) with native oxide).

Another RIE effect, which could influence the final etch rate or etch depth is micro-loading. This effect takes into account the influence of local exposed surfaces surrounded by a masked area for a given feature size. Thus, in this case the etch process depends on the pattern density and local depletion of reactance [29]. To study the influence of micro-loading on the obtained results of this work, behaviour of the etch rate versus the mask's porosity (table 1) was carefully investigated. There is no distinct correlation between the porosity of the DBC masks and the obtained etch rate on Si. According to table 1, the B67 mask has the highest porosity of 21.4%; nevertheless, its etch rate is in between the other two DBC models. This result is in contrast to the definition of micro-loading. Consequently, micro-loading could not be the cause of the obtained etch behaviours in Si by different DBC mask types.

ARDE is another known RIE effect, which can have some influence on the final etch rate for a given feature size. The ARDE effect describes the common observation that the etch rate decreases as a function of etch time for identical features. Thus, ARDE is usually reported by plotting the etch rate versus aspect ratio in Si (etch depth divided by pore diameter) for the given feature size. In our study, the etch processes were performed in a narrow aspect ratio window in Si (low aspect ratio regime). Since the etch process of this work belongs to the very beginning part of the ARDE plot (etch rate versus aspect ratio), the influence of this effect for individual feature size is not yet evident. This is confirmed by the fact that the measured etch rate was constant through all DBC masks, as reported in figure 5(b). To conclude, also ARDE does not play any role in the obtained results of this study. The experimental setup was well designed to have a feature-dependent etch, or RIE-lag, as the only contributor to the obtained results. The obtained trends for the etch rate and etch depth were purely due to the difference in DBC mask features.

As stated before, the feature-size-dependent etch or RIE-lag was not well studied in the literature and RIE-lag was reported to have similar physical sources as the ARDE effect. Indeed, most of the studies were focused on the ARDE process, due to its influence on high aspect ratio applications such as the fabrication of microelectromechanical systems [27–29]. The main parameters contributing to these effects are reported: Knudsen transport of neutrals, ion shadowing, neutral shadowing, and image force (IF) [27–31]. However, in the literature there is some controversy about the main source of these phenomena and it also highly depends on the adopted RIE etch recipe: type of gases, pressure, temperature, etc. In some studies, the use of a thin layer of inhibitor is reported as a promoter of IF effect and finally, feature-size dependency of the profile [16]. In the case of the cryogenic mixing mode of SF_6/O_2, adopted in this work, the etch process is predominantly a chemical etch rather than milling and neutrals were reported as the main cause of this chemical etching. Some studies have already been performed for ARDE, specifically by the cryogenic process and the fluorine radical depletion was stated as the primary source of this effect [32]. Since the mean free path of fluorine radicals in plasma is larger than the pore diameter of DBC masks, the transport of fluorine radicals is described by the Knudsen transport. The Knudsen transport provides the probability coefficient K for fluorine radicals to reach the Si at the bottom of the etching. This probability depends on many parameters of the plasma, mostly pressure, and also the dimension of the channel through which the radicals are passing, which is usually expressed as a function of the aspect ratio including mask thickness. Based on the previously mentioned studies in the literature and considerably small features of DBC masks, Knudsen transport is proposed as the main contributor in RIE-lag for the cryogenic process at nanoscale.

5. Conclusions

Feature-dependent RIE of Si in sub-20 nm scale has been carefully studied using the self-assembly of a DBC mask and cryogenic mixing mode of SF_6-O_2. Three different PS-b-PMMA perpendicular-oriented cylinders with different pore diameters, ranging from 13–19 nm, were obtained by tuning the DBC's molar mass (M_n). The obtained results reveal that

the etch rate on bare Si is roughly 450% higher compared to the results obtained with all the DBC masks. Moreover, by reducing the mask pore diameter from 19 to 13 nm, about a 14% decrease in the etch rate was observed. Although the adopted etch process has selectivity of about 15:1 between bare Si and non-patterned PS film, the apparent selectivity of the patterned DBC mask was obtained to be less than 1:1. Furthermore, there is no gain from using a thicker DBC mask and indeed a 33% increase in the mask thickness results in about a 40% decline in the final etch depth and etch rate. Finally, no significant modification in the electronic structure of Si has been observed in the nanostructured surfaces.

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