PROCEEDINGS OF SCIENCE

ALICE Pixel Detector Operations and Performance

Rosario Turrisi[*†]
INFN - Sezione di Padova
E-mail: rosario.turrisi@pd.infn.it

The ALICE Silicon Pixel Detector (SPD) is designed to provide the tracking and vertexing performance required to measure heavy flavor production via the detection of displaced vertices. The SPD constitutes the two innermost layers of ALICE, placed at r=3.9 cm and 7.6 cm from the beam axis and counts $\sim 10^7$ pixel cells to cope with the high multiplicities expected in heavy-ion collisions. The overall thickness has been contained within 2.28% of X_0 to minimize the multiple scattering and it has been implemented with the feature, unique at LHC, to provide a level-0 trigger. In this paper a description of the key features of this detector is presented and selected commissioning results are shown.

19th International Workshop on Vertex Detectors - VERTEX 2010
June 06 - 11, 2010
Loch Lomond, Scotland, UK

[*]Speaker.
[†]On behalf of Silicon Pixel Detector Project in the ALICE Collaboration

PoS(VERTEX 2010)007

1. Introduction

The ALICE experiment is dedicated to the study of nucleus-nucleus, proton-proton and proton-nucleus collisions at the CERN Large Hadron Collider (LHC)[1, 2]. The main physics goal of the experiment is to investigate the properties of strongly-interacting matter in the conditions of high energy density (> 10 GeV/fm^3) and high temperature ($\gtrsim 0.2$ GeV), expected to be reached in central Pb-Pb collisions at $\sqrt{s_{NN}} = 5.5$ TeV, when, according to lattice QCD calculations and the evidence from the RHIC experiments [3], a deconfined Quark-Gluon Plasma should be formed [1]. The measurement of heavy flavors (charm and beauty) production in Pb-Pb collisions at the LHC is one of the main items of the ALICE physics program, because it will allow to investigate the properties of quarks in the deconfined matter and obtain, by comparison with the results from proton-proton collisions, informations about the new phase. This goal will be pursued e.g. by the analysis of the quenching of high p_{t} charged particles and the study of flavor-tagged jets. Open heavy-flavor production measurement constitutes also the baseline for quarkonia suppression studies [2].

The ALICE design [4] was driven by the physics requirements as well as by the experimental conditions expected in nucleus-nucleus collisions at the LHC. The most stringent design constraint is the extremely high particle multiplicity, which could be up to three orders of magnitude larger than in typical pp interactions at the same energy. The tracking was made particularly safe and robust by using mostly three-dimensional hit information with many points in a moderate field of 0.5 T provided by the large L3 solenoid magnet. This was achieved with a combination of very low material thickness to reduce multiple scattering at low pt and a large tracking lever arm of up to 3.5 m to guarantee a good resolution at high pt.

To measure the separation, from the interaction vertex, of the decay vertices of heavy flavored hadrons, which have mean proper decay lengths $c\tau \sim 100 - 500$ μm, a resolution on the track impact parameter (distance of closest approach to the vertex) well below 100 μm is required. This requirement is met by the Inner Tracking System and in particular the SPD is the component delivering the performance on the impact parameter and vertexes position resolution in the bending plane.

2. SPD overview

2.1 Structure of the detector

The two SPD layers constitute the innermost detector of ALICE, with radii of 3.9 and 7.6 cm [4]. In figure 1 a series of pictures illustrating the detector segmentation is presented. The basic building block is a module consisting of a two-dimensional sensor matrix of reverse-biased silicon detector diodes, 200 μm thick, bump-bonded to 5 front-end chips, thinned down to 150 μm. The sensor matrix consists of 256$\times$160 cells, each measuring 50 μm (rϕ) by 425 μm (z). Two modules are mounted together along the z direction to form a 141.6 mm long half-stave which is able to cover $\pm$1.9 and $\pm$1.4 pseudorapidity units on the first and second layer, respectively. Two mirrored half-staves are attached, head-to-head along the z direction, to a carbon-fibre-composite support sector (CFSS). Each sector supports six staves: two on the inner layer and four on the outer layer. The sensors are mounted in such a way that there is a 2% overlap between the active regions in rϕ,

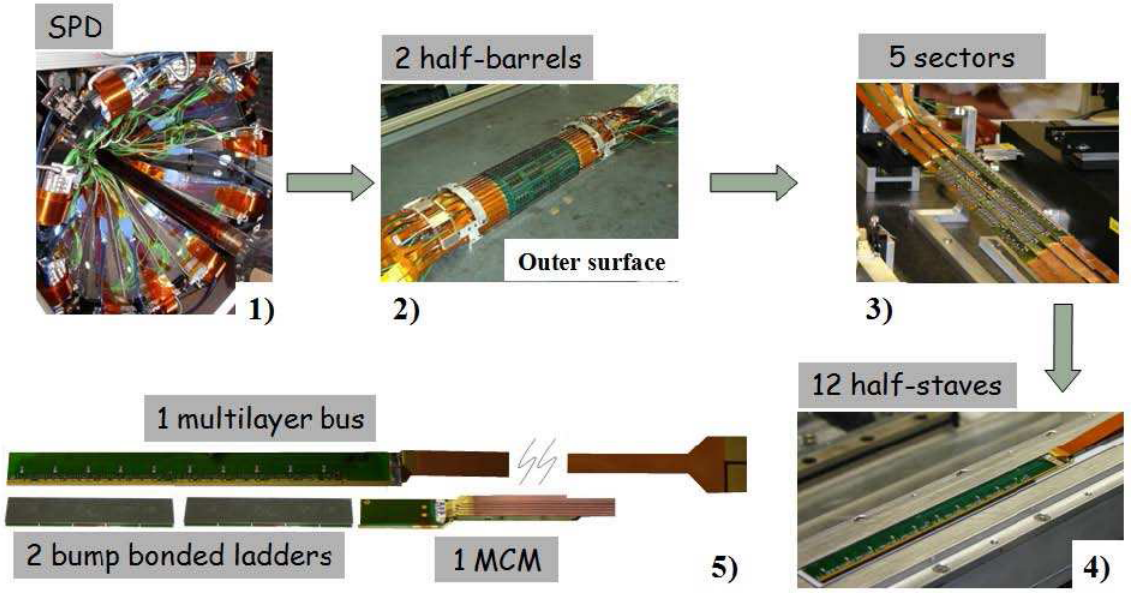

Figure 1: The SPD segmentation. Clockwise: 1) the detector in its final position around the beam pipe; 2) the outer surface of the first completed half-barrel; 3) the first assembled sector; 4) one half-stave just glued and 5) all the components constituting the half-stave.

but along z there is a gap between each two consecutive sensors. Five sectors are then assembled to form a half-barrel and finally the two (top and bottom) half-barrels are mounted face to face around the beam pipe to close the full barrel which is actually composed of 10 sectors. In total, the SPD includes 60 staves, consisting of 240 modules with 1200 readout chips for a total of 9.8×10^6 cells. To minimize the multiple scattering, special care has been taken in the choice of all materials the detector bus, the mechanical support and the cooling system are made of, together with the limited detector and chip thickness, obtaining a total material budget of 2.28% of X_0 (for more details see [4]). The spatial precision of the SPD sensor is determined by the pixel cell size, the track incidence angle on the detector, and by the threshold applied in the readout electronics. The values of the resolution along rϕ and z extracted from beam tests for perpendicular tracks are 12 and 100 μm, respectively. The overall design has been developed to keep the occupancy as low as 1.5% and 0.4% on the inner and outer layer respectively, assuming a maximum multiplicity of 8000 charged particles per unit of rapidity at midrapidity, corresponding to ≈ 90 particles/cm^2 on the first layer.

2.2 On-detector electronics

The ALICE1LHCB pixel ASIC contains 256 x 32 pixels and the read-out is based on a binary concept, where the full matrix is shifted out on a 32 bit bus in 256 consecutive 10 MHz clock cycles. Each pixel chip generates a pulse (Fast-OR) whenever at least one pixel cell detects a particle signal above threshold. The Fast-OR is used to implement a prompt trigger which contributes to the ALICE L0 trigger. Every chip contains 42 internal DACs, 8 bits each, to provide voltage and current references to the analog and digital circuitry of the chip. At the end of each half-stave a multi chip module (MCM) reads out the 10 pixel chips. The MCM contains 4 ASICs, the RX40

to receive an LHC synchronous clock and serial data on optical fibers, the digital pilot chip to configure and read-out the pixel chips, the 800 Mbit/s serializer chip (Gigabit Optical Link, GOL) to send the data on one optical fiber from the detector to the control room and the analog pilot chip to provide bias voltages to the pixel chip. The connection between the pixel chips and the MCM is done with a 5-layer aluminum/kapton flat cable, the pixel bus. The pixel bus is 166 mm x 13.8 mm x 0.35 mm in size. Aluminum was chosen as conductor in order to reduce the material budget of the half-staves to a minimum. Two layers are reserved for power and ground connections. Three planes were used for the transmission of signals, the 32-bit data bus, the 10-bit Fast-OR bus and the 25-bit control bus. The final bus was equipped with SMD decoupling capacitors, pt1000 temperature sensors and pull-up resistors. An aluminium-kapton foil, the grounding foil, separates the half-stave electrically from the CFSS. For more details, see [4] and references therein.

2.3 Off-detector electronics

The 120 half staves are controlled and read-out via 20 VME based electronic boards, the router cards, which are sitting in the control room located at about 100 m from the detector. Each of the router cards houses 3 daughter cards (link receiver) each communicating with two half staves. The routers multiplex the data from the link receiver cards and send them via the ALICE detector data link (DDL) to the DAQ. Furthermore the routers form the interface to the ALICE central trigger processor via the LHC-standard TTC (Timing, Trigger and Control) interface and detector control system via a VME connection. One of the challenges during the production of the router cards was to gain experience with the mounting of large ball grid arrays (BGA) and produce 9U VME cards with a flatness compatible with BGA mounting. The acceptance tests were based on boundary scan methods allowing to pin point directly faulty solder connections using a board wide JTAG chain. The basic commissioning of the FPGA firmware was simplified as the entire system including the detector ASICs and PCB board connections was simulated using HDL (Hardware Description Language) system simulations prior to board fabrication. This allowed the verification of the interfaces to the DAQ, the trigger, the ALICE DCS and the SPD detector modules already before the system installation. The Fast-OR output, which is activated if at least one out of the 8192 pixels has been hit, is transmitted on the optical fiber to the pixel trigger processor (PIT). The PIT extracts the 1200 Fast-OR bits and applies the pixel trigger algorithm in order to provide a L0 input trigger signal to the ALICE central trigger processor CTP within 800 ns. The PIT system comprises one 9U sized mainboard with one Xilinx Virtex4, 1513 pin FPGA acting as the trigger processor. The main board carries 10 daughter cards which receive 12 optical fibers each, extract the Fast-OR bit information and send it to the main board. As the system is very compact in design initial concerns about cooling issues were studied using cooling simulation models. Currently, ten different trigger classes can be defined, allowing choices e.g. on the position of the firing chip and the multiplicity (see [5]).

2.4 Cooling

The major contribution to the on-detector power dissipation is due to front-end chips; they generate a nominal heat load of 23W per stave (20 chips). The design of the cooling system was driven by several constraints such as low material budget, long-term stability against corrosion, chemical compatibility, minimal temperature gradients, cooling duct temperature above the dew

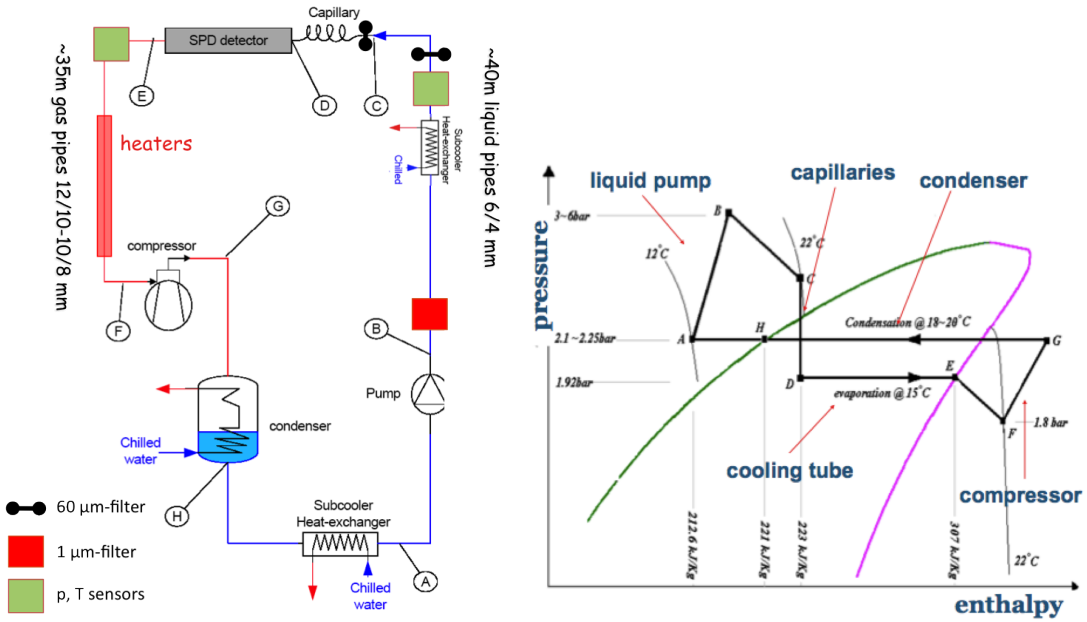

Figure 2: Left: cooling system simplified schema. Right: an example of Joule-Thomson cycle for the circuit on the left panel. The letters on the cycle correspond to the points of the circuit schema.

point. Several possible solutions based on different coolants were considered [6]. The final choice of an evaporative system with C_4F_{10} as coolant was found to fulfill all the requirements. In figure 2 a simplified scheme of the cooling circuit and a sketch of the thermodynamical cycle are shown [7]. The C_4F_{10} follows a Joule-Thomson cycle (rapid expansion at constant enthalpy and subsequent evaporation). The liquid, subcooled in a heat-exchanger tank, is compressed by a pump to a pressure sufficient to bring it in the liquid phase to the detector, along ten stainless-steel pipes about 40 m long. Below each stave, a groove in the CFSS hosts a cooling duct, kept in thermal and mechanical contact with the detectors by a thermal grease layer. The cooling duct is obtained using Phynox tubes with a wall thickness of 40 μm and an initial diameter of 2.6 mm, squeezed down to oval profile with an overall size of 600 μm in the thin dimension. The freon is brought to the coexistence phase inside the cooling duct by a pressure drop along the capillaries (0.5 mm internal diameter, 550 mm long). Heat abduction through phase transition takes place inside the cooling tube at 15°C corresponding to a coexistence pressure of 1.92 bar. On the return lines, approximately 35 m long, self-regulating heating cables are installed in order to get rid of any liquid remnants that could a) modify the return impedance, b) harm the compressors downstream. A compressor raises then the pressure pushing the gas towards a condenser, where the liquid phase is re-established by heat transfer to cold water (6°C). The evaporation temperature can be controlled by regulating the pressure in the return line, setting then the coexistence conditions of the mixed phase, currently common to the ten lines. The flow at the inlet is set by regulating the frequency of the pump, namely the liquid pressure, and a pressure regulator is installed on each line, which can be then independently tuned. Each sector is equipped with cooling collectors at the two ends, one functioning as an inlet and the other as an outlet for the whole sector. Each cooling line then feeds

the 6 staves of a sector. Extensive corrosion tests were performed on tubes, together with tests to optimize the choice of surface treatment and of fitting materials. In the final test, detectors were turned on at nominal power. An infrared camera was used to measure in the Departmental Silicon Facility (DSF) clean room the temperature distribution on the external part of the stave (i.e. the bus), on the MCM and on the power extenders (copper-polyimide laminates). Residual gaps due to mechanical tolerances of the surfaces in contact, partially compensated for by a thicker layer of thermal grease, can locally affect the quality of thermal coupling. The effect typically observed is a deviation from the average temperature (in the range of 25 °C to 30 °C) of ± 2°C along the stave. In normal operation, if a sudden failure of the cooling were to occur, the temperature at the half-stave would increase at a rate of 1 °C/s, whose disastrous effects are prevented by continuous monitoring and a fast, reliable safety interlock on each half-stave based on the on-bus Pt1000 temperature transducers. Two daisy chains of 5 transducers each (interleaved positions) provide redundant measurements of the average temperature. One chain is read out in the MCM, the other is hard-wired to the remote interlock system, based on a programmable logic controller (PLC) that is part of the detector control and safety system. Temperature values are logged. If the temperature reaches a preset threshold, the low-voltage power supply (which feeds a half sector, i.e. 6 half-staves) is promptly switched off by the safety interlock and an alarm is generated. A more refined control over the thermal behavior is provided using the temperature information fed to the MCM and then available in the data stream. Whenever a half-stave exceeds a given temperature threshold, the system is instructed to turn off that half-stave. While this implementation is much slower than the hardware interlocks (which are anyway present) it has the advantage of maintaining an alarm level which is lower and safer. When this alarm is triggered just one half-stave is shut down, while the hardware interlock acts on a half sector, allowing a faster recovery and limiting the thermal stress of the detector.

2.5 System controls

The ALICE Detector Control System is supervised by a SCADA system (Supervisory Control and Data Acquisition) based on the PVSSII software package [8]. The aim of the system is to supervise all the operations carried out in its structure and to react in case of misbehaviors. The ALICE Control Coordination (ACC) team in collaboration with every detector foresaw a series of constraints to integrate the control system of each sub-detector into a unique system. The detector control system (DCS) of SPD was designed according to such requirements, using where possible standard components for the ease of maintenance, while dedicated components have been developed for specific tasks. The logic state of the subsystems (power, cooling, front-end electronics) is controlled by the Finite State Machine (FSM), based on a State Management Interface (SMI++) and it is the logical part of the DCS since it manages the starting, intermediate and final states of the subsystems and it also reacts according to their changes. PVSSII is the link between the hardware components and the control logic which is controlled by the FSM. It can turn macroinstructions (i.e.: Go Off, Go Ready, etc) into a sequence of operations directed to the hardware. The correct sequence of actions is checked and errors are notified in case of hardware misbehavior. The FSM is the link between the SPD and the Alice DCS as it informs the latter on the general status of the detector (i.e.: Ready for data-taking, calibrating, etc.). About 5×10^4 parameters (DAC) are required to configure the SPD front-end electronics. For this reason a dedicated Front-End Device

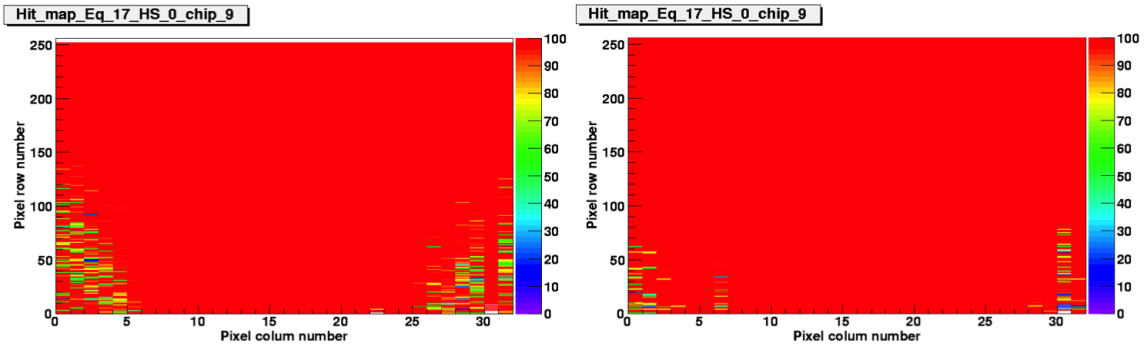

Figure 3: Left panel: hit map of a chip obtained with the internal pulser, before optimization. Right panel: the same as the left panel, after optimization. The efficiencies are respectively 92.6% and 98.6%.

(FED) driver was build to interface the PVSS layer with the SPD electronics. The FED receives macroinstructions and autonomously operates the front-end off-detector electronics. A direct connection reads and saves all the required parameters in the configuration Oracle database (CDB). The DCS of SPD is a distributed system composed of 4 PVSSII sub-projects which operate in 4 PCs (3 working nodes and 1 operator node). The working nodes, accessible only to expert users, are the computers used to control the detector. The User Interface (UI) is installed in the operator node where all users can login. One of the specific tasks in charge of the SPD DCS is the control of software interlocks on the cooling system, as explained in the previous section.

3. Commissioning and operation experience

The final integration and full pre-commissioning of the SPD was performed in the Departmental Silicon Facility at CERN using the final cooling plant and a full-scale configuration of power supplies, interlock and central systems such as data-acquisition and trigger. A large fraction of the debugging needed to bring the detector to full functionality has been done then, when a full set of configuration parameters for all the half-staves has been established. After the installation in the experimental hall of ALICE, the commissioning of all the components of the detector has been carried out, first with the internal pulser, which injects in each channel a charge equivalent to the one generated by a minimum-ionizing charged particle traversing the sensor, then with cosmic rays and finally a continuous verification and fine tuning is currently performed with proton-proton collisions [9]. The number of events amounts to $\approx 10^8$, which allowed a deep deployment of the detector, whose commissioning is still proceeding onto finer tuning. The original efficiency as of the day before the installation, obtained in the DSF laboratory, amounts to 100% concerning the cooling (all half staves were turned on at maximum power dissipation). The number of dead pixels measured by a Sr^{90} electron source, was $\sim 10^4$. During the commissioning with proton beams we were able to keep the number of noisy pixels to < 0.15 %. The overall number of dead pixels in working chips is less than 1.2%. The optimization of the detector goes through the tuning of the 42 8-bit DACs embedded in the front-end chip: most impact on the working conditions comes from the tuning of the current and voltage references, the trigger delay, the global voltage threshold and the leakage current compensation. In figure 3 a frequent situation is depicted, where the

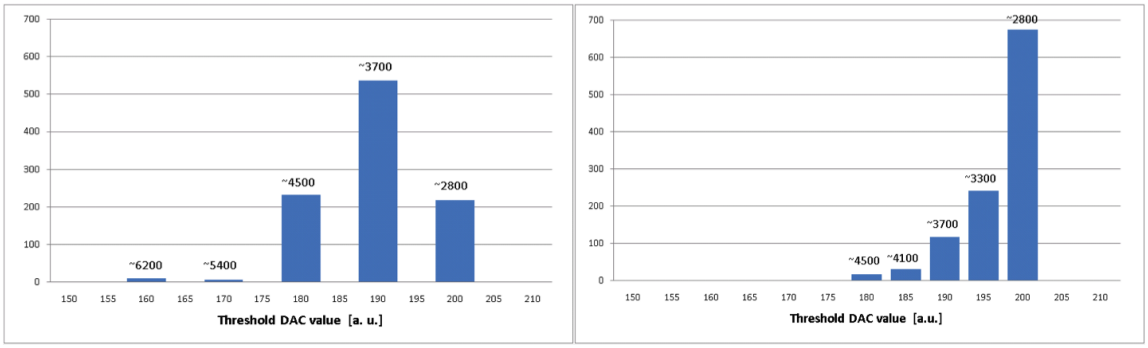

Figure 4: Thresholds distribution (in electrons) before (left) and after (right) the fine tuning.

inefficiency on the chips is mainly concentrated on the corners. In the specific case, the search of the best configuration, varying the reference current and voltage, the thresholds and the current to the charge preamplifier had as a result the improvement of the efficiency from 92.6 to 98.6%. The procedure is iterated for all the chips, with 100 test pulses per chip, asking for more than 95% efficiency of the response to pulses. The percentage of efficient chips went from 91% to 99% after the tuning, with a fraction of non-responding pixels from 2×10^{-3} to 7×10^{-4}. The analysis of these inefficiencies is still ongoing. The thresholds have been also optimized, with little impact on the number of noisy pixels. In figure 4 the distribution of the threshold values in electrons in shown before and after the optimization procedure. For the Fast-OR calibration an automatic procedure has been developed in order to obtain uniform results and to minimize the time needed for the 1200 chips (now 2-4 hours). This procedure is performed by means of dedicated computers running the calibration package based on the offline and DCS framework of ALICE. Four parameters are involved: the common chip threshold (Pre_VTH), the Fast-OR current pulse source (Fast_FOPOL), the current mirror voltage bias (Fast_CONVPOL), the Fast-OR comparator reference (Fast_COMPREF). Figure 5 shows a typical result of the Fast-OR calibration: the procedure has been applied over the full range of the DACs, the Fast-OR is plotted as a function of the two DACs Fast_CONVPOL and Fast_FOPOL. Three different regions can be identified: a) inefficiency, dark area with Fast-OR counts near zero, b) noise, bright area with very high Fast-OR counts and c) good region, area with Fast-OR counts equal to the number of test pulses sent. For the majority of chips (>95%) it is possible to find DAC values that have a 100% efficiency. These values have been verified in various trigger configurations, i.e. in cosmic runs (coincidence between the upper and lower half of the barrel) and in minimum-bias proton-proton runs (at least one hit in SPD). A reduced efficiency of the cooling system has been observed in certain detector areas. The temperature rises locally to values exceeding the safe limits, and the half-staves concerned cannot be continuously powered. This is currently the main limitation to the SPD efficiency, which is stable around 83%. The outcome of the in depth investigation indicated a lack of cooling fluid underneath some half-staves; this could be due to impurities clogging in the particulate sintered filters with 60 μm granularity placed right before the cooling collectors, in a region which is unfortunately not accessible at this moment due to the peculiar ALICE layout. A second set (see fig. 1), placed upstream SPD and always reachable during access permission in the experimental hall, have been

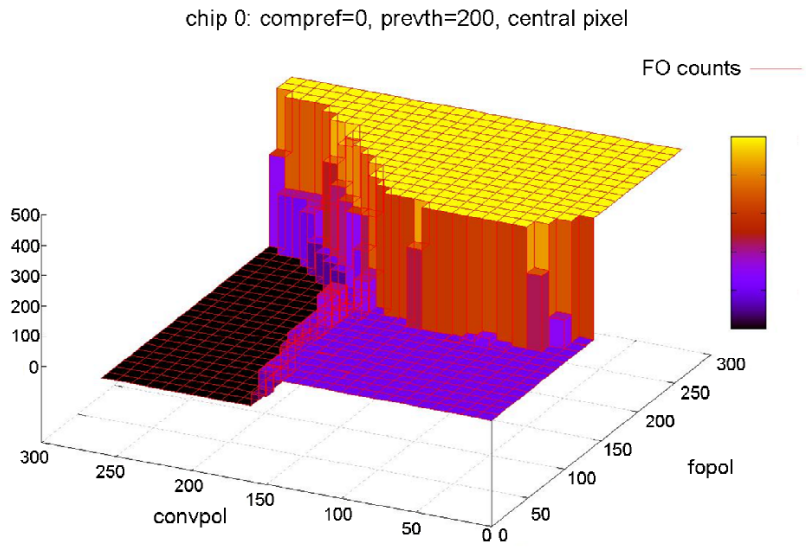

Figure 5: Results of the scan through the range of two DAC parameters on the Fast-OR efficiency (see text).

replaced and analyzed by electron microscope scanning; they have shown partial clogging due to micro-particles (sized 10-100 μm) of various substances. The unfavorable thermodynamic condition, which may also cause a degradation of the cooling performance, could be due to an earlier evaporation of the C_4F_{10} before it reaches the detector. This effect was ruled out by sub-cooling the C_4F_{10} close to the detector entrance (see fig. 1) by installing ten supplementary heat exchangers fed by water at 8°C. A careful tuning of the power dissipation from the chips, reducing the main current feed, while keeping the same level of performance in terms of efficiency and noise level, allowed a larger number of half staves to work in stable operation. The power and temperature distributions are shown in figure 6. The average temperature is quite satisfactory with respect to the design value. This observation is again related to a lack of freon flow in some lines, where the half stave cannot be turned on at all, while where the fluid heat capacity matched the requirement from the detector power consumption, the temperature is kept at an acceptable value. Despite the fact that the cooling system was designed with significant overcapacity with respect to the expected needs, the overall performance is not fully satisfactory. The proper actions will be taken during the next long shutdown; meanwhile, the monitoring and the tuning of the working conditions have been extensively improved and in particular the flow of the cooling fluid is continuously recorded, this being one of the key parameters for the operation of an evaporative cooling system, from which one can infer the amount of power that can be removed, although the regime of the fluid inside the circuitry, which plays also a fundamental role, cannot be unambiguously established.

Concerning the overall timing performance the detector readout time has been proven to be $\approx$300 μs, in very good agreement with the design value, and very slightly dependent on the occupancy, even at values well beyond those expected in collisions runs. The four-slot multi-event buffer embedded in the front-end chip allows a 0% dead-time up to a $\approx$3kHz trigger rate; the dead time increases at higher rate depending on the probability to fill an empty slot of the multi-event buffer. At 40 MHz the dead time becomes $\approx$3300 μs, corresponding to a maximum readout rate of

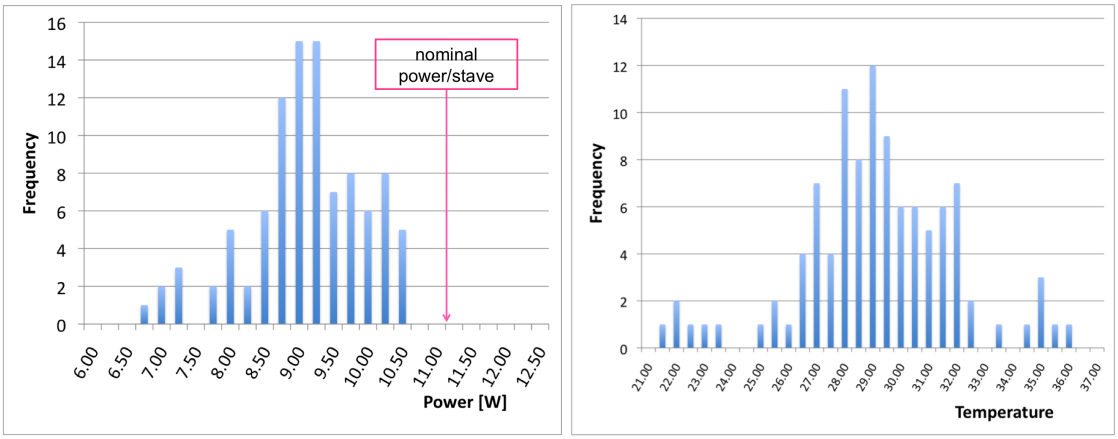

Figure 6: Left: power distribution of the active half-staves. The average is 9.8 W/half-stave. Right: temperature distribution, the average is 29°C, against a design value of 25°C.

≈3.3 kHz with 100% dead time.

4. Summary

The SPD detector has been installed and commissioned to reach a highly reliable and stable operation. The first few months of experience have permitted the collaboration a fine tuning of the system, notably of the Level-0 trigger (the Fast-OR) signal which is a unique feature, for a vertex detector, among the LHC experiments. It operates at 100% efficiency on >95% of the chips. The noisy pixels are contained in 0.15% and dead channels are approximately 1.2% (in operable chips). The first results are very satisfactory from the point of view of the tracking (see [10]): gross primary vertex localization, impact parameter resolution and track finding, which are the pillars of several ongoing analyses, have matched the expected performance. The first paper concerning LHC-collisions data has been published and is principally based on SPD data. Nonetheless, the status is not completely satisfactory. Apart from a few issues on the understanding of the behavior of electronics, our main concern is the reduced efficiency due to lack of cooling power. We have identified a few points that are responsible for this issue which is due to lack of flow and, possibly, thermodynamical conditions far from ideal in few spots of the cooling circuit. A partial solution has been applied, while the main intervention will be possible only during the long period of maintenance foreseen in 2012.

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