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Frequency Multiplier and Mixer MMICs Based on a Metamorphic HEMT Technology Including Schottky Diodes

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ABSTRACT This paper reports on the monolithic integration of layout-optimized Schottky diodes realized in an established 50-nm gate-length metamorphic high-electron-mobility transistor technology for use in multifunctional nonlinear circuits. The suitability of the realized Schottky diodes is demonstrated by a broadband millimeter-wave I/Q-mixer (In-phase/Quadrature) and local oscillator (LO) chain comprising two power amplifiers and a frequency tripler, fabricated on monolithic microwave integrated circuits (MMICs). Both circuits are based on an anti-parallel Schottky diode topology. The subharmonically-pumped I/Q-mixer covers an RF (radio frequency) and IF (intermediate frequency) range of at least 75 GHz to 110 GHz and 0.5 GHz to 15 GHz, respectively. The single-sideband conversion loss is between 14 dB and 16 dB across most of the entire RF and IF bands. The core of the LO chain consists of a frequency tripler (multiplier by three) and features a bias-adjustable output power with almost constant conversion efficiency and a control range of more than 8 dB. The fully-integrated LO chain MMIC matches the needs of the presented I/Q-mixer and exhibits an average output power of 16.3 dBm with a covered frequency range of 38 GHz to 60 GHz. The unwanted harmonics are suppressed by at least −25.9 dBc below the third harmonic for the entire frequency range and better than −32.1 dBc for most part of the band. Thus, the mixer and tripler MMICs demonstrate state-of-the-art performance with regards to, e.g., covered bandwidth, output power, harmonic suppression, or 1 dB compression point.

INDEX TERMS High-electron-mobility transistors (HEMTs), Ku-band, millimeter wave (mmW), monolithic microwave integrated circuits (MMICs), mixers, frequency multipliers, power amplifiers (PAs), Schottky diodes, U-band, varactors, W-band.

I. INTRODUCTION

Nonlinear circuits are core building blocks in several systems implementations. Due to a considerably wide atmospheric window, the W-band frequency range (75 GHz to 110 GHz) is appealing for a multitude of applications, such as radio astronomy, wireless communication, or radar systems. Commonly, radio astronomy aims for an even wider bandwidth of at least 72 GHz to 116 GHz and for an extensive integration of system building blocks on a single piece of semiconductor. State-of-the-art nonlinear circuits, e.g. mixers and frequency multipliers, are successfully realized with Schottky diodes [1], [2], whereas state-of-the-art low-noise amplifiers (LNAs) [3] or power amplifiers (PAs) [4], require transistors for signal amplification. In the frequency range of 50 GHz to 110 GHz, hybrid diode-based frequency triplers achieve conversion efficiencies (*CE*) of −14 dB to −12 dB with an output power of more than 10 dBm for an entire waveguide band [2]. Monolithic microwave integrated circuit (MMIC) solutions with dedicated Schottky-diode technologies exhibit an average output power and *CE* of about −2 dBm and −18 dB, respectively, and operate in W-band [5]. Active frequency tripler MMICs seem to be rather band limited, at least if a good harmonic suppression is required.

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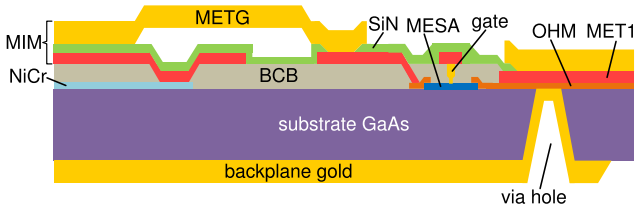


FIGURE 1. Simplified cross section of the layer stack of the utilized 50-nm gate-length mHEMT technology [4].

Therefore, a monolithic integration of Schottky diodes and transistors can help to combine the advantages of both devices. However, especially for field-effect-transistor (FET) technologies, a monolithic integration of diodes and transistors without considerably changing the transistor process is a major challenge. Hence, those technologies commonly tend to realize linear as well as nonlinear circuits with transistors. Though, high-electron-mobility transistors (HEMTs) feature a Schottky gate which offers the possibility of a monolithic integration of HEMTs and Schottky diodes. This was discussed before, e.g., in [6], however, only for diode layouts that use exclusively transistor fingers. Thus, it is the aim of this work to investigate, in an established metamorphic HEMT (mHEMT) technology, possible implementations and layouts of Schottky diodes that are beyond an exclusive use of transistor fingers as diodes. Therefore, Section III analyzes the layout optimization of Schottky diodes which are fabricated in the Fraunhofer IAF 50-nm gate-length mHEMT technology and discusses an optimized diode structure for frequency multiplier and mixer circuits. Based on these results, a dedicated circuit for the varactor and varistor behavior is discussed and Section IV and V demonstrate broadband mixer and frequency multiplier MMICs, respectively. Both MMICs are based on anti-parallel diodes (APD). The mixer utilizes a subharmonically-pumped approach and targets RF and IF bandwidths of at least 75 GHz to 116 GHz and 4 GHz to 12 GHz, respectively. Furthermore, the mixer should be suitable for sideband-separating receiver (2SB) topologies. To drive the mixer MMIC with a local oscillator (LO) with an input frequency and power below 20 GHz and 0 dBm, respectively, the frequency multiplier features a Schottky-diode-based tripler unit cell (x3), as well as input and output driver PAs. This monolithic integration demonstrates as well a major benefit of this work. The multiplier MMIC is matched to the needs of the I/Q-mixer MMIC and aims for an output power of more than 15 dBm over a bandwidth of 40 GHz to 60 GHz. The suppression of unwanted harmonics, especially the neighboring second and fourth harmonics, is of particular importance.

II. 50-NM MHEMT TECHNOLOGY

The presented work is based on the Fraunhofer IAF 50-nm gate-length InAlAs/InGaAs mHEMT technology. For a lattice matched growth of the HEMT layers on 100-mm semi-insulating GaAs wafers, a metamorphic buffer with a linear $In_xAl_{0.48}Ga_{0.52-x}As$ ($x = 0 \rightarrow 0.52$) transition is used. The two-dimensional electron gas is confined in an $In_{0.8}Ga_{0.2}As/In_{0.53}Ga_{0.47}As$ composite channel. The T-gates are defined by electron beam (e-beam) lithography and are encapsulated in benzocyclobutene (BCB). The e-beam lithography and the corresponding four-layer resist stack is designed so that precise 50-nm T-gates and any other rectangular-shaped Schottky contacts are possible. Thus, the Schottky diodes that are investigated in this work are simultaneously available with mHEMTs without changing the established process flow. This is an important feature for the Schottky diode investigation in this work. The wafer is passivated with a 250-nm-thick SiN layer which also acts as the dielectric layer of the on-wafer metal–insulator–metal (MIM) capacitors and is deposited by chemical vapor deposition (CVD). Further passive elements comprise NiCr thin film resistors, an electron beam evaporated Au based interconnection layer, and a 2.7-µm-thick plated Au layer in air bridge technology. The technology includes a full back-side process with wafer thinning to 50-µm thickness, through substrate via holes, and back side metallization. In Fig. 1, a simplified cross section of the layer stack of the 50-nm gate-length mHEMT technology is illustrated. The transistors feature an extrinsic transition and maximum oscillation frequency of 375 GHz and 670 GHz, respectively. The maximum drain current density is 1300 mA/mm and the maximum transconductance is 2100 mS/mm. Further technology details are given in [7].

III. HEMT-BASED SCHOTTKY DIODES

The fundamental principle of a mixer or multiplier is the use of a device with a nonlinear characteristic. HEMT-based Schottky diodes feature two nonlinearities when a diode is used as varistor or varactor. In a varistor the nonlinearity of the junction resistance (R_J) or current-voltage characteristic (IV) is used. Instead, in a varactor junction the capacitance (C_J) or capacitance-voltage characteristic (CV) is utilized. The main parasitic parameters of a diode are the series resistance (R_S) and the extrinsic capacitance. R_S includes the resistances of the ohmic contact at the cathode, the interconnection metals, and the two-dimensional electron gas. The extrinsic capacitance is dominated by, e.g., fringing fields and the coupling between gate head and ohmic contact. It is the aim of this section to investigate possible layouts of Schottky diodes in order to optimize the IV and CV characteristics.

The most obvious layout variation of a Schottky diode that is based on a HEMT process is a single transistor finger in which the source and drain regions are connected together and form the cathode. An advantage of such a finger diode is that the series resistance can be considerably small since the length of the ohmic contact is large compared to the area of the Schottky contact. However, a disadvantage is that the corresponding parasitic capacitance is rather large. For a point-contact-like diode, such as circular or square-shaped Schottky contacts, the advantages and disadvantages are contrary to those of a finger diode. The capacitance of a square-shaped diode layout is dominated by the intrinsic

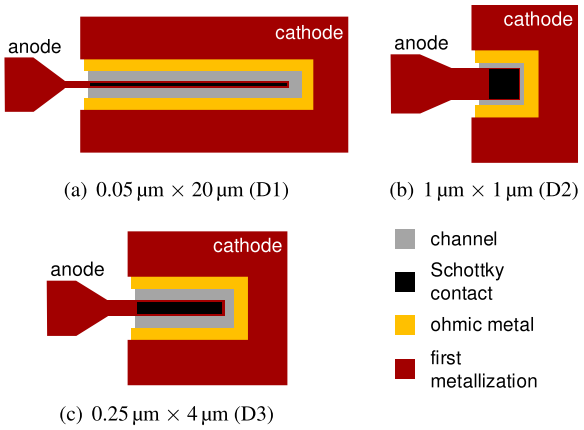


FIGURE 2. Simplified layout of the three discussed Schottky diode variations.

junction capacitance and the parasitic part is considerably small. However, the series resistance will be increased.

Consequently, the investigation comprises three different Schottky diode layouts that are illustrated in Fig. 2. To compare the different parameters adequately, we assume that all diodes have an area of the Schottky contact of 1 µm^2. The first two diodes are a gate-finger diode (D1) and a point-contact diode (D2) with a shape of the Schottky contact of 0.05 µm × 20 µm and 1 µm × 1 µm, respectively. The third variation (D3) is a tradeoff between advantages and disadvantages of the point-contact and gate-finger diode layouts having a shape of 0.25 µm × 4 µm. Hence, D3 can be seen as a finger-diode with a gate length of 0.25 µm.

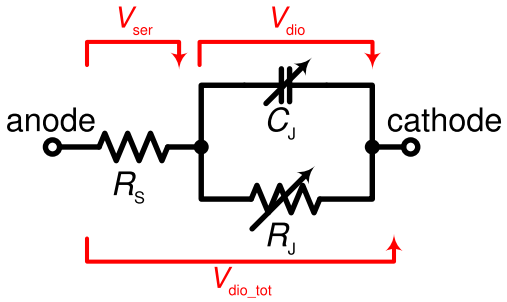


FIGURE 3. Schematic of a simplified diode model.

First, the CV characteristic of the three diode layouts is investigated which is mainly important for diode-based frequency multipliers. The figure of merit that is used to evaluate the behavior of the different diodes in a varactor mode is the cut-off frequency of a varactor ($f_{c,var}$) [8]

$$f_{c,var} = \frac{1/C_{min} - 1/C_{max}}{2\pi R_S}, \tag{1}$$

where C_{min} and C_{max} are the minimum and maximum of the total diode capacitance, respectively. The extraction of the diode parameters is based on a simplified diode model that is illustrated in Fig. 3. The variable capacitance is fitted to 2-port S-parameters of fabricated Schottky diodes that are

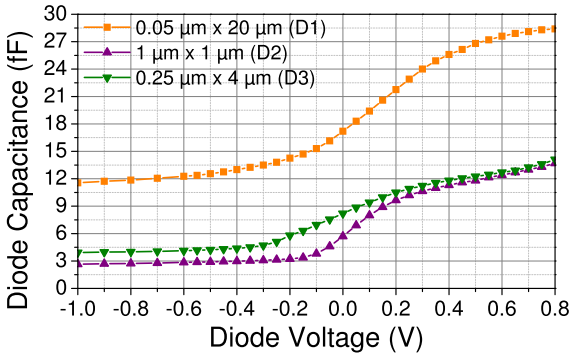


FIGURE 4. Diode capacitance versus diode voltage for three fabricated diode versions.

measured from 0.01 GHz to 150 GHz for diode voltages from −1 V to 0.8 V. The extracted CV characteristic of the three fabricated diodes is shown in Fig. 4. C_{min} and C_{max} are the capacitances for voltages of −0.7 V and 0.7 V, respectively. The nonlinearity of the CV characteristic is important for an efficient frequency multiplication and is visualized by the capacitance modulation ratio (ΔC_{dio}) which is given as

$$\Delta C_{dio} = \frac{C_{max}}{C_{min}}. \tag{2}$$

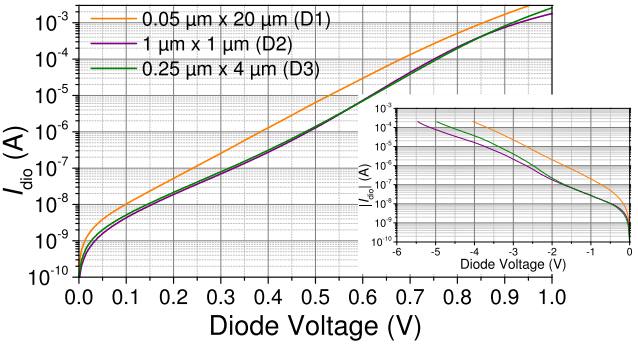


FIGURE 5. Measured diode current versus diode voltage for three fabricated diode versions. The IV characteristic is measured with a forward and reverse voltage sweep using a current limit for reverse and forward direction of 0.2 mA and 3 mA, respectively.

R_S is fitted to dc measurements between 0.5 V to 0.95 V and is verified with measured S-parameters of the diodes. Especially at higher frequencies, R_S starts to dominate the response of a diode. In Fig. 5, the measured IV characteristic for the three diode versions is shown. For all diodes, the reverse breakdown is defined for an absolute current of 0.2 mA. In case of a finger diode, this refers to a normalized gate current of 10 mA/mm (normalized to the gate width). The reverse breakdown voltage of D1, D2, and D3 is about 4 V, 5.4 V, and 5 V, respectively. Consequently, the finger diode features the lowest breakdown voltage, whereas the point-contact diode has the highest breakdown voltage.

The extracted parameters are summarized in Table 1 and confirm the expected behavior of the different diodes. While the finger diode has the lowest R_S, it features the

TABLE 1. Parameters of fabricated schottky diodes.

Diode	C_{min} (fF)	C_{max} (fF)	ΔC_{dio}	R_S (Ω)	I_{sat} (nA)	n	$f_{c,var}$ (GHz)
D1	12.05	28.1	2.3	6.5	3.47	2.61	1161
D2	2.775	13	4.7	38	0.14	2.18	1187
D3	4.05	13.25	3.3	21	0.29	2.33	1299

highest C_{min} and the lowest ΔC_{dio} as a result of an increased parasitic capacitance. The square-shaped diode has the lowest C_{min}, the highest ΔC_{dio}, and the largest relative change of C_{dio} for the smallest voltage range. Thus, the square-shaped diode features the strongest CV nonlinearity, however, exhibits also the highest R_{S} of the tested layouts. The 0.25-µm × 4-µm-shaped diode is for both parameters, R_{S} and ΔC_{dio}, between the values of D1 and D2. Due to a considerably high ΔC_{dio} and a moderate R_{S}, D3 features the highest $f_{\text{c,var}}$ and is considered as the best tradeoff for a varactor-based application. Consequently, the U-band frequency-tripler MMIC which is presented in Section V utilizes 0.25-µm × 4-µm-shaped diodes.

For mixer applications, the nonlinearity of R_{J} is the most important characteristic. For the evaluation of the three diode layouts, the diode ideality factor (n) and the saturation current (I_{sat}), in combination with R_{S}, are used. I_{sat} and n are intrinsic diode parameters. The intrinsic diode current (I_{dio}) is given as [9]

$$I_{\text{dio}} = I_{\text{sat}} \left(e^{\frac{V_{\text{dio}}}{nV_{\text{t}}}} - 1 \right), \tag{3}$$

where V_{t} is the thermal voltage and V_{dio} is the voltage across the intrinsic part which includes R_{J} and C_{J}. However, when measuring the dc characteristic of a diode, the measured diode voltage is the total voltage ($V_{\text{dio\_tot}}$) across R_{S} and R_{J}

$$V_{\text{dio\_tot}} = V_{\text{dio}} + V_{\text{ser}} \tag{4}$$

$$= nV_{\text{t}} \cdot \ln \left(\frac{I_{\text{dio}}}{I_{\text{sat}}} + 1 \right) + I_{\text{dio}} R_{\text{S}}. \tag{5}$$

Based on (5), I_{dio} is given as

$$I_{\text{dio}} = \frac{nV_{\text{t}}}{R_{\text{S}}} \cdot W \left(\frac{I_{\text{sat}} R_{\text{S}}}{nV_{\text{t}}} e^{\left(\frac{I_{\text{sat}} R_{\text{S}}}{nV_{\text{t}}} + \frac{V_{\text{dio\_tot}}}{nV_{\text{t}}} \right)} \right) - I_{\text{sat}}, \tag{6}$$

where $W(x)$ is the Lambert W function of x. For extracting n and I_{sat}, (6) is fitted to measured IV curves between 0.2 V and 0.7 V. D1 to D3 exhibit ideality factors and saturation currents of 2.61, 2.18, and 2.33, as well as 3.47 nA, 0.14 nA, and 0.29 nA, respectively. The point-contact diode (D2) shows the lowest n and I_{sat}. The 0.25-µm × 4-µm-shaped diode (D3) yields very comparable performance, whereas the saturation current of the finger diode (D1) is more than an order of magnitude higher and the ideality factor is also by far the highest. Since, compared to D3, R_{S} of D2 is almost by a factor of two larger, it is concluded that D3 also features the best tradeoff for mixer circuits. Hence, the W-band mixer MMIC which is demonstrated in Section IV utilizes diodes with a Schottky contact of 0.25 µm × 4 µm.

IV. BROADBAND W-BAND I/Q-MIXER MMIC

In this section, a broadband W-band I/Q-mixer MMIC is presented. The aim is to use this circuit in a sideband-separating receiver in combination with an off-chip 90° IF hybrid, which is not part of this work. The presented mixer MMIC contains a Lange coupler as 90° RF hybrid, two subharmonically-pumped mixer unit cells, and a Wilkinson power splitter for the LO distributions. A block diagram of the mixer MMIC is illustrated in Fig. 6. The intended baseline frequency ranges for the RF input (f_{RF}), IF output (f_{IF}), and LO input (f_{LO}) are summarized in Table 2 including the design goals with slightly increased frequency ranges. For each part of the RF bandwidth, the LO frequency is fixed. In order to cover the entire RF range with the given IF bandwidth, the LO steps within the LO frequency range. In combination with a frequency tripler in the LO chain, the LO input signal for the mixer can be provided by a signal generator operating in a frequency band of 14.5 GHz to 18 GHz (baseline, 13.67 GHz to 18 GHz goal) thus avoiding leakage into the IF band due to the fundamental drive of the tripler or the various mixing products within the LO chain.

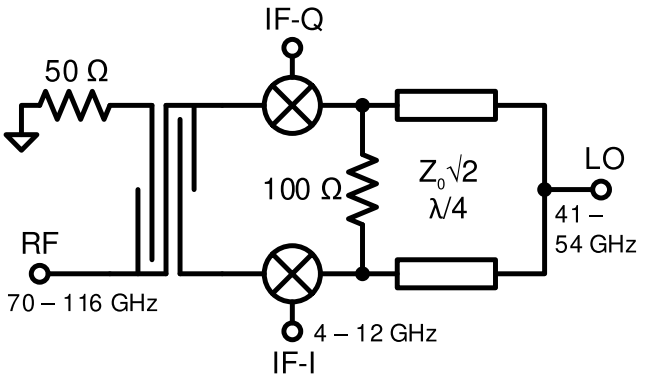


FIGURE 6. Block diagram of the presented subharmonically-pumped W-band I/Q-mixer MMIC.

TABLE 2. Design goals for the broadband I/Q-mixer MMIC.

	Baseline	Goal
RF input (GHz)	75–116	70–116
IF output (GHz)	4–12	2–16
LO input frequency (GHz)	43.5–54	41–54

This section discusses, first, the 90° RF hybrid and, secondly, the entire subharmonically-pumped W-band I/Q-mixer MMIC. In this work, conversion loss (CL) or conversion gain of a mixer is understood as a single-sideband parameter. This results in a factor of two higher CL when compared to double-sideband values.

A. W-BAND LANGE COUPLER

For a sideband-separating mixer, the symmetry of the I and Q paths is essential. This means that the sideband separation

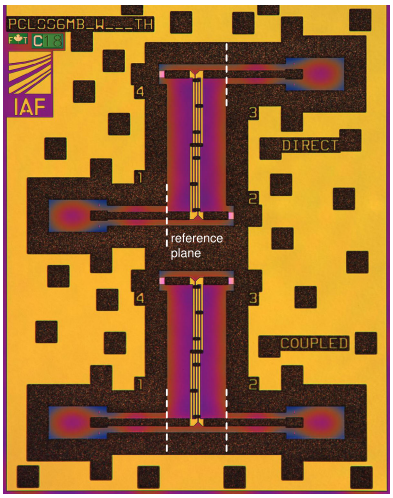


FIGURE 7. Chip photograph of a two-port on-wafer test structure of the fabricated W-band Lange coupler. The dashed lines indicate the calibration reference planes.

depends on an amplitude and phase balance between the I and Q paths, which should be as close as possible to unity and 90°, respectively. Since the 90° RF hybrid splits the RF input signal into the I and Q signals, these requirements are especially important for the Lange coupler. Thus, the design goal for the Lange coupler is an amplitude balance and phase error of better than ±0.5 dB and ±1°, respectively. The return loss of all ports should be as good as possible in order to avoid reflections or standing waves mainly at the RF input of the mixer MMIC.

The Lange coupler is based on the commonly-known approach with four interdigitated strips [10]. The coupler is designed in a microstrip-line environment and is fed by grounded-coplanar-waveguide (CPWG) transmission lines. A major challenge for Lange couplers on a 50-µm-thick GaAs substrate is the width and spacing of the strips since both parameters are typically close to the limits of the design rules. Thus, four additional air bridges are used to slightly increase the coupling between the interdigitated strips so that the design goals can be accomplished. Fig. 7 shows a chip photograph of the fabricated test structure. The simulated and measured results are depicted in Fig. 8. A good agreement between measurements and simulations can be observed. For a frequency range from 66 GHz to 118 GHz, the amplitude and phase balances are within the design targets of ±0.5 dB and ±1°, respectively. The loss of the coupler is in the range of 0.4 dB to 0.6 dB. The return loss of input and output ports is better than 20 dB for the entire frequency range.

B. SUBHARMONICALLY-PUMPED W-BAND I/Q-MIXER MMIC

The I/Q-mixer contains the described Lange coupler at the RF input port, two mixer cells, and a Wilkinson power splitter for LO distribution. A simplified schematic of the mixer cell is illustrated in Fig. 9. The mixer cell is based on a

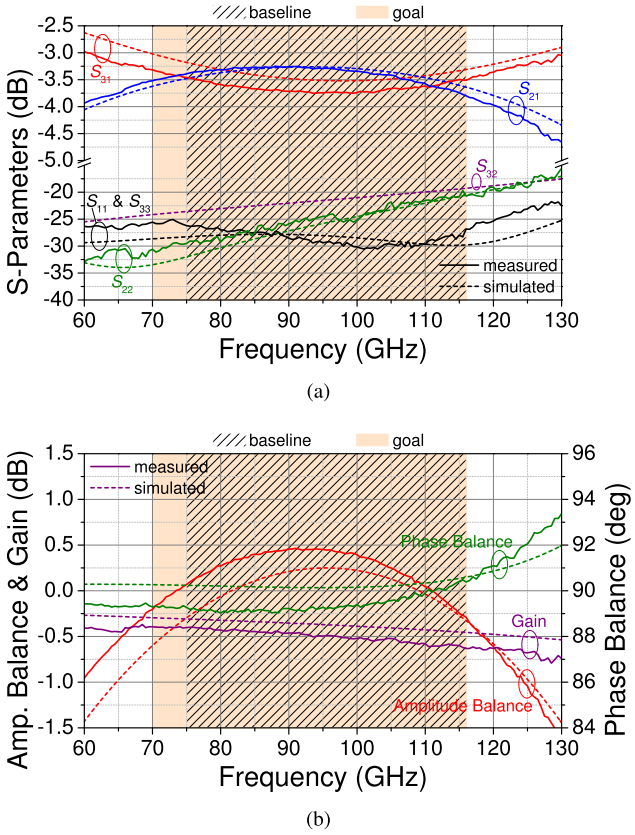


FIGURE 8. (a) S-parameters and (b) amplitude balance, phase balance, and gain of the fabricated W-band lange coupler.

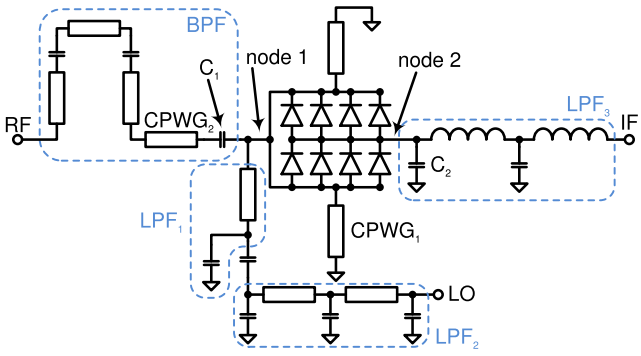


FIGURE 9. Simplified schematic of the mixer cell which is utilized by the presented subharmonically-pumped W-band I/Q-mixer MMIC.

subharmonically-pumped anti-parallel Schottky-diode mixer topology so that the RF is given as

$$f_{RF} = 2 \cdot f_{LO} \pm f_{IF}. \tag{7}$$

Due to the APD approach, the mixer can operate as up- or downconverter. However, this work aims for receiver applications and, thus, focuses on the down conversion.

In order to achieve a considerably high input 1 dB compression point ($P_{1\,dB}$), the circuit comprises eight Schottky diodes as described in Section III. The LO and RF input signals are supplied on one side of the anti-parallel diodes (node 1),

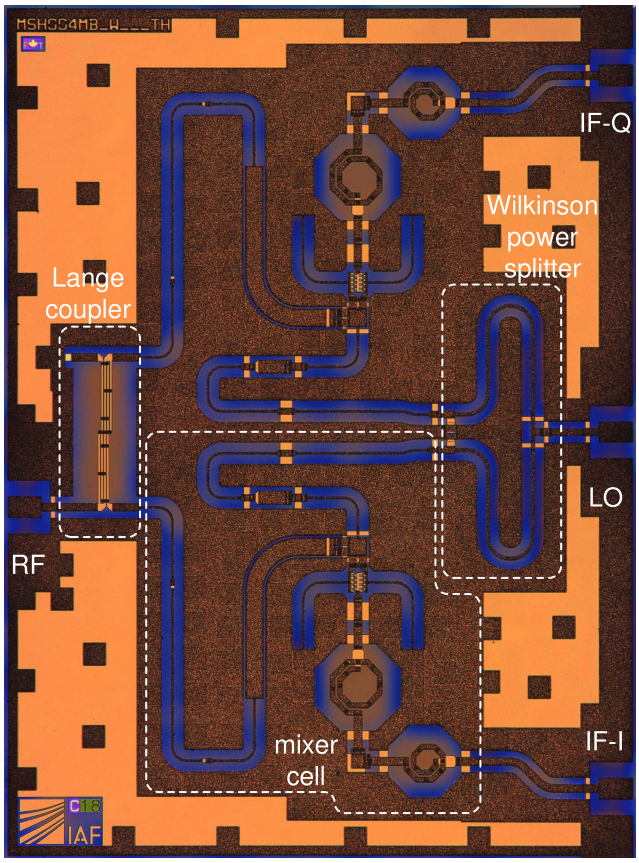


FIGURE 10. Chip photograph of the I/Q-mixer MMIC with a size of 1.5 mm × 2 mm.

whereas the IF output is on the other side (node 2). At node 1, a shorted stub ($CPWG_1$) is connected which is mainly used for matching the RF input. The length is about 80 % of a quarter-wave transformer for W-band frequencies. It also provides a dc ground to the diodes. For a wideband frequency response, $CPWG_1$ features a high characteristic impedance. The band-pass filter (BPF) at node 1 includes two features. First, it blocks the injected LO signal to leak into the RF path. Secondly, $CPWG_2$ (quarter-wave transformer) transforms the internal impedance level of about 20 Ω at node 1 to 50 Ω at the RF input port. In order to present an open circuit to the LO signal towards the RF path at node 1, a considerably small capacitor (C_1) is used. A further blocking of the LO signal is achieved by two sections of a series line-capacitor-line topology. The transmission lines feature again a high characteristic impedance. The LO blocking is important to avoid a loss of LO input signal into the RF path, which would increase the required LO drive, and to prevent possible standing waves of the LO signal in case the RF port is highly reflective for LO frequencies, e.g., below the cut-off of a WM-2540 (formerly WR-10) waveguide ($\nu_{TE10} = 59$ GHz).

The low-pass filter at node 1 (LPF_1) presents an open circuit for the RF input signal towards the LO supply path. This improves the conversion gain of the mixer cell since the leakage of RF signal into the LO path is distinctly reduced. LPF_2 has two features. First, it further improves the open circuit for RF signals at node 1 and, secondly, it blocks unwanted higher harmonics that might be present in the injected LO signal. At node 2 (IF port), LPF_3 is connected. C_2 is chosen to present a short circuit for RF and LO frequencies. This improves the conversion gain and reduces the required LO drive power since the voltage swing of the RF and LO input signal now mainly drops across the Schottky diodes. Additionally, C_2 increases the RF-to-IF and LO-to-IF isolation. LPF_3 contains an inductor-capacitor-inductor tee network which further improves RF&LO-to-IF isolation of the IF port and matches the IF port to an impedance of 50 Ω. The first of which prevents a possible compression of a subsequent IF LNA due to a high (out-of-band) LO input signal. The latter of which avoids standing waves of the IF signal in case the input matching of a subsequent IF network is poor.

The W-band mixer MMIC was tested on wafer level as downconverter. The LO drive signal was provided by a Keysight signal generator with an additional power amplifier. The RF signal was supplied by a chain which consists of a Keysight signal generator, a multiplier by 6, a power amplifier module, and a motorized waveguide attenuator for adjusting the RF test signal. Due to the multiplier by 6, the measurement setup limits the RF input range to 75 GHz–110 GHz. The IF output signal was connected to a Keysight signal analyzer (N9030A). All ports were calibrated to the probe tip. When measuring the IF output signal at port IF-I, IF-Q was terminated with a coaxial termination at the connector of the probe tip or vice versa.

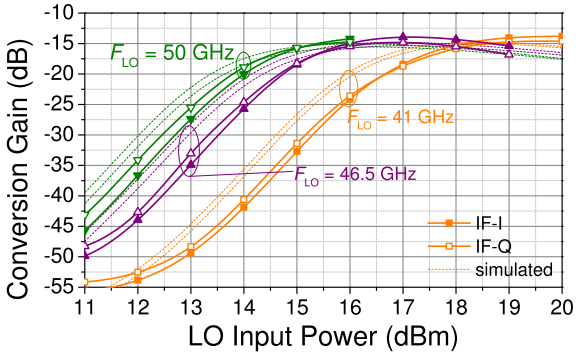


FIGURE 11. Measured conversion gain versus LO input power of the presented mixer MMIC for three different LO frequencies. The IF of the USB is 4 GHz. The conversion gain of the IF-I and IF-Q output is indicated by filled and open symbols, respectively.

Fig. 11 shows the upper-sideband (USB) conversion gain versus LO input power for LO frequencies of 41 GHz, 46.5 GHz, and 50 GHz. The RF signal was injected at frequencies of 86 GHz, 97 GHz, and 104 GHz with a power of −20 dBm. An optimum conversion gain for LO frequencies of 41 GHz, 46.5 GHz, and 50 GHz can be observed for an LO power of 19 dBm, 17 dBm, and 16 dBm, respectively. For these power levels, the conversion gain is measured for the lower sideband (LSB) and USB for the same LO frequencies. The results are illustrated in Fig. 12. For the three measured

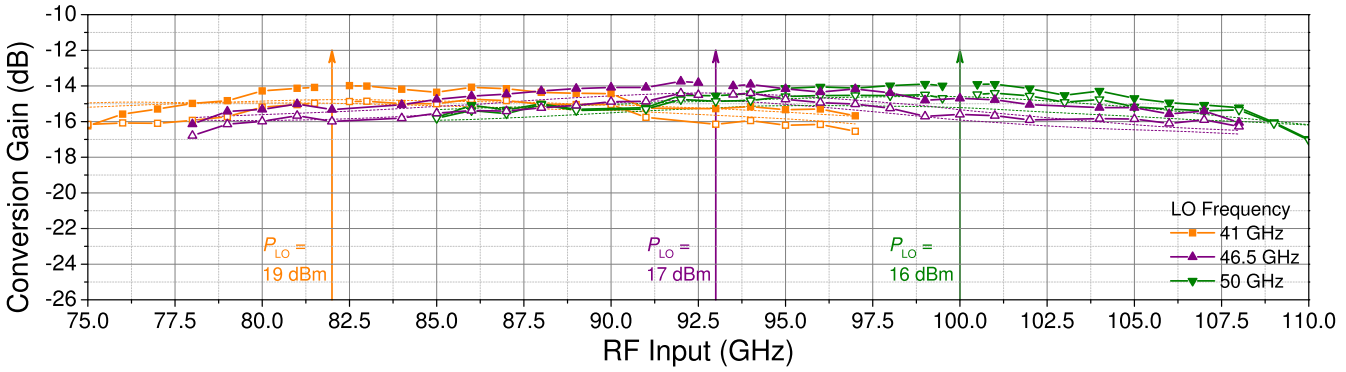


FIGURE 12. Measured conversion gain of LSB and USB versus RF input for three different LO frequencies. The arrows indicate the doubled LO frequencies. The RF input power is set to −20 dBm and the conversion gain of the IF-I and IF-Q output is indicated by filled and open symbols, respectively.

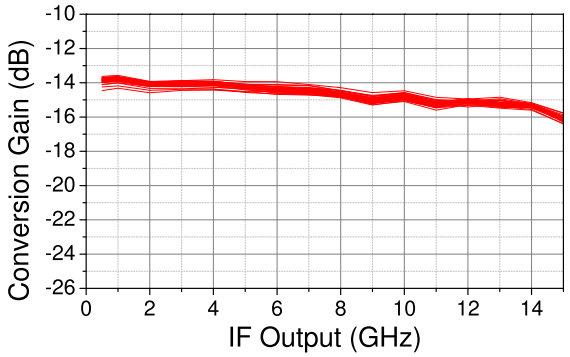


FIGURE 13. Wafer mapping of the fabricated W-band I/Q-mixer MMIC including 35 measured cells out of 37 cells on a wafer. The conversion gain of the LSB of the I path is measured for an LO frequency and input power of 46.5 GHz and 17 dBm, respectively. The RF input power is fixed at −20 dBm.

LO frequencies, the conversion gain exhibits peak values of about −14 dB, whereas the difference between I and Q path is 1 dB or less. The IF is measured from 0.5 GHz to 15 GHz for the three LO frequencies and both sidebands. Almost for the entire W-band, the conversion gain lies between −14 dB and −16 dB so that a drop of only 2 dB or less can be observed for high intermediate frequencies. Dashed lines indicate the simulated conversion gain and show a very good agreement with the measured results. Fig. 13 shows the measured LSB conversion gain for 35 devices of a 37-cell wafer. The conversion gain of the LSB shows a spread of less than 0.8 dB over the entire wafer. In Fig. 14, the conversion gain compression is given for an LO frequency and RF input of 46.5 GHz and 97 GHz, respectively. Measurements and simulations are in good agreement and exhibit a $P_{1\,\mathrm{dB}}$ of 5 dBm RF input power.

V. BROADBAND FREQUENCY TRIPLER MMIC

For broadband frequency multipliers, the suppression of unwanted harmonics can be a major challenge or even impossible if the suppression is primarily based on filtering of already generated harmonics. For example, in the case of LO-systems with a wide tuning range, neighboring harmonics of the desired LO-signal often fall into the LO's frequency band. This precludes using filters for their suppression at all. Therefore, anti-parallel diode triplers are highly beneficial since even harmonics of the input frequency will be suppressed completely in the case of a perfectly symmetric circuit. In practice however, achievable suppression will be finite due to unavoidable asymmetries in the diodes and the circuit. Thus, the core of the presented MMIC is an anti-parallel Schottky-diode tripler. Harmonic suppression on an LO-system is further discussed in [11].

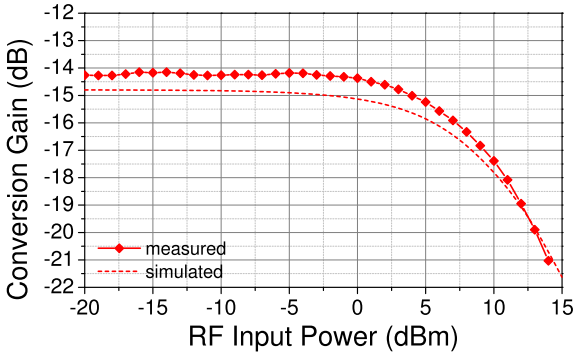


FIGURE 14. Measured (symbols) and simulated (dashed) conversion gain versus RF input power for an LO frequency and RF of 46.5 GHz and 97 GHz, respectively. The LO input power is 17 dBm.

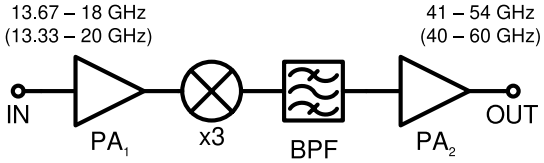


FIGURE 15. Block diagram of the presented frequency tripler MMIC. The intended frequency range is given in brackets.

The frequency tripler MMIC contains a Ku-band driver PA (PA_1), a Schottky-diode-based x3, and an output PA (PA_2). The MMIC features a monolithic integration of the described varactor diodes. A simplified block diagram of the

circuit is illustrated in Fig. 15. The design specifications of the tripler MMIC are based on the measurement results of the I/Q-mixer MMIC (see Section IV). The required output frequency range of the third harmonic (H3) is from 41 GHz to 54 GHz. However, the aim is to cover at least the entire U-band (40–60 GHz). The output power and the suppression of the unwanted harmonic frequencies should be more than 15 dBm over the band and below −20 dBc, respectively. The harmonic suppression is understood as the output power of an unwanted harmonic relative to the output power of the wanted third harmonic at a corresponding input frequency.

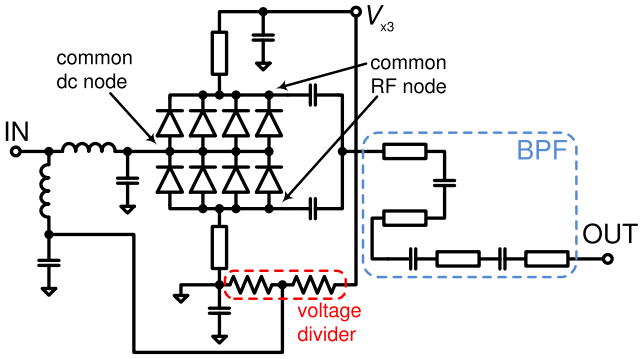
In general, nonlinear circuits tend to generate broadband noise at the output when operated in saturation. For narrowband applications this imposes no problems since a band-pass filter can be used to suppress most of the generated noise floor. However, for broadband applications this is hardly possible. Thus, it is the idea of this circuit that amplifiers operate as linearly as possible and that the x3 unit cell generates as much output power at the third harmonic as possible. The first requirement allows to avoid the generation of unwanted harmonics and broadband noise. The second requirement leads to less gain of PA_2 at the output of the tripler needed to achieve the desired output power of the multiplier MMIC. This is beneficial since thereby signal to noise ratio at the input of PA_2 can be improved thus minimizing broadband noise at the output of the tripler MMIC. All circuits and subcircuits are designed in a CPWG environment to allow a compact layout while avoiding strong coupling between subcircuits. The ground-to-ground spacing of the CPWG is 50 µm.

This section is organized according to the design flow of the presented monolithic integrated frequency tripler MMIC which is shown in Section V-D, following the investigation of individual subcircuits. First, the tripler unit cell is discussed in Section V-A. Secondly, based on the results of Section V-A, the design and results of the Ku-band and U-band driver PAs are demonstrated in Section V-B and V-C, respectively.

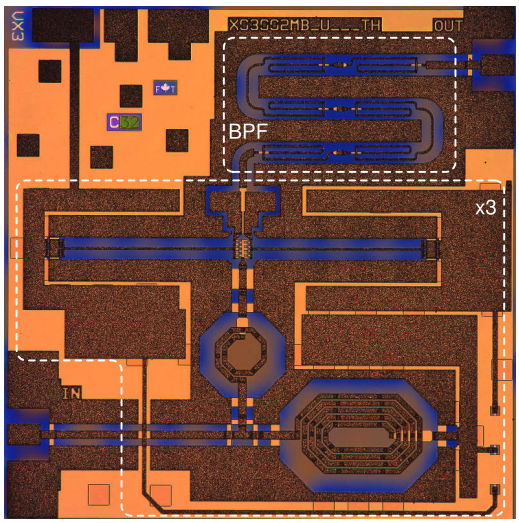
A. FREQUENCY TRIPLER UNIT CELL

The frequency tripler unit cell is based on an anti-parallel diode topology that was introduced by [12]. Therefore, the varactor characteristic of the presented Schottky diodes is used. A major design feature of this APD approach is that, even though it is a series APD multiplier, a bias voltage can be supplied to the diodes. This enables the adjustment of the output power of the x3 while keeping the conversion efficiency constant. By supplying a negative voltage across the diode below the threshold voltage of the CV characteristic, a large magnitude of the RF voltage swing across the diode is achieved. The more negative the bias voltage, the more input power can be injected. Theoretically, the lower limit of the bias voltage is when the voltage swing across the diode reaches the breakdown voltage.

A simplified schematic of the tripler unit cell is depicted in Fig. 16(a). A major goal of the input drive of a varactor-based frequency multiplier is to achieve a voltage



(a)



(b)

FIGURE 16. (a) Schematic and (b) chip photograph of the presented diode frequency tripler unit cell MMIC. The chip size is 1.25 mm × 1.25 mm.

swing across the APDs which drives the diode capacitance from minimum to maximum. Thus, more diodes reduce the input impedance at the diode level and allow for a high input drive. However, at the same time, due to a finite Q factor of matching networks, the achievable bandwidth is limited since the impedance transformation ratio at input and output of the x3 is increased. Consequently, the number of diodes is a trade-off between the capability of generating high output power at the third harmonic and a broadband frequency response. Based on simulations, the tripler core contains eight Schottky diodes in total, as described in Section III.

At the input, the tripler is matched to the fundamental frequency (H1) by using a planar inductor in air-bridge technology and a shunt capacitor. In addition, the low-pass-filter characteristic of the input matching network improves the conversion efficiency of the x3 by avoiding the third harmonic (H3) to leak into the input. The RF input power is injected at the common dc node of the APDs. The corresponding dc potential can be supplied via a large inductor that acts as an open circuit for the RF input signal. At the common RF node, two RF shorted stubs are connected. For a wideband frequency response, the stubs feature a high characteristic

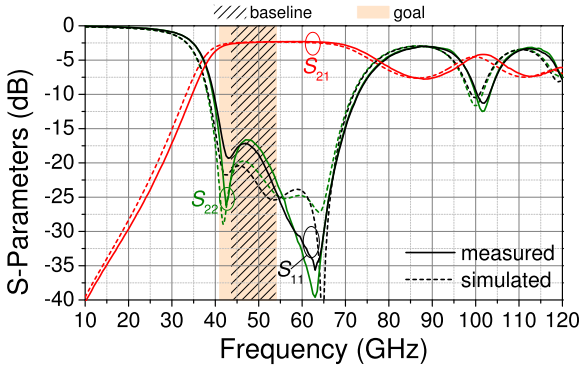


FIGURE 17. Measured and simulated S-parameters of the band-pass filter.

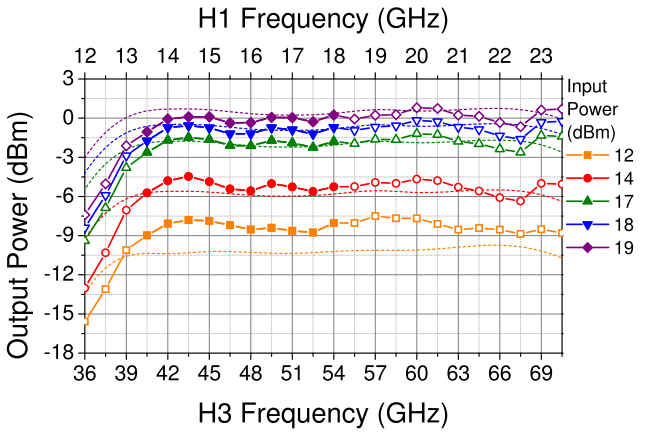


FIGURE 18. Measured (symbols) and simulated (dashed) output power of the third harmonic of the presented diode frequency tripler unit cell MMIC. The lower and upper x-axes refer to the frequency of the third and first harmonic, respectively. The baseline frequency range (H3 frequency: 40.5–54 GHz) is indicated by filled symbols.

impedance by using a 4-µm-wide signal strip. The shorted stubs are used to match the output at the third harmonic and, secondly, for providing a low impedance for the fundamental frequency which improves the conversion efficiency of the x3. Additionally, the stubs are used to dc-bias the diodes. The reverse bias voltage is generated out of a single voltage (V_{x3}) with a resistive voltage divider. The diodes are connected so that V_{x3} is positive. This avoids the need for a negative control voltage which simplifies the dc-bias circuit. Thus, in conjunction with the RF choke at the input of the tripler, a symmetric operation of the APD's is ensured, which is crucial for the suppression of even harmonics. Two series capacitors with a capacitance of about 1 pF each are utilized as dc blocks at the output of the tripler.

Still, slight asymmetries of the circuit and the anti-parallel diode pair will cause the suppression to remain finite. In particular, suppression of the first harmonic is a major challenge since the magnitude at the output of the x3 is considerably high and could saturate PA_2 even though it is out of band. Simulations indicate that the output power of the fundamental frequency is in the same range as the wanted third harmonic. Thus, a BPF is used with a suppression of the

TABLE 3. Correlation control voltage vs. input power of the x3.

P_{in} (dBm)	V_{x3} (V)
12	0
14	1
17	2
18	2.5
19	3

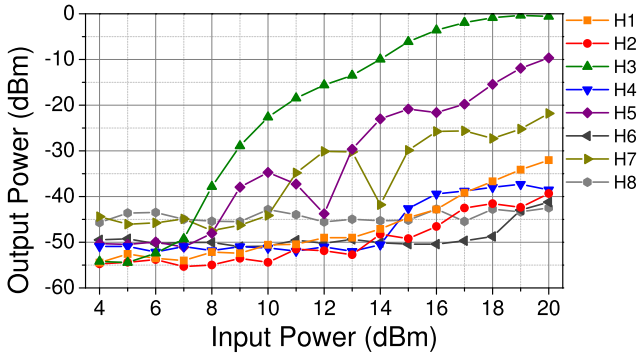


FIGURE 19. Measured output power of first to eighth harmonic of the presented diode frequency tripler unit cell MMIC for an input power sweep from 4 dBm to 20 dBm at an input frequency of 15.5 GHz (H3 frequency: 46.5 GHz).

fundamental frequency range of at least −20 dBc. The filter uses a series line-capacitor-line topology with three sections (as depicted in Fig. 16). In order to minimize the required chip area, the transmission lines are meandered which reduces the total length almost by a factor of three. The filter is simulated with CST Microwave Studio. Simulated and measured S-parameters of the band-pass filter are depicted in Fig. 17 and a very good agreement can be observed. The insertion loss is better than 2.5 dB for most part of the passband with a slight roll-off at the band edges. For the fundamental frequency range (below 20 GHz), the filter exhibits an insertion loss of more than 30 dB. This was the main objective for the BPF. The frequency range of the high harmonics shows only a limited rejection. However, this was accepted as a result of the tradeoff between insertion loss, stopband rejection, passband bandwidth, and occupied chip area. PA_2 will help to further suppress, especially, the higher harmonics so that good suppression of all harmonics is expected for the fully-integrated tripler MMIC. A chip photograph of the MMIC is given in Fig. 16(b).

The frequency tripler unit cell MMIC was tested on wafer. The RF input signal was provided by a Keysight signal generator with an additional amplifier (Keysight 83050A) close to the RF input probe. The output signal was measured by an Anritsu MS2760A Spectrum Analyzer which was directly connected to the RF probe. The measurement results include the insertion loss of the BPF. In Fig. 18, the output power of the third harmonic frequency is depicted for different input drive levels from 12 dBm to 19 dBm. V_{x3} is adjusted for each input power level according to Table 3. By doing so, the output power of the x3 can be varied by about 8 dB with

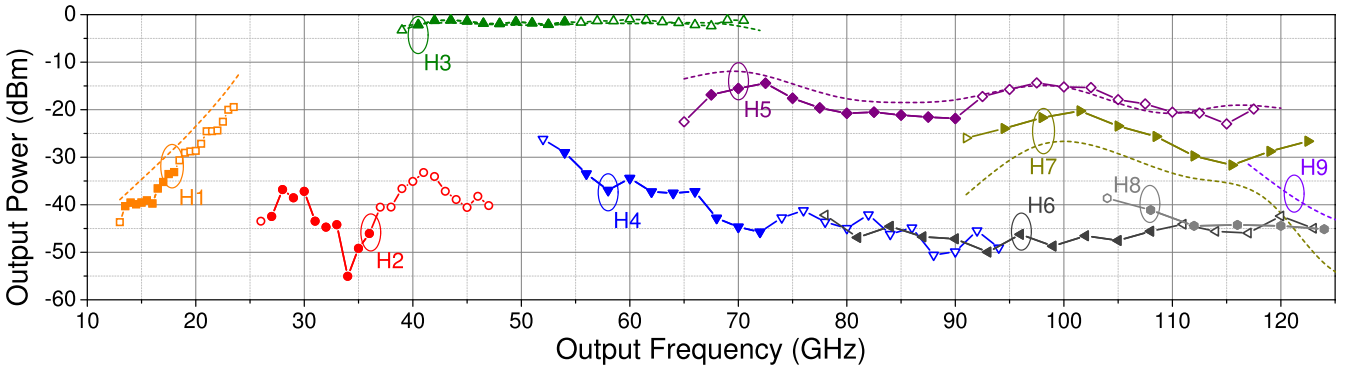


FIGURE 20. Measured (symbols) and simulated (dashed) frequency response of the presented diode frequency tripler unit cell MMIC for a constant input power of 17 dBm and a control voltage of 2 V. The baseline frequency range (H3 frequency: 40.5–54 GHz) is indicated by filled symbols.

almost constant conversion efficiency. For the lower setting (P_{in} = 12 dBm and V_{x3} = 0 V), the mean output power for an output frequency range from 40.5 GHz to 70.5 GHz is −8.3 dBm. For the highest setting (P_{in} = 19 dBm and V_{x3} = 3 V), the mean output power is 0.1 dBm. The ripple of the output power is below ±1 dB. In Fig. 19, the input power is swept from 4 dBm to 20 dBm at an input frequency of 15.5 GHz (H3 frequency: 46.5 GHz). The control voltage is set to 2 V. As it is demonstrated by Fig. 19, an optimal operation point is given for an input power of about 17 dBm since the harmonic suppression is maximized and the output power of H3 starts to saturate.

In Fig. 20, the frequency response of the presented tripler unit cell MMIC is given for a constant input power of 17 dBm and a V_{x3} of 2 V. For the baseline frequency range (filled symbols; 40.5–54 GHz), the suppression of the most unwanted harmonics is better than −30 dBc. Due to the limited rejection of the upper stopband of the BPF, the strongest unwanted harmonics are the fifth (H5) and seventh harmonic (H7). Still, H5 and H7 achieve values of below −13.3 dBc and −20 dBc, respectively. Simulations and measurements are in good agreement. Predictably, the even harmonics are underestimated since simulations assume perfectly matched devices resulting in infinite suppression. Still, the even harmonics are suppressed by −30 dBc or better for most of the band. Furthermore, the extended frequency range shows a harmonic suppression of better than −15 dBc almost over the entire band.

B. KU-BAND POWER AMPLIFIER

Based on the results of the previous section, a Ku-band PA with an output power of 15 dBm to 17 dBm over the band (minimum: 13.67 GHz to 18 GHz) is required. The input power should not exceed 0 dBm. Therefore, a two-stage amplifier topology with common-source devices is used. A simplified schematic is illustrated in Fig. 21. The transistors have a unit gate width of 125 µm. In order to achieve the power target, the output stage utilizes a six-finger transistor with a total gate width of 750 µm. For a linear operation of the input stage, a four-finger transistor with a total gate with

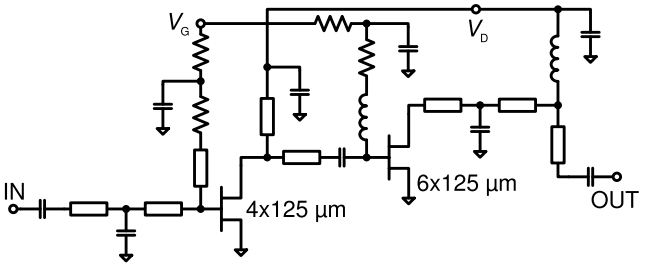


FIGURE 21. Schematic of the presented unit cell Ku-band power amplifier MMIC.

of 500 µm is used. The input matching network includes a series capacitor for dc blocking. The gate voltages (V_G) of the first and second stage are provided by an RF-shorted stub and parallel inductor, respectively, which are directly connected to the gate of the transistors. The gate bias networks are also used for the compensation of the input capacitance of the transistors. For stability reasons, the gate bias networks include 10-Ω resistors in series. The impedance transformation to 50 Ω is obtained through a line-capacitor-line tee network. Since the input matching of the Ku-band PA will also be the input matching of the entire frequency tripler MMIC, the design targets an input return loss greater than 20 dB.

The drain bias of the first and second stage is provided by an RF-shorted stub and parallel inductor, respectively. At the output, the impedance transformation to 50 Ω is again realized by a line-capacitor-line tee network and a series capacitor is used as dc block. The RF choke of the second stage is connected to the second line of the impedance transformation network. The gate and drain bias networks are connected to single gate and drain bias pads, respectively. In order to prevent possible low-frequency instability issues, the gate branches are isolated by two 50-Ω resistors. A chip photograph of the fabricated unit cell Ku-band PA is depicted in Fig. 22. To reduce the occupied chip area of the Ku-band PA test circuit, the last transmission line of the output matching network utilizes a 90° bent with the same electrical length as a straight transmission line. Apart from that, the layout of the Ku-band PA subcircuit of the fully-integrated tripler MMIC is identical to the depicted test MMIC.

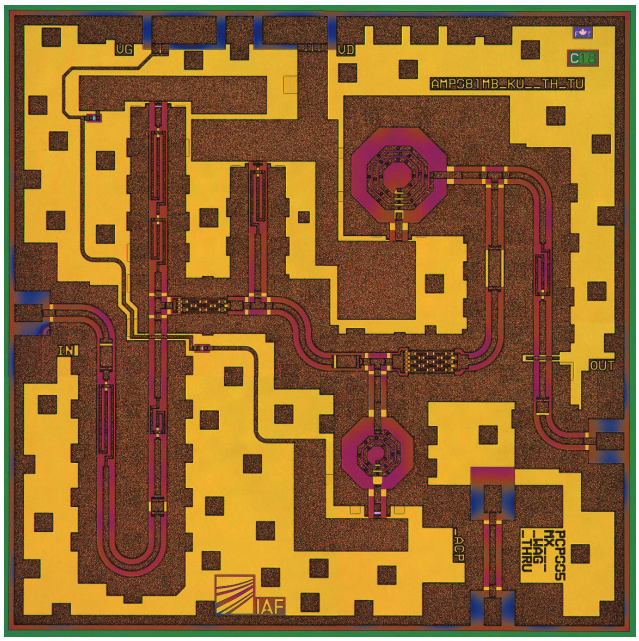


FIGURE 22. Chip photograph of the presented unit cell Ku-band power amplifier MMIC. The MMIC has a size of 1.75 mm × 1.75 mm.

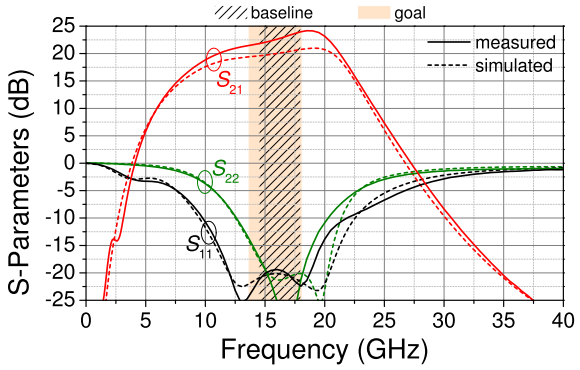


FIGURE 23. Measured and simulated S-parameters of the presented unit cell Ku-band PA MMIC.

The measured and simulated small-signal performance of the Ku-band PA MMIC is shown in Fig. 23. The S-parameters are measured for a drain voltage (V_D) at dc pad level of 1.2 V and a drain current of 250 mA (200 mA/mm). From 11 GHz to 21 GHz, S_{21} is above 20 dB, whereas the input matching is better than −19 dB for a frequency range from 12 GHz to 19 GHz. A good agreement between simulation and measurement can be observed. The measured continuous-wave (CW) large-signal performance of the Ku-band PA is illustrated in Fig. 24. In Fig. 24(a), output power (P_{out}), transducer gain (G_t), and power-added efficiency (*PAE*) are given for a constant input power of −2 dBm and different drain voltages of 1.2 V and 1.4 V. The quiescent drain current is 250 mA. For frequencies above 13 GHz and a drain voltage of 1.2 V, an output power of more than 16 dBm is achieved with a peak value of 17 dBm at 17 GHz. If the drain voltage is set to 1.4 V, the output power increases by about 0.8 dB. In the

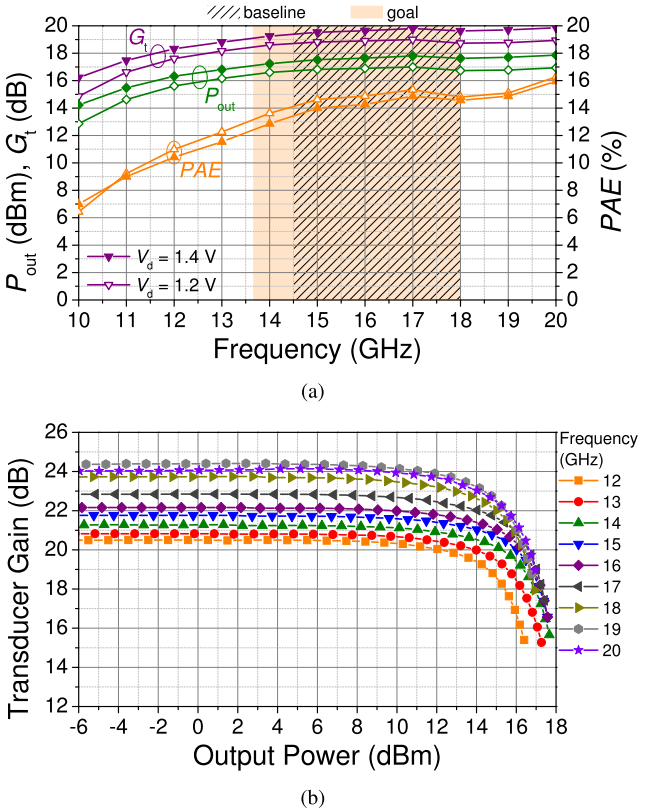


FIGURE 24. Measured CW large-signal performance of the Ku-band PA MMIC. (a) P_{out}, G_t, and *PAE* versus operating frequency for drain voltages of 1.2 V and 1.4 V and a constant input power of −2 dBm. (b) Transducer gain versus output power for a drain voltage of 1.2 V.

same frequency range, G_t and *PAE* are in the range of 18 dB to 20 dB and 12 % to 16 %, respectively. A power sweep for a drain voltage of 1.2 V is shown in Fig. 24(b). The measured large-signal performance demonstrate that the presented Ku-band PA meets the target for driving the x3 unit cell, which is described in Section V-A.

C. U-BAND POWER AMPLIFIER

Based on the measurements of the x3 unit cell and the I/Q-mixer MMIC, the U-band PA has an available input power in the range of −8 dBm to 0 dBm and should deliver an output power of about 15 dBm to 17 dBm. The minimum required operating frequency range is 41 GHz to 54 GHz. Thus, a three-stage amplifier topology with common-source transistors is used. The output stage utilizes an eight-finger transistor with a unit gate width of 80 µm. The first two stages have transistors with a total gate width of 4 × 65 µm. Both stages feature an RC high-pass filter at the gate in order to achieve unconditional stability, especially at low frequencies. The input matching network of the amplifier consists of a line-capacitor low-pass filter which matches the input of the first transistor to an impedance of about 15 Ω. A quarter-wave impedance transformer realizes the matching to 50 Ω. The gate bias for all stages is supplied via large resistors with values that are reciprocal to the total gate width

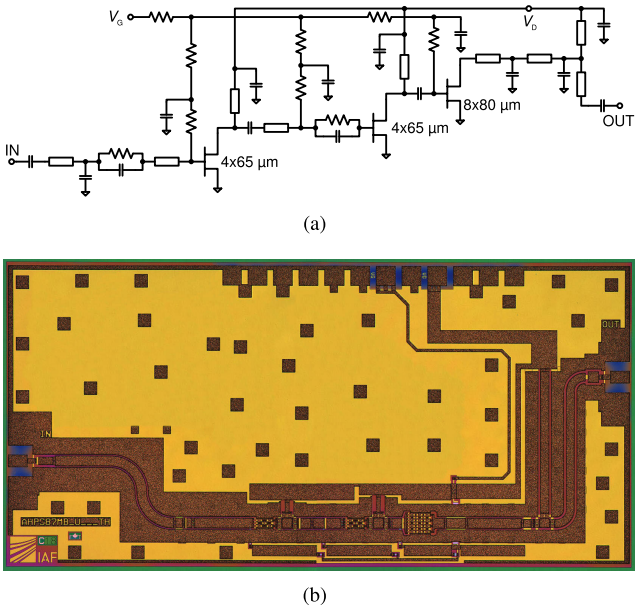


FIGURE 25. (a) Schematic and (b) chip photograph of the presented unit cell U-band power amplifier MMIC. The MMIC has a size of 2.5 mm × 1.25 mm.

of the corresponding transistor. The drain bias is supplied via RF-shorted stubs. For the first two stages, the stubs are directly connected to the HEMTs for compensating the output capacitance. The output stage is matched to 50 Ω by a combination of a two-section line-capacitor low-pass filter network and a quarter-wave impedance transformer. The stub of the output stage has a quarter-wave length and is mainly used to supply the drain bias. The bias of all stages is combined to a common V_G and V_D. Fig. 25 shows a schematic and chip photograph of the fabricated U-band PA MMIC. The layout of the test MMIC is in the final configuration the fully-integrated frequency tripler MMIC utilizes. However, in order to allow on-wafer testing, an S-shaped transmission line is used at the RF input, which is replaced by a U-shaped transmission line with identical length in the fully-integrated version.

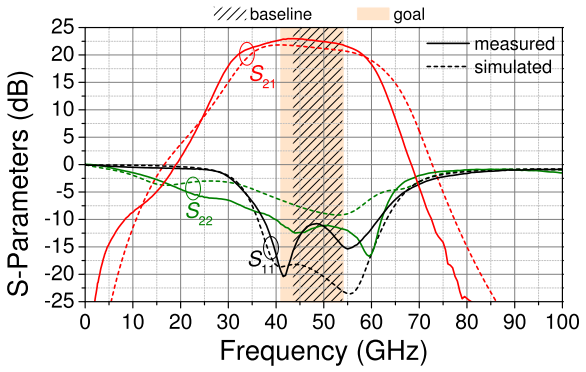


FIGURE 26. Measured and simulated S-parameters of the presented unit cell U-band PA MMIC.

The measured and simulated S-parameters of the U-band PA MMIC are shown in Fig. 26 for a drain voltage (at the

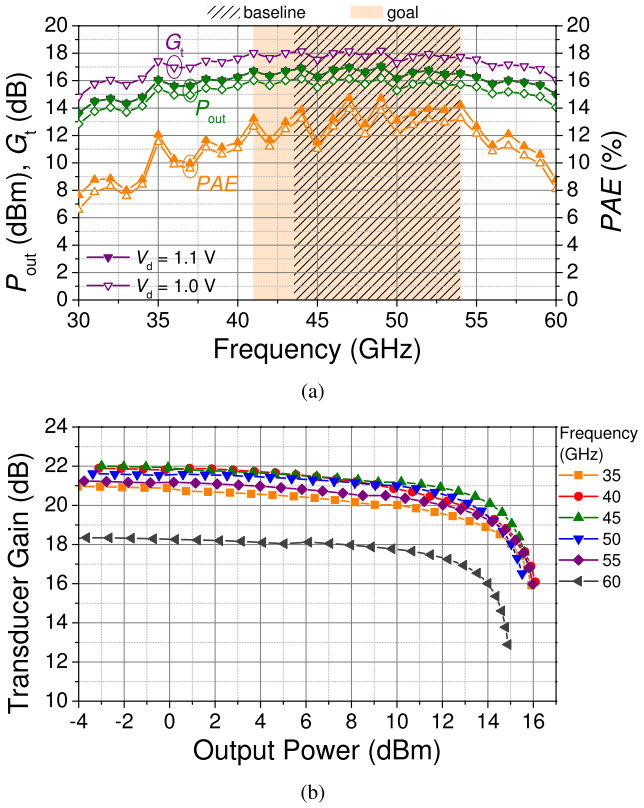


FIGURE 27. Measured CW large-signal performance of the U-band PA MMIC. (a) P_{out}, G_t, and *PAE* versus operating frequency for drain voltages of 1 V and 1.1 V (at the dc pad) and a constant input power of −2 dBm and 0 dBm, respectively. (b) Transducer gain versus output power for a drain voltage of 1 V and operating frequencies from 35 GHz to 60 GHz.

dc pad) of 1 V and a drain current of 232 mA (200 mA/mm). From 32 GHz to 58 GHz, S_{21} is above 20 dB with a peak gain of 23 dB at 44 GHz. S_{11} and S_{22} are below −10 dB almost over the entire frequency range. The measured CW large-signal performance is given in Fig. 27. In Fig. 27(a), P_{out}, G_t, and *PAE* are depicted for constant input power of −2 dBm and 0 dBm and drain voltages of 1 V and 1.1 V, respectively. The quiescent drain current is 232 mA. For $V_D = 1.1$ V and an operating frequency from 35 GHz to 60 GHz, PA_2 exhibits an output power of more than 15 dBm with average and peak values of 16.3 dBm and 17 dBm, respectively. For $V_D = 1$ V, the output power is reduced by 0.8 dB. Fig. 27(b) shows a power sweep for a drain voltage of 1 V and operating frequencies from 35 GHz to 60 GHz.

D. U-BAND FREQUENCY TRIPLER MMIC

The fully-integrated frequency tripler MMIC is a combination of the presented PAs and the x3 unit cell. As described above, the layouts of the subcircuits are only slightly adjusted for compactness of the tripler MMIC. A chip photograph of the fabricated MMIC is depicted in Fig. 28.

The on-wafer measurement setup employs a Keysight signal generator and an Anritsu spectrum analyzer. Since the required input power level is less than that of the x3 unit

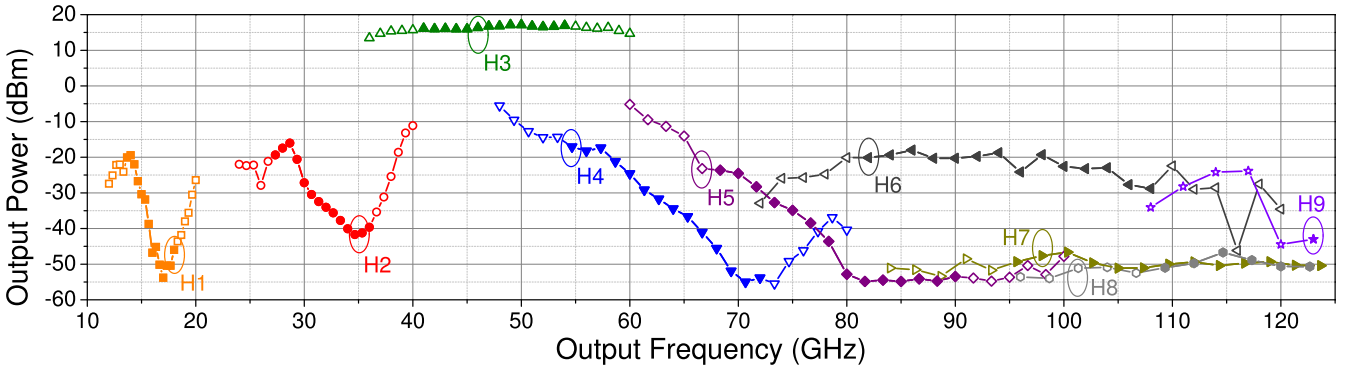


FIGURE 29. Measured frequency response of the fully-integrated frequency tripler MMIC for a constant input power of −5 dBm. The baseline frequency range (H3 frequency: 41–54 GHz) is indicated by filled symbols.

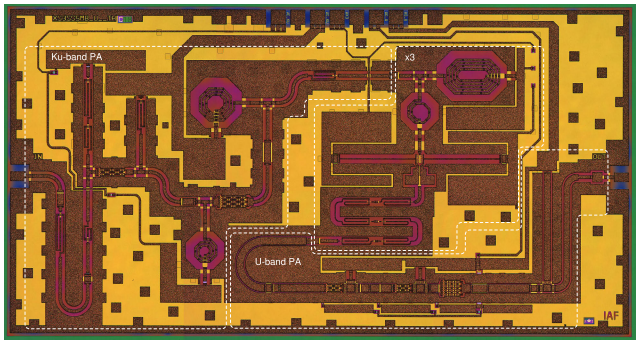


FIGURE 28. Chip photograph of the fabricated fully-integrated U-band frequency tripler MMIC. The chip size is 3.25 mm × 1.75 mm.

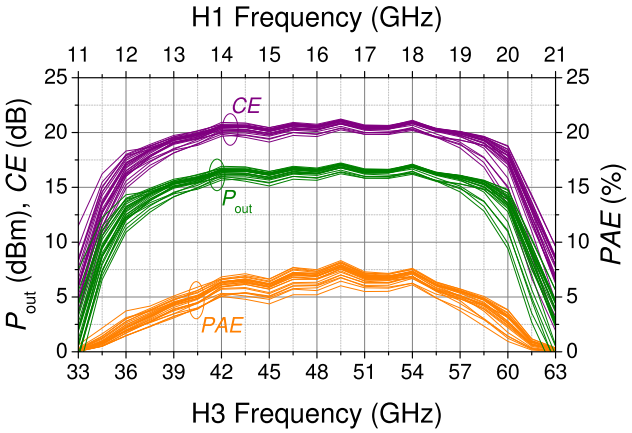


FIGURE 30. Wafer mapping of the fabricated fully-integrated U-band frequency tripler MMIC including 25 measured cells out of 37 cells on a wafer.

cell, no additional amplifier is used at the input. In order to reduce the maximum delivered power to the spectrum analyzer, a 10-dB attenuator (Anritsu 41W-10) is connected to the output probe tip. The x3 is biased with a fixed voltage of $V_{x3} = 2$ V. PA_1 and PA_2 are biased with drain voltages and quiescent drain currents of 1.2 V and 1.5 V and 250 mA and 684 mA, respectively. The measured output power of the first to ninth harmonic of the presented fully-integrated tripler MMIC is shown in Fig. 29 for a constant input power of −5 dBm. The input frequency is swept from 12 GHz to 20 GHz. The baseline frequency range (H3 frequency: 41–54 GHz) reveals an output power of the wanted third harmonic of more than 16 dBm (average 16.5 dBm). A peak output power of 17.1 dBm is achieved at 50 GHz. For the frequency range from 38 GHz to 60 GHz, the measured output power is above 14.7 dBm (average 16.3 dBm). For the baseline frequency range, the suppression of all measured unwanted harmonics is −32.1 dBc or better. Even for an extended frequency range of the third harmonic from 38 GHz to 60 GHz, the suppression of the unwanted harmonics is better than −25.9 dBc. These results confirm the design goal that PA_2 further suppresses unwanted harmonics, in particular H5 or H7.

In Fig. 30, P_{out}, *CE*, and *PAE* of 25 measured cells out of 37 on a wafer are shown for a constant input power of −4 dBm. The mean values of P_{out} and *CE* exhibit a spread of only 1 dB. The *PAE* is above 5 % for the most part of the band.

VI. COMPARISON TO STATE-OF-THE-ART

In Table 4 and 5, the performance of the presented I/Q-mixer and frequency tripler MMICs are summarized. When comparing I/Q and image-reject mixers (IRMs), one should keep in mind that for an IRM the I and Q signals are already combined. Thus, the corresponding CL of an IRM is expected to be lower compared to an I/Q-mixer, theoretically up to 3 dB. The presented mixer MMIC demonstrates a conversion loss which is comparable to dedicated Schottky-diode MMIC technologies [14], whereas featuring an even larger RF and IF bandwidth. Additionally, $P_{1\,dB}$ exhibits the highest value. This is an important measure for linear receivers and transmitters. Also the lowest I/Q imbalance is demonstrated. In combination with a yield and spread of functioning cells on a wafer of better than 94 % and <0.8 dB, respectively, a major benefit of an established MMIC process is illustrated. Consequently, to best of the authors' knowledge, this work presents the first I/Q-mixer MMIC covering the entire W-band with an IF bandwidth of about 15 GHz, a $P_{1\,dB}$ of 5 dBm, and an I/Q imbalance of less than 0.8 dB.

TABLE 4. State-of-the-art W-band I/Q and image-reject down-conversion mixer MMICs.

Ref.	Technology	Topology	Chip Area (mm^2)	RF (GHz)	IF (GHz)	LO Freq. (GHz)	P_{LO} (dBm)	P_{dc} (mW)	I/Q Imbal. (dB)	$P_{1\,dB}$ (dBm)	CL (dB)
[13]	0.13-µm pHEMT	subh. APD IRM	5.46*	71–86	1–9	78	>17	n/a	n/a	4	<12
[14]	GaAs Diode	subh. APD I/Q	1.96	90–110	1–10	50	10	n/a	<4	n/a	12–19
[15]	50-nm mHEMT	fund. res. I/Q	2.81	70–84	0.1–7	77	5	0	<2.6	>2	9.8–15.3
[16]**	100-nm pHEMT	fund. res. IRM	3.91	71–86	5–20	66	5	290	n/a	n/a	≈16
[17]	0.15-µm mHEMT	fund. res. IRM	3	71–86	0.5–10	70–90	4	0	n/a	1	7–19
[18]	0.15-µm pHEMT	fund. res. IRM	n/a	77–87	0.5–5	41	15	0	n/a	n/a	20–27
[19]	100-nm pHEMT	fund. res. IRM	5.4***	70–92	1–12	80	7	n/a	n/a	n/a	9–10.1
This work	50-nm mHEMT	subh. APD I/Q	3	75–110	0.5–15	41–50	16–19	no	<0.8	5	13.7–17

* Including occupied area for LO chain; ** Includes a PA at the LO port; *** Including occupied area for LO chain and RF LNA

TABLE 5. State-of-the-art frequency tripler MMICs.

Ref.	Technology	Topology	Chip Area (mm^2)	Frequency (GHz)	Tested Harmonics	P_{dc} (mW)	In-Band Suppression (dBc)	Out-of-Band Suppression (dBc)	CE (dB)	P_{out} (dBm)
[20]*	0.25-µm pHEMT	Balanced HEMT	2.32	42–51 (19.4 %)	1–3	n/a	n/a	<−20	n/a	6.5–12.5
[21]	0.13-µm SiGe HBT	HBT	0.96	46–54 (16 %)	1–4	62	n/a	<−31	−7.4–−4.4	−7.4–−4.4
[21]**	0.13-µm SiGe HBT	HBT	n/a	48–57 (17.1 %)	1–4	220	n/a	<−28	9–12	6.5–9.5
[22]***	90-nm CMOS	Cascode FET	0.46	49.5–60 (19.2 %)	1–3	5.4	n/a	<−31	−2.1–1.2	−7.8–−3.8
[23]	0.15-µm pHEMT	HEMT	2	58.5–64.5 (9.8 %)	1–3	54	n/a	<−18	−4.1–−1.1	−3.1–−0.1
[24]	0.15-µm pHEMT	HEMT	0.56	30–70 (80 %)	1–3	87.4	<−11.3	<−18	−26–−11	−34–−17
[25]	65-nm CMOS	FET	0.45	57–75 (27.3 %)	1–3	60	n/a	<−21	−1.7–1.3	−6.7–−3.7
[26]	0.13-µm SiGe HBT	Distributed HBT	0.53	43–79 (59 %)	1–7	362	<−10	<−10	−26.3–−18.8	−8.3–−0.8
[27]	0.15-µm mHEMT	HEMT	1.5	71–76 (6.8 %)	1–4	n/a	n/a	<−20	−11.5	−5.5
				81–86 (6 %)	1–3	n/a	n/a	<−20	−15–−13	−9–−7
[20]*	0.25-µm pHEMT	HEMT	2.32	94–100 (6.2 %)	3	n/a	n/a	n/a	n/a	1.2–5
[28]	0.15-µm pHEMT	APD	1.5	87–102 (15.9 %)	3	no	n/a	n/a	−20.1–−18.4	−6.1–−4.4
[5]	GaAs diodes	APD	1.48	75–110 (37.8 %)	2–5	15.5	−20	−12	−20.6–−17.3	−4.6–−1.3
[29]	0.15-µm mHEMT	APD	1	75–110 (37.8 %)	1–3	no	n/a	<−14	−18.3–−13.5	−0.3–4.5
[30]	GaAs diodes	APD	0.47	75–110 (37.8 %)	2–5	n/a	−10	−10	−21.4–−17.8	−8.4–−4.8
				75–140 (60.5 %)				<−25	−22.4–−17.7	−19.4–−14.7
This work	50-nm mHEMT	APD	1.56	40.5–54 (28.6 %)	1–8	0	<−26.8	<−13.3	−19.2–−18.2 (avg. −18.6)	−2.2–−1.2 (avg. −1.6)
				40.5–70.5 (54.1 %)			<−14.8	<−13	−19.4–−17.9 (avg. −18.6)	−2.4–−0.9 (avg. −1.6)
This work****	50-nm mHEMT	APD	5.69	41–54 (28.4 %)	1–9	1050	n/a	<−32.1	21–22.1 (avg. 21.5)	16–17.1 (avg. 16.5)
				38–60 (44.9 %)			<−25.9	<−25.9	19.7–22.1 (avg. 21.3)	14.7–17.1 (avg. 16.3)

* Includes a driver PA; ** Includes post amplification; *** Not all data for same input power available; **** Includes pre and post amplification

In the upper part of Table 5, the presented frequency tripler MMICs are compared to previously-published results in a similar frequency range. Since there is only a limited number of comparable tripler MMICs in this frequency range, Table 5 includes also state-of-the-art examples in W-band and D-band. In addition, if a fundamental mixer approach is used as it is the case for [15]–[19], an LO drive signal in W-band would be necessary. Since the achievable bandwidth of a frequency multiplier and the suppression of unwanted harmonics is a tradeoff, it is important to mention that most previous publications present only limited information about harmonic suppression. To the best of the authors' knowledge,

the presented fully-integrated tripler is the first MMIC that covers at least the entire U-band while demonstrating the highest published output power (average: 16.3 dBm) with a suppression of unwanted harmonics up to the ninth harmonic of better than −25.9 dBc.

VII. CONCLUSION

In this work, the investigation, design, and realization of U-band frequency tripler and subharmonically-pumped W-band I/Q-mixer MMICs are demonstrated. The circuits are realized in an established 50-nm gate-length mHEMT technology. A major part of this analysis is the layout optimization of the integrated planar Schottky diodes without changing the existing HEMT processing. The investigation of different diode layouts shows that a diode with a Schottky contact of 0.25 µm × 4 µm yields the best performance for varactor as well as for varistor applications for the given technology. The presented nonlinear circuits demonstrate state-of-the-art performance with large operating bandwidths. The capability of realizing state-of-the-art nonlinear circuits, e.g. frequency multipliers or mixers, in combination with state-of-the-art LNAs and PAs, highlights the benefit for new multifunctional MMICs with superior performance. This is appealing for several applications, such as focal-plane arrays or other highly-integrated scenarios in the field of radio astronomy, wireless communication, or mmW imaging systems.

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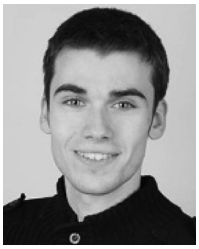

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