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An FPGA-based flexible demo-board for endoscopic capsule design optimization

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Abstract

This work presents a flexible demo system, based on Field Programmable Gate Array (FPGA), that was specifically designed for testing all elements which have to be integrated in an endoscopic capsule, such as an image compression engine, a high-speed telemetric system, illumination system and inertial sensors.
Several elements were tested and evaluated, obtaining a maximum frame rate of 19 fps over a transmission channel of 1.5 Mbit/s. The final configuration was chosen for the development of a miniaturized endoscopic capsule prototype.

"Keywords: FPGA, Wireless Capsule Endoscopy, sensor;"

1. Introduction

Wireless Capsule Endoscopy (WCE) is an emerging technology which is having a big impact on the practice of endoscopy. Typical capsules are equipped with a camera, an illumination system, a power source and a wireless transmitter. They are swallowable, and thus it reduces the invasiveness and pain of traditional gastrointestinal (GI) procedures, and it results more acceptable for patients [1]. The WCE seems to be superior in the diagnosis of the small bowel pathologies to the other painless imaging modalities, such as X-ray, computerized tomographic enterography and magnetic resonance enteroclysis, because it provides a direct vision of the inside wall of GI tract [2]. Since its commercial availability in 2002, several enhancements were done [3]. However, the main challenge still remains the integration of different systems with high performances inside a pill with a maximum dimension of 11(d) x 31(l) mm, taking into account the limited power supply and the difficulty to connect each component in this small volume. Our aim is to develop a WCE system with real time vision, a minimum frame rate of 15 frames per second (fps), which are transmitted through a high speed telemetry. As a first step, we designed a demo-board, based on an FPGA, for testing all elements which could be integrated in the capsule. The main feature of the proposed demo-board is the high flexibility, in order to test each element and possibly different configurations of the system. When all elements were evaluated, we started to design the miniaturized prototype for WCE.

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2. Demo board architecture

The demo system is composed by three units: a dedicated vision board, a main control board and a third board for debug purposes (Fig. 1). In the following sections the boards will be described in details.

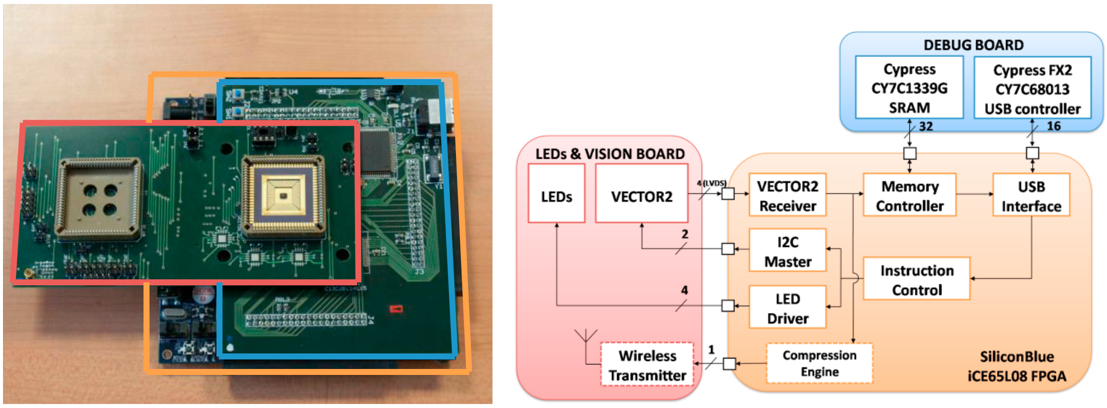

Fig. 1. The demo system (a) and its block diagram (b)

2.1. Vision board

The core of the vision board is a custom Complementary Metal-Oxide Semiconductor (CMOS) image sensor, called “Vector2”. The chip was produced in the UMC 0.18µm-CIS (CMOS Image Sensor) technology and includes a 320x240 pixel array. All the internal blocks were designed to guarantee high sensitivity, low power consumption and a simple control of the full chip [4]. Taking into account the physical dimension of the Vector2 sensing area (1.408(h) x 1.056(v) mm) and the focal length, that are driven by the final application, a commercial positive focal lens (NT45-589, Edmund Optics [5]) was chosen, thus achieving a field of view of 82°(h) x 61°(v). A plastic, unreflective holder was also designed in order to fix and align the optical module in front of the chip (Fig.2).

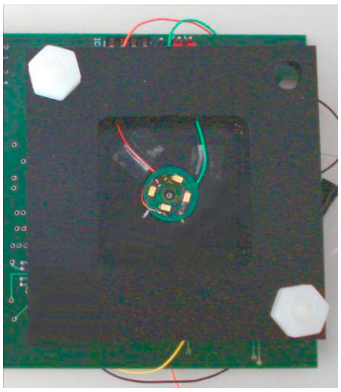

Fig.2 The illumination system with the unreflective holder and the optical system

The illumination system was designed considering a trade-off between power consumption, size and the amount of light necessary for diagnostic purposes. The high efficiency Nichia Nesw007AT LEDs [6] were chosen because of the small dimension (1.2 x 2 x 1.3 mm), the high value of light intensity (from 720 to 1000 mcd) and the low power consumption (15mA @3.3V). Four LEDs were arranged onto a round shape PCB. The amount of light and the power consumption can be precisely controlled with a simple Pulse Width Modulation (PWM) technique.

2.2. Control and debug board

Since programmable logic devices are characterized by high-flexibility and re-programmability, the FPGA represents the best choice for testing different solutions for WCE applications. In order to achieve the power and dimensional requirements, the SiliconBlue iCE65L08 FPGA was chosen as the core of the control system of the demo-board. The selected FPGA is 4.37 mm x 4.79 mm and the typical power consumption is very low (30uA@32kHz). These features make the iCE65L08 suitable to be fit in an endoscopic pill. In order to increase the flexibility of the proposed test system, a debug board was also developed. The board is equipped with the Cypress FX2 USB controller that provides high-speed connection and the Cypress CY7C1339G SRAM chip which is used as frame buffer for the acquisition of images from the sensor chip. Additionally, several connectors are used to monitor each pin of the FPGA.

2.3. FPGA Architecture

As can be seen in Fig. 1.b, several logic blocks were written in Very High Speed Integrated Circuits Hardware Description Language (VHDL) and implemented on the FPGA in order to control the vision board through the USB connection. A simple software, running on a standard PC, was used to send instructions to the FPGA and the Vector2 chip, and to receive and show the acquired images on the screen. The instructions sent by the PC are managed by the *USB Interface* block, which interconnects the FPGA with the external USB controller, and by the *Instruction Control* block, which decodes the instructions and configures the FPGA registers and the Vector2 internal registers through an I2C bus. After the setup of the sensor chip, the *VECTOR2 Receiver* decodes the acquired frames converting the Low-Voltage Differential Signaling (LVDS) signals to a 10-bit parallel format and storing them in the frame buffer. When there is a request, the images are read from the memory and sent to the PC through the USB connection. The logic blocks implemented in this configuration use about 31% of the total FPGA (2400 logic cells) and can operate at a maximum frequency of about 41MHz. The power consumption of the developed demo-board is less than 360mW and it splits as follows: 40mW for the Vector2 chip, about 10mW for the FPGA, and the rest for the debug blocks which will be not integrated in the final miniaturized prototype.

To reach the desired frame rate a low-power low-complexity compression engine was also implemented on the FPGA. This compressor was chosen because its performances are comparable with JPEG2000, but lowering the complexity and therefore the power consumption [7]. This configuration consumes about 77% of the resources of the FPGA (including 25 block RAMs) and can work at a frequency of about 39MHz. A low-power wireless transmission based on near-field technology was integrated and tested on the demo system to transmit the images [8]. The maximum frame rate is limited by the transmitter bit-rate and compression ratio, chosen as a trade-off between the amount of data to be transmitted and image quality. Since the compression engine mentioned above allows a reduction of the transmitted data by a factor of 8 and considering the bit-rate of the high data rate wireless transmitter of about 1.5Mbit/s, the resulting frame rate was about 19 fps.

For the LED control, a simple *LED* driver was implemented in the FPGA. This block is able to drive the LEDs by a PWM technique. Thanks to the high flexibility of the control board, the white LEDs could be replaced with color LEDs with no major design changes to obtain white light by color light combination [9] or to enable spectroscopic imaging, such as autofluorescence imaging (AFI) [10].

3. Miniaturized prototype

Considering the results obtained with the demo system, a miniaturized endoscopic pill board was developed (Fig. 3). The prototype consists of two boards connected by permanent flexible interconnection and three flexible circuit platforms for attaching other boards such as battery or wireless power supply as presented in [11], high data rate transmitter [8], and inertial sensors [12]. The first board was dedicated to the vision system, while the second board includes a Serial Peripheral Interface (SPI) Flash memory on top layer and the SiliconBlue FPGA on the bottom part. Near the outer ring of the first board there are five pads and two holes to connect the LED board and the optic holder. The boards have a diameter of 9.9 mm in order to be fit in a pill which has an inner diameter of 10 mm.

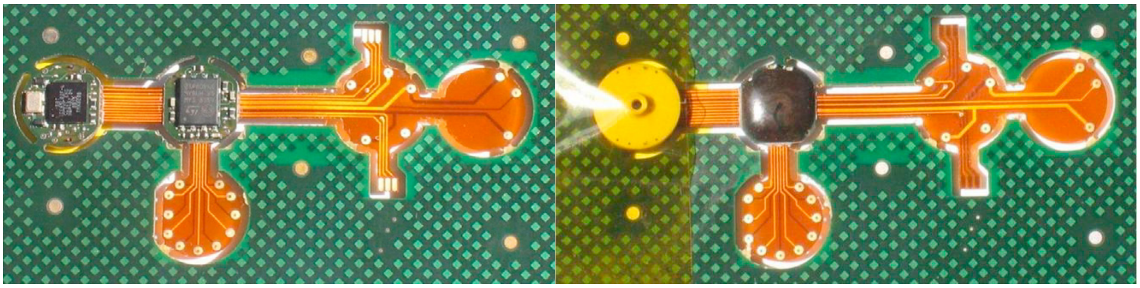

Fig.3 The miniaturized prototype, bottom layer (a), top layer (b)

4. Conclusions

An FPGA-based demo-system was developed in order to implement and test the different sub-modules which will be included in a WCE system. After the testing phase, the best configuration of the whole system was chosen thus achieving 19 fps transmitted through a 1.5 MHz telemetry. A first miniaturized WCE prototype was designed and developed and now it is under test.

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