Semi-Analytical Model for the Transient Operation of Gate-All-Around Charge-Trap Memories

Salvatore Maria Amoroso, *Student Member, IEEE*, Christian Monzio Compagnoni, *Member, IEEE*, Aurelio Mauri, Alessandro Maconi, Alessandro S. Spinelli, *Senior Member, IEEE*, and Andrea L. Lacaita, *Fellow, IEEE*

***Abstract*—We present a detailed semi-analytical investigation of the transient dynamics of gate-all-around (GAA) charge-trap memories. To this aim, the Poisson equation is solved in cylindrical coordinates, and a modification of the well-known Fowler–Nordheim formula is proposed for tunneling through cylindrical dielectric layers. Analytical results are validated by experimental data on devices with different gate stack compositions, considering a quite extended range of gate biases and times. Finally, the model is used for a parametric analysis of the GAA cell, highlighting the effect of device curvature on both program/erase and retention.**

***Index Terms*—Charge-trap (CT) memories, Fowler–Nordheim (FN) tunneling, gate-all-around (GAA) memories, semiconductor device modeling.**

I. Introduction

THREE-DIMENSIONAL architectures appear today as viable solutions for the integration of nonvolatile memory cells in terabit arrays [1]–[6]. In particular, the gate-all-around (GAA) charge-trap (CT) (GAA-CT) cell with a vertical channel is considered one of the most promising structures for future NAND Flash technologies, showing improved program/erase and retention performance with respect to planar devices [7]–[10]. Moreover, thanks to the reduction of corner and fringing field effects during both program/erase and read, GAA-CT cells allow more uniform trapped charge distributions in the storage layer and steeper incremental step pulse programming transients than planar cells [11], [12].

Given their interesting performance, GAA-CT cells have been investigated by many 1-D numerical models, exploiting the cylindrical symmetry of the device [13], [14]. However, these approaches rely on numerical solutions of the electrostatic and tunneling equations and may lack computational efficiency. The aim of this paper is instead to present an accurate yet simple semi-analytical model for both the program/erase and retention dynamics of GAA-CT memory cells. The model is based on an analytical solution of the Poisson equation in cylindrical coordinates and on a modified Fowler–Nordheim (FN) formula for the tunneling current. Results are validated against experimental data for different gate stack compositions. Then, a detailed analysis of the GAA-CT cell performance is presented, investigating the program/erase and retention transients as a function of the parameters of the cylindrical structure and highlighting the effect of device curvature. Owing to the computational efficiency and the accuracy, the model represents a useful tool for the investigation of the ultimate performance of GAA-CT memory devices.

Manuscript received January 27, 2011; revised May 13, 2011; accepted May 26, 2011. Date of publication July 12, 2011; date of current version August 24, 2011. This work was supported in part by the European Commission under the FP7 research contract 214431 "GOSSAMER." The review of this paper was arranged by Editor M. Ieong.

S. M. Amoroso, C. Monzio Compagnoni, and A. Maconi are with the Dipartimento di Elettronica e Informazione, Politecnico di Milano, 20133 Milano, Italy, and also with the Italian University NanoElectronics Team, 20133 Milano, Italy.

A. Mauri is with the R&D Technology Development, Micron Technology, Inc., 20041 Agrate Brianza, Italy.

A. S. Spinelli and A. L. Lacaita are with the Dipartimento di Elettronica e Informazione, Politecnico di Milano, 20133 Milano, Italy. They are also with the Italian University NanoElectronics Team, 20133 Milano, Italy, and also with the Istituto di Fotonica e Nanotecnologie, Consiglio Nazionale delle Ricerche, 20133 Milano, Italy.

Digital Object Identifier 10.1109/TED.2011.2159010

II. Physics-Based Analytical Model

In the following, we will refer to a template cylindrical MONOS device, assuming the following parameters: substrate radius $r_0 = 3$ nm, bottom-oxide thickness $t_{\rm bot} = r_{\rm bot} - r_0 = 4.5$ nm, nitride thickness $t_n = r_n - r_{\rm bot} = 6$ nm, and top-oxide thickness $t_{\rm top} = r_{\rm top} - r_n = 7$ nm. Aluminum was assumed for the gate. For the sake of generality, different dielectric constants will be considered for the bottom and top oxides and for nitride ($\epsilon_{\rm bot}$, $\epsilon_{\rm top}$, and ϵ_n, respectively), although final results will consider $\epsilon_{\rm bot} = \epsilon_{\rm top} = \epsilon_{\rm ox}$ (the SiO_2 dielectric constant). Axial symmetry is assumed, and the model is developed only as a function of the radial coordinate r, thus precluding the possibility to deal with any potential difference between source and drain of the memory cell in the longitudinal direction. Some concerns about the applicability of a 1-D (radial) model may arise when the gate length reaches values small enough to make the short-channel effects [15], [16] nonnegligible. However, GAA-CT memories are designed for a 3-D integration in vertical arrays [2] with the aim of achieving high densities per wafer without an excessive reduction of the gate length.

A. Electrostatic Solution

The electrostatics of the GAA cell can be straightforwardly calculated by solving the Poisson equation in cylindrical coordinates

$$\frac{\partial^2 V(r)}{\partial r^2} + \frac{1}{r}\frac{\partial V(r)}{\partial r} = -\frac{q n_t}{\epsilon_n}\left[H(r-r_{\rm bot}) - H(r-r_n)\right] \quad (1)$$

where q is the electron charge, $V(r)$ is the electrostatic potential along the radial coordinate, and n_t (units: $\rm cm^{-3}$) is the

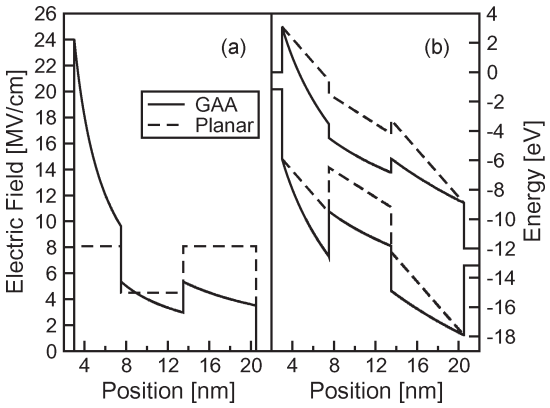


Fig. 1. (a) Electric field and (b) energy-band profile for the template GAA MONOS cell and a planar CT cell having the same thickness of the gate dielectrics, for $V_G = 12$ V and neutral nitride.

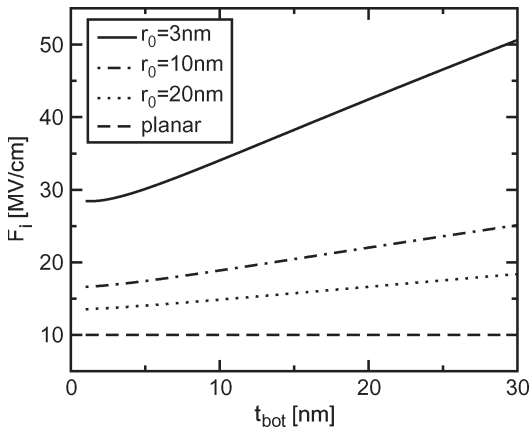


Fig. 2. Maximum electric field at the substrate/bottom-oxide interface of the template GAA cell when modifying $t_{\rm bot}$ (with fixed t_n and $t_{\rm top}$). A constant $V_G/EOT = 10$ MV/cm is assumed.

volumetric trapped electron density in the nitride, which is assumed constant. The Heaviside functions H in (1) are used to include electron trapping in the nitride volume only and not in the oxide layers. We initially neglect the potential drop in the silicon substrate, whose impact will be addressed in Section II-D, and integrate (1) to obtain $V(r)$ in the bottom oxide, nitride, and top oxide (namely, $V_{\rm bot}(r)$, $V_n(r)$, and $V_{\rm top}(r)$, respectively), when a gate bias V_G is applied to the gate contact

$$\begin{cases} V_{\rm bot}(r) = C_1 \ln \frac{r}{r_0} \\ V_n(r) = C_1 \ln \frac{r_{\rm bot}}{r_0} + C_2 \ln \frac{r}{r_{\rm bot}} + \frac{qn_t}{4\epsilon_n}\left(r^2 - r_{\rm bot}^2\right) \\ V_{\rm top}(r) = V_G - C_3 \ln \frac{r_{\rm top}}{r} \end{cases} \quad (2)$$

where explicit expressions for the constants C_i $(i = 1{-}3)$ are given in the Appendix. Note that (2) has been obtained considering a grounded silicon surface and applying the continuity of the potential and of the electric displacement vector (Gauss law) at the interface between the different materials.

From (2), the electric field in the device regions results in

$$\begin{cases} F_{\rm bot}(r) = -C_1 \frac{1}{r} \\ F_n(r) = -C_2 \frac{1}{r} - \frac{qn_t}{2\epsilon_n} r \\ F_{\rm top}(r) = -C_3 \frac{1}{r}. \end{cases} \quad (3)$$

Fig. 1 shows a comparison between the electrostatics of the template GAA MONOS cell (solid) and of a planar CT cell having the same thickness of the gate dielectrics (dashed) in the case of $V_G = 12$ V and neutral nitride (i.e., $n_t = 0$). As shown in (3) and differently from the planar case, the electric field is not constant in the GAA dielectrics, with a maximum value F_i located at the substrate/bottom-oxide interface [see Fig. 1(a)]. The maximum value is about three times larger than that in the planar device, allowing a strong improvement of the programming dynamics [17]–[19], as will be discussed in Section II-C. This is further shown by the energy-band profile in Fig. 1(b), where a thinner barrier for electron tunneling clearly appears in the cylindrical case. Note also that the electric field in the top oxide is lower in the GAA case, suggesting a lower electron leakage from the nitride to the gate during programming. The maximum electric field F_i of the template GAA cell is shown in Fig. 2 as a function of $t_{\rm bot}$ (with fixed t_n and $t_{\rm top}$), assuming a constant $V_G/EOT = 10$ MV/cm, where $EOT = \epsilon_{\rm ox}(t_{\rm bot}/\epsilon_{\rm bot} + t_n/\epsilon_n + t_{\rm top}/\epsilon_{\rm top})$ is the equivalent oxide thickness of the planar dielectric stack. An increase of F_i with $t_{\rm bot}$ clearly appears, representing a main feature of the cylindrical system. Moreover, the field increase is enhanced as the substrate radius is reduced, suggesting the possibility of an improvement in both the programming and retention dynamics.

From (3), the threshold-voltage shift ΔV_T resulting from electron storage in the nitride volume can be easily calculated as the increase of V_G required to restore the same F_i present in the cell when $n_t = 0$. From a straightforward analysis of (3) and of the coefficient C_1 given in the Appendix, we obtain

$$\Delta V_T = -\frac{qn_t}{2\epsilon_n}\left[r_{\rm bot}^2 \ln \frac{r_n}{r_{\rm bot}} - \frac{1}{2}\left(r_n^2 - r_{\rm bot}^2\right)\left(1 + \frac{2\epsilon_n}{\epsilon_{\rm top}} \ln \frac{r_{\rm top}}{r_n}\right)\right]. \quad (4)$$

This equation directly provides ΔV_T after uniform electron storage in the nitride and allows the extraction of the capacitance per unit length in the wire direction ($C_{\rm NG}$; units: F/cm) between the centroid of stored electrons and the gate

$$C_{\rm NG} = -\frac{Q}{\Delta V_T} = \frac{qn_t\pi\left(r_n^2 - r_{\rm bot}^2\right)}{\Delta V_T} \quad (5)$$

where $Q = -q\int_{r_{\rm bot}}^{r_n} 2\pi r n_t dr$ is the stored charge per unit length in the nitride (units: C/cm). Fig. 3 shows, however, that a rather negligible error occurs if $C_{\rm NG}$ is calculated assuming the trapped electron centroid in the middle of the nitride layer, i.e.,

$$C_{\rm NG}^{-1} = \frac{\ln(r_{\rm top}/r_n)}{2\pi\epsilon_{\rm top}} + \frac{\ln\left(r_n/(r_{\rm bot} + t_n/2)\right)}{2\pi\epsilon_n}. \quad (6)$$

Finally, it must be pointed out that the maximum electric field is located at the substrate/bottom-oxide interface even for negative V_G. This enhances the hole tunneling current from the substrate to the nitride during erase, as will be discussed in Section II-C. In addition, the quite lower electric field at the

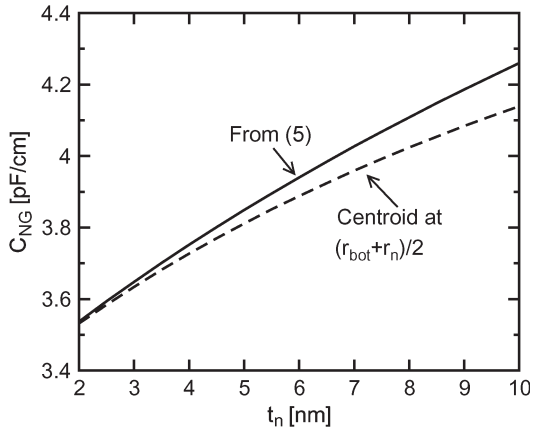


Fig. 3. $C_{\rm NG}$ calculated from (5) and assuming the trapped electron centroid at the middle of the nitride layer, for increasing t_n and fixed r_0, $t_{\rm bot}$, and $t_{\rm top}$.

gate/top-oxide interface should prevent electron injection from the gate, therefore relieving the erase saturation issues [19].

B. Tunneling Current Calculation

When quantization effects are accounted for in a cylindrical geometry, the energy eigenvalues are given by [20]

$$E_{l,i} = \frac{\hbar^2 \lambda_{l,i}^2}{2m^* r_0^2} \tag{7}$$

where $\lambda_{l,i}$ is the ith zero of the lth-order Bessel function. The electron concentration per unit length on each level $n_{l,i}$ is given by

$$n_{l,i} = \sqrt{\frac{4 g_l m_D^* k_B T}{\pi \hbar^2}} \mathcal{F}_{-1/2}\left(\frac{E_F - E_{l,i}}{k_B T}\right) \tag{8}$$

where $\mathcal{F}_{-1/2}$ is the Fermi–Dirac integral of order $-1/2$, $g_l = 1$ for $l = 0$ and 2 otherwise, and m_D^* is an "effective" density-of-state mass in the axial direction. Its value was computed requiring that the quantum charge concentration approaches the classical value for large quantization radii. In our case, we have chosen $m^* = m_l$ (the longitudinal mass of silicon), obtaining $m_D^* = 36 m_t^2/m_l$ (m_t is the silicon transverse mass). We have verified that the choice of m^* affects the results by less than an order of magnitude, which is good enough for our purposes. The tunneling current density (cm^{-1}) can now be calculated as

$$J_n' = q \sum \frac{n_{l,i}}{\tau_{l,i}} T_{l,i} \tag{9}$$

where $T_{l,i}$ is the tunneling probability and $\tau_{l,i}$ is the inverse of the attempt frequency. The tunneling probability is computed with the transfer-matrix method, following the work in [21], while for $\tau_{l,i}$, we have taken the radial round-trip time, adopting the same approach as in a planar geometry (which is somewhat justified by the similarity between the cylindrical and planar tunneling times reported in [22]).

Such a numerical approach may become unsuitable when fast evaluation of the device performance is needed; for this reason, a simplified WKB approximation mimicking a planar behavior has been proposed [13]. We instead follow an approach similar to [23] and analytically express J_n' via an FN equation [24], [25]

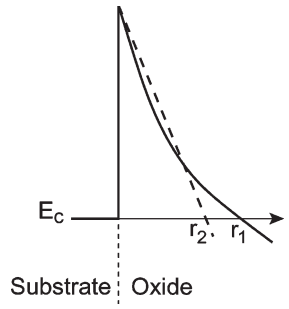


Fig. 4. (Solid line) Pictorial conduction-band profile in the GAA cell and (dashes) linear approximation providing the same tunneling probability.

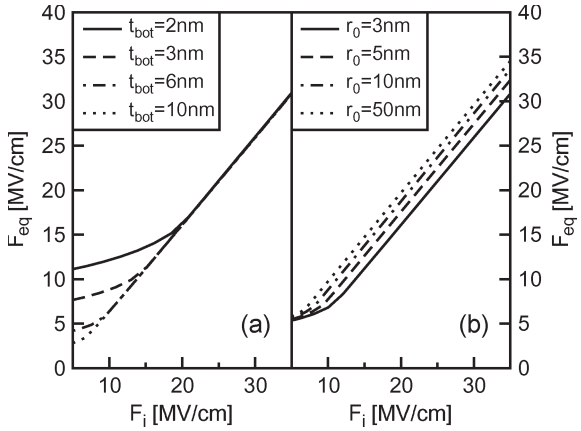


Fig. 5. $F_{\rm eq}$-versus-F_i relationship for different (a) $t_{\rm bot}$'s and (b) r_0's.

$$J_n' = A' F_{\rm eq}^2 \exp\left[-\frac{B}{F_{\rm eq}}\right] \tag{10}$$

where A' and B are constants including the physical parameters of the potential barrier and $F_{\rm eq}$ is an *effective* electric field. Its value can be computed requiring that the tunneling probability through the effective triangular barrier equals the one through the hyperbolic barrier given by (2). An analytical expression for $F_{\rm eq}$ can be obtained via the WKB approximation, leading to (see sketch in Fig. 4)

$$\int_0^{r_2} \sqrt{E_{\rm FN}(r)}\,dr = \int_0^{r_1} \sqrt{E_c(r)}\,dr \tag{11}$$

where E_c is the conduction-band energy profile, $E_{\rm FN}$ is its triangular approximation, and r_1 and r_2 are the tunneling distances. The result is

$$F_{\rm eq} = \frac{2\Phi_B^{3/2}}{3q\int_0^{r_1}\sqrt{E_c(r)}\,dr} \tag{12}$$

where $\Phi_B = 3.1$ eV is the electron tunneling barrier height (only tunneling from the bottom of the band is assumed for simplicity). Fig. 5 shows $F_{\rm eq}$ as a function of F_i for the template GAA MONOS cell when changing $t_{\rm bot}$ (a) or r_0 (b). A linear relation of unit slope clearly appears for sufficiently high F_i, with negligible dependence on $t_{\rm bot}$. For low values of F_i,

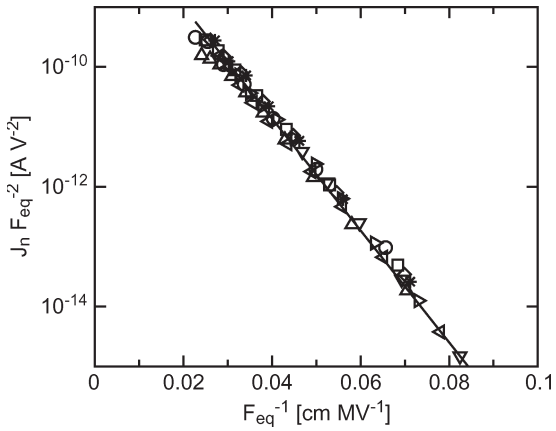


Fig. 6. Comparison between (symbols) (9) and (line) (14) for different r_0's ranging from 3 to 10 nm and $t_{\rm bot} = 3$ and 6 nm.

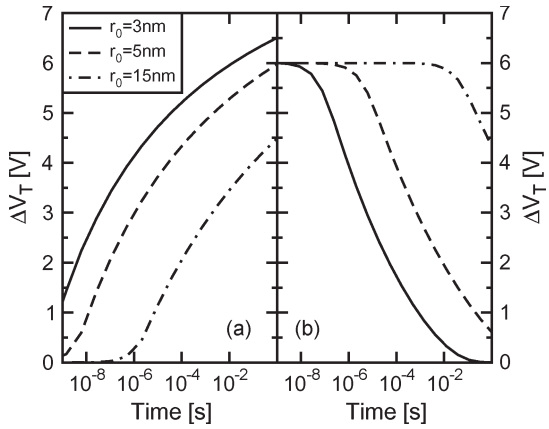


Fig. 7. Calculated (a) program and (b) erase transients at $V_G = \pm 12$ V on the template GAA-CT MONOS cell, for different r_0's. Note that the starting time is 10^{-12} s and $\Delta V_T = 0$ for all the program simulations.

instead, a departure from this relation is observed, due to a change in the tunneling regime from FN to direct tunneling. This region is not addressed in our analysis, as the resulting tunneling currents are too low to meet the programming specifications of nonvolatile devices. Fig. 5(b) shows, in addition, that the straight line describing the $F_{\rm eq}$-versus-F_i relation shifts toward higher F_i values when r_0 is decreased and can be fitted by

$$F_{\rm eq} = F_i - \frac{V_0}{r_0} \tag{13}$$

where $V_0 = 1.2$ V.

Fig. 6 shows a comparison between results obtained via (9) and (10). To achieve a better fit, however, the FN equation was not applied to J_n' but rather to the areal current density at the oxide/nitride boundary

$$J_n = \frac{J_n'}{2\pi r_{\rm bot}} = AF_{\rm eq}^2 \exp\left[-\frac{B}{F_{\rm eq}}\right]. \tag{14}$$

Note that a very good fit is achieved in the investigated range of $t_{\rm bot} = 3$ and 6 nm and r_0 ranging from 3 to 10 nm and beyond (the structure more closely resembles a planar one as r_0 increases). Moreover, the parameter values $A \approx 10^{-7}$ A $\cdot$ V^{-2} and $B \approx 215$ MV $\cdot$ cm^{-1} are basically the same as those extracted from planar structures. This is a consequence of the adoption of the effective field (12), which captures the main effect of the curvature on the tunneling barrier. The previous analysis was then extended to hole tunneling under negative V_G, yielding the following fitting parameters for (13) and (14): $V_0 = 1.5$ V, $B \approx 275$ MV $\cdot$ cm^{-1}, and A about a factor of two smaller than the electron value. However, it is worth pointing out that the reported values of A depend on the adopted approximation and parameter values and should not be regarded as definitive.

C. Transient Dynamics

Once analytical solutions for the electrostatic and tunneling problems are known, the program transients of the GAA-CT cell can be calculated with the following equation [26]:

$$\frac{dn_t}{dt} = \frac{J_n}{q}\left(\frac{r_{\rm bot}}{r_{\rm bot} + t_n/2}\right)\sigma_n(N_t - n_t) - e_n n_t \tag{15}$$

where N_t is the trap density in the nitride (units: cm^{-3}), σ_n is the electron trapping cross section (units: cm^2), and e_n is the Poole–Frenkel emissivity (units: s^{-1}) from filled nitride traps

$$e_n = \nu_0 \exp\left[-\frac{E_T - \beta\sqrt{\overline{F_n}}}{kT}\right]. \tag{16}$$

Here, ν_0 is the attempt-to-escape frequency from nitride filled traps (units: s^{-1}), E_T is the trap depth from the nitride conduction band, $\overline{F_n}$ is the average electric field in the nitride, and β is the Poole–Frenkel coefficient [27]. Note that (15) assumes that all the empty nitride traps see the same tunneling current, i.e., it neglects both distributed trapping along the nitride thickness and electron transport in the nitride conduction band, which were shown to barely impact the program operation of planar cells [26]. As a consequence, traps are concentrated in the middle of the nitride, and conservation of J_n leads to a correcting factor $r_{\rm bot}/(r_{\rm bot} + t_n/2)$ in (15). Fig. 7(a) shows the calculated programming transient on the template GAA MONOS cell at $V_G = 12$ V, assuming $N_t = 6 \times 10^{19}$ cm^{-3}, $\sigma_n = 5 \times 10^{-13}$ cm^2, and $\nu_0 = 5 \times 10^8$ s^{-1}. The programming dynamics are faster when r_0 is reduced, owing to a larger $F_{\rm eq}$ (hence J_n), as shown by (13) and in Fig. 2. This effect overrides the decrease of ΔV_T that is predicted by (4) for smaller r_0 and fixed thickness of the dielectrics.

To describe the erase operation, (15) was modified according to

$$\frac{dn_t}{dt} = -\frac{J_p}{q}\left(\frac{r_{\rm bot}}{r_{\rm bot} + t_n/2}\right)\sigma_r n_t - e_n n_t \tag{17}$$

where σ_r is the electron/hole recombination cross section (units: cm^2). Note that (15) and (17) do not have an analytical solution. However, they can be directly solved discretizing the time variable and updating the electric field (and, in turn, J_n, e_n, and J_p) at each time step.

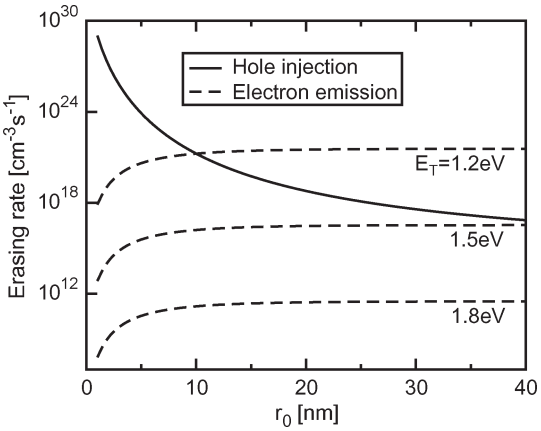


Fig. 8. Trap emptying rates due to hole injection and electron emission at the beginning of the erase transient on the template GAA-CT MONOS cell.

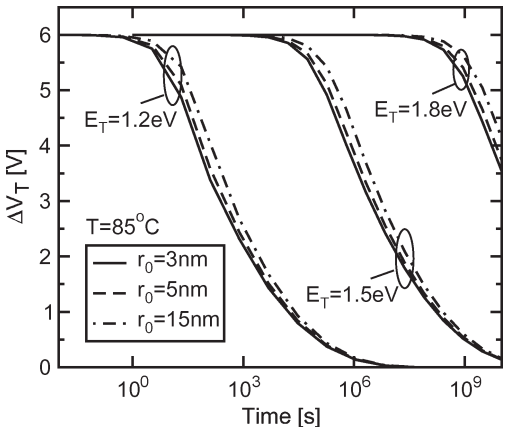


Fig. 9. Calculated retention transients at 85 °C on the template GAA-CT MONOS cell for different E_T's and r_0's.

Fig. 7(b) shows the calculated erase transients at $V_G = -12$ V for different r_0's when assuming $E_T = 1.5$ eV and $\sigma_r = 5 \times 10^{-13}$ cm^2. Also in this case, faster ΔV_T dynamics appear when reducing r_0, owing to the larger $F_{\rm eq}$. The roles of holes and electrons on the erase transients are shown in Fig. 8, where the trap emptying rates given by hole recombination $(J_p \sigma_r n_t/q)$ and electron emission $(e_n n_t)$ at the beginning of the erase transient ($\Delta V_T = 6$ V and $V_G = -12$ V) are shown as a function of r_0. Considering typical values of $E_T = 1.2-1.8$ eV [14], [19], [26], electron emission appears as the dominant erase mechanism for large r_0, while hole injection gains importance for small radii, due to the increase of $F_{\rm eq}$ and J_p. The value of r_0 marking the transition between the two mechanisms decreases as lower E_T is considered, due to the larger emission rate given by (16).

Finally, note that (17) can be also used to investigate the retention transients. Typical results at $T = 85$ °C are shown in Fig. 9, where the ΔV_T loss from the programmed state appears to depend strongly on E_T and more weakly on r_0. This is due to the dominant role played by electron emission from the nitride over hole injection from the substrate, as evident in Fig. 10, where the trap emptying rates given by hole recombination $(J_p \sigma_r n_t/q)$ and electron emission $(e_n n_t)$ at the beginning of the retention transient ($\Delta V_T = 6$ V and $V_G = 0$ V) are shown as a function of r_0.

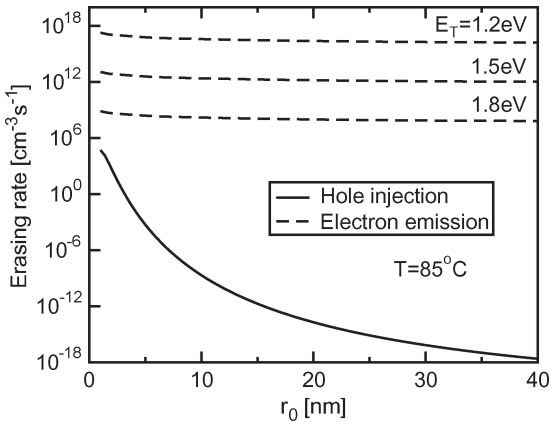


Fig. 10. Trap emptying rates due to hole injection and electron emission at the beginning of the retention transient on the template GAA-CT MONOS cell, at $T = 85$ °C.

D. Substrate Effects

Detailed analysis of the electrostatics of GAA MOSFETs [28], [29] showed that the surface potential saturates at around 0.6 V for increasing V_G, with rather negligible dependence on r_0. As a consequence, a first-order account of both the potential drop in the substrate and the built-in potential derived from the work-function difference between the metal gate and the silicon can be obtained by adding a correcting factor to the gate bias V_G. Such a term should be constant for programming and long-term retention, while a dependence on V_G should be included for cell erase. In fact, the potential profile in the substrate strongly depends on the hole supply mechanism during the short erase pulses, which is related to the carrier generation process. This may depend on physical cell details, such as source/drain junction doping, and its accurate inclusion is not straightforward even in advanced models [14]. As a result, we followed the approach in [19] and adopted a linear increase of the surface potential with V_G.

III. Modeling Results

The model will now be compared with experimental data on GAA SONOS cells taken from the literature to assess its validity. A parametric analysis of the program, erase, and retention performance of GAA-CT memory devices will then be presented, focusing on the dependence on r_0.

A. Comparison With Experimental Data

Fig. 11 shows a comparison of our model results with experimental data for the program/erase transients of a GAA SONOS cell with $r_0 = 3$ nm and oxide/nitride/oxide layers of 6/5/8 nm [19]. A reasonably good agreement appears, using the following parameters: $N_t = 5.3 \times 10^{19}$ cm^{-3}, $\sigma_n = 2 \times 10^{-12}$ cm^2, $\sigma_r = 10^{-12}$ cm^2, $\nu_0 = 5 \times 10^8$ s^{-1}, and $E_T = 1.5$ eV. Note that the mismatch between data and modeling results during programming at $V_G = 18$ V can be attributed to a reduction of the trapping efficiency at large bias, as previously reported in [26], which is not included in the current model. Moreover, at

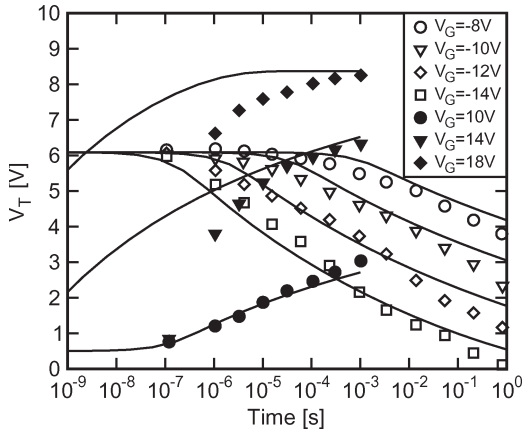


Fig. 11. (Symbols) Experimental data [19] and (lines) calculated results for the program/erase transients on a GAA-CT SONOS cell with $r_0 = 3$ nm. Note that the starting time of all the simulations is 10^{-12} s.

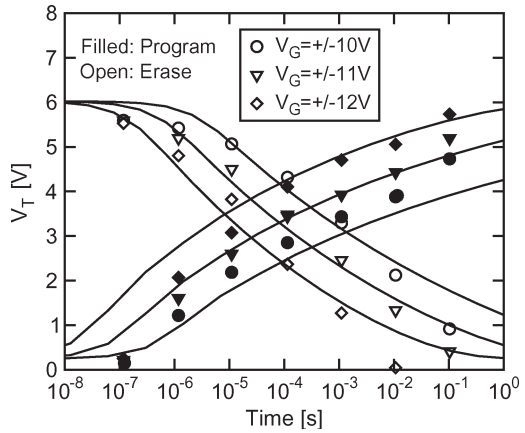


Fig. 12. (Symbols) Experimental data [10] and (lines) calculated results for the program/erase transients of a GAA-CT TAHOS cell with $r_0 = 12$ nm.

the shortest times experimentally investigated in the figure, the possibility for spurious delays to compromise the pulse shape reaching device gate should be accounted for.

Recently, the employment of high-k dielectrics in conjunction with a metal gate has been shown feasible for the GAA technology [10]. Fig. 12 shows that a good agreement between modeling and experimental results is also achieved for a GAA TAHOS ($TaN/Al_2O_3/HfO_2/SiO_2/Si$) cell having $r_0 = 12$ nm and an A/H/O gate stack of 10/7/5 nm (data taken from [10]; see this paper for more details on the device structure). Parameter values used for modeling are $N_t = 5 \times 10^{19}$ cm^{-3}, $\sigma_n = 5 \times 10^{-13}$ cm^2, $\sigma_r = 5 \times 10^{-13}$ cm^2, $\nu_0 = 5 \times 10^8$ s^{-1}, $E_T = 1.5$ eV, $\epsilon_{\rm top} = 10\epsilon_0$, and $\epsilon_n = 18\epsilon_0$, where ϵ_0 is the vacuum dielectric constant. Note that we have considered the alumina as an ideal dielectric, neglecting any possibility of charge trapping in this layer. Previous works [30]–[32] have shown that alumina trapping may play a role for long pulse durations, when large ΔV_T is reached. This can slightly impact the evaluation of N_t, without changing the overall conclusions. Although our model can be straightforwardly extended to include the trapping in the top oxide layer, this is beyond the scope of this paper.

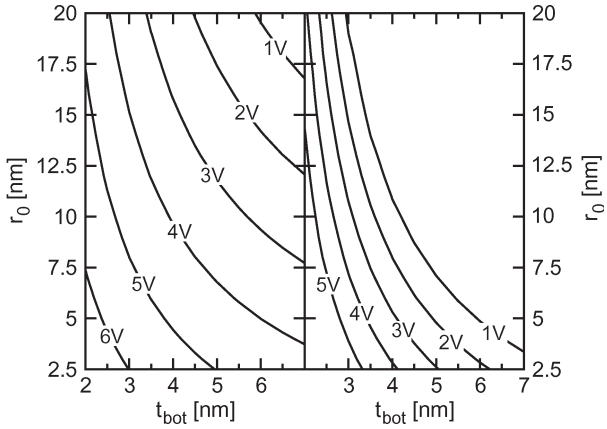


Fig. 13. Iso-ΔV_T curves corresponding to the V_T shift after 1-ms (left) program or (right) erase pulse for the template GAA-CT cell.

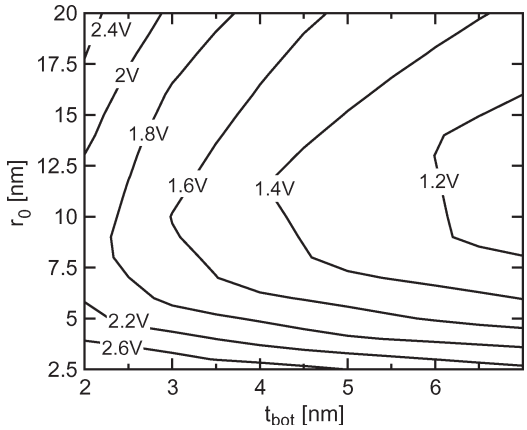


Fig. 14. Same as in Fig. 13 but for the iso-ΔV_T curves after 10^6 s at 85 °C from a 6-V programmed level.

These results confirm that the simple model can reproduce the main features of the program/erase dynamics on different GAA-CT cells and can be used as an easy-to-implement tool for device optimization.

B. Parametric Analysis of GAA-CT Cells

We first investigated the impact of r_0 and $t_{\rm bot}$ on ΔV_T after a 1-ms program or erase pulse on the template GAA-CT cell, keeping $t_n = 6$ nm and $t_{\rm top} = 7$ nm and retaining the same parameters used in Section II-C, which are similar to those extracted from the experimental data and in good agreement with those in [14] and [26]. ΔV_T was measured from the neutral state during program and from a programmed V_T shift of 6 V during erase. Fig. 13 shows the iso-ΔV_T curves in the $t_{\rm bot}-r_0$ plot, revealing that a reduction of these parameters accelerates the program/erase dynamics, with a stronger sensitivity to $t_{\rm bot}$. For a careful cell design, however, these results should be coupled with those shown in Fig. 14, displaying the iso-ΔV_T curves after 10^6 s of data retention at 85 °C from a 6-V programmed state. A nonnegligible increase of the retention loss appears when r_0 is reduced below 5 nm for the whole explored range of $t_{\rm bot}$, making it clear that a tradeoff must be considered.

IV. Conclusion

This paper has presented a physics-based analytical model for the transient operation of GAA-CT cells, based on an FN tunneling through an effective barrier which captures the cylindrical geometry. The model represents a computationally efficient tool for the electrical investigation of the GAA-CT memory technology.

Appendix

The expressions for the constants C_i $(i = 1-3)$ appearing in (2) are

$$C_1 = \frac{V_G}{\alpha} + \frac{qn_t}{2\epsilon_n \alpha}\left[r_{\rm bot}^2 \ln\frac{r_n}{r_{\rm bot}} \frac{1}{2}\left(r_n^2 - r_{\rm bot}^2\right)\left(1 + 2\frac{\epsilon_n}{\epsilon_{\rm top}} \ln\frac{r_{\rm top}}{r_n}\right)\right]$$

$$C_2 = \frac{\epsilon_{\rm bot}}{\epsilon_n} C_1 - \frac{qn_t}{2\epsilon_n} r_{\rm bot}^2$$

$$C_3 = \frac{\epsilon_{\rm bot}}{\epsilon_{\rm top}} C_1 - \frac{qn_t}{2\epsilon_{\rm top}}\left(r_{\rm bot}^2 - r_n^2\right)$$

where α is given by

$$\alpha = \frac{\epsilon_{\rm bot}}{\epsilon_{\rm top}} \ln\frac{r_{\rm top}}{r_n} + \ln\frac{r_{\rm bot}}{r_0} + \frac{\epsilon_{\rm bot}}{\epsilon_n} \ln\frac{r_n}{r_{\rm bot}}.$$

Acknowledgment

The authors would like to thank M. Buttafava of Politecnico di Milano and P. Cappelletti, E. Camerlenghi, R. Bez, and L. Baldi of Micron Technology, Inc., for discussions and support.

References

[1] Y. Fukuzumi, R. Katsumata, M. Kito, M. Kido, M. Sato, H. Tanaka, Y. Nagata, Y. Matsuoka, Y. Iwata, H. Aochi, and A. Nitayama, "Optimal integration and characteristics of vertical array devices for ultra-high density, bit-cost scalable Flash memory," in *IEDM Tech. Dig.*, 2007, pp. 449–452.

[2] R. Katsumata, M. Kito, Y. Fukuzumi, M. Kido, H. Tanaka, Y. Komori, M. Ishiduki, J. Matsunami, T. Fujiwara, Y. Nagata, L. Zhang, Y. Iwata, R. Kirisawa, H. Aochi, and A. Nitayama, "Pipe-shaped BiCS Flash memory with 16 stacked layers and multi-level-cell operation for ultra high density storage devices," in *VLSI Symp. Tech. Dig.*, 2009, pp. 136–137.

[3] J. Jang, H.-S. Kim, W. Cho, H. Cho, J. Kim, S. Shim, Y. Jang, J.-H. Jeong, B.-K. Son, D. W. Kim, K. Kim, J.-J. Shim, J. S. Lim, K.-H. Kim, S. Y. Yi, J.-Y. Lim, D. Chung, H.-C. Moon, S. Hwang, J.-W. Lee, Y.-H. Son, U.-I. Chung, and W.-S. Lee, "Vertical cell array using TCAT (terabit cell array transistor) technology for ultra high density NAND Flash memory," in *VLSI Symp. Tech. Dig.*, 2009, pp. 192–193.

[4] J. Kim, A. J. Hong, S. M. Kim, E. B. Song, J. H. Park, J. Han, S. Choi, D. Jang, J.-T. Moon, and K. L. Wang, "Novel vertical-stacked-array-transistor (VSAT) for ultra-high-density and cost-effective NAND Flash memory devices and SSD (solid state drive)," in *VLSI Symp. Tech. Dig.*, 2009, pp. 186–187.

[5] W. Kim, S. Choi, J. Sung, T. Lee, C. Park, H. Ko, J. Jung, I. Yoo, and Y. Park, "Multi-layered vertical gate NAND Flash overcoming stacking limit for terabit density storage," in *VLSI Symp. Tech. Dig.*, 2009, pp. 188–189.

[6] A. Hubert, E. Nowak, K. Tachi, V. Maffini-Alvaro, C. Vizioz, C. Arvet, J.-P. Colonna, J.-M. Hartmann, V. Loup, L. Baud, S. Pauliac, V. Delaye, C. Carabasse, G. Molas, G. Ghibaudo, B. D. Salvo, O. Faynot, and T. Ernst, "A stacked SONOS technology, up to 4 levels and 6 nm crystalline nanowires, with gate-all-around or independent gates (ϕ-Flash), suitable for full 3D integration," in *IEDM Tech. Dig.*, 2009, pp. 637–640.

[7] J. Fu, K. D. Buddharaju, S. H. G. Teo, C. Zhu, M. B. Yu, N. Singh, G. Q. Lo, N. Balasubramanian, and D. L. Kwong, "Trap layer engineered gate-all-around vertically stacked twin Si-nanowire nonvolatile memory," in *IEDM Tech. Dig.*, 2007, pp. 79–82.

[8] K. H. Yeo, K. H. Cho, M. Li, S. D. Suk, Y.-Y. Yeoh, M.-S. Kim, H. Bae, J.-M. Lee, S.-K. Sung, J. Seo, B. Park, D.-W. Kim, D. Park, and W.-S. Lee, "Gate-all-around single silicon nanowire MOSFET with 7 nm width for SONOS NAND Flash memory," in *VLSI Symp. Tech. Dig.*, 2008, pp. 138–139.

[9] M. Chen, H. Y. Yu, N. Singh, Y. Sun, N. S. Shen, X. Yuan, G.-Q. Lo, and D.-L. Kwong, "Vertical-Si-nanowire SONOS memory for ultrahigh-density application," *IEEE Electron Device Lett.*, vol. 30, no. 8, pp. 879–881, Aug. 2009.

[10] J. Fu, N. Singh, C. Zhu, G.-Q. Lo, and D.-L. Kwong, "Integration of high-k dielectrics and metal gate on gate-all-around Si-nanowire-based architecture for high-speed nonvolatile charge-trapping memory," *IEEE Electron Device Lett.*, vol. 30, no. 6, pp. 662–664, Jun. 2009.

[11] H.-T. Lue, T.-H. Hsu, S.-Y. Wang, E.-K. Lai, K.-Y. Hsieh, R. Liu, and C.-Y. Lu, "Study of incremental step pulse programming ISPP and STI edge effect of BE-SONOS NAND Flash," in *Proc. IRPS*, 2008, pp. 693–694.

[12] H.-T. Lue, T.-H. Hsu, Y.-H. Hsiao, S.-C. Lai, E.-K. Lai, S.-P. Hong, M.-T. Wu, F. H. Hsu, N. Z. Lien, C.-P. Lu, S.-Y. Wang, J.-Y. Hsieh, L.-W. Yang, T. Yang, K.-C. Chen, K.-Y. Hsieh, R. Liu, and C.-Y. Lu, "Understanding STI edge fringing field effect on the scaling of charge-trapping (CT) NAND Flash and modeling of incremental step pulse programming (ISPP)," in *IEDM Tech. Dig.*, 2009, pp. 839–842.

[13] E. Nowak, M. Bocquet, L. Perniola, G. Ghibaudo, G. Molas, C. Jahan, R. Kies, G. Reimbold, B. D. Salvo, and F. Boulanger, "New physical model for ultra-scaled 3D nitride-trapping non-volatile memories," in *IEDM Tech. Dig.*, 2008, pp. 559–562.

[14] E. Gnani, S. Reggiani, A. Gnudi, G. Baccarani, J. Fub, N. Singh, G. Lo, and D. Kwong, "Modeling of gate-all-around charge trapping SONOS memory cells," *Solid State Electron.*, vol. 54, no. 9, pp. 997–1002, Sep. 2010.

[15] S. Bangsaruntip, G. M. Cohen, A. Majumdar, and J. W. Sleight, "Universality of short-channel effects in undoped-body silicon nanowire MOSFETs," *IEEE Electron Device Lett.*, vol. 31, no. 9, pp. 903–905, Sep. 2010.

[16] H. Borli, S. Kolberg, T. A. Fjeldly, and B. Iniguez, "Precise modeling framework for short-channel double-gate and gate-all-around MOSFETs," *IEEE Trans. Electron Devices*, vol. 55, no. 10, pp. 2678–2686, Oct. 2008.

[17] T.-H. Hsu, H.-T. Lue, E.-K. Lai, J.-Y. Hsieh, S.-Y. Wang, L.-W. Yang, Y.-C. King, T. Yang, K.-C. Chen, K.-Y. Hsieh, R. Liu, and C.-Y. Lu, "A high-speed BE-SONOS NAND Flash utilizing the field-enhancement effect of FinFET," in *IEDM Tech. Dig.*, 2007, pp. 913–916.

[18] T.-H. Hsu, H.-T. Lue, Y.-C. King, Y.-H. Hsiao, S.-C. Lai, K.-Y. Hsieh, R. Liu, and C.-Y. Lu, "Physical model of field enhancement and edge effects of FinFET charge-trapping NAND Flash devices," *IEEE Trans. Electron Devices*, vol. 56, no. 6, pp. 1235–1242, Jun. 2009.

[19] E. Nowak, A. Hubert, L. Perniola, T. Ernst, G. Ghibaudo, G. Reimbold, B. D. Salvo, and F. Boulanger, "In-depth analysis of 3D silicon nanowire SONOS memory characteristics by TCAD simulations," in *Proc. IMW Tech. Dig.*, 2010, pp. 116–119.

[20] L. Wang, D. Wang, and P. Asbeck, "A numerical Schrödinger–Poisson solver for radially symmetric nanowire core-shell structures," *Solid State Electron.*, vol. 50, no. 11/12, pp. 1732–1739, Nov./Dec. 2006.

[21] E.-X. Ping, "I–V characteristics by radial tunneling in double-barrier tunneling diodes with cylindrical barriers," *IEEE J. Quantum Electron.*, vol. 31, no. 7, pp. 1210–1215, Jul. 1995.

[22] E.-X. Ping, "Büttiker–Landauer traversal times in the radial direction of cylindrical single and double barriers," *J. Appl. Phys.*, vol. 76, no. 3, pp. 1929–1931, Aug. 1994.

[23] W. Brown and J. Brewer, *Nonvolatile Semiconductor Memory Technology*. Piscataway, NJ: IEEE Press, 1997, pp. 163–166.

[24] M. Lenzlinger and E. H. Snow, "Fowler–Nordheim tunneling into thermally grown SiO_2," *J. Appl. Phys.*, vol. 40, no. 1, pp. 278–283, Jan. 1969.

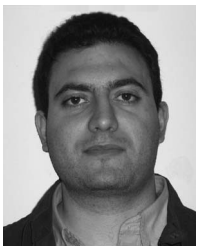
[25] Y. L. Chiou, J. F. Gambino, and M. Mohammad, "Determination of the Fowler–Nordheim tunneling parameters from the Fowler-Nordheim plot," *Solid State Electron.*, vol. 45, no. 10, pp. 1787–1791, Oct. 2001.

[26] C. Monzio Compagnoni, A. Mauri, S. M. Amoroso, A. Maconi, and A. S. Spinelli, "Physical modeling for programming of TANOS memories in the Fowler–Nordheim regime," *IEEE Trans. Electron Devices*, vol. 56, no. 9, pp. 2008–2015, Sep. 2009.

[27] S. Manzini and F. Volonté, "Charge transport and trapping in silicon nitride-silicon dioxide dielectric double layers," *J. Appl. Phys.*, vol. 58, no. 11, pp. 4300–4306, Dec. 1985.

[28] J. He, Y. Tao, F. Liu, J. Feng, and S. Yang, "Analytic channel potential solution to the undoped surrounding-gate MOSFETs," *Solid State Electron.*, vol. 51, no. 5, pp. 802–805, May 2007.

[29] D. Jiménez, B. Iñíguez, J. Suñé, L. F. Marsal, J. Pallarès, J. Roig, and D. Flores, "Continuous analytic I–V model for surrounding-gate MOSFETs," *IEEE Electron Device Lett.*, vol. 25, no. 8, pp. 571–573, Aug. 2004.
[30] S. M. Amoroso, A. Mauri, N. Galbiati, C. Scozzari, E. Mascellino, E. Camozzi, A. Rangoni, T. Ghilardi, A. Grossi, P. Tessariol, C. Monzio Compagnoni, A. Maconi, A. L. Lacaita, A. S. Spinelli, and G. Ghidini, "Reliability constraints for TANOS memories due to alumina trapping and leakage," in *Proc. IRPS*, 2010, pp. 966–969.
[31] L. Larcher, A. Padovani, V. della Marca, P. Pavan, and A. Bertacchini, "Investigation of trapping/detrapping mechanisms in Al_2O_3 electron/hole traps and their influence on TANOS memory operation," in *Proc. VLSI-TSA*, 2010, pp. 52–53.
[32] G. Molas, L. Masoero, P. Blaise, A. Padovani, J. P. Colonna, E. Vianello, M. Bocquet, E. Nowak, M. Gasulla, O. Cueto, H. Grampeix, F. Martin, R. Kies, P. Brianceau, M. Gely, A. M. Papon, D. Lafond, J. P. Barnes, C. Licitra, G. Ghibaudo, L. L. S. Deleonibus, and B. De Salvo, "Investigation of the role of H-related defects in Al_2O_3 blocking layer on charge-trap memory retention by atomistic simulations and device physical modelling," in *IEDM Tech. Dig.*, 2010, pp. 536–539.



Salvatore Maria Amoroso (S'10) was born in Catania, Italy, in 1983. He received the B.S. and M.S. degrees in physics engineering from Politecnico di Milano, Milano, Italy, in 2005 and 2008, respectively, where he has been working toward the Ph.D. degree in information technology in the Dipartimento di Elettronica e Informazione since 2009.

He is also currently with the Italian University NanoElectronics Team, Milano. His research activities include modeling and numerical simulation of semiconductor devices, with particular interest on innovative nonvolatile memories.

Christian Monzio Compagnoni (M'08) was born in Busto Arsizio, Italy, in 1976. He received the Laurea degree (*cum laude*) in electronics engineering and the Ph.D. degree in information technology from Politecnico di Milano, Milano, Italy, in 2001 and 2005, respectively.

Since 2002, he has been with the Dipartimento di Elettronica e Informazione, Politecnico di Milano, where he has been an Assistant Professor since 2006. He is also currently with the Italian University NanoElectronics Team, Milano. His research interests include characterization and modeling of advanced nonvolatile memories and metal–oxide–semiconductor devices.

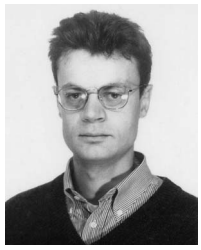
Dr. Monzio Compagnoni was a member of the memory committee of the IRPS in 2009 and 2010. He was the recipient of the Outstanding Paper Award at the IRPS in 2008.

Aurelio Mauri was born in 1969. He received the M.S. degree (*cum laude*) in plasma physics from the University of Milano, Milano, Italy, in 1995, after classical studies.

Then, he was with Rutherford Appleton Laboratory, Didcot, U.K., and ENEA-Frascati, Frascati, Italy, where he spent a research period on characterization and modeling of the high dense plasmas produced by laser confinement. In 1996, he started to work for a semiconductor company focused on chemistry treatment of the silicon surfaces. From 1998 to 2000, he spent a "nonworking" time helping young generation. In 2000, he was with STMicroelectronics, where he worked in the Nonvolatile Technology Development TCAD Group in 2004. He is currently with R&D Technology Development, Micron Technology, Inc., Agrate Brianza, Italy (formerly, Numonyx). His research interests include, for electronics, modeling of advanced nonvolatile memories and tunneling in dielectrics media and, for physics, advanced modeling of impurity diffusion in silicon with kinetic Monte Carlo approach and of materials properties with *ab initio* approach.

Alessandro Maconi was born in Carate Brianza, Italy, in 1983. He received the Laurea degree in electronics engineering from Politecnico di Milano, Milano, Italy, in 2008, where he has been working toward the Ph.D. degree in the Dipartimento di Elettronica e Informazione since 2009.

He is also currently with the Italian University NanoElectronics Team, Milano. His research activities mainly involve characterization and modeling of advanced nonvolatile memories, with particular interests to TANOS memories.



Alessandro S. Spinelli (M'99–SM'07) was born in Bergamo, Italy, in 1966. He received the Laurea (*cum laude*) and Ph.D. degrees in electronics engineering from Politecnico di Milano, Milano, Italy.

In 1995, he was a Visiting Scholar with the University of Tennessee Space Institute, Tullahoma, where he worked on single-molecule detection in solution. In 1996, he was a Consultant with the Central Department of Research and Development, STMicroelectronics, Agrate Brianza, Italy. In 1997, he was an Assistant Professor with Politecnico di Milano. In 1998, he was an Associate Professor of electronics with Università degli Studi dell'Insubria, Como, Italy. In 2001, he was a Visiting Professor with the Institute National Polytechnique de Grenoble, Grenoble, France. Since 2006, he has been a Full Professor of electronics with Politecnico di Milano. He is also currently with the Italian University NanoElectronics Team, Milano, and with the Istituto di Fotonica e Nanotecnologie, Consiglio Nazionale delle Ricerche, Milano. He has conducted experimental and theoretical research in electronics instrumentation and microelectronics, coauthoring more than 140 papers published in international journals or presented at international conferences. His current research interests include experimental characterization and modeling of nonvolatile memory cells reliability, development of innovative nonvolatile memories, and circuit design for neural signal readout.

Dr. Spinelli has served in the technical committees of the IEDM and IRPS conferences.

Andrea L. Lacaita (F'09) received the Laurea degree in nuclear engineering from Politecnico di Milano, Milano, Italy, in 1985.

In 1989–1990, he was a Visiting Scientist/Professor with the AT&T Bell Laboratories, Murray Hill, NJ. From 1987 to 1992, he was a Researcher with the Italian National Research Council (CNR). In 1999, he was a Visiting Scientist/Professor with IBM T.J. Watson Research Center, Yorktown Heights, NY. He is currently with Politecnico di Milano, Milano, Italy, where he was an EE Professor, the Department Chair of the Dipartimento di Elettronica ad Informazione from 2006 to 2008, and a member of the Academic Senate from 2007 to 2008 and has been the Head of the Micro and Nanoelectronics Laboratory since 1992 and a Full Professor of electronics since 2000, currently teaching "electron devices" and "electronic circuit design." He is also currently with the Italian University NanoElectronics Team, Milano, and with the Istituto di Fotonica e Nanotecnologie, Consiglio Nazionale delle Ricerche, Milano. In the field of device physics, he has contributed to study quantum effects as well as experimental characterization techniques and numerical models of nonvolatile memories, both Flash and emerging (PCM and RRAM). He is the coauthor of several patents and educational books in electronics and more than 200 papers published in international journals or presented to international conferences.

Dr. Lacaita has been serving in several scientific committees: IEEE-IEDM (2001–2002), IEDM European Chair (2003–2004), ESSDERC (2005 and 2009), and IEEE VLSI Symposium (2005–2008).