Reliable bounds for the propagation delay in VLSI nano interconnects based on Multi Wall Carbon Nano Tubes

Biagio De Vivo, Patrizia Lamberti, Member IEEE, Giovanni Spinelli, Vincenzo Tucci, Member IEEE
Dept. of Electrical and Information Engineering – University of Salerno
Via Ponte don Melillo, 1 84084 Fisciano (SA) Italy
e-mail: {bdevivo, plamberti, gspinelli, vtucci}@unisa.it.
Phone: +39-089-964161

Abstract

The upper and lower bounds of the time-delay due to the variations of some physical and geometrical characteristics of a nano-interconnect based on Multi Wall CNTs, suitable for the 32 and 22nm technology, are evaluated. Interval Analysis is used to define the ranges of the of the p.u.l. parameters of a Transmission Line modeling the interconnect. The Vertex Analysis is then exploited on the parameter space to obtain in a reliable way the time-delay bounding without extensive and costly simulation burden. The obtained results are compared with those of scaled down copper-based structures.

Introduction

Carbon NanoTubes (CNTs) have been proposed as a possible alternative to copper interconnects for future very large scale integration (VLSI) systems [1]. The CNTs, characterised by electron mean-free path of the order of the micrometers, high current carrying capability and remarkable thermal and mechanical stability may be single-walled (SWCNTs, i.e. only one shell) or multi-walled (MWCNTs i.e. nested tubes). The most promising interconnect solutions allowing the reduction of the considerable contact resistance of a SWCNT are based on bundles of SWCNTs and on MWCNTs due to the possibility to contact also their interior conducting shells [3]. A comprehensive state-of-the-art concerning the different research efforts connected with the production use of CNTs in future nano-interconnects can be found in a very recent paper [4].

In order to predict the propagation characteristics along CNTs structures equivalent Transmission Line (TL) models have been developed which take into account the peculiar CNTs conduction characteristics [5]. However, studies based on these models do not usually take into account the variations of different physical properties and geometric parameters of the interconnect structure, which in turn may sensibly affect the propagation performances [10]. Indeed, a knowledge not only of the nominal value, but also of the range in which the desired performance is expected to vary may prove useful for a more accurate and reliable design of the considered system.

Therefore, in this paper the range of the 50% time delay, due to the variability of some relevant process-dependent parameters for two MWCNTs-based interconnect (22 and 32nm), in presence also of variability on both driver and load characteristics, is evaluated by exploiting the peculiarities of the Interval Arithmetic (IA) and the Vertex Analysis (VA). In particular, the monotonic inclusion property of IA [11] is used in order to obtain the ranges, due to the uncertainties, assumed by the per unit length (p.u.l.) parameters of a widely used Transmission Line (TL) modelling the electrical dynamics of the MWCNTs-based interconnect. The VA is then exploited on the parameter space to identify proper sets to be adopted in a few simulations leading to a reliable time-delay bounding without repetitive simulator runs, as required, for example, with Monte Carlo approach. A commercial circuital simulator (Simulink®) is adopted to perform the time domain simulations allowing to evaluate the time-delay. Also the variability of the driver and load parameters are taken into consideration. The results obtained for the MWCNTs interconnect are compared with those of scaled down copper-based structures.

Nano-IC based on MWCNTs and associated TL model

The schematic set-up of the considered device is shown in Figure 1 a) whereas the cross section of the MWCNT-based line is shown in Figure 1 b). Two values are assumed for the linewidth w=22 or 32nm, according to the technological developments described by the ITRS [13]. An aspect ratio A_r=1 is adopted. The MWCNT, with external radius r_N=w/2, is at the distance d from a perfect electric conductor (PEC) ground plane and is immersed in a medium characterised by a relative permittivity ε_r.

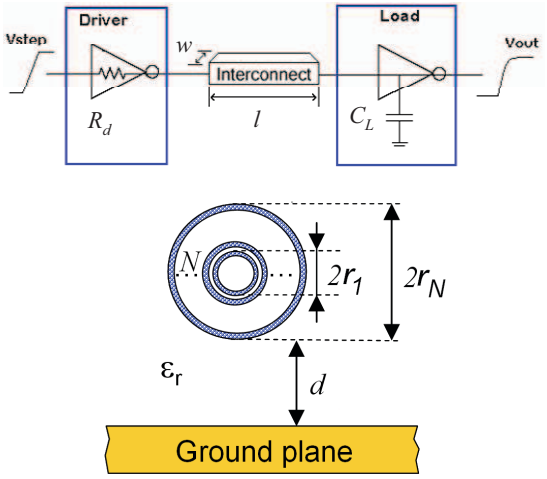

Figure 1. Schematic illustration of the MWCNT-based nano-IC, a) and the cross section of the MWCNTs structure, b).

The number of shells (walls) N is chosen by fixing the internal radius r_1 of the MWCNTs to be ½*r_N and the distance between adjacent shells δ to be 0.34 nm (van der Waals distance):

$$N = int\_part\,[(r_N - r_1)/\delta] - 1 \qquad (1)$$

where *int_part* represent the integer part of the number.

The ranges, chosen by considering either technological uncertainties or future manufacturing improvements, of the relevant geometric and physical parameters of the considered nano-IC configurations are indicated in Table I.

Table I. Variable parameters and their ranges

parameter	Nominal value	Variation/Range
$w=2\times r_N$ [nm]	22, 32	±10%
ε_r	3	[3, 10]
d [nm]	50	±10%
T [K]	293.15	[293.15, 393.15]
r_1 [nm]	$w/4$	±10%
R_{mj} [kΩ]	100	[0,120]

According to [9] the interconnect is modelled by an equivalent Single Conductor lossy TL, as depicted in Figure 2.

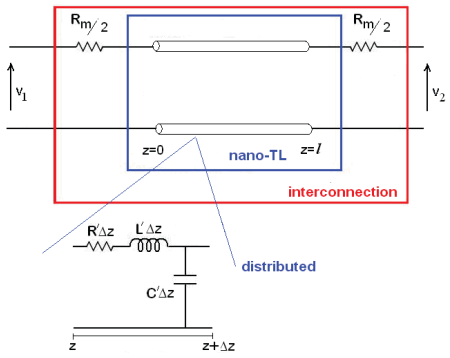

Figure 2. TL modeling the MWCNT-based nano-IC.

The lumped parameter R_m takes in to account the contact resistance, R_{mj}, of each shell and the intrinsic resistance, R_i, of each conducting channel:

$$R_m = \left[\sum_{j=1}^{N} \left(\frac{R_i}{2n_j} + R_{mj} \right)^{-1} \right]^{-1} \tag{2}$$

where n_j is the number of conducting channels of the j-th shell in the statistic conduction model [5]. This quantity is dependent from the operating temperature T and the shell radius r_j

$$n_j = \begin{cases} 2aTr_j + b & r_j > \dfrac{d_T}{2T} \\ \dfrac{2}{3} & r_j < \dfrac{d_T}{2T} \end{cases} \tag{3}$$

with a =3.87×10−4 nm$^{-1}K^{-1}$, b=0.2, and d_T = 1300 nm K.
The total number of conducting channel, n_{tot}, is given by the sum of the conducting channel of each shell $n_{tot} = \sum_{j=1}^{N} n_j$. The conduction mechanism taking place in the CNTs may be nominally ballistic (lossless) or dissipative. In fact, every shell is characterized by a different mean free path, $\lambda_{mfp,j}$, that can be expressed as:

$$\lambda_{mfp,j} = \frac{2*10^3 r_j}{(T/T_0) - 2} \tag{4}$$

with T_0=100°K. When the length of the interconnect is lower than the critical mean free path corresponding to the external tube $\lambda_{mfp,N}$, the wall is characterised by ballistic transport. Thus it short-circuits all the other walls leading the entire structure to ballistic transport. Therefore, depending on the length of the interconnect the TL model may include or not the p.u.l. resistances R' associated to the conduction mechanism:

$$R' = \begin{cases} \left[\sum_{j=1}^{N} \dfrac{2n_j}{R_i} \lambda_{mfp,j} \right]^{-1} & if \quad l > \lambda_{mfp,N} \\ 0 & otherwise \end{cases} \tag{5}$$

The p.u.l. inductance L' takes into account both the magnetic, $L_{m_{MWCNT}}$ and the kinetic inductance of each conducting channel, $L_k = h/\left(2e^2 \upsilon_F\right)$:

$$L' = L_{m_{MWCNT}} + \frac{L_k}{2n_{tot}} = \frac{\mu_0}{2\pi} \cosh^{-1}\left(\frac{r_N + d}{r_N} \right) + \frac{L_k}{2n_{tot}} \tag{6}$$

The p.u.l. capacitance C' includes the effect of the electrostatic capacitance of the MWCNT, C_e and the quantum capacitance of each conducting channel, $C_q = 2e^2/\left(h\upsilon_F\right)$:

$$C' = \left(\frac{1}{C_e} + \frac{1}{2n_{tot}C_q} \right)^{-1} = \left(\frac{\cosh^{-1}\left[(r_N + d)/r_N \right]}{2\pi\varepsilon_0\varepsilon_r} + \frac{1}{2n_{tot}C_q} \right)^{-1} \tag{7}$$

Range evaluation of the circuital parameters by using IA

In [14] it has already been shown that, in presence of parameters variations, IA permits a straight determination of an interval that certainly includes the true range of a function. In particular, by substituting the operations on real numbers $\underline{x} \in \Re^n$ with those on intervals $\underline{X} \in I\Re^n$, we get the Interval Extension (IE) $F(\underline{X})$ of a function $f(\underline{x})$: $\underline{x} \to \underline{X} \Rightarrow f(\underline{x}) \to F(\underline{X})$.

Due to the "inclusion property" [11], the IE certainly includes the range of $f(\underline{x})$ $\forall \underline{x} \in \underline{X}$, $f(\underline{X})$, i.e. $f(\underline{X}) \subseteq F(\underline{X})$. Therefore, the ranges of the circuital parameters in Figure 2 can be obtained by considering $f(\cdot)=\{R_m, R', L', C'\}$ and $\underline{x}=(w, \varepsilon_r, d, T, r_1, R_{mj})$.

In presence of variations on the input variables, the hypercube

$\underline{X}=[w_{min},w_{max}]\times[\varepsilon_{r,min},\ \varepsilon_{r,max}]\times[d_{min},d_{max}]\times[T_{min},T_{max}]\times[r_{1,min},r_{1,max}]\times[R_{mj,min},R_{mj,max}]$ gives the parameter space in which the range assumed by the circuital elements of Figure 2 must be evaluated. In Table II the nominal values and the ranges for the two considered technologies are reported.

Table II. Nominal values and ranges of the circuital parameters

***w*=22nm**				
	nominal		**range**	
R_m **[kΩ]**	6.07		[0.08, 13.85]	
***R'* [MΩ/m]**	*l*<=28.60μm	0	*l*<12.19 μm	[0, 0]
			l∈[12.19,31.93]μm	[0.0, 15.41]
	l>28.60μm	10.04	*l*>31.93 μm	[3.10, 15.41]
L' [μH/m]	230.25		[95.50, 638.60]	
C' [pF/m]	68.90		[63.30, 245.40]	
***w*=32nm**				
R_m **[kΩ]**	4.26		[0.04, 8.79]	
***R'* [MΩ/m]**	*l*<=33.97μm	0	*l*<18.03 μm	[0, 0]
			l∈[18.03,45.14]μm	[0, 5.02]
	l>33.97μm	3.50	*l*>45.14 μm	[1.12, 5.02]
L' [μH/m]	116.22		[48.91, 273.75]	
C' [pF/m]	79.19		[73.07, 283.00]	

Bounds for the propagation delay by means of VA

The driver and load components are modelled respectively by means of the input resistance and load capacitance. Their values, reported in Table III, are chosen according to ITRS. In particular, given the values at Minimum Size Gate (MSG), the adopted figure depends on the length of the interconnection according to the following analytical expressions:

$$R_t = R_{t\_MSG} \ / \ K; \qquad C_L = C_{L\_MSG} \times K;$$

where K is a scaling parameter which in the present case is chosen in the range [10, 50].

Then, the simulation of the network in Figure 1a requires the selection of the values of 6 parameters, *i.e.* 4 relative to the TL and the other 2 associated to the driver and load. By performing time domain simulations on such a circuit, the minimum and maximum value assumed by the 50% time-delay, $\tau_{50\%}$, can be evaluated.

Table III. Driver and load parameters and their ranges

w	parameter	Nominal value	Range
22 nm	C_L [fF]	4.2	[1.4, 7]
	R_t [kΩ]	0.556	[0.333, 1.667]
32 nm	C_L [fF]	7.5	[2.5,12.5]
	R_t [kΩ]	0.462	[0.277,1.385]

The use of the Vertex Analysis [15] is computationally appropriate when *n* is small and the evaluation of the function is not too heavy. In this case, in order to find the range of $\tau_{50\%}$, only 2^6 simulations in the hypercube vertexes are required.

Results and Discussion

Intermediate nanoICs *i.e.* with *l* in the range 10-200 μm are considered. The simulations, are performed on the circuit of Figure 1a by using the commercial package Simulink®. The TL is modeled by considering a fixed *dz*=5um in order to have a comparable quality of the results. In order to consider also the nominal combination of the parameters, for each length 2^6+1 simulations are performed. The bounding of the propagation delay, together with its nominal behaviour, is reported for the two technologies in Figure 3.

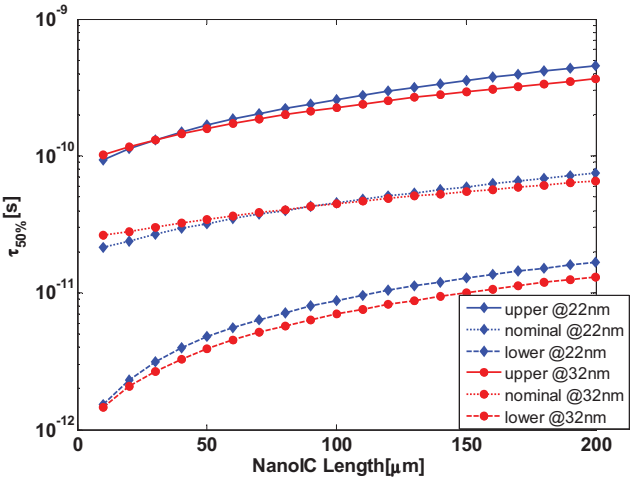

Figure 3. Bounds of $\tau_{50\%}$ for the two technologies

If only the nominal values (central curves in Figure 3) are taken into account, it can be noted that the 22nm technology exhibits better performances (lower propagation delay) than the 32nm solution for interconnect lengths up to about 90μm. But, if the worst case is considered (uppermost curves in Figure 3 corresponding to upper bounds) the 32nm solution surpasses the performances of the 22nm realization for IC lengths as low as about 30 μm. Moreover, the wider (32nm) linewidth is characterized by a greater robustness since, as shown in Figure 4, the amplitude of its variability range is lower than that corresponding to the narrower linewidth.

To assess the actual improvement introduced by the use of a MWCNT solution, it is appropriate to refer to the delay ratios of the MWCNT with respect to that of a Cu-based interconnect. The Cu-based interconnect is modeled as a lossy TL [16] with variable resistivity and therefore characterized by uncertain parameters. The comparison among the two solutions is shown in Figure 5. It can be noted that, while for the nominal values, the ratio becomes lower than unity (i.e. the MWCNTs performs better that the Cu-interconnect), for interconnect length of about 30μm, in the worst case (the uppermost curves corresponding to the upper bounds), the ratio never reach unity in the considered length range. These results clearly indicate that for a reliable design of future interconnects it is appropriate to perform an analysis not

limited to nominal conditions, but including the performance ranges.

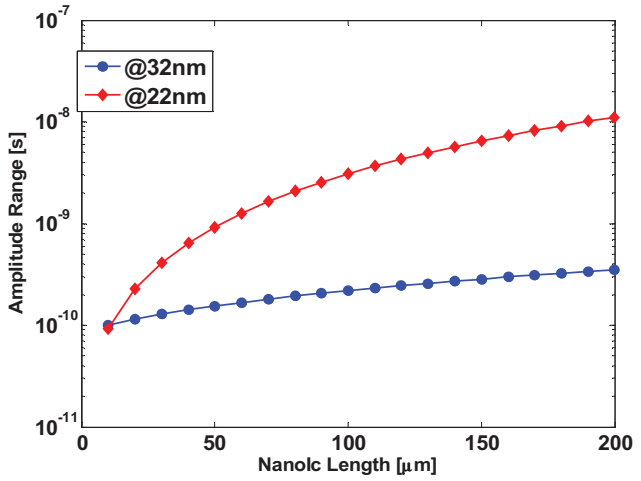

Figure 4 Amplitude of the $\tau_{50\%}$ range for the two technologies: the higher values corresponding to the 22nm technology denotes a lower robustness of this solution.

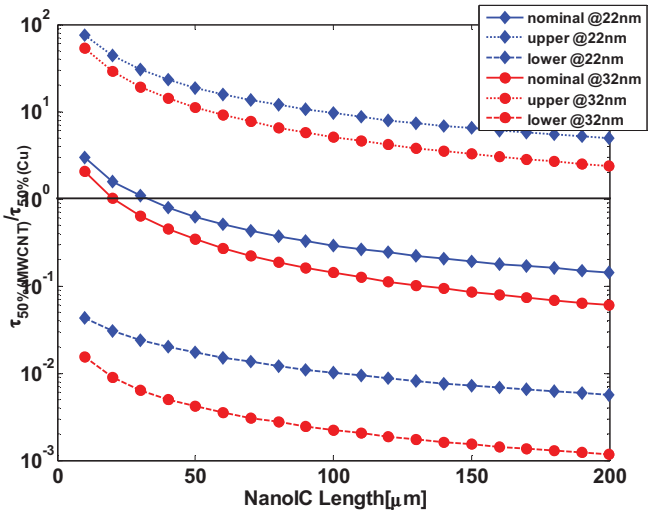

Figure 5. Signal delay ratios of MWCNT interconnect with respect to Cu interconnect at the intermediate level, for 32-and 22-nm technology nodes.

Conclusions

Reliable bounds of the time-delay due to the variations of some physical and geometrical characteristics of the a nano-interconnect based on Multi Wall CNTs, suitable for the 22 and 32nm technology, have been evaluated. Also the variability of the driver and load parameters have been taken into consideration. A commercial circuital simulator (Simulink®) is adopted to perform the time domain simulations allowing to evaluate the time-delay. The combined use of Interval Analysis and Vertex Analysis allows to identify proper sets of parameter values to be adopted in time domain simulations which allow the evaluation of the minimum and maximum value assumed by the 50% time-delay. A sensible reduction of the number simulations is achieved when compared for example, with Monte Carlo approach. Moreover the 32nm technology is characterized by a variability range narrower than that relative to the 22nm-solution. In any case a choice of a MWCNTs-based interconnect exploited only on the basis of the nominal values of the propagation delay may prove not appropriate. The uncertainties may, in fact determine inferior performances of such solution with respect to Cu-based devices.

Acknowledgments

This work has been performed under EC's funded research project CATHERINE – Carbon nAnotube Technology for High-speed nExt-geneRation nano-InterconNEcts - (GA no. 216215).

References

[1] J. Davis, J. D. Meindl, "Interconnect Technology and Design for Gigascale Integration", Springer, London, 2003.

[2] F. Kreupl, et al., "Carbon nanotubes in interconnect applications", Microelectronic Eng., 64, 2002, pp. 399-408.

[3] A. Naeemi and J. D. Meindl, "Carbon Nanotubes Interconnects", Annu. Rev. Mater. Res. 2009. 39:3.1–3.21, doi: 10.1146/annurev-matsci-082908-145247.

[4] H. Li, C. Xu, N. Srivastava, K. Banerjee, "Carbon Nanomaterials for Next-Generation Interconnects and Passives: Physics, Status, and Prospects", IEEE Trans. On Electron Devices, vol. 56, no.9, Sept. 2009, pp. 1799-1821.

[5] A. Naeemi, J.D. Meindl, "Compact physical models for multiwall carbon nanotube interconnects", IEEE Electron Device Letters, Vol. 27, 2006, pp. 338- 340.

[6] P. J.Burke, "An RF circuit model for carbon nanotubes", IEEE Trans.s on Nanotechnology, Vol. 1, Mar. 2003, pp.393-396.

[7] A. Maffucci, G. Miano, F. Villone, "A transmission line model for metallic carbon nanotube interconnects," Int. J. Circ. Theor. Appl., 36, pp. 3151, 2008.

[8] Y. Xu, A. Srivastava, "A model for carbon nanotube interconnects," International Journal of Circuit Theory and Applications, 2009, DOI: 10.1002/cta.58

[9] M. S. Sarto, A. Tamburrano, "Single-Conductor Trasmission Line Model of Multiwall Carbon Nanotubes", IEEE Trans. Nanotechnology, Vol. 9, January 2010, pp. 82–92.

[10] Y. Massoud, A. Nieuwoudt, "On the Impact of Process Variations for Carbon Nanotube Bundles for VLSI Interconnect", IEEE Trans. on Electron Devices, March 2007, pp. 446-455

[11] R.E. Moore, (1966), Interval Analysis, Prentice-Hall, Englewood Cliffs, NJ.

[12] P. Lamberti, V. Tucci, "Interval Approach to Robust Design", Int. Journal for Computation and Mathematics in Electrical and Electronic Eng., COMPEL, vol. 26, 2007, pp. 285-297.

[13] International Technology Roadmap for Semiconductors. Available Online at: http://public.itrs.net.

[14] B. De Vivo, L. Egiziano, P. Lamberti, V. Tucci: "Range Analysis on the Wave Propagation Properties of a Single Wall Carbon Nano Tube", Proc. Of the 12th IEEE Workshop on Signal Propagation in Interconnects, Avignon (France), May 12-15 2008, DOI: 10.1109/SPI.2008.4558355.

[15] R. Spence and R. Soin, *Tolerance design of electronic circuits*, Addison-Wesley, 1988.

[16] W. Steinhögl, G. Schindler, G. Steinlesberger, M. Traving, and M. Engelhardt, " Comprehensive study of the resistivity of copper wires with lateral dimensions of 100 nm and smaller", J. Appl. Phys. 97, 023706 (2005); doi:10.1063/1.1834982.