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An 8 bit current steering DAC for offset compensation purposes in sensor arrays

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Abstract. An 8 bit segmented current steering DAC is presented for the compensation of mismatch of sensors with current output arranged in a large arrays. The DAC is implemented in a 1.8 V supply voltage 180 nm standard CMOS technology. Post layout simulations reveal that the design target concerning a sampling frequency of 2.6 MHz is exceeded, worst-case settling time equals 60.6 ns. The output current range is 0–10 µA, which translates into an LSB of 40 nA. Good linearity is achieved, INL < 0.5 LSB and DNL < 0.4 LSB, respectively. Static power consumption with the outputs operated at a voltage of 0.9 V is approximately 10 µW. Dynamic power, mainly consumed by switching activity of the digital circuit parts, amounts to 100 µW at 2.6 MHz operation frequency. Total area is $38.6 \times 2933.0\,\mu m^2$.

1 Introduction

Sensor arrays implemented on CMOS chips with thousands up to millions of sensor sites repeated in a regular manner have found many applications in today's world: Whereas the most prominent example may be the imaging chip in CMOS cameras from consumer to professional applications (http://isscc.org/doc/2011/2011_Trends.pdf), other applications are found in space industry (Lin et al., 2009), security (Perenzoni et al., 2011), biomedical research (Eversmann et al., 2003; Frey et al., 2010), and further fields. There, the output signal of the sensor sites can be given in the voltage domain – which usually applies to the pixels of CMOS imaging chips – or in the current domain. Frequently, the output date received from the respective sensor sites are prone to biasing offsets and random parameter variations.

In this work, we consider sensor sites with current output, i.e. the sensors can be modeled as current sources, whose output currents consist of a bias value (I_{BIAS}), which is prone to variations (ΔI_{BIAS}), and a signal dependent portion (I_{SIGNAL}). Under worst-case conditions, the following relation holds:

$$I_{\mathrm{BIAS}} \gg \Delta I_{\mathrm{BIAS}} \gg I_{\mathrm{SIGNAL}} \tag{1}$$

In such cases, it can be advantageous to implement compensation mechanisms for the deviation ΔI_{BIAS}. In this work, a digital-to-analog converter (DAC) is presented, operated at the sensor array border and used for the compensation of the bias current deviations. The required data patterns used for compensation are derived in an initial calibration phase.

For our purposes – aiming for an application in the biomedical domain, the following design specifications have been identified: full-scale current range = 10 µA, resolution = 8 bit, operating frequency should at least amount to 2.6 MHz and, moreover, the layout must not measure more than 40 µm in one direction.

Many different solutions implementing current steering DACs are available in the literature, e.g. Bastos et al. (1996), Bastos et al. (1998), Miki et al. (1986), Chen and Gielen (2007), Lei Luo (2008) and many more. However, these solutions are designed for full scale output current ranges of order 10 mA and cannot simply be adjusted to our design targets with 10 µA full scale range. Moreover, all state of the art DACs achieve their performances thank to the application of symmetrical layouts, which cannot be adapted to our aspect ratio of order 100.

The paper is organized as follows: in Sect. 2 the fundamental concepts of current steering DACs are introduced. Section 3 presents mismatch considerations whose understanding is necessary for the design. Section 4 briefly comments on the transistor-level implementation, and Sect. 5 focuses on layout issues. In Sect. 6, post-layout simulation results are presented, and finally, in Sect. 7, the paper is concluded.

2 Current steering DAC topologies

Current steering digital-to-analog converters are based on the principle of providing a digitally controlled sum of currents. Depending on the manner how respective current sources are tailored and summed, Binary Weighted (BW) and Unary Weighted (UW) topologies are distinguished (Baker et al., 1998). In the latter case, all current sources provide a unity current value (associated with the Least Significant Bit, LSB). The number of current sources equals the number of quantization levels, and their connection to the DAC's output is controlled by a thermometer code signal derived from the input word. The Binary Weighted architecture uses only N current sources with N being the resolution in bits. Consequently, they are binary weighted and directly controlled by the N input signals.

Both architectures have advantages and drawbacks: for instance, the simplicity of the BW approach allows to save area and power but leads to worse accuracy, in the worst-case even to non-monotonic behavior. On the other hand, for high resolutions UW converters require huge binary-to-thermometer decoders, which increase latency, limit the operating frequency, and lead to very expensive solutions in terms of area. However, monotonic behavior is always guaranteed and a linear dependence between output glitch and transition value is obtained (Lin and Bult, 1998).

A mixture of UW and BW topologies leads to the so-called segmented current steering topology, where the advantages of both approaches are merged by concurrently converting the more significant bits through a UW DAC and the less significant bits by means of a BW converter (Maloberti, 2008).

3 Mismatch considerations

As shown in Cong and Geiger (2002), Differential Non Linearity (DNL) and Integral Non Linearity (INL) errors of unary weighted current steering DACs can be analytically related to the matching properties of the unity current sources. Moreover, since binary scaled current sources consist of ensembles of unity current sources, it can be shown that the worst INL error occurs at midcode. This applies to UW, BW, and segmented current steering topologies, and it amounts to:

$$E[\mathrm{INL}^2_{\mathrm{WORST}}] \simeq \frac{\sigma^2_{I,\mathrm{Rel}}}{4}\left(2^N - 1 - \frac{1}{2^N-1}\right) \quad (2)$$

There, $E[\mathrm{INL}^2_{\mathrm{WORST}}]$ is the variance of the INL error at midcode, N is the resolution in bits, i.e. (2^N-1) is the total number of unity current sources. The parameter $\sigma_{I,\mathrm{Rel}}$ is the standard deviation of the relative error of the unity current sources' output current. This mismatch is mainly dependent on the dimensions of the transistor responsible for the current generation and on its operating point (Pelgrom et al., 1989; Sansen, 2008; Bastos et al., 1996).

On the basis of similar considerations it can be shown that, if the DAC is segmented or binary weighted, the worst-case DNL code is given by the code which shares the smallest number of current sources with its previous one: in a BW-DAC that is the midcode, while in a segmented architecture it is every code, that makes the BW part convert a zero. If m is the number of bits with binary weighted conversion, we achieve:

$$E[\mathrm{DNL}^2_{\mathrm{WORST}}] = \left(2^{m+1} - 1 - \frac{1}{2^N-1}\right)\sigma^2_{I,\mathrm{Rel}} \quad (3)$$

From Eqs. (2) and (3) the optimum percentage of segmentation and the required precision of the unity current source can be evaluated, once maximum INL and DNL are defined. For this work, aiming for an 8 bit input signal and a monotonic behavior with high probability (99.9 %), a maximum $\sigma_{I,\mathrm{Rel}}$ of 1.904 % and an m-value of ≤ 5 are calculated, respectively. Consequently, in the next paragraphs the related blocks of a current steering DAC with a segmentation of 50 % and unity current sources with a target current of 40 nA and an absolute standard deviation of less than 760 pA are presented.

4 Transistor level design

As shown in Fig. 1, the binary weighted part of the converter consists of four scaled current sources which generate 1×LSB, 2×LSB, 4×LSB, and 8×LSB currents, respectively. They are controlled by the four inputs for the less significant bits. The 4 more significant bits are fed into a binary-to-thermometer decoder. Its fifteen outputs control the 16×LSB current sources which are used in the DAC's unary weighted part.

4.1 Binary-to-thermometer decoder

Figure 2 shows the small decoder that translates the four input signals into the 15 thermometer outputs. The clear hierarchical structure with its exponential dependence on the number of bits to be converted is the issue to be faced when designing high-precision high-bit unary weighted DACs. Some sophisticated solutions have been developed to bypass this challenge taking advantage of the unary weighted topology (Miki et al., 1986; Bastos et al., 1998): There, use of a row-column selection architecture reduces the area demand on the cost of additional digital gates in every current source unit. Another solution has been reported by Jeong et al. (2010), where sub-arrays are used. However, since in this work we are aiming to interface the DAC with a small-pitch sensor array, harvesting of any opportunity to save area is mandatory. Thus, we have chosen not to implement any sophisticated strategy but to accept a slight linearity degradation due to the segmented topology.

4.2 LSB current cell

If the LSB current source is operated in strong inversion the following equation applies (Pelgrom et al., 1989):

$$\sigma^2_{I,\mathrm{Rel}} = \frac{A^2_\beta}{WL} + \frac{4A^2_{V_{\mathrm{TH}}}}{WL(V_{\mathrm{GS}} - V_{\mathrm{TH}})^2} \tag{4}$$

On this basis the following considerations can be drawn:

1. Given the mismatch related parameters A_β and $A_{V_{\mathrm{TH}}}$ with A_β being the transistor constant related matching constant in [% µm] and $A_{V_{\mathrm{TH}}}$ being the threshold voltage related matching constant in [mV µm], the required standard deviation $\sigma_{I,\mathrm{Rel}}$ can be achieved by choosing an adequate channel area WL and/or by choosing an appropriate effective gate voltage $V_{G,\mathrm{EFF}} = (V_{\mathrm{GS}} - V_{\mathrm{TH}})$.

2. Consequently, for a given standard deviation, the application of a higher effective gate voltage always translates into the option to decrease the active transistor area.

3. However, given a defined current to be generated by the MOSFET, the only way to increase $V_{G,\mathrm{EFF}}$ is to make the ratio W/L smaller.

A comparison with the mismatch behavior for devices operated in the subthreshold region yields:

$$\sigma^2_{I,\mathrm{Rel}} = \left(\frac{q}{nkT}\right)^2 \frac{A^2_{V_{\mathrm{TH}}}}{WL} \tag{5}$$

There, q is the elementary electronic charge, k the Boltzmann constant, T the absolute temperature, and n the so-called non-ideality factor. For a chosen standard deviation and a fixed current, transistors operated in strong inversion at sufficiently high effective gate voltage are smaller than transistors operated in subthreshold region.

Given the boundary conditions in this work, this, however, would translate into an extremely high L/W ratio as the required current is small. This is not convenient from the layout related point of view. As a consequence, the LSB current cell in this work is based on an NMOS transistor operated in subthreshold region, with more reasonable values for W and L at an active transistor area of roughly 60 µm^2.

The entire schematic of the LSB current source is shown in Fig. 3. Two output nodes are used to ensure an optimum transient response by never switching off the current sources (Baker et al., 1998; Sansen, 2008). A cascode transistor is added in order to minimize the parasitic capacitance at the source of the switch transistors, and thus to optimize the settling-time of the circuit. For the same reason the switches have minimum dimensions and dummy switches are avoided as the use of dummies would imply doubling the amount of switch transistors and related parasitics.

As shown in Fig. 4, the effect of using a cascode transistor on current source mismatch is negligible. Associated to

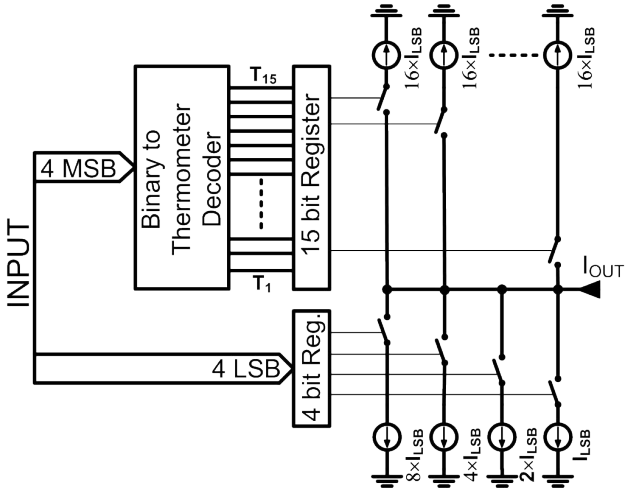

Fig. 1. Block diagram.

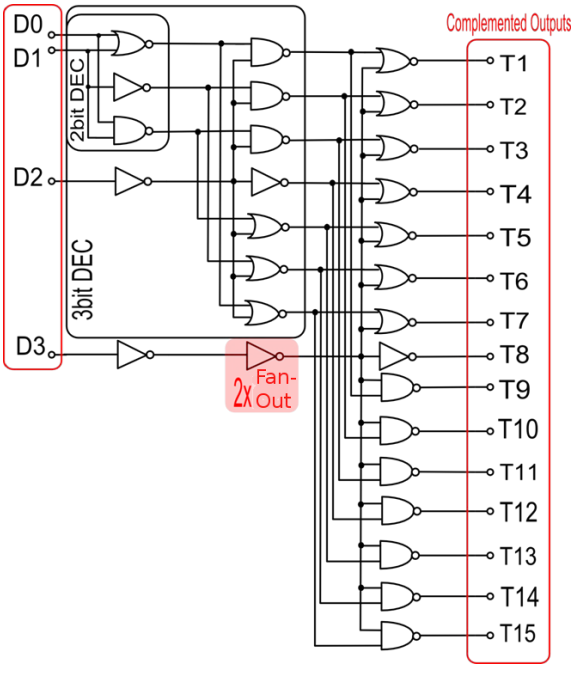

Fig. 2. Binary-to-thermometer decoder.

the switchable current source is also a small driver (Fig. 3). By means of that circuit the control signals SW and SWn are generated: their voltage swing is limited to the window from 0.7 V to 1.2 V in order to reduce the clock feedthrough (CFT) to the output while still maintaining proper switching functionality. Moreover, a slower transient drive capability caused by the minimum dimensions of the output stage of the driver is advantageous in the sense that CFT is further reduced. Thus, the voltage error induced on node Vs of the current source is minimized, which is also advantageous for the overall settling time.

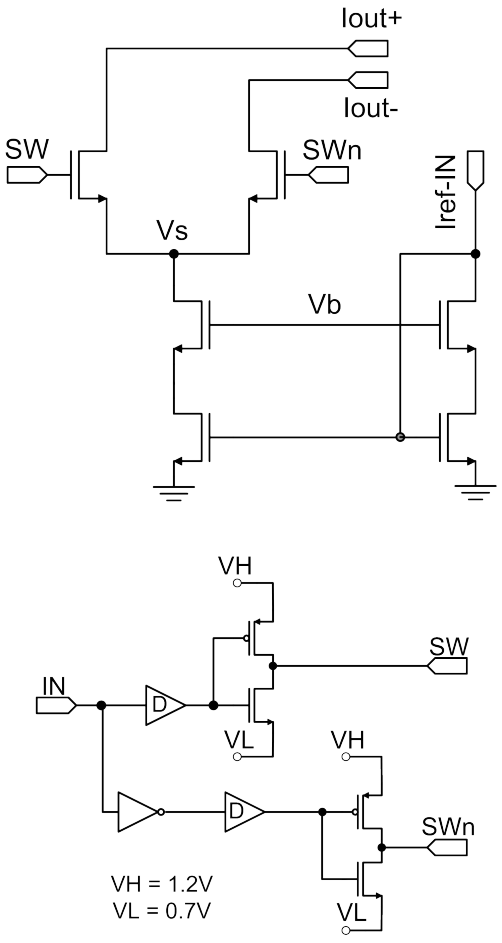

Fig. 3. LSB current source with related driver. Bias transistors connected to input "Iref-IN" are shared by the entire array.

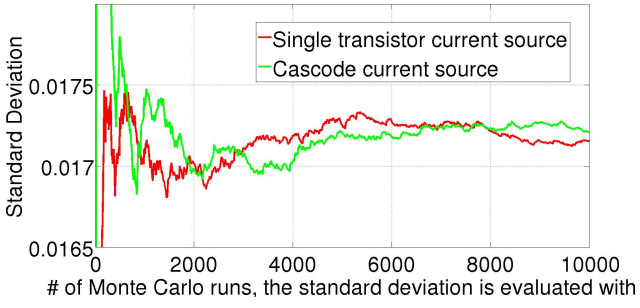

Fig. 4. Relative output current standard deviation of a single transistor based and of a cascode current source.

4.3 Scaled current cells

The current sources required for the unary weighted part of the DAC and for the other bits of the binary weighted part can be directly derived from the circuit presented in Sect. 4.2. The generic weighted cells are implemented as replica cells of the LSB current cell (i.e. LSB current source with related driver) since the small driver in Fig. 3 is optimized only for one LSB current source. Although the area consumption consequently slightly increases, the layout regularity due to the replication of the entire cell has a positive impact on the linearity and suppresses the sensitivity to on-chip parameter gradients.

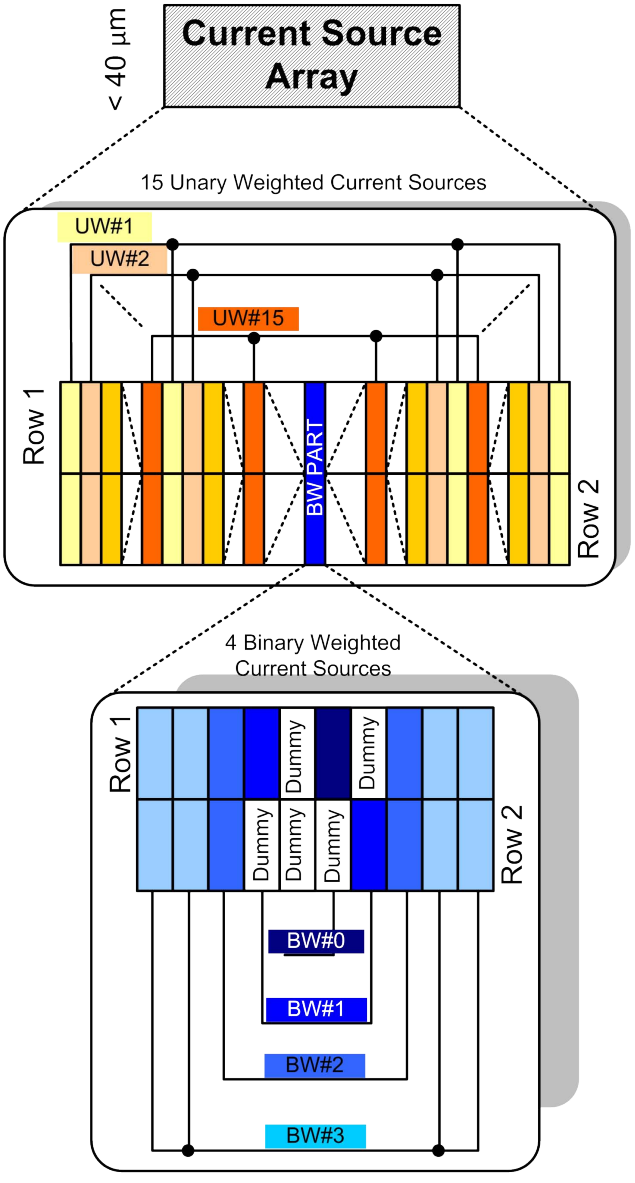

Fig. 5. Schematic plot of the realized layout.

5 Layout

As e.g. emphasized by Bastos et al. (1998), the performance of digital-to-analog converters is strictly related to their layout implementation. As the array of current sources can demand a huge area depending on the number of bits, precision,

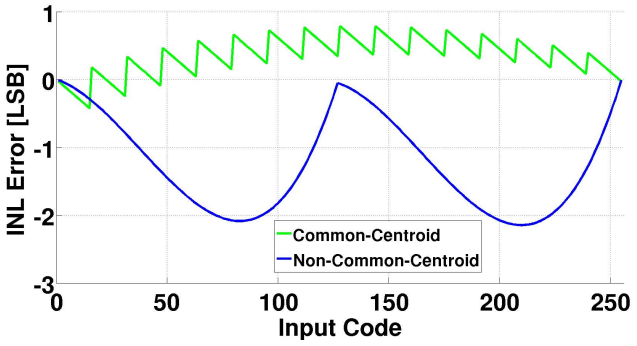

Fig. 6. Example for the impact of a systematic error applied to the array of current sources for a Common-Centroid and a Non-Common-Centroid layout. Details concerning the assumed error function see Eq. (6).

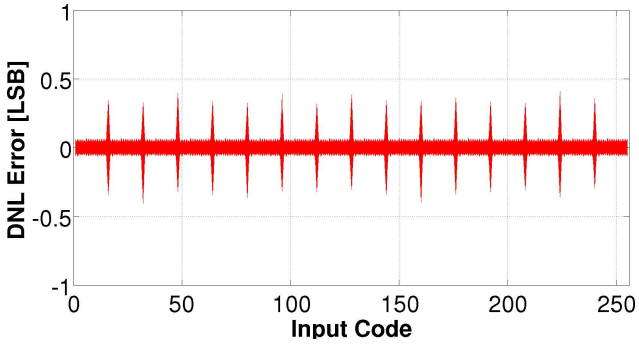

Fig. 7. DNL error vs. input code for 5000 Monte-Carlo simulations.

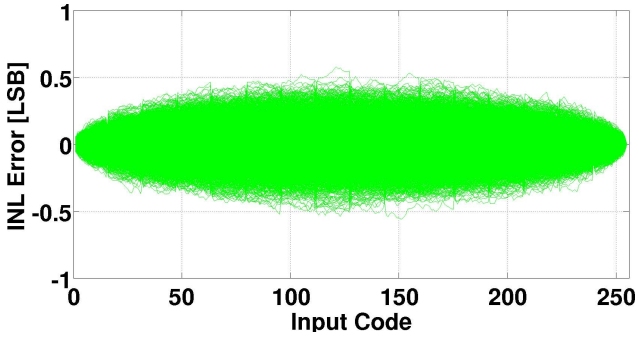

Fig. 8. INL error vs. input code for 5000 Monte-Carlo simulations.

and full-scale current, CMOS process parameter gradients on the chip cannot be neglected. A systematic error of the current sources' parameters would indeed determine a distortion of the static characteristics and might have a severe negative impact on DNL and INL. For that reason a Common Centroid layout is used. Some further techniques may additionally give rise to even better results (Van der Plas et al., 1999; Nakamura et al., 1991), however, as they also require to invest a huge amount of extra area, layout constraints do not allow for their implementation in this work.

In Fig. 5, details are depicted of the Common Centroid layout used here. The current sources of the binary weighted part are placed in the center of the array in a symmetrical manner supported by the use of dummy LSB cells. The current cells of the unary weighted part form the rest of the array. The 15 UW cells, each one consisting of 16 LSB cells connected together, are not arranged side by side in space but symmetrically distributed with respect to the binary weighted part within the entire array. The effects of such a local distribution are exemplarily shown in Fig. 6, where for instance a parabolic error as a function of the current source location is considered following the relation

$$\Delta I(x,y) = I_{\mathrm{LSB}}\left[K_X(x-x_0)^2 + K_Y(y-y_0)^2\right] \qquad (6)$$

with $K_X = 5\times10^{-8}\ \mu\mathrm{m}^{-2}$, $K_Y = 1\times10^{-7}\ \mu\mathrm{m}^{-2}$, $x_0 = -500\ \mu\mathrm{m}$, $y_0 = 100\ \mu\mathrm{m}$, $x \in [-1311;1311]\,\mu\mathrm{m}$, $y \in [-2.3;2.3]\,\mu\mathrm{m}$.

6 Results

Figures 7 and 8 provide post-layout simulation results of DNL and INL, respectively. For these simulations, a low-ohmic 0.9 V (=VDD/2) voltage source is connected as a load to the DAC's output. The shown results are based on 5000 Monte-Carlo runs: the data are generated by means of a Matlab script, which computes the transfer characteristics on the basis of DC simulations of 255 equal independent LSB cells. With the DNL being always smaller than half of an LSB, the Integral Non Linearity error is ≤ 0.5 LSB with a probability of 99.82 %. The slight deviation from the targeted 99.9 % may originate from the limitations of the model used in Eq. (5), from the impact of the cascode transistor, but also from the finite number of Monte-Carlo runs. Anyway, the result is considered to be acceptable.

Using transient simulations and the same output configuration as above, the overall correct functionality, settling time, glitch values, and the dynamic power consumption are considered. The results are summarized in Table 1. Since the settling time at 5 % of LSB level in a full scale transition is much smaller than required for the specified 2.6 MHz operating frequency, a maximum operating frequency calculated as reciprocal of the 3-sigma worst-case Monte-Carlo settling time appears to be 10.2 MHz. At 1.8 V supply voltage a dynamic power of 100 µW is dissipated at the operating frequency of 2.6 MHz, and a DC power of 10 µW is absorbed mainly by the low-ohmic load.

7 Conclusions

An 8 bit, 2.6 MHz, 10 µA full scale CMOS current steering DAC with high linearity, low noise, and small area has been presented. Using a standard 180 nm CMOS technology,

Table 1. Summary of simulation results.

Parameter	Value
LSB Current	40 nA
DNL	< 0.5 LSB
INL	< 0.5 LSB
Settling Time (nominal, 5 %-LSB)	60.6 ns
Settling Time (Monte-Carlo, 5 %-LSB)	$\mu = 68.2$ ns
	$\sigma = 9.98$ ns
Output Noise [20 Hz; 2.6 MHz]	2.75 nA
Average Glitch Current (1 LSB transition)	14 pA
DC Power Consumption	10 µW
Dynamic Power Consumption (2.6 MHz Full Scale Transition)	100 µW
Maximum Operating Frequency	10.2 MHz

it dissipates 100 µW from a single power supply voltage of 1.8 V at 2.6 MHz operating frequency. Monte-Carlo simulations reveal DNL and INL of $\leq$0.4 LSBs and $\leq$0.5 LSB, respectively. Maximum operating frequency is 10.2 MHz. Following the target application, a layout with total dimensions $38.6 \times 2933\ (\mu m)^2 = 0.113\ mm^2$ is provided. Common Centroid layout techniques are applied to the crucial blocks in order to minimize the impact of possible on-chip gradients.

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