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Impact of the substrate and buffer design on the performance of GaN on Si power HEMTs

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ABSTRACT

This paper presents an extensive analysis of the impact of substrate and buffer properties on the performance and breakdown voltage of E-mode power HEMTs. We investigated the impact of buffer thickness, substrate resistivity and substrate miscut angle, by characterizing several wafers by means of DC and pulsed measurement.

The results demonstrate that: (i) the resistivity of the silicon substrate strongly impacts on the breakdown voltage and vertical leakage current. In fact, highly resistive substrates may partly deplete under high vertical bias, thus limiting the total potential drop on the epitaxial layers. As a consequence, the vertical I–V plots show a "plateau", that limits the vertical leakage. (ii) the depletion of the substrate may worsen the dynamic performance of the devices, due to an enhancement of buffer trapping. (iii) Larger buffer thickness results in an increased robustness of the vertical stack, due to the thicker insulating region. (iv) the miscut angle (0°, 0.5°, and 1°) can significantly impact on both threshold voltage and the 2DEG density; devices with miscut substrate have higher current density. On the other hand, the dynamic on-resistance variation is comparable in the three cases.

1. Introduction

GaN based High Electron Mobility Transistors (HEMTs) are ideal devices for power switching applications in the voltage range of 200 V–1200 V [1–3]. The high carrier mobility of the 2-dimensional electron gas (up to 2000 $cm^2 V^{-1} s^{-1}$ [4]) results in a low on-resistance, while the high breakdown field of GaN (> 3 MV/cm) guarantees an excellent robustness against the high electric field reached in the OFF-state conditions. Furthermore, the compatibility with silicon process considerably reduces the production costs, and is made possible by the availability of large size (up to 8″) silicon substrates.

One of the main problems of the GaN-on-Si technology is the high lattice mismatch between silicon and the III-Nitride semiconductors. The resulting defects may limit the vertical stack robustness [5, 6], favor buffer trapping [7] and degrade the dynamic performance of the devices.

In this paper, we investigate the effect of three approaches to increase device reliability and performance: (i) the use of a thicker superlattice (SL), (ii) the use of highly-resistive substrates and (iii) the use of an off-axis substrate (Table 1).

2. Experimental details

The studied devices are enhancement-mode HEMTs grown on silicon substrates. The normally-off operation was achieved thanks to the use of a p-GaN gate. Since this work is focused on the impact of different substrate and buffer design, the most important aspect of the studied devices is the vertical stack in Fig. 1(a), composed by different layers between the drain contact and the substrate. All the epi-layers are grown on 8 inches silicon substrates; three different silicon substrates resistivities are available ($\rho = 0.01\ \Omega$ cm, $\rho = 1\ \Omega$ cm, $\rho = 6\ \Omega$ cm). An AlN nucleation layer is grown directly on the Si substrate in order to avoid the eutectic reaction between Ga and Si and to provide a proper platform for the growth of subsequent layers. The buffer is composed of a superlattice and a carbon doped back-barrier (GaN) layer; these two layers prevent the punch-through effect and limit the drain-to-substrate leakage current, increasing the vertical robustness. Two types of buffers are available: a 25 × 1565 nm thick superlattice and a 50 × 3190 nm thick one. Over the C-doped GaN layer there is an unintentionally doped GaN region in which the 2DEG is formed at the interface with an AlGaN barrier layer. To explore the impact of miscut, devices were also grown with three different miscut angles: on axis wafer with 0° miscut angle, wafers miscut towards in-

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Table 1
Variants of wafers used for this paper.

Superlattice thickness	Substrate resistivity	Miscut angle
25×	0.01 Ω cm	0°
50×	1 Ω cm	0.5°
	6 Ω cm	1°

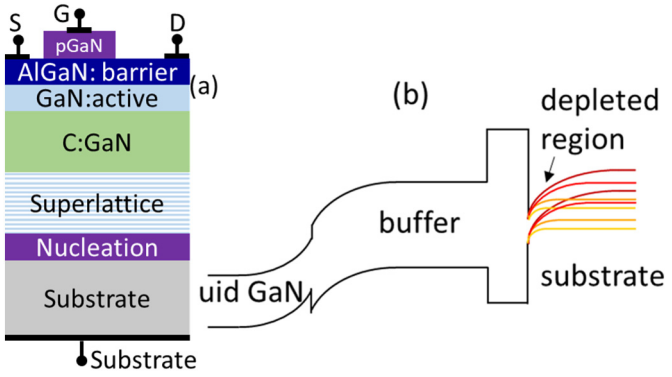

Fig. 1. (a) Schematic representation of the tested devices. (b) Band diagram of the vertical stack during the plateau region.

plane [11 − 2] direction with miscut angle of 0.5° and 1°, respectively. The results presented within this work were obtained in a devices lying parallel to the miscut direction: nevertheless the devices orientation with respect to the miscut do not affect the sheet resistance (i.e. $R_{sh[11-20]} = R_{sh[1-100]}$).

The results presented within this work are obtained by means of DC and pulsed measurements. The DC characterizations (below 200 V) were carried out with a parameter analyzer Keysight 5260A, while the high voltage measurements were performed by a Keysight B1505 (up to 3000 V). Pulsed measurements were carried out with a custom setup described in [8] with pulse width of 3 µs.

3. Results and discussions

3.1. Substrate resistivity and superlattice thickness

As specified above, different silicon substrates were used: a conductive substrate with ρ = 0.01 Ω cm, and two more resistive substrates with ρ = 1 Ω cm and ρ = 6 Ω cm. Both 25× SL and 50× SL buffers were grown on the three different silicon substrates, so that a complete comparison among 25× SL and 50× SL can be presented.

A vertical leakage characterization has been performed on the six wafers under test (as can be seen in Fig. 2) by sweeping the drain voltage from 0 V up to the failure, keeping the source and the gate floating and the substrate grounded. There is a clear dependence of the vertical leakage behavior on the silicon substrate resistivity. In all the measured IV characteristic, except for the two ρ = 0.01 Ω cm, three regions can be identified (as marked in Fig. 2).

Within region 1, no dependence of the leakage current on the substrate resistivity can be noticed; this means that the applied voltage drops on the epi-layers, which are identical in the three tested devices. It is worth noticing that the slope of region 1 in 50× SL is significantly lower than 25× SL, therefore the 50× SL has a more resistive behavior than the 25× SL buffer, that results in a higher robustness of the devices with thicker buffer (higher breakdown voltage of the drain-to-substrate stack).

After region 1, in the devices grown on highly resistive substrates (independently on the buffer thickness) the IV characteristic shows an abrupt change of slope, and the current stops increasing (region 2 in Fig. 2); this behavior can be ascribed to the limited amount of carriers

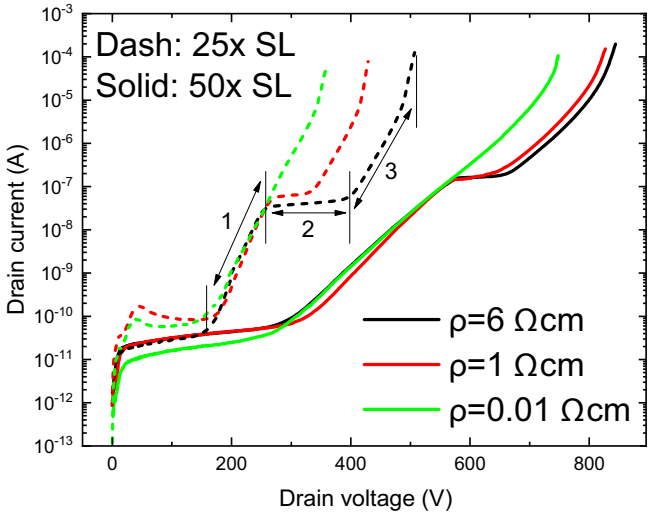

Fig. 2. Drain-to-substrate IV characteristic of 25× SL buffer (dashed) and 50× SL buffer (solid), with different substrate resistivity. Three different regions are marked for the black-dash curve (25× SL, 6 Ω cm).

can be supplied by the depleted region of the silicon substrate (i.e. thermally generated). This bring to a substrate depletion [9, 10], that occurs only with the highly resistive substrates. The depletion of the substrate limits the voltage drop on the epitaxial layers, thus resulting in a constant vertical leakage. Within this region the voltage drop on the GaN buffer remains constant, and so does the vertical current.

As the substrate depletes, the electric field on the silicon increases, and different carrier generation processes can occur, such as SRH generation and/or impact ionization. For sufficiently high voltages, such processes favor again the generation of carriers within the substrate, and this allows the vertical leakage current to recover the initial slope (same as in region 1). Current can then increase up to the failure of the stack (region 3 in Fig. 2).

So far, we showed that the vertical leakage current is strongly affected by the silicon substrate resistivity; in the following, the impact of the substrate resistivity on the dynamic behavior of the devices will be discussed. For this purpose, devices with different substrate resistivity and 25× SL buffer layer have been submitted to an OFF-state double pulse characterization. Since the breakdown voltage of the vertical stack is higher in highly resistive device, the maximum off-state voltage applied during the measurement is higher in the devices with higher substrate resistivity (respectively 400 V and 300 V).

The results of this measurement are presented in Fig. 3, which shows that the lowly resistive substrate has a very stable I_DV_D characteristic, and the on resistance is almost constant despite the high off-state bias applied. On the other hand, the devices with highly resistive substrate showed a collapse of the drain current and an increase of the on-resistance (Fig. 4), which almost doubles its value. It is worth noticing that, in these devices with a highly resistive substrates (ρ = 6 Ω cm), the pulsed I_DV_D characteristics degradation occurs for off-state voltages higher than 200 V, while they are stable for baselines lower than 200 V. The 25× superlattice buffer used on these substrates, has been designed for sub-200 V applications; please notice that the Vth/Ron variation occurs outside of the operational regime and is thus not critical for device operation. Comparing this behavior with the vertical leakage curve of highly resistive substrates, it can be observed that the pulsed I_DV_D drift occurs exactly within the plateau region (region 2 in Fig. 2), meaning that there is a buffer trapping process activated by the silicon substrate depletion that occurs only in highly resistive substrates, in the plateau voltage range; the capacitance coupling of the depleted region within the substrate results in a positive backgating bias that bring to the observed Vth/Ron shift [10]. The

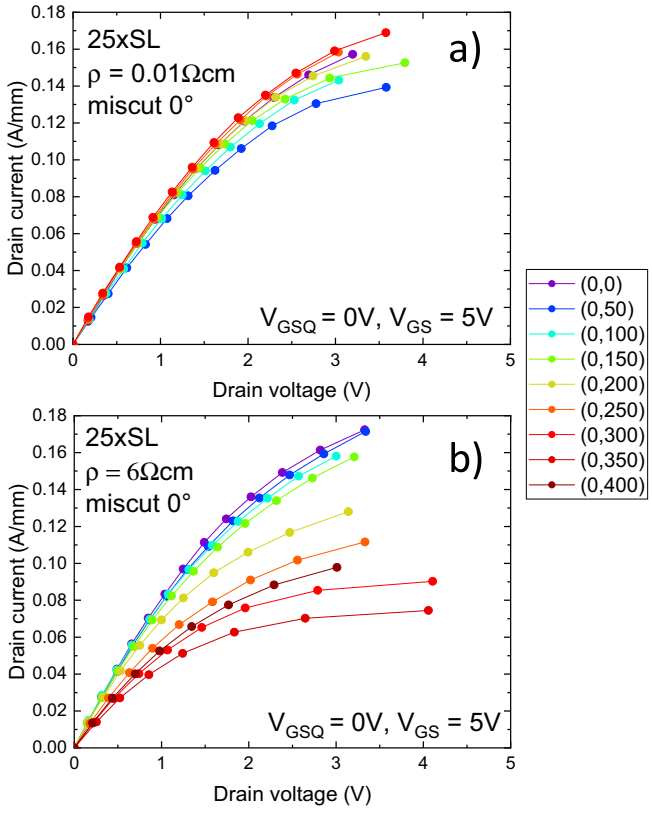

Fig. 3. Pulsed IDVD characterization (tpulse = 3 µs) of devices with 25× L grown substrate with (a) low resistivity and (b) high resistivity. The trapping effect is stronger in highly resistive substrate.

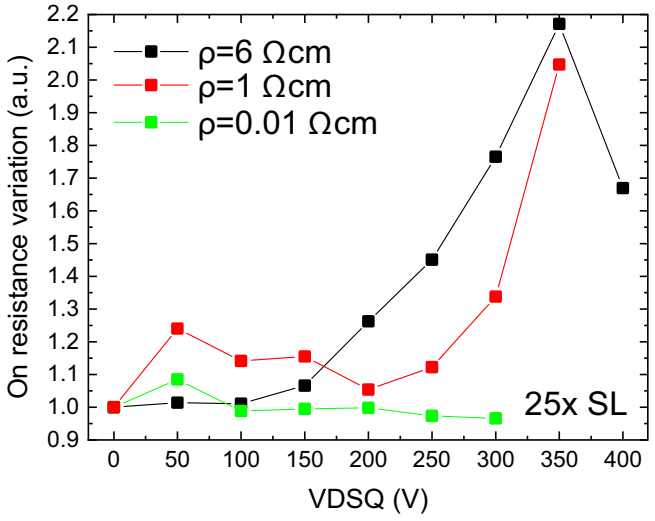

Fig. 4. on-resistance variation during an OFF-state pulsed characterization.

results described within this section therefore indicate that the use of a resistive silicon substrate can bring benefits in terms of breakdown voltage and leakage reduction. However, the depletion of the substrate can lead to additional trapping effects, which are not observed with low-resistivity substrates. A trade-off between breakdown voltage and trapping effects must therefore been considered when defining substrate resistivity.

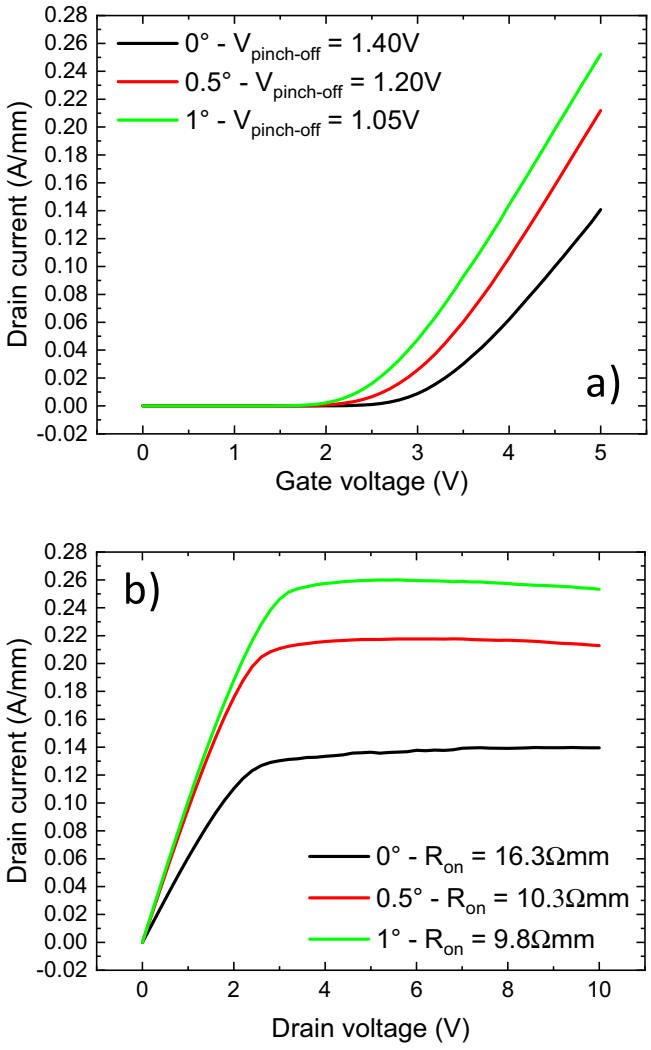

Fig. 5. (a) IDVG and (b) IDVD characteristics (DC) of three devices grown with miscut angle 0°, 0.5° and 1°. Miscut angle results in both lower on-resistance and lower pinch-off voltage (@1 mA/mm) as consequence of a higher carrier density in the 2DEG.

Table 2
sheet resistance, 2DEG-charge density and mobility of epi grown on on-axis and 1° off-axis substrate.

	R_{sh} [Ω/sq]	n_s [10^{12} cm^{-2}]	µ [$cm^2/(V·s)$]
On-axis	517	8.8	1360
1° off-axis	463	9.5	1400

3.2. Miscut angle

In this section we discuss the benefits given by growing the devices on a silicon substrate with a miscut angle. Furthermore, a pulsed characterization has been carried out in order to evaluate possible drawback of this technique.

A first DC characterization has been carried out in three devices having miscut angle of 0°, 0.5° and 1°. As can be noticed in Fig. 5, the miscut angle affects both the I_DV_G (Fig. 5(a)) and the I_DV_D (Fig. 5(b)) characteristics. Both the threshold voltage and the on-resistance decrease with the miscut angle, while the drain current in the saturation region increases. Such improvement can be ascribed to the enhanced electron density in the 2DEG as a consequence of a stronger

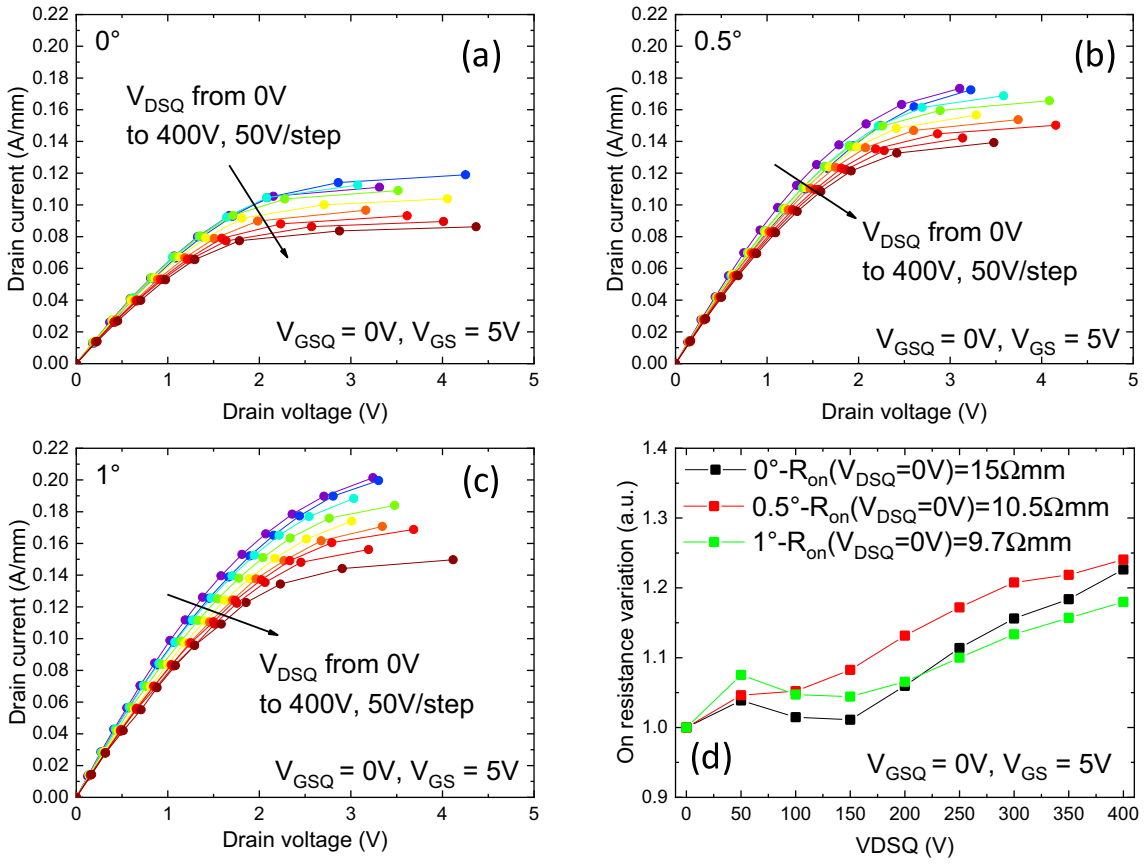

Fig. 6. Pulsed IDVD characterization on three devices with 50× SL buffer, grown on substrate with miscut angle of (a) 0°, (b) 0.5° and (c) 1°. A weak variation of the on-resistance can be observed since the maximum baseline voltage (400 V) is lower than the onset of the plateau region (550 V in 50× SL buffer devices). The variation of the on-resistance (d) is comparable in the three wafers (~20%).

piezoelectric charge or to a better material quality of the epi-layers of the devices grown with a non-zero miscut angle. Further investigations were carried out by means of Hall measurement on both on-axis and 1° off-axis wafers. The results are shown in Table 2.

An important aspect that has been investigated is the impact of the miscut angle on the dynamic performance of the devices, in order to understand if there is an impact on the buffer trapping process. The OFF-state pulsed I_DV_D characteristic of the three tested devices is shown in Fig. 6. Once again it can be observed that the miscut angle guarantees better performances in terms of both drain current level and on-resistance. Nevertheless, only a small variation of the on-resistance with the increasing OFF-state voltages is measured; all the three devices show the same on-resistance variation, which is lower than 20%. This reveals that the miscut angle is not causing a higher buffer traps density, and can be promising for increasing carrier density.

4. Conclusions

In this work a complete investigation on the impact of different techniques to improve power devices performance has been presented. The results can be summarized as follow: (i) thicker buffer layer results in an improved robustness of the vertical stack; (ii) highly resistive silicon substrates increase the breakdown voltage of the devices, but result in a strong buffer trapping process as the silicon starts depleting; (iii) a miscut angle significantly improves the device performance in terms of on-resistance and drain saturation current, without any drawback on the dynamic behavior of the devices.

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