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Editors' Choice—Effects of Parasitic Elements of Interconnection Lines in CNT Embedded Integrated Circuits

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In this paper we present a study of the effects of parasitic elements of interconnection lines in integrated circuits (I.C.) where Carbon NanoTubes (CNTs) are embedded. In particular the Drain/Source pads dimensions of CNT are analyzed, as well as the interconnection lines between a CNT and an appropriate load are sized.Furthermore the time domain and frequency simulations of some circuits are presented in order to see how the parasitic elements could limit the high-speed performances of CNTs.
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Carbon NanoTubes (CNTs) are a promising material that can be used to realize the channel of Carbon NanoTube Field Effect Transistors (CNTFETs), a new kind of molecular device able to work better at nanometer scale.[1–13]

In this paper we present a study of the effects of parasitic elements (capacitances, inductances and resistances) of interconnection lines in integrated circuits (I.C.) where Carbon NanoTubes (CNTs) are embedded. In particular the Drain/Source pads dimensions of CNT are analyzed, as well as the interconnection lines between a CNT and an appropriate load are sized.

Moreover, through a simulation study of some A/D circuits based on CNTFETs, both in the time and frequency domain, we show how the parasitic elements limit the high-speed performances of CNTs.

The presentation of the paper is organized as follows. At first we describe briefly the CNTs structure. Then we present a brief review of the CNTFET model used in the designs shown in this paper, and already proposed by us in.[14,15]

The simulation results are shown and discussed, together with conclusions and future developments.

A Brief Review of CNTs

A Carbon Nanotube (CNT) is a sheet of hexagonal arranged carbon atoms rolled up in a tube of a few nanometers in diameter, which can be many microns long. Graphene is a single sheet of carbon atoms arranged in the well known honeycomb structure.[1]

A CNT can be single-wall (SWCNT) or multi-wall (MWCNT). In particular a SWCNT is composed by a single cylinder, having a diameter between 0.7 nm and 2 nm. Therefore the high length/diameter ratio allows to consider it as a one-dimensional structure.

As it is known,[1] the electronic properties of CNTs depend strongly on the chirality of the nanotube, i.e. on the indices n and m, with $0 \leqslant m \leqslant n$ for reasons of symmetry related to the honeycomb lattice: m values outside this range provide the same results. In fact, depending on their chiral vector, CNTs have either semi-conducting or metallic behaviour.

In particular, if $n = m$ or $n–m = 3i$, where i is an integer, the nanotube is metallic; in other cases it shows semi-conducting properties.[16]

CNTs offer several advantages compared to Cu/low-κ interconnects because of their one dimensional nature, the peculiar band-structure of graphene, and the strong covalent bonds among carbon atoms. In particular:

1. higher conductivity dueue to their one-dimensional nature, the phase space for electron scattering in CNTs is limited, and electron mean free path is in the micron range for high quality nanotubes, in contrast to 40 nm in bulk copper. The conductivity of densely-packed CNTs is higher than scaled Cu interconnects for large lengths. Conductivity of short CNT bundles, however, is limited by their quantum resistance. Metallic SWCNTs have two conduction channels, and their quantum resistance is 6.5 kΩ;
2. resistance to electromigration: the strong sp^2 carbon bonds in graphene lead to an extraordinary mechanical strength and a very large current conduction capacity for CNTs, 10^9 A cm^{-2} in contrast to 10^6 A cm^{-2} in Cu. However, contacts may limit the maximum current density in CNT interconnects;
3. thermal conductivity: the longitudinal thermal conductivity of an isolated CNT is expected to be very high, on the order of 6000 W mK^{-1}, as suggested by theoretical models and extrapolations on measured data from porous bundles. The thermal conduction in CNTs is highly anisotropic, and the transverse conduction is orders of magnitude lower than the longitudinal conduction.[17]

However there are still numerous problems to be addressed before CNTs can be utilized as interconnects, which are mainly:

1. achieving a high-density integration with CNTs: CNT-bundles can outperform copper wires in terms of conductivity only if they are dense enough;
2. selective growth of metallic SWCNTs: SWCNT growth processes developed to date cannot control chirality;
3. achieving low-resistance contacts: the metal electrode contact with CNTs may cause reflection effects and cause contact resistance.[17]

The main electronic applications of CNTs are the channel in field effect transistors.[18–20]

In the simulations presented in this paper, in order to show how the parasitic elements limit the high-speed performances of CNTs, we have used a CNTFET model, already proposed by us in,[14–16] which we briefly refer to here.

A Review of our CNTFET Model

An exhaustive description of our CNTFET model is in.[14–16] Therefore we suggest the reader to consult these References.

It is a compact, semi-empirical model directly and easily implementable in simulation software to design analog and digital

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Table I. 50 nm design rules.

Technology	50 nm
lambda:	25 nm
Metal minimum length	3*lambda (75 nm)
Metal minimum width	3*lambda (75 nm)
Metal thickness	350 nm
Metal minimum spacing	4*lambda (100 nm)
Contact minimum width	2*lambda (50 nm)
Contact minimum spacing	3*lambda (75 nm)

Table III. 3 nm design rules.

Technology	3 nm
lambda:	2 nm
Metal minimum length	3*lambda (6 nm)
Metal minimum width	3*lambda (6 nm)
Metal thickness	50 nm
Metal minimum spacing	4*lambda (8 nm)
Contact minimum width	2*lambda (4 nm)
Contact minimum spacing	3*lambda (6 nm)

circuits: in fact the most complex part of the model is contained in Verilog A. In particular, the software used is Advanced Design System (ADS) which is compatible with the Verilog A programming language. We have considered a single wall n-CNTFET in the ballistic transport hypothesis. This assumption allowed to define an analytical formula for CNT current.

When a positive voltage V_{GS} is applied between gate-source, the conduction band at the channel beginning decreases by qV_{CNT}, where q is the electron charge and V_{CNT} is the surface potential, whose expression is reported in our Refs. 13–16.

With the hypothesis that each sub-band decreases by the same quantity along the whole channel length, the total drain current can be expressed as:[2]

$$I_{DS} = \frac{4qkT}{h}\sum_{p}[\ln(1 + \exp\xi_{Sp}) - \ln(1 + \exp\xi_{Dp})] \qquad [1]$$

where k is the Boltzmann constant, T is the absolute temperature, h is the Planck constant, p is the number of sub-bands, while ξ_{Sp} and ξ_{Dp}, depending on temperature through the sub-bands energy gap, and V_{CNT}, have the expressions reported in.[2]

In order to simulate correctly the CNTFET behaviour, we needed to estimate parasitic capacitances and inductances as well as the drain and source contact resistances.

In this paper we have achieved this goal using an empirical method,[2,3] more suitable for simulations in CAD environment. This method requires the extraction of the previous parasitic elements comparing the device characteristics with the measured ones. In this way all elements of the equivalent circuit can be determined.[2,3]

Design Rules of I.C.

In order to estimate parasitic elements in CNTs embedded I.C., we have analyzed 50 nm technology. Moreover it is also possible a predictions analysis on 10 nm and 3 nm technology.[21,22]

The first step of this work is to know the length, width and thickness of metal interconnection lines in integrated circuits. For this we have referred to MICROWIND software.[23]

In particular MICROWIND is truly integrated software encompassing IC designs from concept to completion, enabling chip designers to design beyond their imagination. MICROWIND integrates traditionally separated front-end and back-end chip design into one flow, accelerating the design cycle and reduces design complexities.

Table II. 10 nm design rules.

Technology	10 nm
lambda:	5 nm
Metal minimum length	3*lambda (15 nm)
Metal minimum width	3*lambda (15 nm)
Metal thickness	100 nm
Metal minimum spacing	4*lambda (20 nm)
Contact minimum width	2*lambda (10 nm)
Contact minimum spacing	3*lambda (15 nm)

It tightly integrates mixed-signal implementation with digital implementation, circuit simulation, transistor-level extraction and verification—providing an innovative education initiative to help individuals to develop the skills needed for design positions in virtually every domain of IC industry.

For our purposes, MICROWIND 3 has been used. The software provides, over a tool for layout design itself, a list of design rules for every current type of technology.

In Table I we have summarized the obtained results.

As we can see from this table, dimensions in integrated circuits are usually expressed in function of lambda, which most of the times is half of the technology length, thus half of the channel length.

The 10 nm target has been achieved using FinFET, which were commercialized in the first half of the 2010 s. In 2018, microchips utilizing FinFET gates first became the dominate gate design at 14 nm, 10 nm, and 7 nm process nodes.[24]

Regarding CNTs, a theoretical limit of 10 nm should be set, because of various complex quantum mechanics phenomena which affect the sub-10 nm regime.[12]

Therefore, design rules of CNT embedded in I.C. have been predicted considering design rules of previous technologies and lithography limits. In Tables II and III reasonable values have been summarized also for 10 nm and 3 nm technology.

Estimation of Parasitic Elements of Interconnection Lines

To characterize interconnection lines, the classical transmission line model, reported in Fig. 1, is useful to the final purpose of estimating parasitic elements.

In this paper, all the parasitic elements (except for the mutual capacitance value) have been calculated with Wcalc software,[25] based on the studies reported in.[26–29]

In particular Wcalc is a tool for the analysis and synthesis of transmission line structures and related components and provides the ability to analyze the electrical parameters of a particular structure based on the physical dimensions and material parameters. The synthesis portion calculates the required physical parameters to meet desired electrical specifications. Wcalc includes several models and places an emphasis on accuracy. Several frontends provide the user with several options for its use.

Regarding the expression of mutual capacitance, we referred to the articles.[30–32]

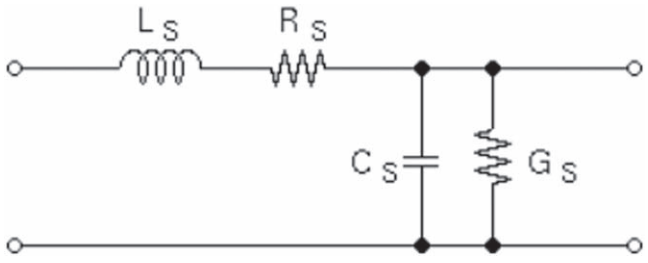

Figure 1. Transmission line model.

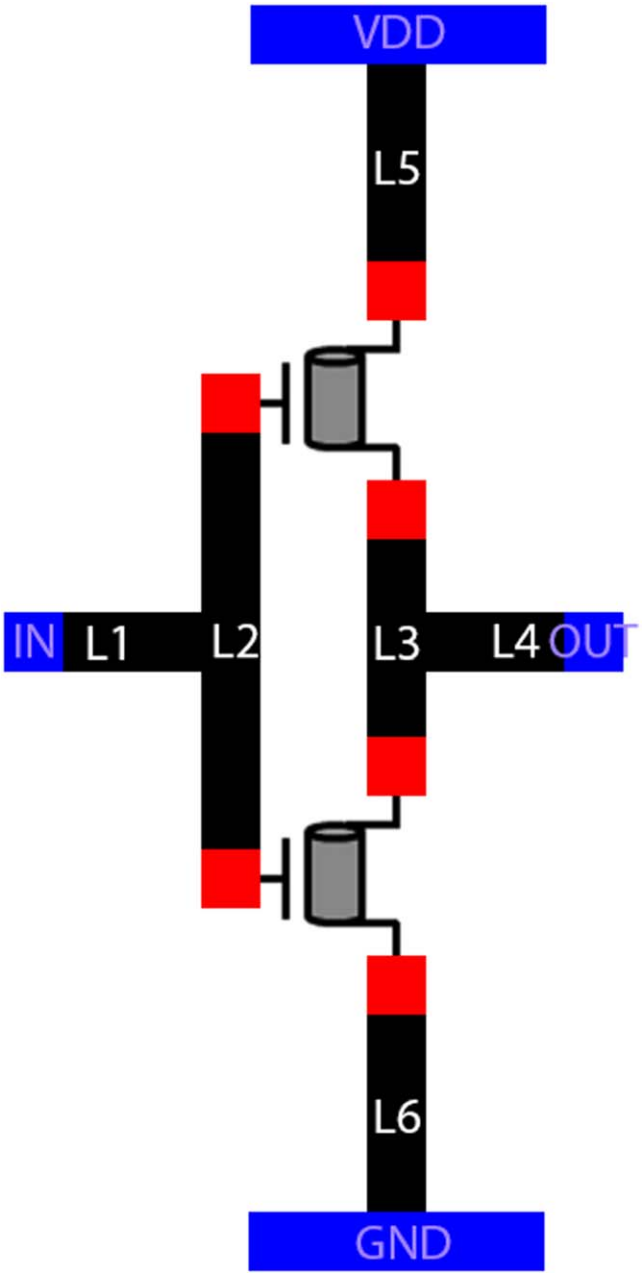

Figure 2. CNTFET symmetrical inverter layout.

Experimental Set-up and Methodology

Symmetrical inverter circuit.—As the aim of this paper is to see how parasitic elements of embedded CNT in I.C. could affect the performances of circuits, now we want to study a symmetrical inverter circuit, whose layout is reported in Fig. 2.

The metal is Cu (resistivity = 1.72e-8 Ωm) and the substrate is Si (relative permittivity = 11.8).

At first we have characterized the transmission lines, according the design rules of I.C. previously examined, and in Table IV we reported the parameter values in 50 nm technology.

The next step has been to estimate the values of parasitic elements of lines L_i (i = 1.6), using Wcalc software tool,[25] as we have already said.

The obtained results are reported in Table V.

The mutual inductance between L2-L3 is 6.92114e-15 H (coupling coefficient equal to 0.424981) and the mutual capacitance between L2-L3 is 2.1335e-20 F.

Table IV. Values of parameters in 50 nm technology.

Parameter	Value
L1,L3,L4,L5,L6 length	100 nm
L2 length	150 nm
L1,L2,L3,L4,L5,L6 width	75 nm
Pad dimensions	50 nm × 50 nm
Channel length	50 nm
Substrate thickness	50 μm
Metal thickness	350 nm
L2-L3 distance	100 nm

Similarly, in Table VI we reported the parameter values in 10 nm technology and the relative values of parasitic elements of lines L_i (i = 1.6) in Table VII.

In this case the mutual inductance between L2-L3 is 1.24882e-15 H (coupling coefficient = 0.469816) and he mutual capacitance between L2-L3 is 5.7596e-21 F.

At last, in Table VIII we reported the parameter values in 3 nm technology and the relative values of parasitic elements of lines L_i (i = 1.6) in Table IX.

The mutual inductance between L2-L3 is 6.63808e-16 H (coupling coefficient = 0.505178) and the mutual capacitance between L2-L3 is 2.8008e-21 F.

Common source amplifier.—Now we study a common source amplifier, whose layout is reported in Fig. 3.

In this layout, the length L of the interconnection lines are all the same. For the 50 nm technology, the length is equal to 100 nm, whilst other corresponding values are the same as listed in Table IV and Table V.

For the 10 nm technology, the length is equal to 20 nm, whilst other corresponding values are the same as listed in Table VI and Table VII.

For the 3 nm technology, the length is equal to 8 nm, whilst other corresponding values are the same as listed in Table VIII and Table IX.

ADS Simulations

The following simulations in Advanced Design System[33] show how the different values of parasitic elements in 50, 10 and 3 nm technology affect the performances of circuits. In particular we present the time domain analysis of symmetrical inverter and the frequency response simulations on a common source amplifier, both based on CNTFETs.

Time domain analysis of symmetrical inverter based on CNTFET.—The symmetrical inverter schematic, full up of parasitic elements, is shown in Fig. 4.

The schematic is the same for 50 nm, 10 nm and 3 nm: only the values of parameters change.

As we can see from Fig. 4, in order to make the circuit totally symmetrical, L2 and L3 lines (Fig. 2) parasitic elements have been split in two parts. Therefore a mutual inductance between inductors L7-L9 and L8-L10 must be considered.

In Table X we have reported the calculated values of the mutual inductance and of coupling coefficient.

The first step was to choose a proper power supply voltage because the circuit must work as a good inverter, which means that the negative derivative of the gain must pass only two times across an horizontal straight line of value 1.

To choose the power supply, we have used the circuit shown in Fig. 5.

The two boxes of Fig. 5 symbolize the schematic of Fig. 4.

A DC sweep on the input voltage provides the results shown in Fig. 6.

Table V. Values of parasitic elements in 50 nm technology.

Line	Rs (0.000658314 Ω nm^{-1})	Ls (1.38946e-15 H nm^{-1})	Cs (4.75384e-20 F nm^{-1})	Gs (6.78442e-13 s nm^{-1})
L1,3,4,5,6	0.0658 Ω	1.3895e-13 H	4.75384e-18 F	6.78442e-11 S
L2	0.0987 Ω	2.0842e-13 H	7.1308e-18 F	1.0177e-10 S

Table VI. Values of parameters in 10 nm technology.

Parameter	Value
L1,L3,L4,L5,L6 length	20 nm
L2 length	30 nm
L1,L2,L3,L4,L5,L6 width	15 nm
Pad dimensions	10 nm × 10 nm
Channel length	10 nm
Substrate thickness	50 μm
Metal thickness	100 nm
L2-L3 distance	20 nm

On the left, the negative derivative of the gain is shown. As we can see, it passes only two time across a horizontal straight line of value 1, which means that the gain has only two points with a unitary derivative. These two points, approximately 0.47 V and 0.75 V, are the thresholds of the inverter. For values of Vin between the thresholds, the gain must have a negative derivative greater than one. This peculiarity is usually called "regenerative gate inverter."

On the right, a plot of Vout/Vin is shown. As we can see, the plot features a classical inverter characteristic.

Similarly Figs. 7 and 8 show the inverter gain in 10 nm and 3 nm technology respectively.

The measured thresholds have almost the same value for all the technologies used.

50 nm time domain analysis.—To analyze the performance of the 50 nm symmetrical inverter, the simulation circuit used is shown in Fig. 9, in which every box symbolizes the schematic of Fig. 4.

Four CNTFET inverter, full of parasitic, have been used. This choice is justified by the fact that to perform a transient analysis it is necessary to simulate the non-linear load effects on a certain device. So, the useful output voltage is the one of the third stage.

The simulation results are reported in Fig. 10.

On the right there is the output waveform out of the third stage, which is almost the inverted ideal pulse generator waveform.

On the left, there are the output waveforms out of the second stage and the third stage. The measured fall time and rise time[34] are respectively 3.96 ps and 3.37 ps.

The measured 50% delay[34] is 1.97 ps.

Similarly in Figs. 11 and 12 we have reported the simulation results in 10 nm and 3 nm technology respectively. For the first we have considered the parameters values of Table VII, for the second those of Table IX.

From the previous figures it easy to determine the fall time and rise times, and 50% delay time, as shown in Table XI.

As was to be expected, these times decrease with technology dimensions.

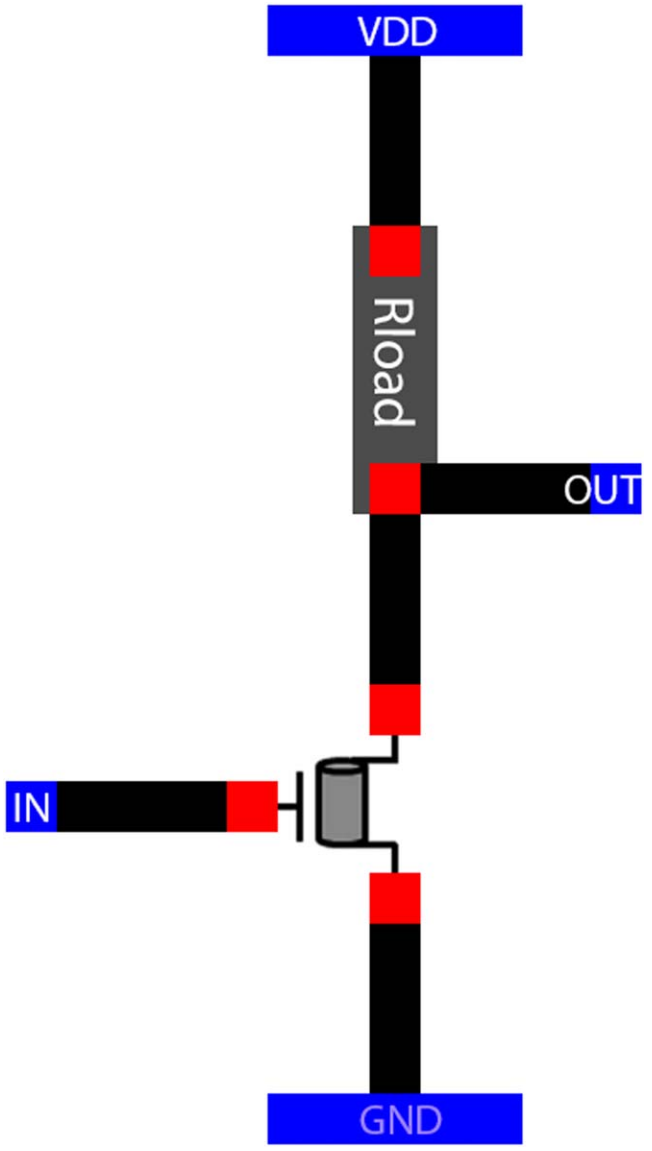

Figure 3. CNTFET common source layout.

CNTFET common source stage frequency response analysis.—The CNTFET C-S amplifier schematic, full up of parasitic elements, is shown in Fig. 13. The relative layout has been reported in Fig. 3.

The schematic is the same for 50 nm, 10 nm and 3 nm: only the values of parameters change.

Table VII. Values of parasitic elements in 10 nm technology.

Line	Rs (0.0121242 Ω nm^{-1})	Ls (1.83023e-15 H nm^{-1})	Cs (3.9155e-20 F nm^{-1})	Gs (5.67659e-10 S nm^{-1})
L1,3,4,5,6	0.2425 Ω	3.6605e-14 H	7.8310e-19 F	1.1353e-08 S
L2	0.3637 Ω	5.4907e-14 H	1.1747e-18 F	1.7030e-08 S

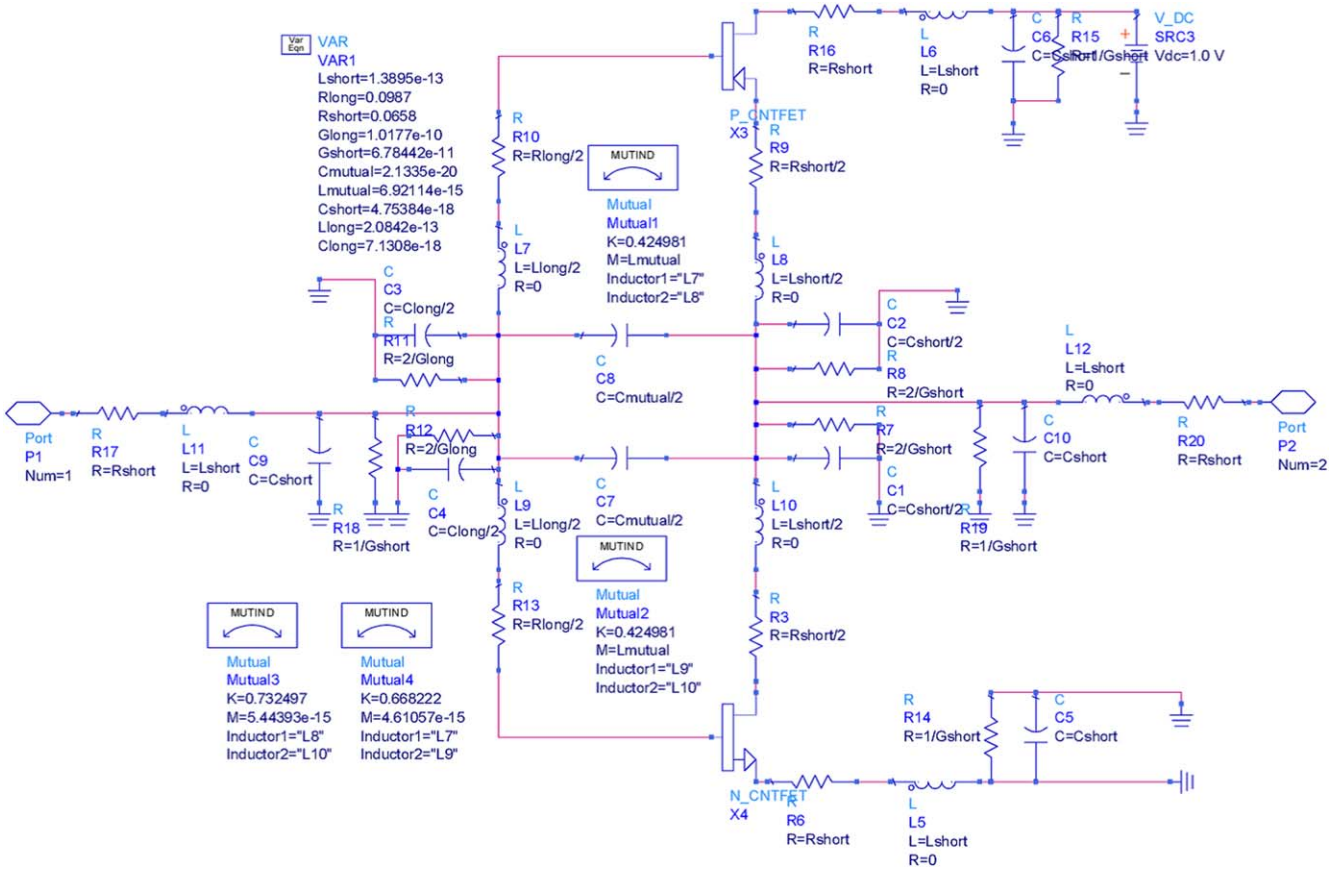

Figure 4. Schematic of 50 nm CNTFET symmetrical inverter with parasitic elements.

The simulation circuit contemplate a frequency sweep of the input source, in order to obtain the amplitude Bode plot.

The aim of this simulation is to estimate the −3dB cutting frequency of a CNTFET common source stage full of parasitic elements in 50 nm, 10 nm and 3 nm technologies.

50 nm AC analysis.—In Fig. 14 we shown amplitude Bode plot of a CNTFET common source stage with parasitic elements in 50 nm technology.

As we can see, the measured cutting frequency was approximately $f_{-3dB} = 0.32$ THz. In this case the high values of parasitic

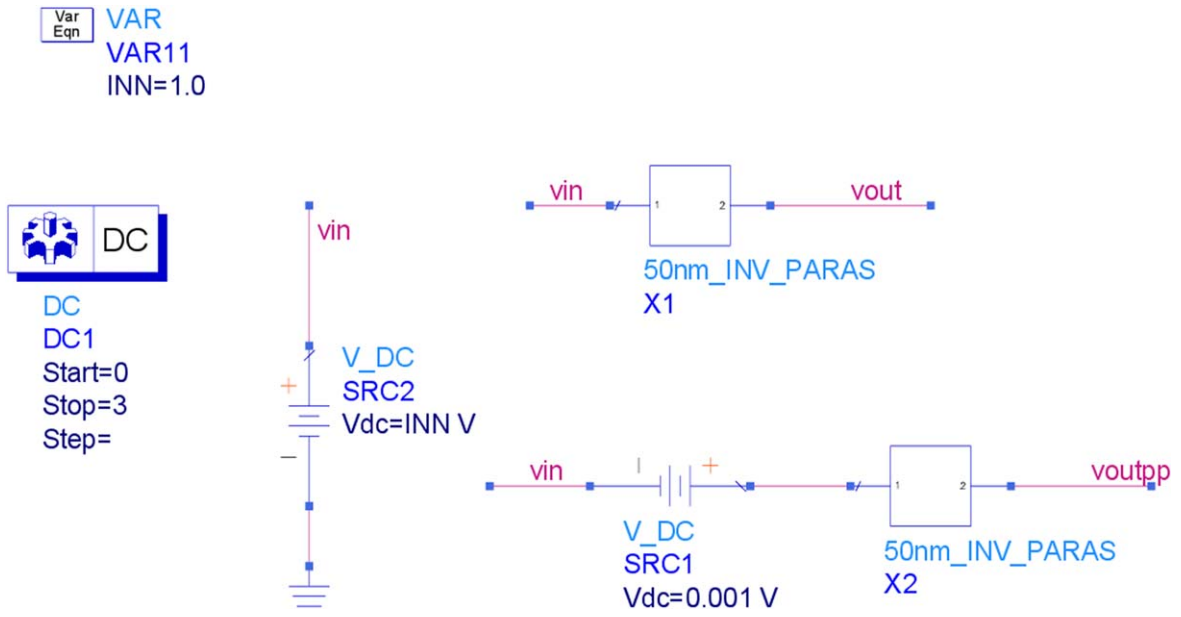

Figure 5. Gain test circuit.

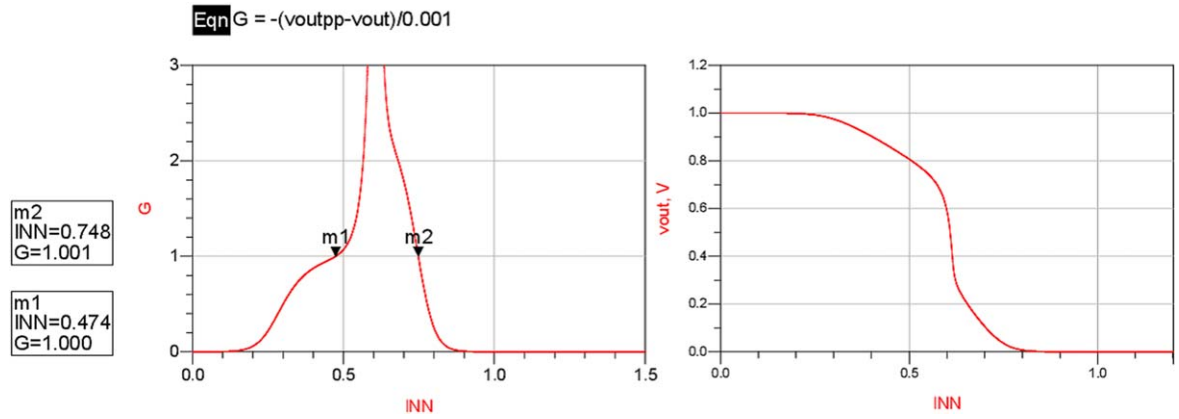

Figure 6. Inverter gain results in 50 nm technology.

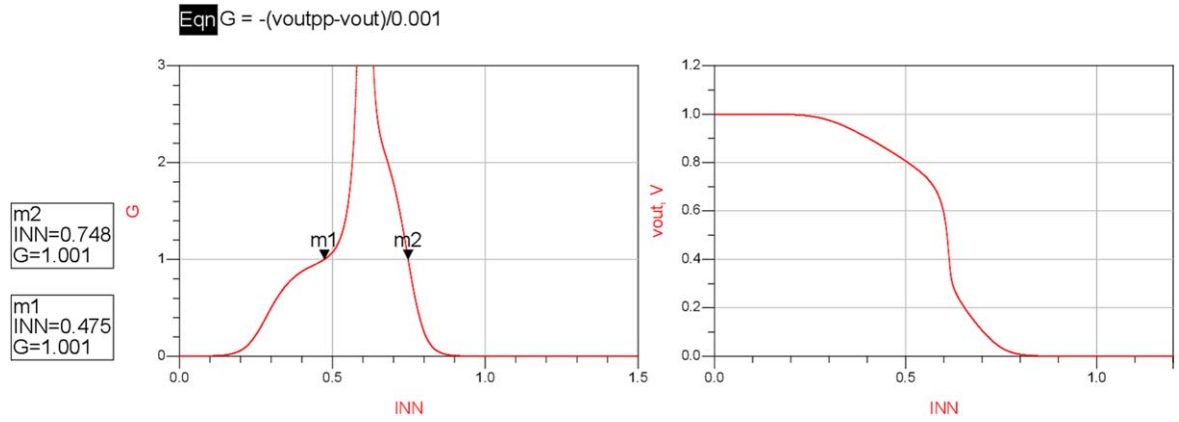

Figure 7. Inverter gain results in 10 nm technology.

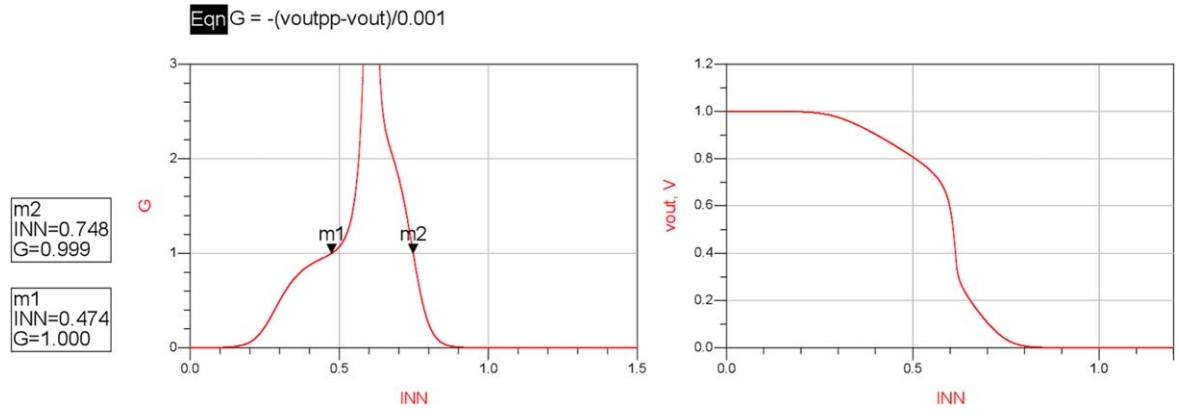

Figure 8. Inverter gain results in 3 nm technology.

Table VIII. Values of parameters in 3 nm technology.

Parameter	Value
L1,L3,L4,L5,L6 length	8 nm
L2 length	18 nm
L1,L2,L3,L4,L5,L6 width	6 nm
Pad dimensions	4 nm × 4 nm
Channel length	10 nm
Substrate thickness	50 μm
Metal thickness	50 nm
L2-L3 distance	8 nm

elements considerably slow down the circuit, as without these, the CNTFET itself could have a much higher cutting frequency.

10 nm AC analysis.—In Fig. 15 we show amplitude Bode plot of a CNTFET common source stage with parasitic elements in 10 nm technology.

As we can see from the Fig. 4, the measured cutting frequency was $f_{-3dB} = 2.00$ THz. The difference between this case and the 50 nm case is considerable. With the decreasing of parasitic elements is possible to achieve a much higher cutting frequency, which goes close to the ideal CNTFET one.

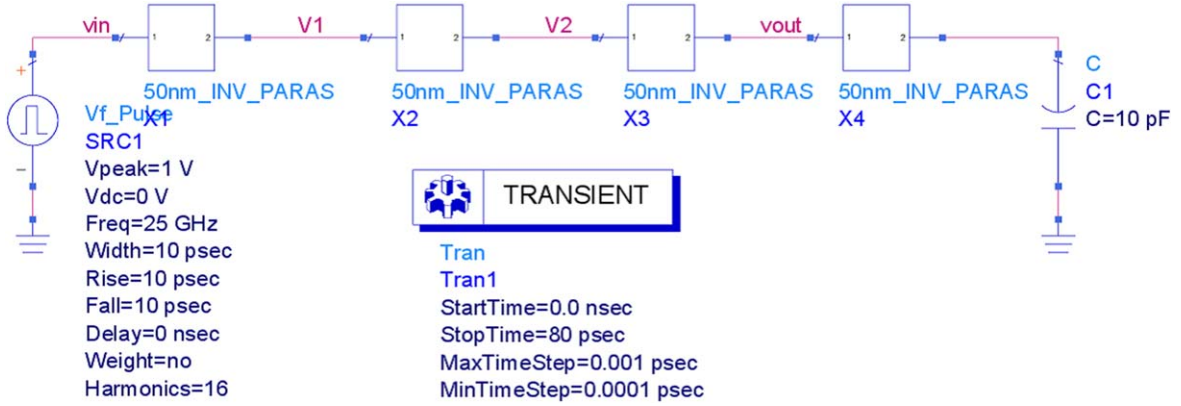

Figure 9. Inverter digital circuit.

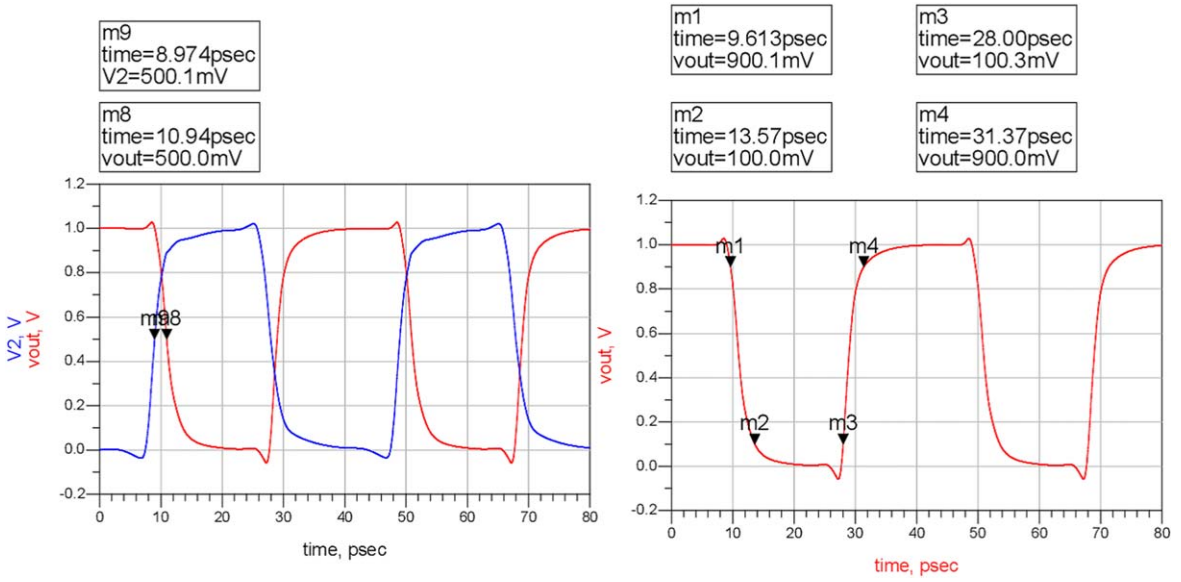

Figure 10. 50 nm time domain analysis.

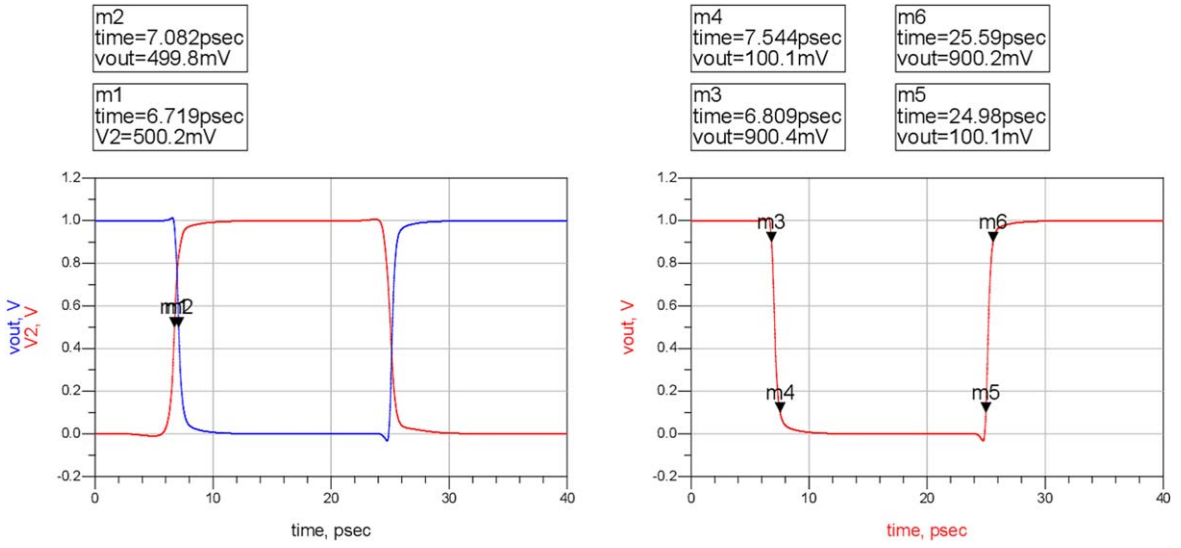

Figure 11. 10 nm time domain analysis.

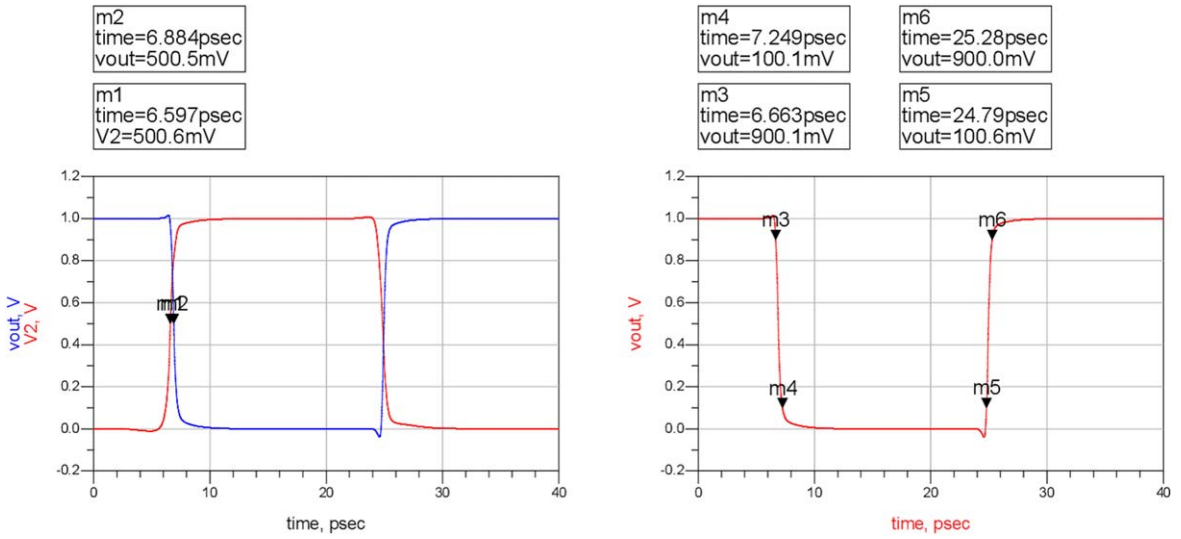

Figure 12. 3 nm time domain analysis.

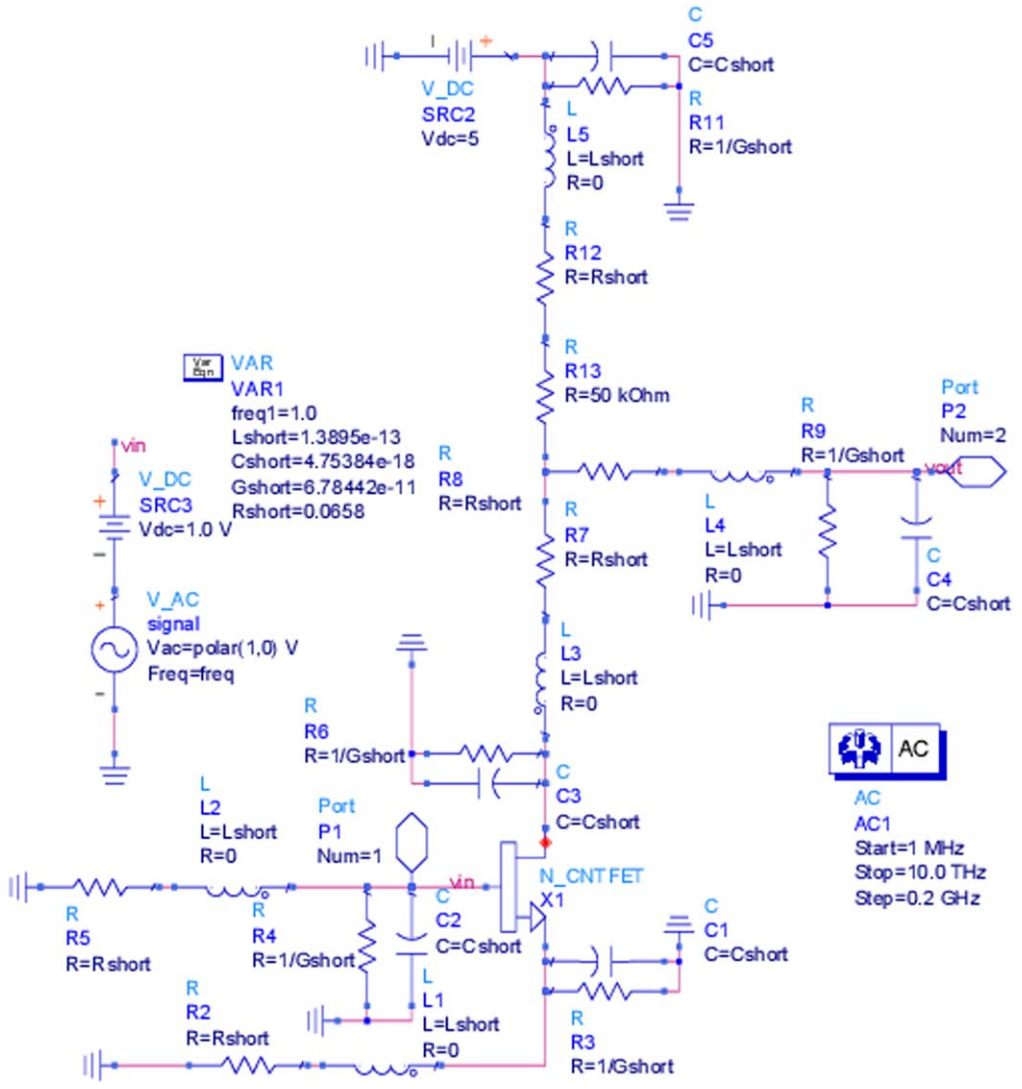

Figure 13. Schematic of 50 nm CNTFET C-S stage with parasitic elements.

Table IX. Values of parasitic elements in 3 nm technology.

Line	Rs (0.0699876 Ω nm^{-1})	Ls (2.00388e-15 H nm^{-1})	Cs (3.58692e-20 F nm^{-1})	Gs (5.20308e-10 S nm^{-1})
L1,3,4,5,6	0.5599 Ω	1.6031e-14 H	2.8695e-19 F	4.1625e-09 S
L2	1.2598 Ω	3.6070e-14 H	6.4565e-19 F	9.3655e-09 S

Table X. L7-L9 and L8-L10 mutual inductances and coupling coefficient values.

Technology	L7-L9 mutual inductance and coupling coefficient	L8-L10 mutual inductance and coupling coefficient
50 nm	4.61057e-15 H 0.668222	5.44393e-15 H 0.732497
10 nm	7.58043e-16 H 0.681533	8.75258e-16 H 0.73618
3 nm	2.2105e-16 H 0.620907	2.94105e-16 H 0.716001

Table XI. Time domain analysis: values of fall, rise time and 50% delay time.

Technology	Fall time	Rise time	50% delay
50 nm	3.96 ps	3.37 ps	1.97 ps
10 nm	0.73 ps	0.61 ps	0.36 ps
3 nm	0.59 ps	0.49 ps	0.29 ps

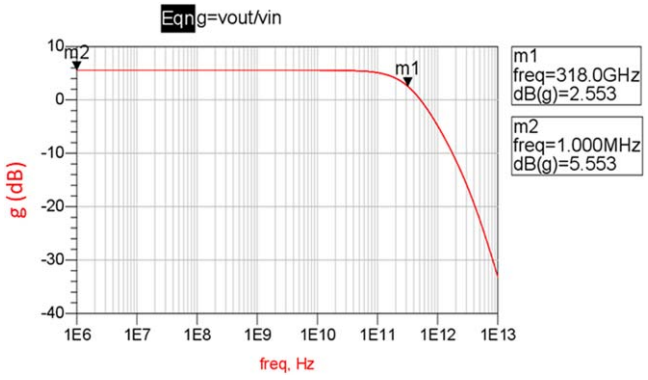

Figure 14. Amplitude Bode plot of a CNTFET C-S stage with parasitic elements in 50 nm technology.

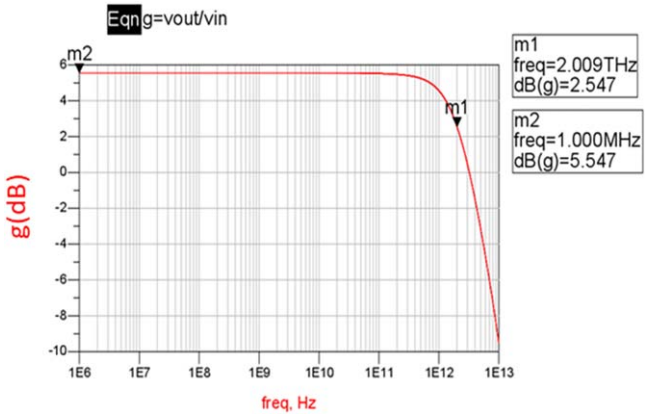

Figure 15. Amplitude Bode plot of a CNTFET C-S stage with parasitic elements in 10 nm technology.

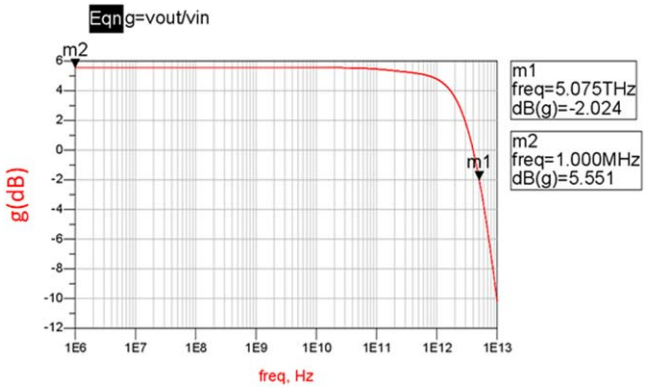

Figure 16. Amplitude Bode plot of a CNTFET C-S stage with parasitic elements in 3 nm technology.

Table XII. Cutting frequencies vs technology.

Technology	f_{-3dB}
50 nm	0.32 THz
10 nm	2.00 THz
3 nm	5.07 THz

3 nm AC analysis.—In Fig. 16 we show amplitude Bode plot of a CNTFET common source stage with parasitic elements in 3 nm technology.

As we can see, the measured cutting frequency was f_{-3dB} = 5.07 THz. Obviously, the more the parasitic values decrease, the more the cutting frequency increase. In these conditions, a very high speed circuit could be realized.

The obtained results can be summarized in Table XII.

Conclusions

In this paper we presented a study of the effects of parasitic elements of interconnection lines in integrated circuits (I.C.) where Carbon NanoTubes (CNTs) are embedded. In particular the Drain/Source pads dimensions of CNT have been analyzed, as well as the interconnection lines between a CNT and an appropriate load are sized. Furthermore the time domain and frequency simulations, obtained in Verilog-A, of some circuits have been presented in order to see how the parasitic elements could limit the high-speed performances of CNTs.

Moreover it is our intention to repeat the proposed technique considering other A/D circuits and using also other CNTFET

models, proposed in literature, such as the VS-CNFET model,[35,36] in order to make further comparisons.

Currently we are investigating about the effects of noise in CNTFET-based A/D circuits.

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