MAGIC: a European program to push the insertion of maskless lithography

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ABSTRACT

With the willingness of the semiconductor industry to push manufacturing costs down, the mask less lithography solution represents a promising option to deal with the cost and complexity concerns about the optical lithography solution. Though a real interest, the development of multi beam tools still remains in laboratory environment. In the frame of the seventh European Framework Program (FP7), a new project, MAGIC, started January 1st 2008 with the objective to strengthen the development of the mask less technology. The aim of the program is to develop multi beam systems from MAPPER and IMS nanofabrication technologies and the associated infrastructure for the future tool usage. This paper draws the present status of multi beam lithography and details the content and the objectives of the MAGIC project.

KEYWORDS : E-Beam, lithography, multi beam, mask less,

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1. INTRODUCTION

Since the 1980s, the optical mask based solution drives the industrial lithographic processes without any share. The constant improvements of the optical tools allowed maintaining this technological leadership thanks to successive improvements: wavelength reduction, numerical aperture increase, the take off of chemically amplified resists, the introductions of immersion principle and Optical Proximity Correction (OPC)... However, linked to these constant innovations, this technique becomes every generation more and more complex and expensive. Today the problematic of contact

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patterning, the multiplication of illumination settings and the high complexity of OPC solutions impacting mask manufacturing are examples of the difficulties to be faced by the semiconductor manufacturers. The optical golden road does not seem to be able to counter this cost and complexity trend with the coming option like Extreme Ultra Violet (EUV) and Double Patterning technique (DP).

With such perspectives and the IC industry willingness to push manufacturing costs down, the Mask Less Lithography (ML2) solution represents a promising option to deal with the present concerns. Recently, several papers promoted the interest of this technique[1,2]. The interest is not only on reducing production price of prototypes, but also for the patterning solution of the contact layers for the coming generations. Moreover cost of ownership results and latest achievement realized with direct write lithography shown in this paper will again confirm the real opportunity represented by this option.

Nevertheless, the ML2 technique is still today in the starting blocks. In the frame of seventh European framework program, a new project, called "MAGIC", started January 1st 2008 with the objective to strengthen the development of the ML2 technology. It is composed of 2 linked poles. The first one is dedicated to tool development where MAPPER and IMS Nanofabrication will separately build ML2 platforms, in a competitive manner, to deliver first alpha platforms compatible for the 32nm half pitch design rules in 2009. In relation with this tool activity, "MAGIC" intends also to develop the required infrastructure for the future usage of these tools in industrial environment.

This European initiative is a first important step to promote the ML2 technology take off and initiate its insertion in an industrial environment in a reasonable time frame. Such an international collaboration is fundamental and needs to be extended, as ML2 technology is recognized today as a powerful solution for the industry. The involvement of end users, resist and software partners around technology solutions is the keystone to ensure the dynamic for the development of the solution up to an industrial maturity level.

2. THE ORIGIN AND THE AIMS OF THE "MAGIC" PROGRAM

2-1. The relevance of the multi beam lithography

In recent years, there have been considerable investments performed in mask-based optical lithography, in particular 193nm immersion and EUV. If these technologies are well-suited for high volume products, they are not cost effective. For the sub-32nm half pitch technology, this feeling is even reinforced with the perspectives of using DPT for 193nm solution or the OPC complexity[3] associated to the tool cost for the EUV alternative. Therefore, logic and Application Specific Integrated Circuit (ASIC) manufacturers, as well as foundries, have problems to maintain reasonable product costs for their short run and low to medium volume devices. Effectively, the number of low/medium runners can represent up to a large amount of the total manufactured products for a low ratio of total wafer production. The figure 1 illustrates this production repartition for the case of a typical ASIC fab. In this figure, 68% and 80% of the products represents only respectively 10% and 20% of the total wafer production. Linked to the associated increase of mask budget, the ML2 solution is recommended for these important low/medium volume segments.

The electron beam systems are today mainly used for advanced masks manufacturing. However, the application field for direct write lithography has always been considered marginal due to its very low throughput capability. Multi beam lithography technology is expected to keep the EBDW advantages and to push production capability above 10 wafers per hours. With such perspective, significant manufacturing cost reduction can be envisioned.

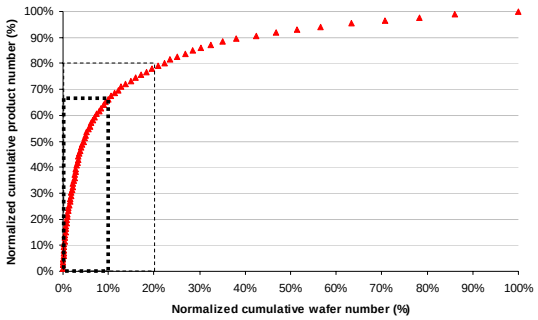


Figure 1 : Example of wafer repartition per product in ASIC fab

3 technologies covered :
- →130-90-45 or 90-65-45 or 65-45-32
- →Percentage repartition 40/40/20

Capability : between 5 up to 10kwspw

Fab loading : production + prototyping
- → 1 prototype started per week /5kw

Litho cell :
- Optical tools (from 248nm up 193nm 1.35NA)
- ML2 : **10wph – 20M$**

Mask budget : based on real cost up to
- 65nm node and 20% increased for next node

Figure 2 : Inputs for cost of owner calculation Fab profile : logic production unit

Latest study[4] summarized in table 1 highlights the maximum reduction of lithography cost offered by introducing ML2 systems in this case of a fab with a wafer in process per product identical to figure 1. It details the gain offered by the insertion of ML2 tools at three different insertion points. The assumptions used for this cost of owner calculation are listed in figure 2. For the model, the factory performs manufacturing on 3 technology nodes. It has a capacity between 5000 to 10000 wafer starts per week and offers prototyping service : 1 prototype per week every 5000 wafers. ML2 systems with 10 wafers per hour (wph) throughput are used to address the prototyping and low/medium runner segments. Mask cost is based on present cost for 130nm to 65nm nodes. Then, for each new technology node, mask set price is increased of 20% compared to previous generation node. Optimum cost reduction is extracted from the simulator. The table 1 highlights the interest of the ML2 alternative. Calculation shows that, if one industrial platform is available today, it already represents a cost saving on lithographic step of 35% by addressing 30% of the manufactured product. And in 2013, this gain will rise up to 45% and ML2 will cover around 50% of product manufacturing.

However the multi beam technology is still developed in the frame of Start-up Company that needs to be supported and highlighted to push their concept up to the industrial level. It becomes evident that the availability of this technology represents a big opportunity for semiconductor industry. This interest is not limited to the market of prototyping as shown in this example, but its usage can be foreseen also in production for key levels in the case of issue encountered by the golden mask-based tools for the future nodes. Finally, mask making market represents as well a potential target for the ML2 to reduce the mask writing time constraint

Foundry profile	2008		2011		2013	
Hp node covers	130/90/65		90/65/45		65/45/32	
Production repartition	40/40/20		40/40/20		40/40/20	
Maximum lithography step cost saving	35%	37%	41%	42%	46%	47%
ML2 tool number	2	4	4	7	6	12
x% product number produced by ML2	30%	30%	40%	40%	50%	50%
WSPW	5000	10000	5000	10000	5000	10000

Table 1 : Cost of owner results in the case of logic fab unit (hypothesis listed in Fig. 2)

2-2. The “MAGIC” objectives

The “MAGIC” program is a **3 year project** with the key objectives to support, promote and demonstrate the interest of the ML2 technology. To execute this project, a consortium driven by CEA-LETI composed of 12 partners has been built comprising key companies involved in direct write environment:

- → Equipment : MAPPER and IMSnanofabrication
- → Data Preparation : SYNOPSYS
- → E-Beam Proximity Correction : SYNOPSYS, Vorarlberg University
- → Simulation : SYNOPSYS and Vorarlberg University
- → Semiconductor Manufacturers : STMicroelectronics, Qimonda
- → Institutes : CEA-LETI, Fraunhofer Institutes (CNT, HHI, ISIT, IZM), IMS-CHIPS
- → Resist supplier : Fujifilm
- → Stage partner for IMS nanotechnology solution : DELONG instruments
- → Metrology : KLA TENCOR

MAGIC is divided in 5 work packages focused on two main areas: tool development and infrastructure setup, as shown in figure 3. MAGIC intends first to support the technology development of two European companies based on two different massively parallel beam concepts: one on low electron beam energy (5kV) for MAPPER and the other on high energy (50kV) for IMS nanofabrication. These two strategies will be evaluated in a competitive manner all along the project, in order to assess the maturity of each solution in respect to the manufacturing needs. The key challenge of this part of the program will be the delivery of a first ML2 alpha tool in the second half of 2009. These platforms will be integrated in an industrial environment to demonstrate their ability to answer the semiconductor manufacturing concerns.

The second activity of this program is related to the development of the infrastructure. This work is mandatory for any future use of this technology in a manufacturing environment. The developments are divided in three main blocks.

The first one is focused on data base preparation. In this topic leaded by SYNOPSYS, the target will be to develop a complete data treatment solution in order to perform exposure on the different ML2 platforms. Then, at the end, the task of this activity will be the development of a fast, robust and commercial data preparation platform compatible with industry requirements providing full support and development perspectives.

The second topic covers the control of the Electron Beam Proximity Effects (EBPC). Accurate models, based on dose modulation and potentially associated to geometrical correction approach, are necessary to ensure CD control in respect with ITRS roadmap requirements. Here also the building of a commercial platform, fully integrated with the data preparation flow, is necessary for the usefulness of

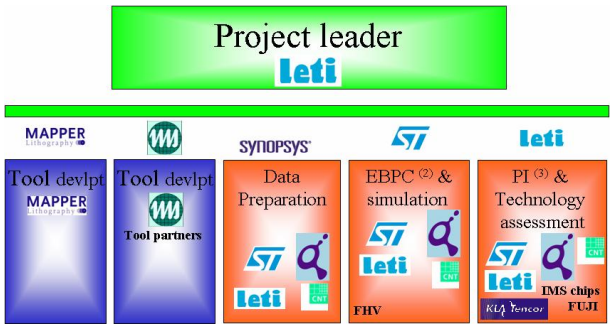


Figure 3 : MAGIC program structure overview

ML2 in manufacturing. After a first definition phase of the proximity correction needs, this part of the project leaded by STMicroelectronics intends to support the development of the future EBPC infrastructure.

The last topic covered by this thematic is related to all aspects of integrating ML2 in manufacturing-like conditions using the tools developed through this project and the different software platforms. The work performed will ensure the promotion of the ML2 technology for sub-32nm nodes. Full process integration will be performed in order to demonstrate the full compatibility of this technology with standard CMOS manufacturing process, system on chips.

3. DETAIL OF MAGIC CONTENT

3-1. The European maskless technologies

Today's commercially available electron-beam lithography machines for exposing 300mm wafers for semiconductor prototyping and/or manufacturing are using electrons at a high (≥50kV) acceleration voltage. Furthermore they use only one electron beam and are therefore limited in throughput (~50 hours per wafer if the full area would be exposed). The choice for high (≥50kV) or low (<10kV) voltage is independent from whether a single beam or a multibeam solution is pursued. The high voltage approach is generally adopted because in this case manufacturers can leverage their existing infrastructure and from a technical point of view it is easier to obtain high resolution with a high-voltage system. There is one important reason why MAPPER has chosen to use a 5kV solution: wafer heating.

3.1.1 : MAPPER concept : The low energy alternative

Multibeam systems become economically attractive when they have the potential to reach throughputs of > 10wph. This implies that large currents are required (MAPPER uses 150µA). The energy deposited on the wafer is therefore 0.75W for 5kV and 7.5W for 50kV. Since stringent overlay budgets (<10nm) prohibit the expansion of the wafer and sufficient cooling solutions are not proven today MAPPER has chosen the low voltage solution. Furthermore if one wants to extend the technology to higher throughputs and/or the next node the required current is even larger (in the latter case due to LER requirements).

Next to the choice for low voltage imaging MAPPER's multibeam system has another important aspect that no other multibeam concept known today has: All electron beams, >13000, are going through the optical system in a fully parallel way, from the source to the wafer.

The MAPPER technology combines massively-parallel electron-beam writing with high speed optical data transport used in the telecommunication industry. The electron optics generates 13,000 electron beams that are focused on the wafer by electrostatic lens arrays. Each beam has its own optical column to avoid a central cross-over, see figure 4. This secures high throughput (> 10 wafers per hour) at high resolution (< 45 nm). The 13,000 e-beams are generated by splitting up a single electron beam that originates from a single electron source. The e-beams are arranged in such a way that they form a rectangular slit with a width of 26 mm, the same width of a field in an optical stepper. During exposure the e-beams are deflected over 2 µm perpendicular to the wafer stage movement, see figure 4. This means that with one scan of the wafer a full field of 26 mm x 33 mm can be exposed. During the simultaneous scanning of the wafer and deflection of the electron beams the beams are switched on and off by 13,000 light signals, one for each e-beam. The light beams are generated in a data system that contains the chip patterns in a bitmap format. This bitmap is divided over 13,000 data channels and streamed to the e-beams at 1-10 GHz.

As can be seen from figure 4, all beams are fully parallel from source to the wafer and no central crossover is required. To achieve this special lens arrays, deflector arrays and blanker arrays are required. MAPPER currently has a 110-beam demonstrator system which shows that these elements can be made and work well together. First results obtained with MAPPER's technology demonstrator are shown in the figure 5 where 41nm dense lines and spaces are properly resolved by multiple electron beams in parallel.

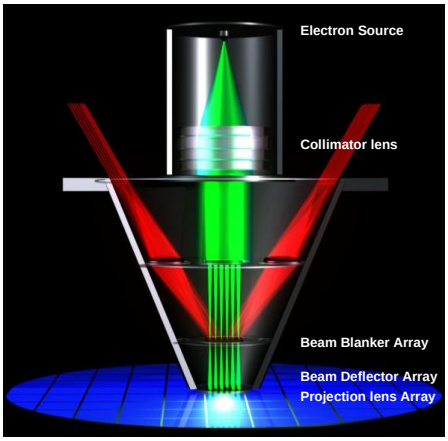


Figure 4-a : Schematic outline of MAPPER's e-beam column

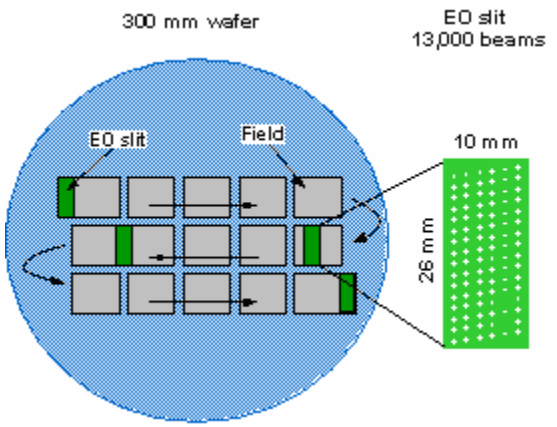


Figure 4-b : Overview of the beam arrangement and writing strategy

Figure 4 : MAPPER concept overview

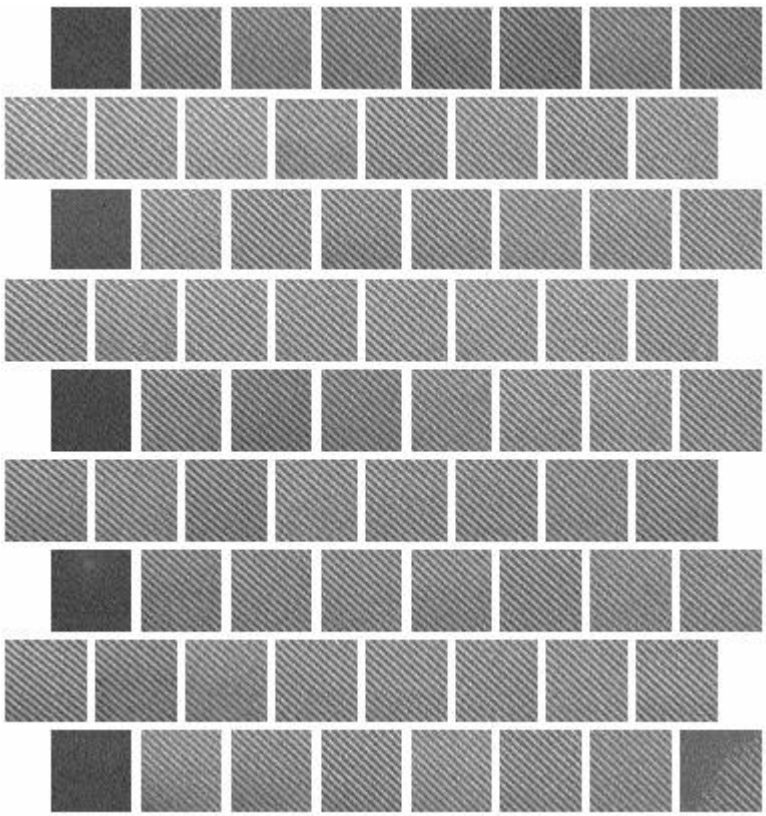


Figure 5 : Overview of 41 nm dense lines in MAPPER's technology demonstrator Each 1 x 1 µm area is exposed by a different beam

3.1.2 IMS Nanofabrication : Projection Mask Less Lithography (PML2) at 50kV

Projection Mask-Less Lithography (PML2) is based on IMS Nanofabrication's *"charged particle large field projection optics"* technology. The main strength of PML2 lies in the fact that pattern transfer is realized using an array of several hundreds of thousands individually addressable electron beams, thereby pushing the potential throughput from hours per wafer into the wafers per hour regime. Single-Axis-PML2 has 2 wph throughput potential for the 32nm node whereas Parallel-Axis-PML2 has a throughput potential of 20wph for the 32nm hp node (including overheads). PML2 is a multi-generational concept with resolution limits below 10nm, which enables the PML2 technology to go several nodes beyond the presently targeted 32nm hp node.

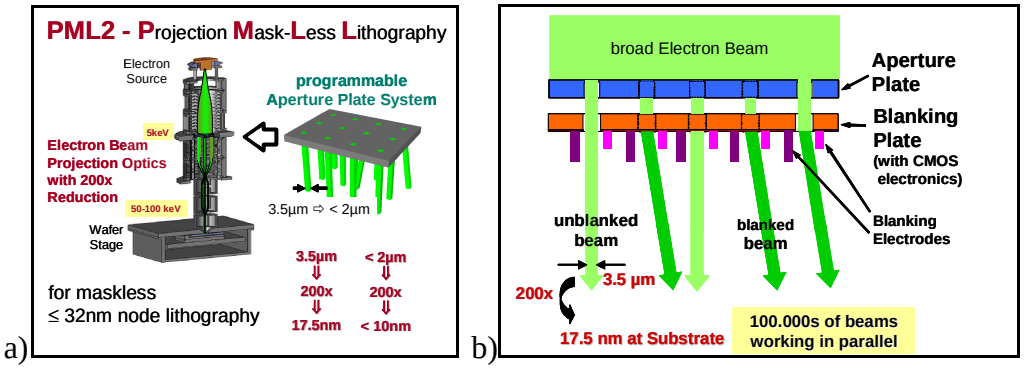


Figure 6 : Principles of Projection Mask-Less Lithography (PML2)

The main PML2 principles are shown in figure 6. In an electron-optical column, electrons are emitted from a flat emitter of high brightness. The condenser below the electron source is used to form a large diameter electron beam of high telecentricity and to direct this beam to a programmable aperture plate system (APS) with 5kV beam energy. Here, the homogeneous electron beam is split into several hundred thousand electron beamlets. These beamlets are accelerated to 50kV and projected with 200x reduction onto a resist-coated wafer. This way, all 3.5µm square openings in the APS are imaged as 17.5nm spots, which are dynamically used for pattern generation. The only moving mechanical part of the system is located in the PML2 tool platform housing: a high-precision laser interferometer controlled vacuum stage which continuously scans the wafer in exposure stripes.

The central part of the PLM2 tool is the programmable APS, which constitutes the object in the imaging electron optics. The APS consists of two silicon plates which exhibit a periodic staggered array of apertures. Individual beamlets are formed by the Aperture Plate while dynamic structuring is realized by the Blanking Plate below (Figure 6-b). Deflection electrodes at every aperture allow for individual control of each beamlet. This is realized by MEMS fabricated deflection electrodes on a CMOS chip. In order to generate any desired pattern on the Si wafer, a high speed optical data link is established between an external high speed data buffer and the CMOS electronics. During operation of a PML2 tool, proximity corrected GDSII data, which have been converted into machine specific code, are continuously transferred to the APS. While the stage is in continuous movement, wafers are exposed in stripes. Dynamic synchronization of APS and stage movement allows for precise pattern transfer. Due to the special design of the APS each point on the wafer can be exposed with high redundancy by a high number of different grey levels. These grey levels enable high dose latitude with a constant value even for 1nm address grid, with and without background dose (nested or isolated CD). All these features allow for optimisation of the projection exposure strategy and enhance the reliability and precision of the tool.

Within the European project “RIMANA” (Radical Innovation MAskless NAnolithography) an electron-optical test-bench with 200x reduction (200xTB) has already been realized (figure7). This PML2 proof-of-concept system contains all crucial components of a full-fledged PML2 tool and unambiguously demonstrates the operability of multi electron-beam projection optics with 200x reduction. In the 200xTB more than 2000 switchable beams are generated by an APS-prototype and projected onto wafer level with 200x demagnification. Current density (~2 A/cm2) and total current (~10 pA) of each beam are the same as in future PML2 tools, resulting in a calculated base resolution below 10nm. Using resolution templates, instead of an APS, the novel electron-optical column, consisting of electrostatic and magnetic lenses has been tested, verifying 200x reduction and the predicted 22nm hp resolution capability on 150mm Si wafers coated with 60nm PMMA positive resist and 50nm HSQ negative resist (figure 8). Currently, the APS-prototype is being tested and first demonstration patterns are being generated on resist coated 150mm Silicon wafers.

Figure 7 : RIMANA electron-optical test bench with 200x reduction (200xTB)

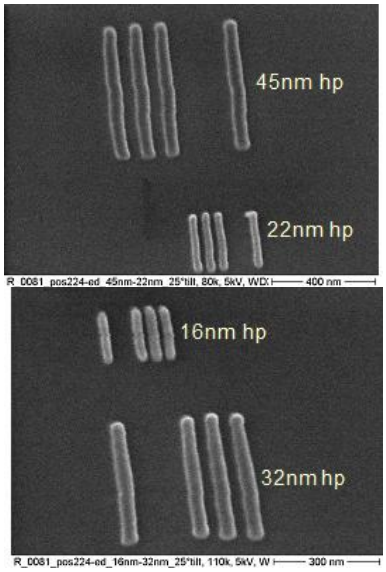


Figure 8 : Resolution in 50nm HSQ resist as achieved with the RIMANA PML2 proof-of-concept

3.2. The infrastructure around ML2 technology

3.2.1. The problematic of data flow

Developing the next generation data path for Multi-Beam Direct Write (MBDW) lithography must consider both the technical and economic challenges expected for data and equipment at 32nm and beyond. Massive file sizes, data path capacity, exposure CD control, along with data exchange formats are expected to be the primary design challenges for consideration when developing the next generation multi-beam maskless lithography data path. Optimizing the data path for different tool architectures with varying beam energies, beam count, and data processing (some have referred to this as ‘Pixel Based Data Prep’) will add another layer of complexity to the final data path solution/architecture and must be considered.

For comparison purposes, the following graphics, figure 9, contrast the key differences between the data prep requirements for mask versus maskless lithography. Although fewer steps can be envisioned overall – the complexities and challenges for the data path solution can be more complex – as the next paragraph will highlight.

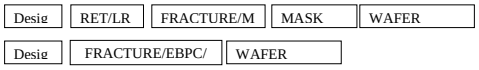


Figure 8 : Data flow difference between mask and ML2 lithography

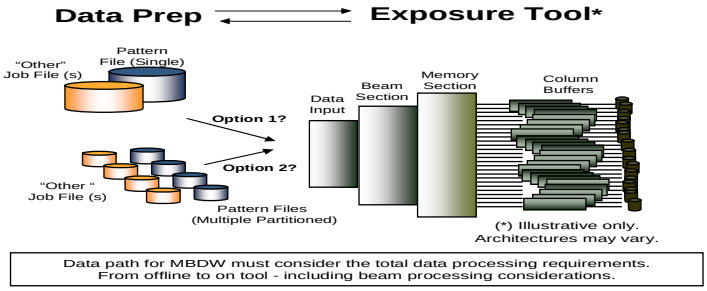


Figure 9 : Data path requirement for MBDW solution

The graphics, figure 10, provide a visual of some of the complexities of the data path requirements for a MBDW lithography tool including the interface to off-tool data preparation operations. One can imagine the final design of the data prep/data path to this type of exposure system would require advanced communication techniques at high speed data rates and as mentioned earlier have flexibility and programmability for a 'pixel based data prep' type design.

MAGIC – Multibeam Direct Write Data Preparation - Synopsys

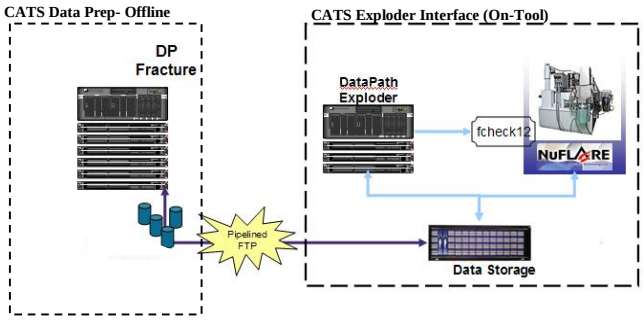
One of the key focus areas (work package) of the MAGIC project is the Data Preparation Software development. Building a data path which can deliver to the following high level requirements will be expected for the overall success of the MAGIC program which is targeting the 32/22nm nodes.

1. Complete data path solution from design tapeout to e-beam writer
2. GDS or OASIS inputs
3. Integrated ebeam proximity correction (dose, geometric) capability
4. Optimized data format and interface to each tool (Mapper, IMS)
5. Processing capability at high data rates compatible with ML2 tool performance demands
6. Develop compute cluster specifications and requirements for the data preparation
7. Extension of data path solution to e-beam writing should be considered

Synopsys, an industry leader in design and manufacturing software with over 20 years in data preparation experience will lead the development for the next generation data path within the "MAGIC" program. Additionally, Synopsys will provide services and expertise in areas such as e-beam simulation, process modelling, etc spanning multiple work packages which is covered in a separate sections of this paper.

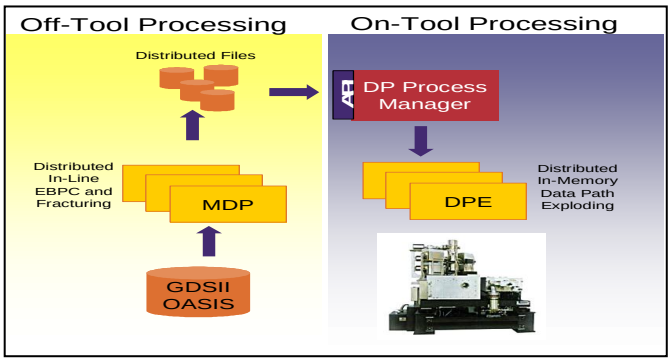
CATS, a mask and maskless (direct write) data preparation software package from Synopsys, will be the anchor product used for the new ML2 data preparation. CATS currently provides data preparation solutions for mask, direct write, inspection and metrology applications. Recent advances in the CATS architecture have focused on reducing turn around time, memory optimization, and direct to tool data path connections. Future development work for MAGIC starts with a solid foundation. The following illustration represents the current state of the art in data path engineering with CATS for the NuFlare EBM5000 Mask Writer (figure 11). Consisting of an off-line and on-tool component, this "Data Exploder" type architecture delivers high speed with low file transfer latency and would be somewhat representative of a similar configuration used in the MAGIC program.

Specific to the "MAGIC" program the figure 12 illustrates the basic concept of the architecture planned for the data path for both Mapper and IMS nanofabrication systems. Creating this type of "integrated data path" is expected to provide the necessary performance required for ML2 tools. Additionally, key focus areas for the data prep work package are listed.



- CATS VSB Exploders
- High Speed Direct Data Path
- 200GB/Hr Demonstrated
- Scalable to Terabytes/Hr
- Built in Data Verification
- High Speed FTP Capable

Figure 11 : CATS Mask Writer "Exploder" – EBM5000 with direct Connect and high Speed Data Path



MAGIC Project – Data Prep Focus Areas

1. Data Prep Flow/Architecture
2. Performance Requirements
3. Design to Wafer Data Format
4. Off-Tool/On-Tool Data Path
5. Proximity Correction Integration

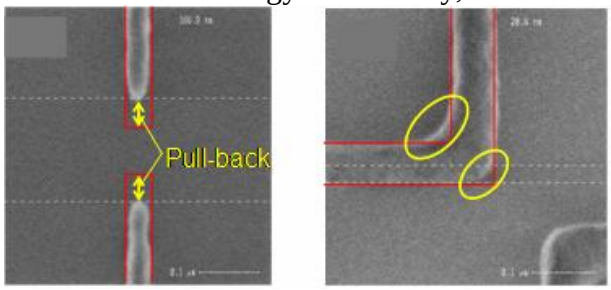
Figure 12 : Future architecture overview

3.2.2 The options for E-Beam proximity solutions

In the frame of the "MAGIC" project, the development proposed for Electron Beam Proximity effects Correction (EBPC) for ML2 writers has to meet the high accuracy requirements of the ITRS and to consider the specific configurations of the multi beam systems. Due to the multi beam writing strategy a smaller dose range (difference between lowest and highest writable doses) is expected.

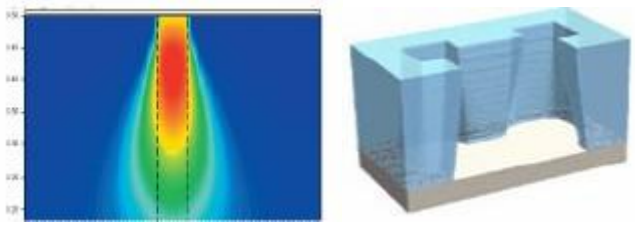
Current dose modulation approach already shows several limitations for the sub-65nm nodes with single variable shaped beam[5]. It has been shown that at a higher resolution even with an optimized proximity effects correction model there are several limitations with a simple dose modulation correction like loss of linearity, line end shortening, corner rounding, biasing. Figure 13 shows 2 examples of patterning degradation on line end control and corner rounding.

Based on this experience, existing EBPC software solutions are estimated insufficient for sub-32nm node technology. In this way, a new dose modulation approach is mandatory and the future ML2



A B

Figure 13 : Examples of line end shortening (A) and corner rounding (B)



A B

Figure 14:
A. Energy deposition in 500 nm resist, 50nm opening; 20 kV; 50000 electron trajectories
B. Example of resist modelling

correction package needs to contain a new correction approach that includes resist process effects e.g. micro-loading, pre- and post-exposure processes, bake and development... This also requires a new flow for exposure model calibration. The aim of this work package will be to develop software solutions, which ensure the control of the electron beam proximity effects. First, specifications requested by the two different accelerating voltage options will be defined through demo work performed on proof of lithography systems developed by MAPPER and IMS Nanofabrication. In parallel, a review of the EBPC tools will be performed, in order to evaluate which software platform for the different correction solutions can address the ML2 EBPC needs. At a later stage, development work through partnerships will be performed to support the availability of a complete set of EBPC tools for the ML2 technology. The covered fields of activity will be the definition of a fast methodology for fast extraction of resist models (PEC functions), the development of EBPC solutions based on dose modulation and geometrical corrections. All the qualification work will be performed on demonstrator products realized in the frame of the process integration workpackage.

In addition, important simulation activities are planned to be developed inside the "MAGIC" project covering heating, charging effect, resist model building and anticipation of process. One of the objectives of this work will be the development of a robust predictive simulation tool optimising the time to get the appropriate EBPC model (figure 14). A close collaboration between Synopsys and the end-users partners will be first to identify the requirements and perform the developments for a robust electron beam lithography simulation tool based on aerial image and resist image for both low and high energies. The improvement points of the simulation tool will be extended to the etch modelling. Another functionality of the e-beam lithography simulation tool will be the possibility to anticipate the validation of dose modulation models to be used for production.

Finally, the local heating and charging effects on electron beam writing quality will be also studied. A software block dealing with these effects will be potentially implemented in this future simulation tool.

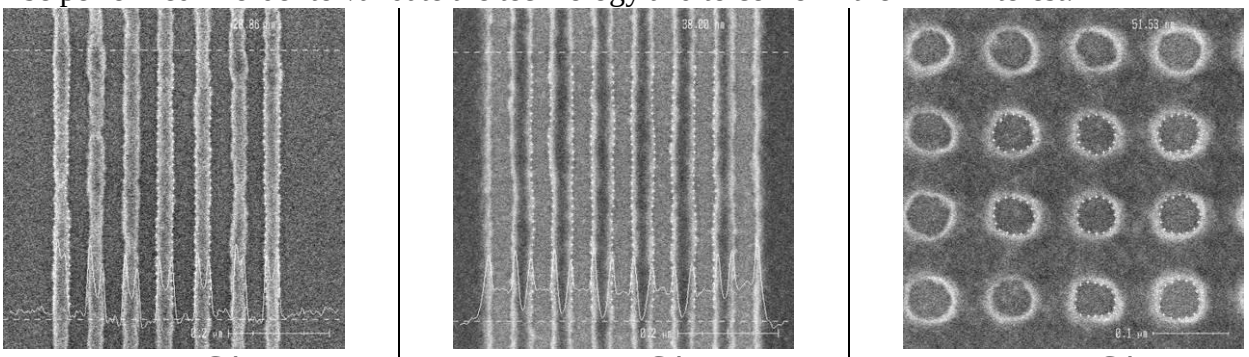
3.2.4 The process development concern

The last field of work in the frame of "MAGIC" program is relative to the validation in production environment of the two ML2 technologies (low and high energy). This effort is sprayed in 5 tasks described afterwards.

The first objective of the activity will be to develop resist processes for tool evaluation and the realization of CMOS demonstrations in relationships with resist suppliers. This task is leaded by IMS-Chip. The first year is dedicated to the set up of the 45nm half-pitch resist process based on Chemically Amplified Resists (CAR) for the evaluation and the follow-up of the first 300mm platforms end 2008. Then, with the increase of the platform functionalities, resist processes are expected to be pushed up to 32nm technology. Figure 15 shows the actual performances of CAR resist obtained on last generation shaped beam platform, VISTEC SB3054DW. As shown on this figure, resolution capability is already well aligned with 45nm node and already close to 32nm. Finally, the third year will be more focused on a long term effort regarding next generation node below 22nm.

In parallel, the work will regularly evaluate the progress of the two technologies MAPPER and IMS-Nanofabrication during the program. This assessment will be done in respect to criteria aligned on ITRS requirements. For that, the effort will be performed in parallel into two dedicated tasks; one for low energy tool evaluation, driven by CEA-LETI and the other one for high energy driven by Qimonda/Fraunhofer-CNT. The work objectives will be identical: check tool performances and improvements, reliability, user interface and usage of each technology. In parallel, software implementation for data preparation and EBPC will be tested and validated on real cases. A task

dedicated to metrology and leaded by KLA-TENCOR will take parts all through the project. The aim of this work is focused on the development of metrology solution for overlay and butting controls which are key parameters of process quality. Finally, electrical demonstrations of DRAM or ASIC circuits will be performed in order to validate the technology and to conform the ML2 interest.



Negative CAR
Dense L/S: 30nm pitch 70nm

Positive CAR
Dense L/S: 40nm pitch 80nm

Positive-CAR
Dense CH: 50nm pitch 100nm

Figure 15 : CAR process performances obtained on last generation shaped beam system (VISTEC SB3054DW)

4. CONCLUSIONS

This European initiative is important to push the massive parallel e-beam lithography option. During 3 years, this support will highlight these technologies and build the necessary infrastructure for its future industrial use. This project is ambitious as it intends to develop future alpha platform and to show their potential use in industry-like environment at the end of the second year. This first support from institutions is essential to initiate the take off of this technology. The presence of key and worldwide partners inside the consortium is also a positive signal showing the intention of each one to ensure the success of this project. Nevertheless, to emphasize the dynamic and to secure the availability of a solution on time, the support for the ML2 lithography needs to reach larger supports from industry represented by end users and equipment manufacturers is also essential.

5. REFERENCES

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