

Designing a Governor Policy for Energy Saving and Heat Control in Frequency-Scaling Green Routers

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Abstract— Energy costs for telecommunications networks are mainly due to the consumption of both devices and cooling facilities. For this reason the target of this paper is to propose an analytical discrete-time Markov model that allows green router designers to both evaluate performance of temperature-constrained green routers and design Governor policies to achieve the best trade-off between quality of service and energy saving in respect of a given target on the working temperature. The proposed model is applied to a case study to show how it can be used to the above purposes.

Keywords; *Green Routers, Heat Dissipation, Power Consumption, Performance Evaluation, Markov model, NetFPGA.*

I. INTRODUCTION

Today's most telecommunications networks are often provisioned for worst-case or busy-hour load, and this load typically exceeds their long-term utilization by a wide margin; moreover, as shown in [1], current network nodes have a power consumption that is practically constant and does not depend on the actual traffic load they face. The implication of these factors is that most of the energy consumed in networks today is wasted.

A non-marginal side effect of high-energy dissipation is the increment of the temperature of the places where network devices reside, with a consequent further waste of energy used by cooling machines to maintain the temperature of the local environment constant.

The steadily rising energy cost and the need to reduce the global greenhouse gas emission make this occurrence unsustainable: today, 37% of the total ICT emissions are due to telecommunications companies infrastructures and devices [2]. For this reason, addressing energy efficiency challenges in wireline networks is receiving considerable attention in the literature today [3-4]; moreover many research projects have been started on this topic (see for example [5-7]). Thus, some novel hardware devices, so-called "green routers", are expected in the near future to allow to enter different power states according to the input traffic. A lot of work was done in the past, focusing on the definition of power management techniques [4]. The energy aware technique to be used in a green router depends on a number of factors, including the role of the router in the network, the profile of incoming traffic, the hardware complexity and the related costs with respect to the energy we can potentially save and the QoS we want to guarantee to the users.

Now, let us note that the introduction of green management techniques to make network routers green has an important

consequence on the decrease of working temperature of the hardware device. As known, temperature is one of the major factors which must be considered and addressed in the design and the manufacture of electronic devices, and specifically routers, since operating at higher temperature degrades system reliability, causes performance degradation and leads to higher cooling and packaging costs.

Moreover, "smaller and faster" are the chief demands driving today's electronic design. These issues translate into high power densities, higher operating temperatures and lower circuit reliability. Therefore, greening a router can be considered as a leveraging approach to move towards this direction. In other words, reduction of the average temperature in green routers due to the application of algorithms aimed at reducing energy consumption will allow designers to modify hardware, reducing its size and the size of the passive and active cooling systems, since a package designed for the worst case is excessive. However, the above hardware modifications can make again router circuits heat beyond their designed thermal limits. For this reason, the working range of temperature becomes again an important issue in green router design.

With all this in mind, the paper target is to extend the router governor policy and the analytical model of a green router introduced in [8] with given requirements in terms of temperature, QoS and energy consumption. Such a governor is in charge to set the current clock frequency. Besides, the analytical model allows the designer to determine in advance if the device will operate within recommended thermal ranges when the green router governor uses a given energy saving policy. In addition, the same model can be used to evaluate the achieved amount of energy saving.

The proposed model is a multi-dimensional discrete-time Markov model. More specifically, in this work we extend the router governor policy introduced in [8] in order to support a generic number of frequencies (in [8] only two frequencies are considered), and consequently we propose a new model to capture it.

The paper is structured as follows. Section II describes the considered green router and introduces the proposed policy. Section III describes the Markov model of the considered system. Section IV shows the case study of a NetFPGA reference router in order to demonstrate the applicability of the model. Section V shows all the results of our analysis. Finally, Section VI ends the paper with some authors' conclusions and future directions.

II. REFERENCE ARCHITECTURE AND PROPOSED POLICY

In this paper we consider a router that implements frequency scaling capabilities to save energy when the input traffic load is low. Frequency scaling, a capability implemented by many routers today, is the possibility of changing the core clock frequency in a set of different values to dynamically scale the energy consumption of the device. The base problem of this approach is that, if on the one hand the device power consumption can be reduced using lower clock frequencies with respect to the higher one, on the other hand such a decision can deteriorate the router performance. For example, in the NetFPGA Reference Router [8] we consider here as a reference platform, clock frequency switches cause a block interval of 2 ms, and therefore all the incoming packets during this interval are lost. Other routers, although with different hardware architecture and implementation, behave at the same way: at each clock frequency variation they present a QoS degradation, in terms of either loss probability, delay and energy consumption peaks. From this perspective, the approach proposed in this paper, which aims at finding the best trade-off between energy efficiency and QoS, is very general since it can be used to minimize such a cost by only changing the particular target parameter.

In order to manage frequency switches maintaining QoS acceptable while decreasing energy consumption, we introduced a Router Governor, that is an entity, which decides the router policy to be adopted to change the router clock frequency. In the following, QoS is defined by the following parameters:

- Probability of packet loss during frequency switching intervals;
- Energy saving gain;
- Mean temperature on the CPU surface.

Energy saving gain is defined as follows:

$$\rho = \frac{P_{MAX} - P_{MEAN}}{P_{MAX}} \cdot 100\% \quad (1)$$

where P_{MAX} is the power consumed if no saving policy is applied, while P_{MEAN} is the mean value of the consumed power when the Router Governor works to save energy. Let us note that other traditional QoS parameters characterizing the router, like for example loss probability and queueing delay, are not considered here because they are not altered by the presence of our Router Governor. More specifically, the Router Governor has the following tasks:

1. Avoiding that the probability of packet loss during clock frequency switches exceeds a given threshold;
2. Maximizing the energy saving percentage while respecting the previous item.
3. Monitoring the mean temperature on the CPU surface.

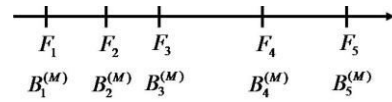
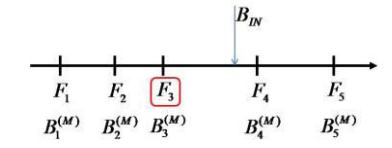
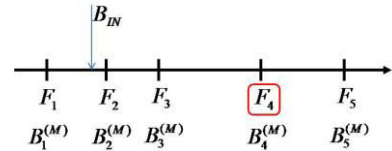


Fig. 1. Set of clock frequencies implemented by the Router, and relative maximum supported bitrates.



(a) Example for rule 1.



(b) Example for rule 2.

Fig. 2. Set of clock frequency implemented by the Router, and relative maximum supported bitrates.

Let Φ be the set of clock frequencies supported by the router CPU, and F_i the i -th clock frequency, sorted in such a way that $F_i < F_{i+1}$. Let us indicate the maximum bitrate that can be supported with no loss when the CPU is working at the frequency F_i as $B_i^{(M)}$. These values are sketched in Fig. 1. Let us now define the Router Governor policy:

- **RULE 1:** if the clock frequency was previously set to F_i (see Fig. 2a, where $i = 3$) and the current input bit rate B_{IN} is greater than $B_i^{(M)}$ ($B_3^{(M)}$ in Fig. 2a), then the clock frequency is switched to the minimum clock frequency belonging to Φ that does not cause losses (F_4 in Fig. 2a);
- **RULE 2:** if the clock frequency was previously set to F_i (see Fig. 2b where $i = 4$) and the current input bit rate B_{IN} is lower than $B_{i-1}^{(M)}$ (lower than $B_3^{(M)}$ in Fig. 2b), then the clock frequency can be switched down to a value F_k less than F_i , but not less than the minimum clock frequency belonging to Φ that does not cause losses (i.e. F_2 in Fig. 2b). However, since a frequency switch causes a QoS deterioration, this is done with a probability $p_G(B_{IN}, i, k)$ which is adaptive to the current input bit rate B_{IN} : the greater the distance between B_{IN} and the maximum bit rate that can be supported by the new clock frequency, the lower the risk of a new frequency switch necessity. To this purpose, referring to the example illustrated in Fig. 2b, the switching probability is defined as follows:

- the new clock frequency is set to F_2 with a probability: $p_G(B_{IN}, 4, 2) = \delta \frac{B_2^{(M)} - B_{IN}}{B_4^{(M)} - B_{IN}}$;

- if the result of the previous draw was negative, and so the clock frequency was not set to F_2 , the new clock frequency is set to F_3 with a probability:

$$p_G(B_{IN}, 4, 3) = \delta \frac{B_3^{(M)} - B_{IN}}{B_4^{(M)} - B_{IN}};$$

- if the clock frequency is not set to F_3 , the clock frequency remains F_4 .

Generally speaking, if the current clock frequency is F_i and the input bit rate B_{IN} is lower than $B_{i-1}^{(M)}$, the clock frequency can be changed in the set $\{F_j, \dots, F_i\}$, where F_j is the minimum clock frequency not causing loss. More specifically, the clock frequency is set to F_k , with $k \in [j, i]$, with a probability:

$$p_G(B_{IN}, i, k) = \prod_{h=j}^{k-1} \left(1 - \delta \frac{B_h^{(M)} - B_{IN}}{B_i^{(M)} - B_{IN}} \right) \cdot \begin{cases} \delta \frac{B_k^{(M)} - B_{IN}}{B_i^{(M)} - B_{IN}} & \text{if } k < i \\ 1 & \text{if } k = i \end{cases} \quad (2)$$

The term $\delta \in [0, 1]$ allows the designer to make clock frequency switches more rare. It is easy to argue that its value plays a very important role in the router performance in terms of loss probability and energy saving. A side but important effect of the Router Governor policy is on the router CPU surface temperature that should not exceed a given threshold. The design of the parameter δ will be assisted by the analytical model that will be described in Section III.

III. MARKOV MODEL

In this section we define a discrete-time model of the system described so far, in order to capture the behavior of both the frequency clock process and the surface temperature of the CPU residing on the considered router. Since it depends on the input traffic bit rate, we define the Markov model state as $S^{(z)}(n) = (S^{(c)}(n), S^{(t)}(n), S^{(r)}(n), S^{(s)}(n))$, where:

- $S^{(c)}(n) \in \mathfrak{Z}^{(c)}$ is the clock frequency process at the generic slot n ;
- $S^{(t)}(n) \in \mathfrak{Z}^{(t)}$ represents the quantized input traffic bit rate at the generic slot n ;
- $S^{(r)}(n) \in \mathfrak{Z}^{(r)}$ is the temperature at the generic slot n ;
- $S^{(s)}(n) \in \mathfrak{Z}^{(s)} = \{0, 1\}$ is the indicator variable of a switch at the generic slot n : $S^{(s)}(n) = 1$ if, in the slot n , the router is switching its clock frequency.

The set $\mathfrak{Z}^{(t)}$ contains the considered quantized input traffic values. The set $\mathfrak{Z}^{(r)}$ is constituted by a set of quantized values the temperature can assume when the router works.

Now, in order to define the system model, we have to decide the slot duration and the time diagram of each slot. As far as the slot duration is concerned, we use the interval

between two consecutive observations of the input bit rate, and we will indicate it as Δ . In our case we will set $\Delta = 2 \mu\text{s}$. In order to define the model time diagram, we consider two generic states: $s_{\Sigma 1} = (s_{c1}, s_{t1}, s_{r1}, s_{s1})$ in the slot n , and $s_{\Sigma 2} = (s_{c2}, s_{t2}, s_{r2}, s_{s2})$ in the slot $n+1$. We assume the following event sequence:

1. The first action at the beginning of the slot $n+1$ is the evaluation of the new value of the input traffic bit rate. This value is obtained sampling the bit rate values smoothed with an EWMA filter with a time constant equal to the time slot.
2. Then, according to the new value of the input traffic bit rate, the Governor decides the clock frequency for the new slot. As said so far, a clock frequency modification determines that the router will remain frozen for a number of slots to make the clock frequency switch. All these slots will be characterized by the state variable $S^{(s)}(n) = 1$. Let \bar{T}_F be the duration of this period.
3. Then, at the end of the slot $n+1$, the system state variables are observed.

Now we can define the generic element of the state transition probability matrix as follows:

$$Q_{[s_{\Sigma 1}, s_{\Sigma 2}]}^{(z)} = \text{Prob}\{S^{(z)}(n+1) = s_{\Sigma 2} \mid S^{(z)}(n) = s_{\Sigma 1}\} = Q_{[s_{t1}, s_{t2}]}^{(t)} \cdot \eta_{[s_{c1}, s_{c2}]}^{(c)}(s_{t2}) \cdot Q_{[s_{r1}, s_{r2}]}^{(r)}(s_{c2}, s_{t2}) \cdot Q_{[s_{s1}, s_{s2}]}^{(s)}(s_{c1}, s_{c2}) \quad (3)$$

where:

- $Q_{[s_{c1}, s_{c2}]}^{(s)}$ is the transition probability of the clock switch indicator variable. It is defined as follows:

$$Q_{[s_{c1}, s_{c2}]}^{(s)}(s_{c1}, s_{c2}) = \begin{cases} 1 & \text{if } (s_{c2} \neq s_{c1}, s_{s1} = 0, s_{s2} = 1) \\ 1 & \text{if } (s_{c2} = s_{c1}, s_{s1} = 0, s_{s2} = 0) \\ \Delta / \bar{T}_F & \text{if } (s_{s1} = 1, s_{s2} = 0) \\ 1 - \Delta / \bar{T}_F & \text{if } (s_{s1} = 1, s_{s2} = 1) \\ 0 & \text{otherwise} \end{cases} \quad (4)$$

where \bar{T}_F is the mean duration of the clock frequency switching period. Thus the term Δ / \bar{T}_F is the probability that the router leaves the switching period.

- $\eta_{[s_{c1}, s_{c2}]}^{(c)}(s_{t2})$ gives the probability of a clock frequency switch depending on the clock frequency switching law used by the Governor to decide the clock according to the input traffic bit rate. It is set to 0 when it is not possible that the Governor sets the value of s_{c2} according to the input traffic value s_{t2} and the current clock frequency s_{c1} . According to the Governor policy illustrated in Section II, it is defined as follows:

$$\eta_{[s_{c1}, s_{c2}]}^{(c)}(s_{t2}) = \begin{cases} 1 & \text{if } \phi(s_{t2}) > s_{c1} \\ & \text{and } s_{c2} = \phi(s_{t2}) \\ 1 & \text{if } s_{c1} = s_{c2} = \phi(s_{t2}) \\ p_G(s_{t2}, s_{c1}, s_{c2}) & \text{if } \phi(s_{t2}) < s_{c1} \\ & \text{and } \phi(s_{t2}) \leq s_{c2} \leq s_{c1} \\ 0 & \text{otherwise} \end{cases} \quad (5)$$

The term $p_c(s_{I_2}, s_{C_1}, s_{C_2})$ is the frequency clock switching probability defined in (2). As said in Section II, it is adaptive with the current value of the input bit rate. The design of this function will be discussed in Section V.

- $Q^{(T)}$ is the state transition probability matrix for the quantized input traffic. It is an input of the problem, because it characterizes the traffic crossing the router;
- $Q^{(T)}(s_{C_2}, s_{I_2})$ is the state transition probability of the temperature. It will be calculated below.

Let us indicate the derivative of the time-variant temperature behavior when the system state is s_{Σ_1} as $\gamma(s_{C_2}, s_{I_2}, s_{T_1})$. Therefore the temperature value in the slot $n+1$ is calculated from the value in the slot n as follows:

$$T_2 = s_{T_1} + \gamma(s_{C_2}, s_{I_2}, s_{T_1}) \cdot \Delta \quad (6)$$

Since T_2 may not belong to the set $\mathfrak{S}^{(T)}$, the new state of the temperature, s_{T_2} , will be one of the two most adjacent states to T_2 belonging to this set. Let us indicate the most adjacent state with a temperature greater than T_2 as $\lceil T_2 \rceil$, and the most adjacent state with a temperature lower than T_2 as $\lfloor T_2 \rfloor$. The new temperature state s_{T_2} will be either $s_{T_2} = \lceil T_2 \rceil$ or $s_{T_2} = \lfloor T_2 \rfloor$ with a probability dependent on the distance between the real temperature calculated as in (6) and the temperature associated to the adjacent states $\lceil T_2 \rceil$ and $\lfloor T_2 \rfloor$.

More specifically:

$$S^{(T)}(n+1) = \begin{cases} \lceil T_2 \rceil & \text{with prob: } (T_2 - \lfloor T_2 \rfloor) / (\lceil T_2 \rceil - \lfloor T_2 \rfloor) \\ \lfloor T_2 \rfloor & \text{with prob: } (\lceil T_2 \rceil - T_2) / (\lceil T_2 \rceil - \lfloor T_2 \rfloor) \end{cases} \quad (7)$$

Now, from the matrix $Q^{(\Sigma)}$ we can derive the system steady-state probability array $\underline{\pi}^{(\Sigma)}$ by solving the following system:

$$\begin{cases} \underline{\pi}^{(\Sigma)} Q^{(\Sigma)} = \underline{\pi}^{(\Sigma)} \\ \underline{\pi}^{(\Sigma)} \cdot \underline{1}^T = 1 \end{cases} \quad (8)$$

where $\underline{1}^T$ is a column array with all the elements equal to one. Its generic element, $\pi_{[s_{\Sigma}]}^{(\Sigma)}$, is the steady-state probability of the state $s_{\Sigma} = (s_c, s_I, s_T, s_S)$.

Now we derive the main important QoS parameters, with the aim of both evaluating router performance and supporting Router Governor design.

First let us calculate the probability of loss occurring during the switching periods. It is defined as:

$$P^{(Loss)} = \lim_{m \rightarrow +\infty} \frac{L(m)}{V(m)} = \frac{\bar{L}}{\bar{V}} \quad (9)$$

where $L(m)$ and $V(m)$ are the cumulative number of lost bits and arrived bits in m consecutive slots. The term \bar{V} is the mean value of arrived bits per slot, and can be calculated from the input bit rate traffic statistics as follows:

$$\bar{V} = \sum_{s_{\Sigma} \in \mathfrak{S}^{(\Sigma)}} s_I \pi_{[s_{\Sigma}]}^{(\Sigma)} \quad (10)$$

The term \bar{L} represents the mean value of bits lost per slot. Since in our case bits are lost only during clock frequency switches, we have:

$$\bar{L} = \sum_{s_c \in \mathfrak{S}^{(C)}} \sum_{s_I \in \mathfrak{S}^{(I)}} \sum_{s_T \in \mathfrak{S}^{(T)}} s_I \pi_{[s_c, s_I, s_T, 1]}^{(\Sigma)} \quad (11)$$

The power saving percentage during periods when the router can reduce its clock frequency can be calculated as in (1), where P_{MEAN} is the mean value of the consumed power when the input bit rate is less than or equal to 2 Gbit/s. It can be calculated as follows:

$$P_{MEAN}(s_I) = \sum_{\forall s_c \in \mathfrak{S}^{(C)}} \Psi(s_c, s_I) \cdot \sum_{\forall s_T \in \mathfrak{S}^{(T)}} \sum_{\forall s_S \in \mathfrak{S}^{(S)}} \pi_{[s_c, s_I, s_T, s_S]}^{(\Sigma)} \quad (12)$$

The term $\Psi(s_c, s_I)$ is a model input, and represents the power consumed when the router is loaded with an input traffic bit rate of s_I and the clock frequency is s_c .

Let us now derive the marginal steady-state probability array for the temperature process when the input bit rate is $B_{IN} = s_I$:

$$\pi_{[s_T]}^{(T|s_I)} = \frac{\sum_{\forall s_c \in \mathfrak{S}^{(C)}} \sum_{\forall s_S \in \mathfrak{S}^{(S)}} \pi_{[s_c, s_I, s_T, s_S]}^{(\Sigma)}}{\sum_{\forall s_c \in \mathfrak{S}^{(C)}} \sum_{\forall s_T \in \mathfrak{S}^{(T)}} \sum_{\forall s_S \in \mathfrak{S}^{(S)}} \pi_{[s_c, s_I, s_T, s_S]}^{(\Sigma)}} \quad (13)$$

Finally, from the probability array in (13) we can calculate the mean temperature value:

$$E\{T | s_I\} = \sum_{\forall s_T \in \mathfrak{S}^{(T)}} s_T \cdot \pi_{[s_T]}^{(T|s_I)} \quad (14)$$

IV. CASE STUDY

In this section we will provide a case study for our model. In particular, starting from a set of measurements achieved for a NetFPGA platform in a previous work of the same authors [8], we extended them in order to provide a complete case study of a device with a higher number of clock frequencies. More specifically, as regards the consumed power, we use the model that allows us to calculate the power consumed when the router works at a clock frequency f_c and is loaded by an input traffic bit rate B_{IN} :

$$\Psi(f_c, B_{IN}) = P_c(f_c) + K P_e(f_c) + N_I(B_{IN}) \cdot E_p(f_c) + R_I(B_{IN}) \cdot E_r(f_c) + R_O E_t(f_c) \quad (15)$$

The term $P_c(f_c)$ is the constant baseline power consumption of the NetFPGA card (without any Ethernet ports connected); $P_e(f_c)$ is the power consumed by each Ethernet port (without any traffic flowing); $E_p(f_c)$ is the energy required to process each packet (parsing, routing lookup, etc.); $E_r(f_c)$ is the energy required to receive, process and store a byte on the ingress Ethernet interface; $E_t(f_c)$ is the energy required to store, process and send a byte on the egress Ethernet interface; K is the number of Ethernet ports connected (1 to 4); $N_I(B_{IN})$ is the input traffic bitrate to the NetFPGA card in packets-per-second (pps); $R_I(B_{IN})$ is the input rate to the NetFPGA card

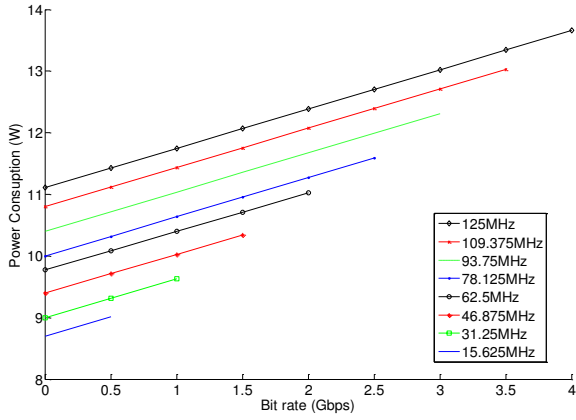


Fig. 3. Power consumption model for a router with 8 clock frequencies.

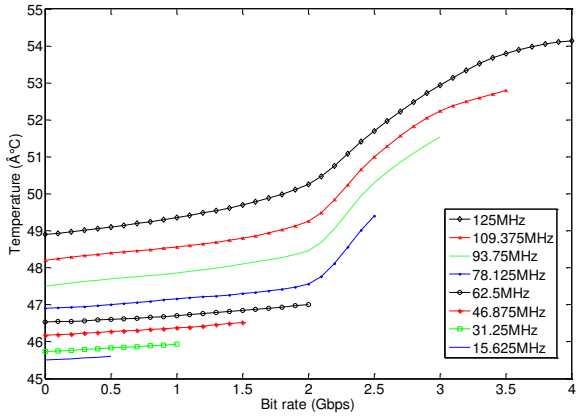


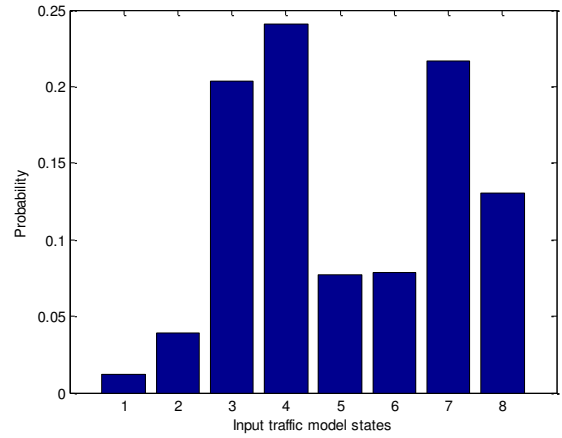
Fig. 4. Temperature model for a generic router with 8 clock frequencies.

in bytes-per-second; $R_o(B_{IN})$ is the output rate from the NetFPGA card in bytes-per-second.

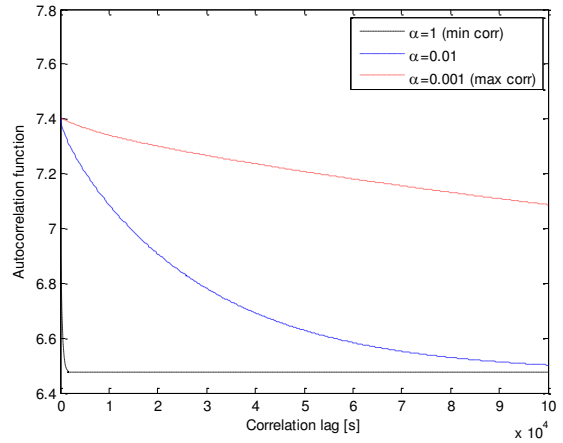
We have extended the set of measurements presented in [8] considering a router supporting eight different clock frequencies (125 MHz, 109.375 MHz, 93.75 MHz, 78.125 MHz, 62.5 MHz, 46.875 MHz, 31.25 MHz, 15.625 MHz). Results achieved by the power model in (15) are shown in Fig. 3.

As far as the CPU surface temperature data are concerned, we extended measurements results presented in [8] with the curves shown in Fig. 4, showing the steady-state values of the temperature when the router CPU works at a clock frequency f_c and is loaded by an input traffic bit rate B_{IN} . Each curve in Figs. 3 and 4 covers only the supported bit rate for each specific CPU clock frequency (i.e. the maximum supported input bit rate without incurring in any packet loss when the system works at 15.652 MHz is 0.5 Gbps, etc ...).

The derivative of the time-variant temperature behavior when the current temperature is T_{curr} , $\gamma(s_{c2}, s_{i2}, s_{T1})$, are a large set of data and are available at [9].



(a) Probability density function.



(b) Autocorrelation function.

Fig. 5. Input traffic first- and second-order statistics.

INFERIOR PSEUDO-DIAGONAL		MAIN DIAGONAL		SUPERIOR PSEUDO-DIAGONAL	
Pos	Value	Pos	Value	Pos	Value
		(1,1)	9.9990e-001	(1,2)	1.0000e-004
(2,1)	3.1569e-005	(2,2)	9.9993e-001	(2,3)	3.5098e-005
(3,2)	6.7811e-006	(3,3)	9.9994e-001	(3,4)	4.8774e-005
(4,3)	4.1255e-005	(4,4)	9.9995e-001	(4,5)	6.3636e-006
(5,4)	1.9848e-005	(5,5)	9.9994e-001	(5,6)	3.8975e-005
(6,5)	3.8314e-005	(6,6)	9.9992e-001	(6,7)	3.8609e-005
(7,6)	1.3970e-005	(7,7)	9.9990e-001	(7,8)	8.6030e-005
(8,7)	1.4286e-004	(8,8)	9.9986e-001		

Table I. Non-null elements of the Input traffic transition probability matrix.

V. MODEL APPLICATION

In this section we apply the model described so far to both evaluate performance of a router with a Router Governor implementing the proposed green clock frequency management policy, and design the δ parameter used in the switching probability $p_G(s_{i2}, s_{c1}, s_{c2})$ by the Governor to

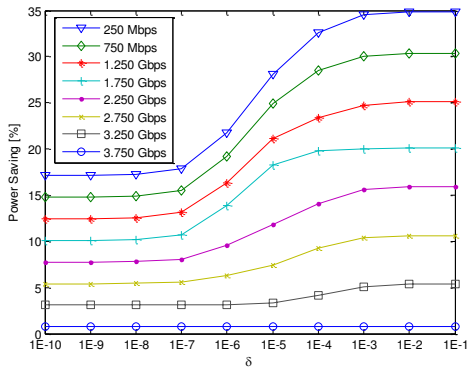


Fig. 6. Power saving for different values of input bit rates.

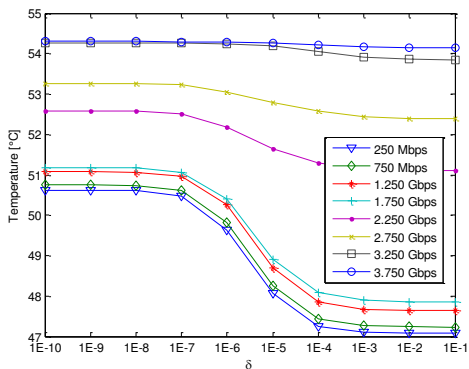


Fig. 7. Mean temperature for different values of input bit rates.

decide whether to switch clock frequency or not according to the current bit rate, B_{IN} .

Quantizing the traffic in eight different bit rate levels, ranging from 0.4 Gbit/s to 3.9 Gbit/s with steps of 0.5 Gbit/s, we measured its first- and second-order statistics in terms of probability density function (pdf) and autocorrelation function (acf), which are represented in Fig. 5. More specifically, the measured autocorrelation function is the one labeled with $\alpha = 1$. Then, solving an inverse eigenvalue problem [10], we derived the input traffic Markov model characterized by the transition probability matrix $Q^{(t)}$, which is a tri-diagonal matrix whose non-null elements are listed in Table I. The considered traffic has a mean value of 2.54 Gbit/s and a standard deviation of 0.965 Gbit/s. Moreover, in order to analyze the impact of the traffic correlation on the achieved performance, we considered two more cases of input traffic, characterized by transition probability matrices derived from the one listed in Table I by multiplying the terms of the pseudo-diagonals by a coefficient $\alpha = 10^{-2}$ and $\alpha = 10^{-3}$. The terms of the main diagonals are then calculated such that the sum of each row is equal to one. In this way first-order statistics remained unchanged, while traffic becomes more correlated for decreasing values of α . The autocorrelation functions evaluated for the two new cases are shown in the same Fig. 5b.

Fig. 6 shows the power saving gain achieved during periods with different values of input bit rates ranging between 250 Mbit/s and 3.750 Gbit/s. The plots are calculated through (12) against the switching parameter δ . The reader can notice that, as expected, for higher values of δ , the power saving gain increases because δ influences the clock frequency switching probability. Moreover, in the case of low input bit rate the power saving gain of the system is more sensitive to the value of δ used into the policy, while it is insensitive in the opposite case. This behavior is due to the fact that when δ takes high values the clock frequency strictly follows the traffic and the CPU is set to lower frequency more often.

Fig. 7 shows the mean temperature for different values of input bit rates; it is possible to notice that the higher the value of δ the lower the heat dissipation of the CPU surface. Also in that figure, we can notice that in the case of low input bit rate the temperature of the system is more influenced by the selected value of δ .

Fig. 8 shows the loss probability for the three different considered cases of traffic correlations, obtained with three different values of α . It is clear that the higher the correlation of the input traffic ($\alpha = 0.001$) the lower the loss probability. This is due to the fact that high-correlated traffic requires less clock frequency switches.

Figs. 9 and 10 respectively show the power saving gain and the temperature against the loss probability. They have been obtained by calculating the three above performance parameters as functions of δ , and then putting them together by associating the values achieved for the same value of δ . From these figures it is possible to see that lower values of loss probability correspond to low power saving gain and, at the same time, to high temperature. Moreover, Figs. 6-10 allow the designer to choose the more suitable value of δ . Moreover, these figures can be used to support the design of the system. For example, we can derive the maximum power saving that can be obtained for the presented case study when we accept a given loss probability (Fig. 9) and the corresponding mean temperature (Fig. 10). The higher the required power saving gain, or the lower the required mean temperature, the higher the loss probability we have to accept.

VI. CONCLUSIONS

In this paper we have proposed a new governor policy for green routers using frequency scaling to save energy. The policy allows to limit the performance worsening due to frequent clock frequency switches. In order to design the frequency switching probability, we have defined an analytical discrete-time Markov model. This model can also be used by green router designers to control the statistics of the temperature on the CPU surface, for given input traffic first- and second-order statistics. Moreover, the model allows the manufacturers to evaluate the energy saving gain which is possible to obtain. In the case study we have shown how the model can be used to design the Router Governor parameters to achieve the target of maintaining the mean temperature below a given threshold and achieve a certain amount of power saving gain for a given threshold on the loss probability. The future directions that we will pursue are related to an extension of the

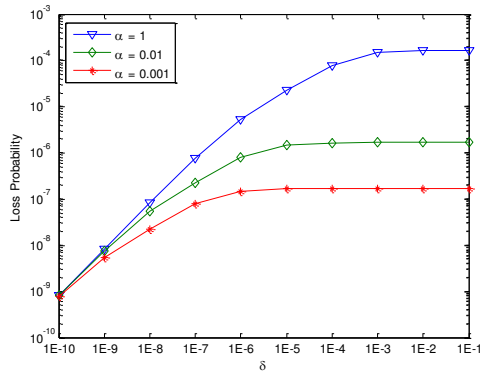


Fig. 8. Loss probability for different input traffic correlation.

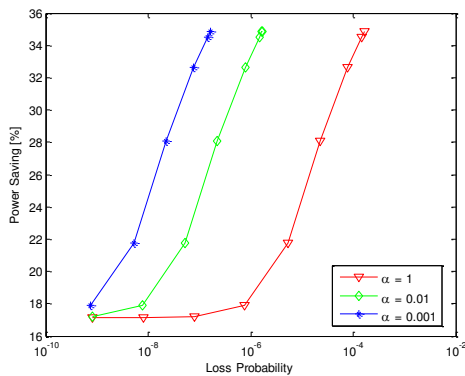


Fig. 9. Power saving gain vs. loss probability.

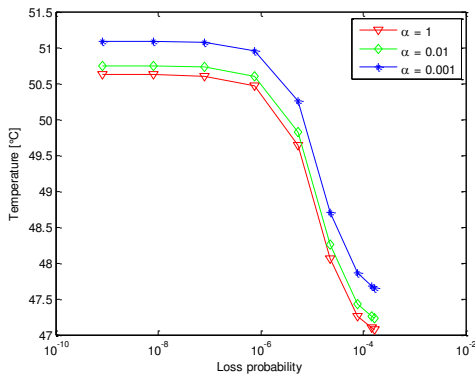


Fig. 10. Temperature vs. loss probability.

model to capture both the dependence of the power on the environmental temperature, and a Governor policy based on the behavior of input and output queues. Moreover, we will apply the model to find the most appropriate number of clock frequencies, as the best tradeoff between the QoS deterioration caused by an increasing of the number of possible clock frequencies, and the energy saving gain improvement given by a router whose clock frequency is able to closely follow the traffic behavior.

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