Phase change materials in non-volatile storage

After revolutionizing the technology of optical data storage, phase change materials are being adopted in non-volatile semiconductor memories. Their success in electronic storage is mostly due to the unique properties of the amorphous state where carrier transport phenomena and thermally-induced phase change cooperate to enable high-speed, low-voltage operation and stable data retention possible within the same material. This paper reviews the key physical properties that make this phase so special, the quantitative framework of cell performance, and the future perspectives of phase-change memory devices at the deep nanoscale.

Daniele Ielmini[1] and Andrea L. Lacaita[1,2,*]

[1]Dipartimento di Elettronica e Informazione and IU.NET, Politecnico di Milano, Milano, Italy

[2]IFN-CNR, Milano, Italy

**E-mail: andrea.lacaita@ polimi.it*

Over the last several decades, processors have improved much faster than storage components[1]. Memory has therefore become the most frequent limiting factor of a system's performance, while the celebrated convergence of consumer, computer, and communication electronics has exponentially increased the need for increased memory size. In the future, additional issues will arise as a multitude of heterogeneous systems will spread integrated intelligence to all manner of products. Pressure will certainly grow in cost and performance optimization, as well as flexibility and integration requirements. From this perspective, novel solutions provided by emerging memory technologies are expected to become essential to meet the cost, bandwidth, and power efficiency requirements of future memory systems.

Phase change memory (PCM) is now the most mature of the emerging memory technologies. Conceived during the golden age of semiconductor research[2,3], PCMs entered the industrial development stage only at the beginning of the last decade, when the development of standard, workhorse technologies had started to slow down[4-6]. After demonstrating that large-scale manufacture was possible, PCM products are entering volume production. In the short term, PCM is expected to replace NOR Flash and some embedded memories. Due to their high speed and remarkable endurance, PCMs may also back-up low-cost NAND Flash that is still scaling below 20 nm, even if with serious performance degradation[1,7]. PCMs are also being considered as a potential disruptive solution for storage-class memory (SCM), replacing disks and allowing faster computation with reduced energy consumption[8].

In addition to new prospects in non-volatile storage, PCMs have also brought completely new physics to the field and novel modeling challenges. An accurate description of device operation must handle

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heat and carrier transport within co-existing solid crystalline and molten phases, as well as within the amorphous phase where threshold switching, structural relaxations, and crystallization occur. This paper reviews the physical framework that has been recently developed to describe the peculiar properties of the amorphous phase as well as the programming dynamics and the scaling trends of PCM cells down to the nanoscale.

Phase change materials and electronic memory devices

Phase change materials are often semiconducting or semi-metallic alloys containing the elements of group VI of the periodic table, excluding oxygen (i.e., S, Se, Te). In 1968 electronic switching in amorphous chalcogenides was first observed[9] opening the way to applications in electronic storage. The first PCM memory array was demonstrated in 1970[3]. In 1971, the rapid reversible laser-induced amorphous-crystalline transition in Ge–Te–Sb–S triggered research on optical recording[10]. The following studies on the fast crystallization dynamics of GeTe[11] led to the discovery of the Ge–Sb–Te ternary alloys (GST) and of the stoichiometric compounds along the GeTe–Sb_2Te_3 pseudo-binary line with their fast nucleation-driven crystallization[12,13]. In the 90s GeTe and SbTe glasses revolutionized rewriteable optical media[14] while, at the beginning of millenium, as the scaling path of mainstream non-volatile technologies appeared more problematic, the industrial development of PCM arrays started with the use of $Ge_2Sb_2Te_5$[4-6] and $Sb_{70}Te_{30}$-based alloys[15,16]. The active material has a critical impact on device performance, and therefore other options are being actively investigated, aimed at increasing speed, improving retention and cycling endurance, and lowering power consumption. The performance can be tuned by changing the alloy stoichiometry[17-19], by adopting proper doping[20-22], or moving to non-chalcogenide phase change compositions[23-26]. However, $Ge_2Sb_2Te_5$ (GST) is still considered as a reference material for phase change electronic storage.

In the crystalline phase, GST has a metastable rock-salt structure, characterized by Te atomic planes interleaved with Ge/Sb planes with 20 % vacancies. Vacancies are essential for the energy stability of the octahedral structure[27], and are responsible for *p*-type conduction (by removing electrons from the valence band). The crystalline phase can be transformed into an amorphous phase by heat-induced melting and fast quenching, resulting in the loss of the long range order and in the development of a covalently bonded structure[28]. However, unlike other amorphous solids, the short-range atomic arrangement also changes. Extended x-ray absorption fine-structure (EXAFS) spectroscopy has demonstrated that upon phase change, some Ge atoms flip into a tetrahedral coordination while the Sb and Te sites remain octahedral[29]. It has been proposed that the higher bonding localization is responsible for the bandgap variation[30]. In addition, the structural disorder results in a large density of localized states with a random distribution in space and in energy[31-36]. Since most of the atoms achieve their natural

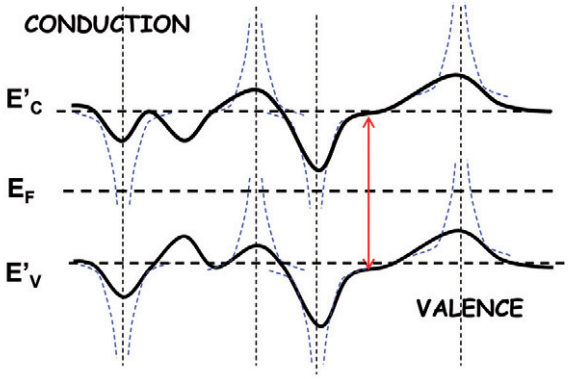

Fig. 1 Schematic representation of conduction and valence band edges in the amorphous phase with potential fluctuations and effective donor/acceptors-like states. Adapted from[36]. © 1972, with permission from Elsevier.

valence, most of these states are trap-like (i.e., neutral when empty) with a density of 10^{20} – 10^{21} cm^{-3}. However, experiments also suggest a much lower, but still significant density of donor/acceptor-like states (i.e., neutral when occupied by an electron/hole) with a density ranging from[31] 10^{18} – 10^{19} cm^{-3}. These states are locally balanced, thus pinning the Fermi level of the amorphous phase mid-gap, as testified by the large values of the conduction activation energy[37]. The larger gap and the deep Fermi level are responsible for the high resistivity of the amorphous phase. In addition, the local potential fluctuations due to Coulombic centers lead to "corrugated" band-edges, such as those schematically depicted in Fig. 1[36].

In a PCM cell, the chalcogenide material is sandwiched between two electrodes, allowing for the application of an electrical voltage and for the consequent phase change between a crystalline (low resistivity) set state and an amorphous (high resistivity) reset state. The inset of Fig. 2 shows a TEM cross-section of a PCM cell[38] where the chalcogenide layer is deposited over a thin, vertical bottom electrode (BE or heater). Programming to the reset state is performed by driving the cell

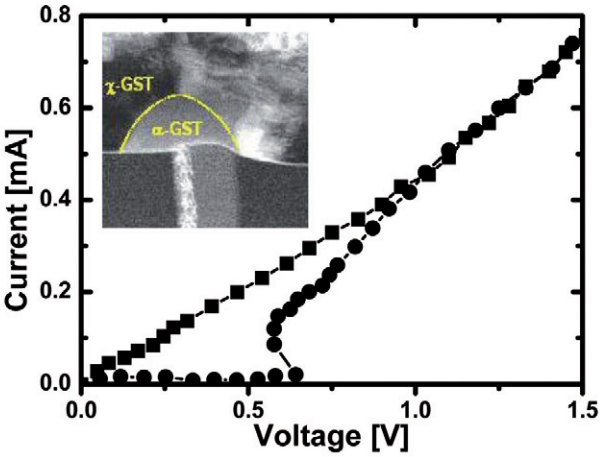

Fig. 2 PCM Cell and I-V curve of a GST PCM cell in the crystalline and in the amorphous states. The inset shows a PCM cell. © 2004 IEEE. Adapted and reprinted, with permission, from[38].

with current pulses of 10 – 100 ns duration and an amplitude large enough to melt the chalcogenide material through Joule heating. The subsequent quenching results in a mushroom-shaped amorphous region, clearly visible in the inset of Fig. 2.

Transport properties of the amorphous phase

Fig. 2 shows the current-voltage (*I-V*) curves of a PCM device, indicating a large resistance difference between the two states that guarantees reliable bit discrimination. Above a threshold voltage, V_T, of 0.6 V in Fig. 2, the amorphous phase switches to a highly conductive state thanks to *threshold switching*[37,39]. The effect plays a key role, as it permits large Joule heating to be generated in the amorphous phase at a practical low bias, thus speeding-up spontaneous crystallization, such that it occurs on the time scale of hundreds of nanoseconds.

The high resistivity and the threshold switching phenomenon in the reset state of Fig. 2 can be understood by considering the electrical properties of the chalcogenide amorphous phase. Fig. 3 schematically shows the band structure of the chalcogenide amorphous phase, displaying potential energy wells that result from the donor states, as in Fig. 1[40]. Electron transport through these states may be due to three effects: (1) pure tunneling between adjacent Coulombic traps; (2) Poole-Frenkel emission from a localized trap to extended states; and (3) thermally-assisted tunneling. Quantitative evaluations indicate that the impact of pure tunneling is negligible while the contributions and the field/temperature dependencies of both Poole-Frenkel emission and phonon-assisted tunneling are similar[39]. These contributions sustain *thermally assisted hopping conduction* that is exponentially enhanced by the electric field. The hopping current depends on the average spacing between the charged traps. If the spacing is below about 5 nm (trap density of about 10^{19} cm^{-3}, see Fig. 3a) the potential barrier between adjacent sites peaks almost midway between them. The lowering of the energy barrier is thus proportional to the applied voltage, and the current can be obtained by[39]:

$$I = 2qAN_T \frac{\Delta Z}{\tau_0} e^{-\frac{E_C - E_{F0}}{kT}} \sinh\left(\frac{qV}{kT}\frac{\Delta z}{2u_a}\right) \quad (1)$$

where q is the elementary charge, A the device cross-section, u_a the amorphous layer thickness, $\tau_0 = 10^{-15}$ s is the *attempt to escape* time from a trapping site, N_T is the density of the Coulomb states between the Fermi level (E_{F0}) and the conduction-band mobility edge, E_C. The sinh dependence in Eq. 1 reduces to a linear ohmic conduction at low bias, while yielding an exponential dependence at higher bias. For a larger trap spacing (Fig. 3b), the barrier lowering follows a conventional Poole-Frenkel dependence[41,42]. Fig. 4 shows the measured and calculated *I-V* curves of a cell programmed in the amorphous state and measured at room temperature before and after a high-temperature bake[43]. Before annealing, the current follows Eq. 1 assuming Δz = 5 nm, while the *I-V* curve measured after bake displays the characteristic Poole-Frenkel dependence. This can be understood through the defect annealing process taking place during annealing and increasing the average trap spacing[40].

Above a critical threshold voltage V_T, the conductivity of the amorphous chalcogenide increases, thanks to threshold switching. This is a fairly general phenomenon, which has been observed not only in chalcogenide glasses[9], but also in amorphous boron[41,42], amorphous silicon[41,44], transition metal oxides[45,46], and amorphous pnictides such as GeSb[47]. Threshold-switching has been explained through several mechanisms, including impact ionization and recombination at deep states[48,49], instability of polarons[50], and field-driven nucleation[51]. However, a thermally-assisted hopping conduction mechanism is able to explain the threshold switching effect based solely on high-field

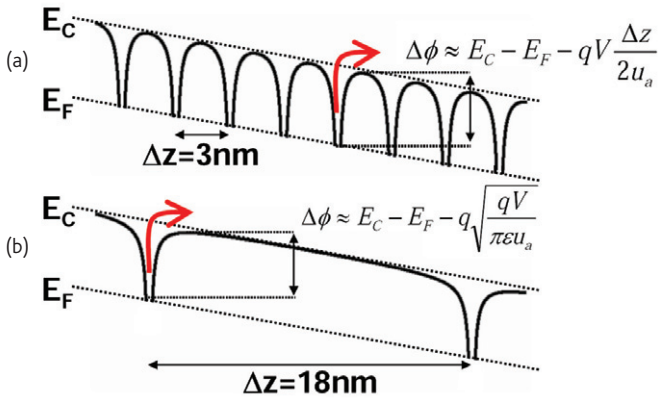

Fig. 3 Schematic representation of carrier hopping from Coulomb-traps in the amorphous phase. If the average trap spacing is below 5 nm, the peak of the potential barrier lies midway between two adjacent sites, thus resulting in a Poole transport regime where the barrier lowering is proportional to the applied voltage. If the traps are farther apart, the usual Poole-Frenkel dependence is recovered. © 2009 IEEE. Reprinted, with permission, from[40].

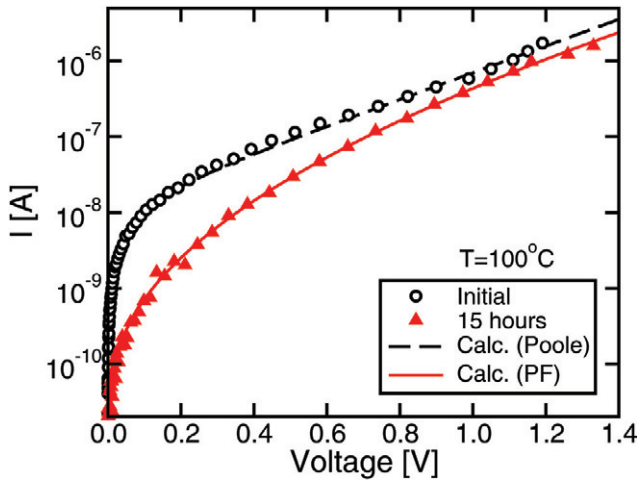

Fig. 4 Experimental curves taken before and after a bake of 1 day at 120 °C. The curve before bake follows a Poole dependence. The curve after bake follows a Poole-Frenkel dependence. Reprinted with permission from[43]. © 2008, American Institute of Physics.

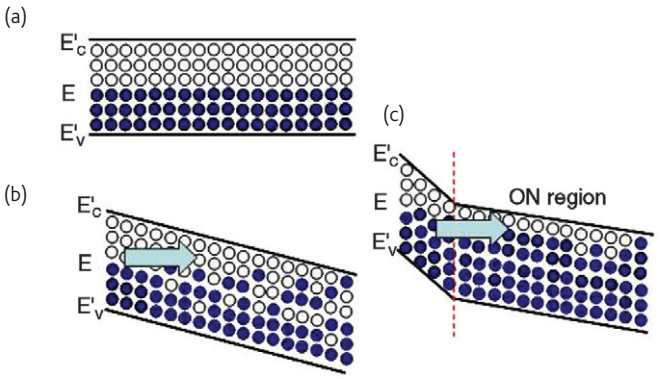

Fig. 5 Schematic dependence of the band edges and of the Fermi level in the amorphous phase at (a) equilibrium, at (b) high field below the switching point, and at (c) high field above the switching point. As the Fermi level approaches the conduction band edge the conductivity of the regions farther from the contact exponentially rises (b). Threshold switching takes place when the current can be sustained at lower voltage. The electric field profile becomes non-uniform (c), with a peak at the injection side and a lower value in the amorphous bulk where the conductivity is enhanced. Adapted and reprinted with permission from[52]. © 2008, American Physics Society.

effects, thus accounting for the almost ubiquitous nature of such a process[52]. Fig. 5 describes the threshold switching dynamics. At a low current bias (a) the material is in an equilibrium state with all carriers obeying a Fermi distribution governed by E_{F0}. As the current bias increases (b), carriers in the bulk chalcogenide increase their kinetic energy due to the electric field, thus occupying states closer to the band edge. The Fermi level departs from its equilibrium value, causing an exponential rise of the conductivity[52]. The conductivity increase with the current bias results in a negative differential resistance (NDR), where a bias current increase can be sustained at a lower voltage. After switching the electric field profile becomes non-uniform (c), with a low electric field in the chalcogenide bulk due to the enhanced conductivity. Threshold switching takes place when the electron energy increases by a critical amount of about kT[52]. This corresponds to a condition of constant power given by[52]:

$$P_T = JF\Omega = \frac{\Omega N_T (kT)^2}{\tau_{rel}\,(E_C - E_{F0})} \qquad (2)$$

where J is the current density, F is the electric field, Ω is the active volume, and τ_{rel} is the relaxation time controlling electron thermalization.

Fig. 6 shows the measured I-V curve for a PCM cell in the reset state, alongside calculations for (a) increasing temperature and (b) an increasing activation energy for conduction $E_C - E_{F0}$. The threshold voltage decreases for (a) increasing temperature and (b) for decreasing $E_C - E_{F0}$, in both cases following the constant power rule in Eq. 2 and in agreement with reported trends in the literature[53-55].

Programming characteristics

While threshold switching only involves a reversible electronic conductivity change, phase (or memory) switching (that constitutes a permanent change of the active material phase) is needed for stable memory program/erase. Phase change in PCMs is promoted by Joule heating from an applied voltage and current in the active chalcogenide volume. The most demanding requirements for phase change are a short programming time t_P, to allow high data throughput (amount of bits that are written/erased per unit time) and a minimum energy consumption, E_P, to enable portable applications and 'green' data storage. The switching energy may be estimated by:

$$E_P = RI_{reset}^2 t_P, \qquad (3)$$

where R is the PCM cell resistance at large current values and I_{reset} is the programming (reset) current. To allow low energy consumption, I_{reset}

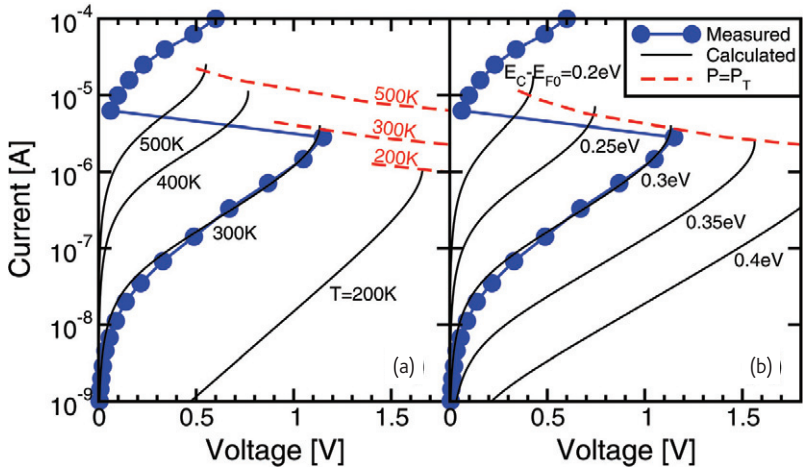

Fig. 6 Calculated curves for a PCM device in the reset state: (a) dependence of threshold switching on temperature by taking constant the activation energy of conduction $E_C - E_{F0} = 0.3$ V; (b) dependence of threshold switching on activation energy of conduction at room temperature. The experimental data refers to a PCM cell with a $Ge_2Sb_2Te_5$ chalcogenide layer. The dashed lines highlight that threshold switching takes place when the average carrier energy increases by about kT, which corresponds to the constant power condition set by Eq. 2. Adapted and reprinted with permission from[52]. © 2008, American Physics Society.

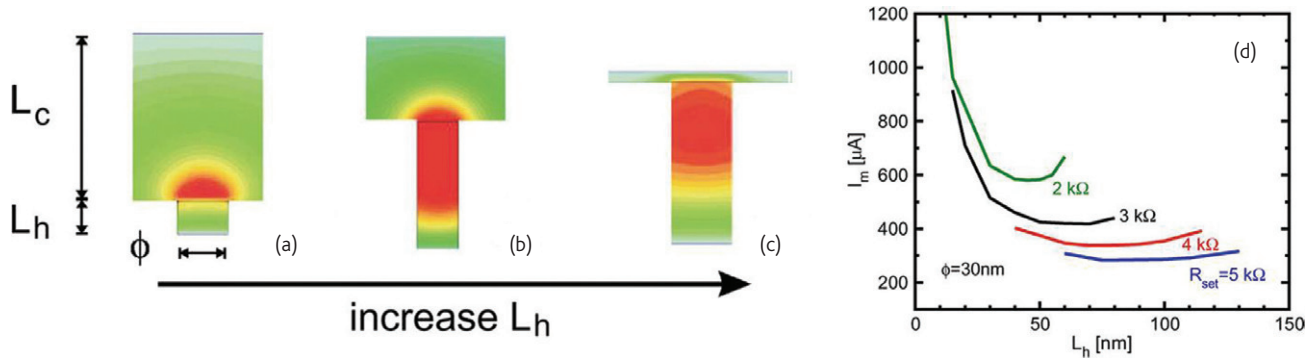

Fig. 7 Temperature maps in mushroom-type cells numerically computed by increasing the bottom electrode length, L_h, but taking a constant L_h+L_c thickness (a, b c). Curves in (d) show the calculated melting current I_m as a function of L_h, for increasing resistance of the set state, R_{set}. The optimized cell geometry corresponds to those L_h and L_c values that result in the peak temperature at the bottom electrode-chalcogenide interface, as shown in (b), leading to the minimum Im in (d). © 2008 IEEE. Reprinted, with permission, from[56].

is minimized following two general approaches, namely cell geometry optimization and device scaling[56]. Cell optimization aims at maximizing the peak temperature at the interface between the confined bottom electrode and the chalcogenide active region. An increase of temperature results from both heat generation, which depends on electrical resistance, and heat conduction, which depends on thermal resistance. Geometry optimization thus requires an ideal balance between the thermal and electrical resistances in the bottom electrode (BE) and the chalcogenide region, which can be obtained through self-consistent calculations of electrical/heat conduction in the PCM device.

Figs. 7a-c show the calculated temperature map within the PCM cell for three different geometries, differing by their respective chalcogenide thicknesses (L_c) and heater lengths (L_h)[56]. The diameter, ϕ, of the cylindrical BE was kept constant and parameters L_c and L_h were jointly selected to provide the same resistance, R, in the set state, which should also be minimized based on Eq. 3. Therefore, as L_h increases from (a) to (c), L_c correspondingly decreases to maintain a constant R. An optimum geometry is found for well balanced L_h and L_c in Fig. 7b, while a relatively short L_h results in excess heating of the chalcogenide layer (Fig. 7a) and a relatively long L_h causes excess heating of the BE (or heater) (Fig. 7c). Fig. 7d shows the calculated melting current I_m, defined as the minimum current needed to melt the chalcogenide in contact with the BE-interface, as a function of the heater length L_h for increasing R[56]. The minimum I_m marks the optimized geometry of the cell. Note that I_m decreases for increasing R, as a result of the larger power dissipation in Eq. 3.

Device scaling is also efficient in reducing I_m. In fact, the maximum temperature reached at the BE-interface may be written as $T = T_0 + RR_{th}I^2$, where T_0 is ambient temperature and R_{th} is an effective thermal resistance. Therefore, the programming current can be roughly estimated as[56]:

$$I_m = \sqrt{\frac{T_m - T_0}{R_{th}R}}, \quad (4)$$

where T_m is the chalcogenide melting temperature. By decreasing ϕ, L_h, and L_c by the same factor, F, (isotropic scaling), both R and R_{th} approximately scale as F^{-1}, thus I_m scales proportionally to F. Therefore, a reduction of the cell size by a factor of two, e.g., from the 45 nm to the 22 nm technology node, results in a twofold reduction of the programming current, and hence of energy, according to Eq. 3. An

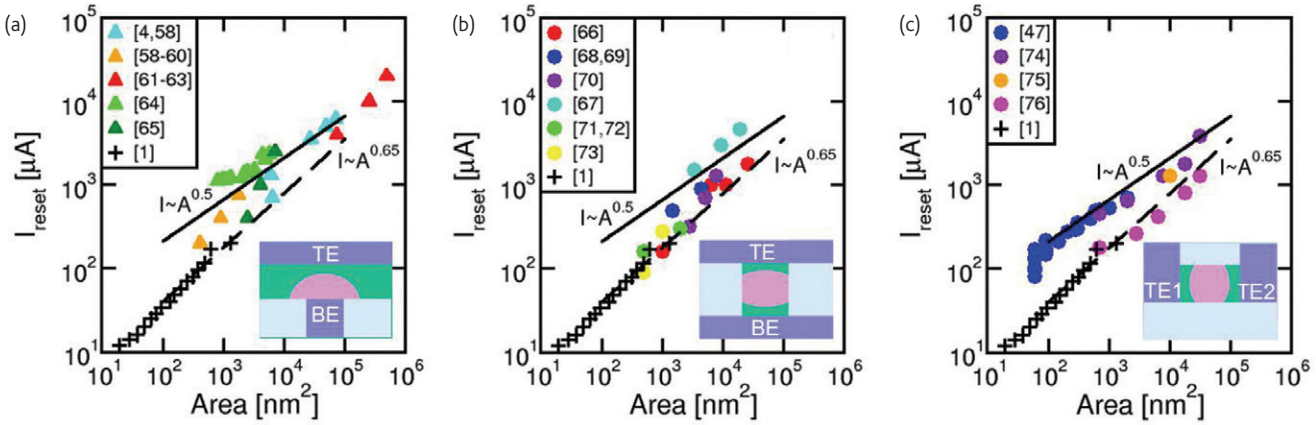

Fig. 8 Experimental reset current as a function of minimum cell cross section A, for (a) mushroom, (b) pore, and (c) line cells. The insets schematically show the corresponding PCM cell structures. ITRS roadmap predictions[1] and model calculations for isotropic and non-isotropic scaling are shown for reference. Reprinted with permission from[57]. © 2010 Cambridge University Press.

alternative scaling approach is to reduce the cell cross-section at constant L_h and L_c. Based on Eq. 4, such a *non-isotropic* scaling approach would result in a current reduction of $I_{reset} \propto F^2$. However, accurate numerical calculations show a current scaling law $I_{reset} \propto F^{1.3}$, as a result of different scaling rules for electrical and thermal resistances[56]. Fig. 8 shows the measured programming current as a function of BE area, A, for various cell architectures[57]. These include (a) mushroom[1,4,58-65], (b) pore[1,66-73], and (c) line cells[1,47,74–76], as schematically shown in the inset. The figure also shows predictive points from the ITRS roadmap[1] and reference lines, indicating the predicted behavior of I_{reset} for isotropic and non-isotropic scaling and assuming $A \propto F^2$. Collected results are in good agreement with the theoretical predictions and highlight the effectiveness of downscaling for programming current reduction.

Amorphous phase stability

An ideal non-volatile memory would require that both crystalline and amorphous phases are thermodynamically stable in the range of voltage, temperature, and times explored by the memory operations. On the other hand, both the amorphous phase and the rock-salt crystalline phase of GST are metastable. However, while the transition from the face centered cubic structure to the hexagonal phase leads to a negligible resistance change, crystallization of the amorphous phase heavily affects resistance, thus making the amorphous stability the most relevant aspect for PCM reliability. Amorphous chalcogenide also undergoes structural relaxation (SR), that is a short-range atomic rearrangement which is ubiquitously observed in amorphous semiconductors and metallic glasses[40,77-89]. SR leads to a progressive increase of atomic network connectivity with defect annealing. As the trap density decreases (Fig. 4), the energy gap and the activation energy for conduction slowly increase[40], resulting in a resistance increase, or *drift*[40,77-80,87-89].

To highlight the resistance drift phenomenon, Fig. 9a shows R values measured at room temperature, after different bake times at various annealing temperatures. As T increases, the slope of the resistance drift increases. This is because the time for SR, τ_{SR}, obeys the Arrhenius law[43]:

$$\tau_{SR} = \tau_0 e^{\frac{E_A}{kT}} \quad (5)$$

where E_A denotes the energy barrier of the process while τ_0 is given by:

$$\tau_0 = \tau_{00} e^{-\frac{E_A}{kT_{MN}}}, \quad (6)$$

where τ_{00} is a pre-exponential *attempt to escape* time and T_{MN} is the iso-kinetic temperature according to the Meyer-Neldel (MN) rule[90,91]. Due to the temperature dependence in Eq. 5, defects are annealed at a faster rate at increasing temperatures, as observed in the experimental drift behavior shown in Fig. 9a[91]. By using the kinetic formulas in Eqs. 5 and 6, a single resistance drift measurement is sufficient to predict the drift evolution at any given time and temperature: for instance, Fig. 9b shows the predicted resistance drift at room temperature T = 25 °C, based on the experimental data from Fig. 9a after renormalization according to the Arrhenius kinetics[92]. These results support the Arrhenius and MN rules in Eqs. 5 and 6 for a reliable prediction of PCM. Resistance drift in Fig. 9 is eventually followed by crystallization, which appears as a sharp resistance drop after 10^4 s at 180 °C (projected to 10^{15} s at room temperature). Such a resistance drop is due to percolation through low-resistivity crystalline grains nucleating and growing in the amorphous region[92].

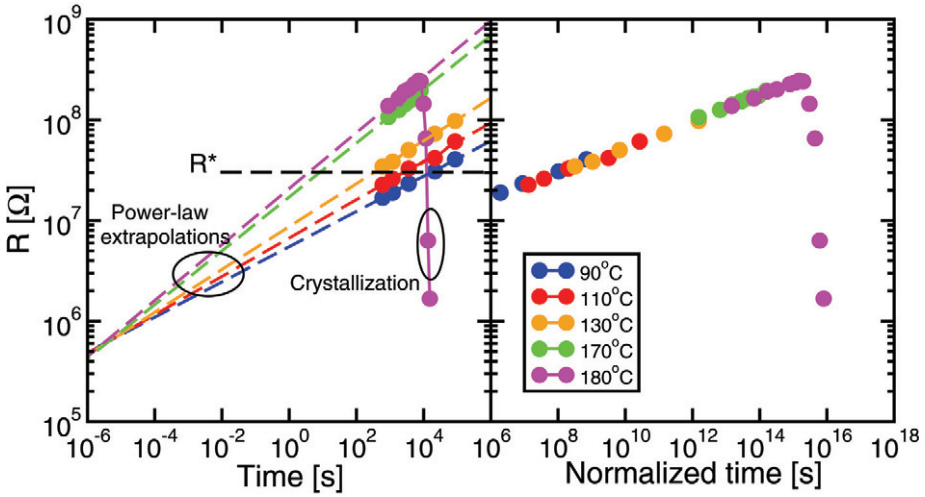

Fig. 9 Measured resistance drift as a function of time for increasing annealing temperature (a). The effect is due to thermally-activated structural relaxation of defects with distributed activation energies. Relaxation taking place at a time t' and temperature T' can be translated into an equivalent time t at temperature T. Drift data in (a) can be therefore reported as a function of time at T = 300 K after normalization according to Eqs. 5 and 6 in (b). Reprinted from[92]. © 2009, with permission from Elsevier.

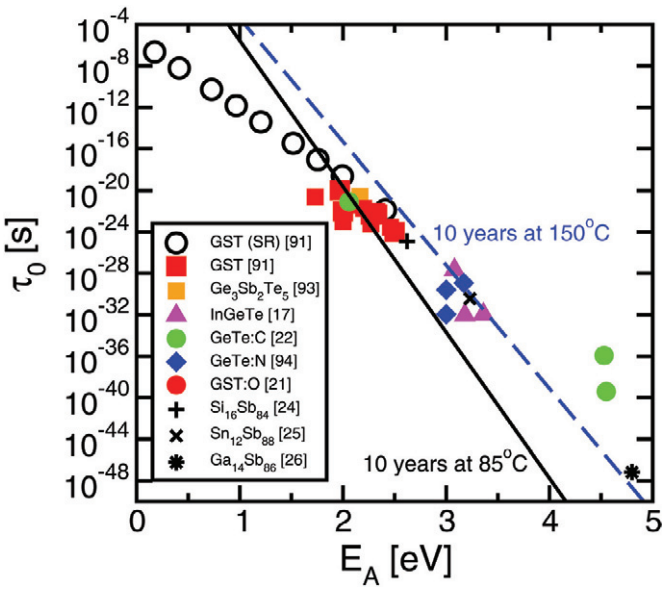

Fig. 10 Experimental dependence of the pre-exponential time, τ_0, as a function of the activation energy, E_A, in the Arrhenius law of Eq. 5. Data are shown for structural relaxation in $Ge_2Sb_2Te_5$ PCM devices and crystallization with different active materials[17,21,22,24-26,91,93,94]. The trends show that the Meyer-Neldel law of Eq. 6 applies, with τ_{00} = 1 μs and T_{MN} = 700 K. Processes with higher activation energy benefit from a lower pre-exponential term with a weak dependence on material composition. Materials corresponding to points located on the upper, right part of the solid and dashed lines correspond to 10 years retention at 85 °C and 150 °C, respectively.

Although crystallization and SR differ in terms of atomic structural change, they are both dictated by the same Arrhenius law in Eq. 5, the only difference being that SR is characterized by distributed E_A values, while crystallization has a rather fixed activation energy around 2.5 eV with a pre-exponential time of about 10^{-23} s for GST[91]. Both activation energy and the pre-exponential time are key parameters for PCM, since they dictate the projected crystallization time for a cell at a given operation temperature. Fig. 10 shows a plot of available pre-exponential times, τ_0, as a function of E_A, for SR and crystallization in GST. Results are also shown for crystallization in alternative chalcogenide materials, such as $Ge_3Sb_2Te_5$[93], InGeTe[17], C-doped GeTe[22], N-doped GeTe[94], and O-doped GST[21]. The figure also shows non-chalcogenide materials, namely antimonides[8,23,47] with compositions $Si_{16}Sb_{84}$[24], $Sn_{12}Sb_{88}$[25], and $Ga_{14}Sb_{86}$[26]. Results indicate that all the data roughly obeys the MN rule of Eq. 6 with τ_{00} = 1 μs and T_{MN} = 700 K, similar to previous findings[91,92]. The retention time can be strongly improved by enhancing the activation energy through material doping (e.g., C in GeTe[22] or O in GST[21]) and/or increasing the content of elements Ge[23], Si[24], Sn[25], or Ga[26] in Sb-based alloys. It is worth noting that the enhanced data retention does not always impact negatively on the set transition, as indicated by the fast switching observed in GeTe-based PCM[19]. Fig. 10 also allows materials satisfying a given crystallization time to be identified; such as 10 years at a temperature of 85 °C (solid line in the figure), which is the typical reliability criterion for non-volatile memories, or 150 °C (dashed line). Points located on the upper, right part of the lines satisfy the reliability criteria. Comparison with data suggests that there is significant room for the tailoring of material composition and doping to meet high temperature retention.

Challenges and perspectives

In the last decade, PCMs have demonstrated their potential in the industrial arena, while remarkable advances in material engineering and in our physical understanding have been made. At the same time, several challenges still remain, in terms of reducing the reset current, improving the reliability, and 3D integration.

PCM is relatively demanding in terms of energy consumption, as the melting of a chalcogenide volume is required for a phase change. To reduce the programming power, several solutions have been proposed, including reducing electrode area[95] and material engineering[17-26,55,93,94,96]. Breakthroughs could also be achieved using chalcogenide superlattices[97] and solid-state amorphization without melting[98].

Device scaling may also impact reliability. Endurance has been shown to be limited by void formation at the BE contact[99,100] while the increasing current density does not seem to adversely impact reliability, yet[101]. Novel materials and/or processes[102] may contribute to improvements in cycling endurance, thus supporting the use of PCM as a DRAM replacement and SCM.

Finally, 3D integration may further promote PCM in high-density memory technologies. Thanks to the 2-terminal device structure, PCM can be implemented in cross-bar architectures with an extremely small cell size of only[57,66] $4F^2$. However, cross-bar architecture requires that the select device is capable of delivering the required programming current, while providing sufficiently small leakage through unselected lines. Poly-silicon *p-n* diodes have been proposed as $4F^2$ select devices for PCM cross-bars[66], although the scaling properties of the diode current have been shown to be unfavorable for PCM[57]. Mixed ionic-electron conductors (MIEC) have been suggested as novel select devices with a high on/off ratio, sufficient endurance, and the capability of 3D stacking[103,104]. 3D PCM cross-bar arrays have been demonstrated using ovonic-threshold switch (OTS) selectors[105]. In OTS, threshold switching permits the transition from a highly resistive to a highly conductive state, although no phase change is achieved. The device therefore acts as a selector providing the necessary on/off swing, switching speed, and drive current to sustain PCM switching. Through extensive validation of the technology, OTS/PCM may become a mainstream memory/storage paradigm, while serving as a brilliant example of the high degree of functionality and complexity that can be achieved through chalcogenide glasses and the study of their physics.

Conclusions

This paper provides a review of the properties and perspectives of phase change materials and memories. The electronic structure of chalcogenide materials has been discussed, describing the mechanisms of conduction and threshold switching in the chalcogenide amorphous phase. The

programming and reliability properties of PCM have been addressed, showing that physics-based analytical models are able to account for the scaling dependence of the programming current and for drift and crystallization. The development of both industrial know-how and physical understanding will be key factors as we face the future PCM challenges of material engineering, 3D integration, and device scaling. mt

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