Research Article

Downconverting Module Architectures for High Performance Multipixel Cameras

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Multipixel cameras represent an emerging topology for arrays receivers, improving speed and accuracy of both security scanning systems and radioastronomical sky surveys by means of a matrix of phased elements. Difficulties in the generation and proper distribution to each pixel of the local oscillator signal still limit their use to frequency ranges below a few GHz or at least seriously affect the complexity of the implementable cameras. This work presents a full comparison between two possible system architectures, alternatively based on LO frequency multiplication or subharmonic mixing strategies, aiming to overcome the aforesaid limitations: design and performance of two compact test vehicles in MMIC technology, both operating in the Q-band frequency range with ultrabroadband IF section, are reported.

1. Introduction

Array receivers have been adopted since the beginning of the 90's in radioastronomical applications [1] and, more recently, in security scanning systems, improving active and passive millimetre-wave imaging capabilities [2].

In radioastronomical applications, this kind of receivers is usually placed at the focus of a large radiotelescope antenna and it is mainly used to survey large areas in a more efficient way than single-pixel receivers. Array receivers can be roughly classified into three different types: focal plane arrays (FPAs), which incorporate distinct superheterodyne receivers performing a spectroscopic analysis of the incoming signal; bolometric arrays (BAs), achieving an integral measure of the total channel power; phased array feeds (PAFs) consisting of a matrix of receiving elements fed by the same local oscillator and then digitally combined [3]. Major research efforts are currently devoted to the latter receiver architecture, exhibiting two key advantages over conventional multibeam horn feeds: firstly it enables the radiotelescope to support many simultaneous beams on the sky, thus increasing the instrument speed; secondly, it offers the opportunity to properly shape the pattern of the feed array in order to match the optical configuration of the telescope [4]. The major

drawback of a PAF, often limiting its use for frequency ranges above a few GHz, is however the necessary requirement of distributing the same LO signal to each pixel, without loss of synchronism between different paths; the research for new circuit topologies allowing to overcome this limitation represents the main purpose of this work. Possible strategies have the common feature of reducing the main local oscillator operating frequency, thus alleviating the critical aspect of distributing a millimetre-wave signal among the different paths, and leaving the task of locally producing the latter to the front-end pixel circuitry.

Viable approaches to this goal can be roughly classified into two different categories: both the integration of $a \times N$ multiplier and the selection of a Nth order mixing product allow the scaling of the LO frequency by the same N factor. Clearly, the two architectures are featured by different pros and cons and undergo different criteria to be properly implemented. In the following sections, the two topologies are compared through the design and the resulting performance of the two subsystems implemented in monolithic technology, both operating at the same Q-band frequency range.

In particular, after the present introduction, in Section 2 the two more promising architectures are introduced and

critically reviewed, while in Sections 3 and 4 the designs and performance of the two test vehicles are described in detail. Respective results are finally compared and summed up in Section 5.

2. Feasible Architectures Description

As already stated, the main factor limiting the use of multipixel cameras at high frequencies is related to the difficulty of correctly synchronizing the local oscillator among different paths. A real case will be adopted in the following to describe the features of the selected design approaches. In particular, a Q-Band receiver will be addressed, able to downconvert the incoming RF full-band signal (33–50 GHz) into the resulting low-frequency 1–18 GHz signal. In the present case, the frequency conversion would require the proper distribution, among the different pixel systems, of a 32 GHz LO signal. In order to circumvent this problem, two feasible strategies may be envisaged: the first one consists in multiplying the original LO signal while the second one in selecting a higher RF-LO mixing product; in the remainder of this work we will refer to the multiplier-based topology as MHM (Multiplied Harmonic Mixing) architecture and to the subharmonic mixing-based topology as SHM (Subharmonic Mixing) architecture. MHM architecture, depicted in Figure 1(a), offers the possibility of LO signal amplification and takes advantage of the higher conversion gain typical in fundamental LO mixing; unfortunately, the insertion of the multiplying-amplifying chain results in the twofold drawback of higher circuit complexity and DC power consumption. Conversely, SHM architecture, depicted in Figure 1(b), hardly allows LO signal amplification and suffers from higher conversion losses related to the use of a higher-order mixing product. On the other hand, circuit complexity and DC power consumption involved in the implementation of a subharmonic mixer are definitely lower. The higher the selected multiplication factor ($\times N$) is or the higher-order mixing product (Nth), the more pronounced the resulting effect is, thus emphasizing advantages and disadvantages of both implementations.

Further notes can be drawn considering the values of N that are actually selected in the present designs: $\times 8$ for the multiplication factor and the selection of 2nd order mixing product. MHM architecture allows in this case the generation and distribution of a lower frequency LO (4 GHz) and maintains 1 GHz separation between LO and RF bands; on the other hand, some external hybrid circuitry is however needed to filter out unwanted LO harmonics. SHM architecture implies the distribution of a higher frequency LO (16 GHz) and an overlap between IF and LO bands (thus imposing a very high LO/IF isolation to the mixer) but, on the other hand, does not need any additional external filtering.

Both implementations have to be properly designed to handle the 180% relative bandwidth (1–18 GHz) at the IF port.

Two test vehicles have been designed and simulated in agilent ADS environment [5]. Given the inherent uniformity and volume production featured by multipixel camera applications, a monolithic approach has to be preferred. To this
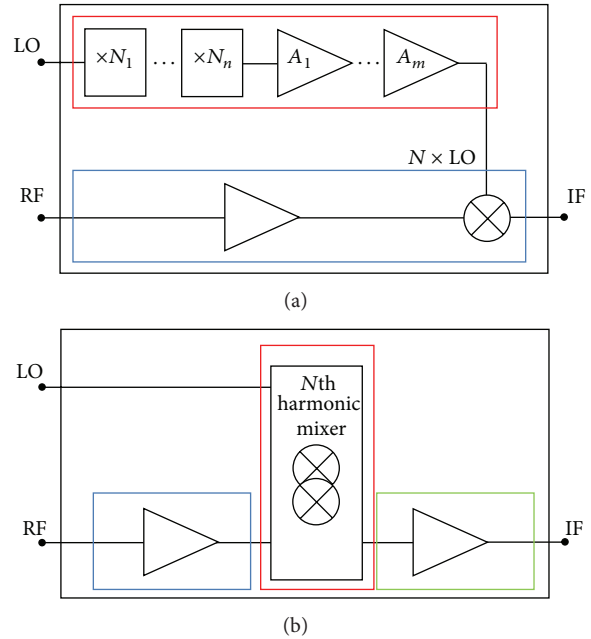

FIGURE 1: MHM (a) and SHM (b) architectures block diagrams.

goal, a metamorphic GaAs 70 nm gate length foundry process by OMMIC (D007IH) has been selected. Such industrial-grade technology is featured by 1.0 dB minimum noise figure and 9.5 dB associated gain at 50 GHz (for a sample $4 \times 25\,\mu\mathrm{m}$ device, biased at $V_{\mathrm{DS}} = 1$V and $I_{\mathrm{DS}} = 20\%\ I_{\mathrm{DSS}}$). The resulting design of the two architectures will be presented in the following.

3. MHM Architecture Test Vehicle Design

As stated above, the harmonic mixing topology (Figure 1(a)) mainly consists in the combination of two different functionalities, namely, an LO amplifying-multiplying chain and a RF mixing section, whose design will be fully described in the present section. The corresponding two subsystems, while intended to operate together, have been designed and implemented as separate ones onto the same MMIC die, for the purpose of testability and resulting design flexibility. The former feature actually allows the on-site measurement of the multiplier harmonic content, while the latter allows the insertion, if unacceptable harmonic levels result, of eventual external highly selective filtering structures.

3.1. Multiplying-Amplifying Chain. The aforementioned technology and the related process offer the possibility of using different nonlinear devices to perform the LO frequency multiplication: Schottky diodes (in varactor-like operation), drain-source-connected FETs (by using the resulting Schottky diodes), and mHEMT FETs (exploiting the pinch-off nonlinearity); however, manifold considerations about the lack of proper varactor diodes for mixing and multiplication purposes and the high losses introduced by the diode resistive multiplier [6] led to the selection of an active FET multiplier
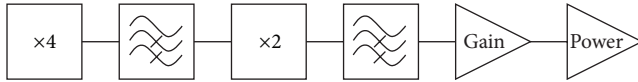
FIGURE 2: Multiplying-amplifying chain.

structure [7], providing at the same time a limited amount of gain.

Different chain architectures [8, 9] can be adopted to obtain the ×8 multiplication: cascading three doublers or using a quadrupler doubler topology, both in single-ended or balanced configurations. Multiplier architecture, made by self-biased ×4 and ×2 blocks, was selected as the best compromise between conversion gain, efficiency, and size requirements; a more accurate analysis allowed to select the single-ended configuration, given the poor performance improvement resulting from the balanced one, in conjunction with a major increase in circuit complexity, power consumption, and area occupation.

Fundamental frequency rejection can be therefore only guaranteed by the insertion, at the output of the two stages, of the proper high-pass filtering structures [10, 11] ensuring large-signal match at the desired harmonic frequency and optimum harmonic loading [12]. The proper conversion gain level and output power were finally achieved by further cascading a gain stage and an output buffer amplifier both maintaining independent gate/drain bias (see Figure 2), with the major consequence of separating the nonlinear operation of the two multiplying sections from the LO input of the mixer.

3.2. Amplifying-Mixing Section. The approach in the design of this subsystem was essentially driven by the wide operating band requested to the mixer and by the close proximity between RF and LO frequency bands; further, minimum area occupation and power consumption, dictated by the large number of pixels that are typically needed, are the driving constraints.

In light of the abovementioned severe specifications, a passive structure providing low noise operation, high linearity, and low DC power consumption was selected; in addition, the adoption of HEMTs in diode configuration as mixing elements typically requires less LO power than using actual diodes [13].

The choice of the most effective mixing topology has been the result of an intense investigation in which advantages and disadvantages of various implementations with different balancing levels and geometric arrangement have been compared: double balanced ring topology was found to guarantee an acceptable level of conversion gain and isolation for the concerned application [10, 14].

Different microstrip realizations of the balancing structures can be found in open literature, ranging from parallel coupled-line balun to Marchand-like baluns and planar transformers [15–17]; however, the need to comply with reduced area and wide bandwidth constraints suggested the use of spiral baluns, considering their extremely compact size and wideband performance [18, 19].
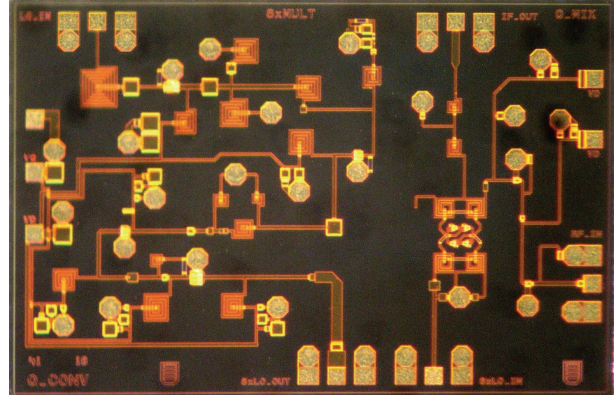

FIGURE 3: Microphotograph of the realized MHM architecture test vehicle MMIC.

The major drawback of the topology under discussion consists in the difficulties of a wideband IF extraction, mainly due to the inductive behaviour exhibited in the physical realization of the single-ended IF port [20], difficult to match over ultrawideband frequencies. To improve IF matching and isolations, an elliptic filter section, featuring low insertion loss in the 1–18 GHz band and high attenuation in the RF and LO frequencies was then inserted at IF port.

Finally, a two-stage buffer amplifier was added at RF port, thus improving input return loss and providing the entire system with a positive gain at the expense of a corresponding reduction of RF to IF isolation. Such an additional amplifier has the further beneficial effect of isolating the nonlinear RF mixer input from the output of the LNA that would likely be inserted just after each receiving pixel antenna; moreover, the resulting noise figure of the overall system is indeed improved.

3.3. MHM Architecture Test Vehicle Performance. The whole system implementation results in a really integrated and compact layout, with an area occupation of about $3 \times 2 \, \text{mm}^2$. The die microphotograph is shown in Figure 3, where both the multiplying-amplifying chain and the amplifying-mixing sections are shown, respectively on the left and right part of the chip: input port for the low-frequency local oscillator and output port for the multiplied LO signal are placed on opposite sides while, regarding the mixer, RF, LO, and IF ports are clockwise arranged on the right, lower, and upper borders of the chip, respectively. Multiplier output and LO mixer ports are juxtaposed specifically to be both directly interconnected by means of a simple wire bond connection or separated by an high-order microstrip hybrid filter selecting the desired 8th LO harmonic and rejecting an eventually higher unwanted spurious level.

In Figure 4, a comparison between measured and simulated multiplier port matching is reported, demonstrating better than 25 dB input return losses and 15 dB output matching.

The whole multiplying-amplifying chain exhibits a total DC power consumption of approximately 200 mW, with gain and output power performance, at 3 dBm input power from
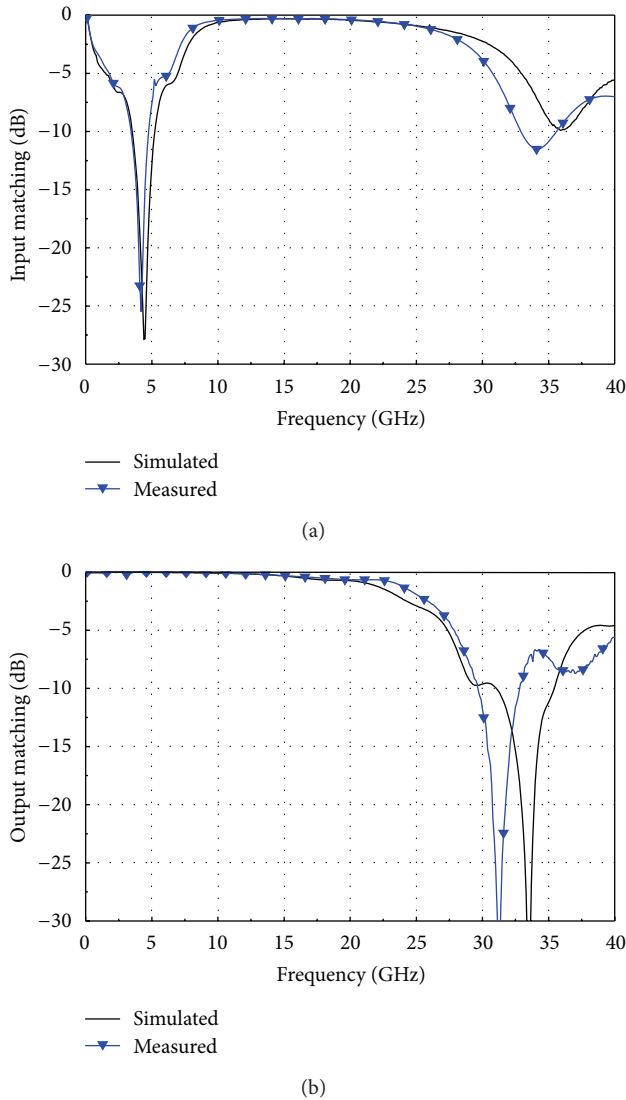
(a)

(b)

FIGURE 4: Simulated (black trace) and measured (blue trace) multiplying-amplifying chain input (a) and output (b) matching.
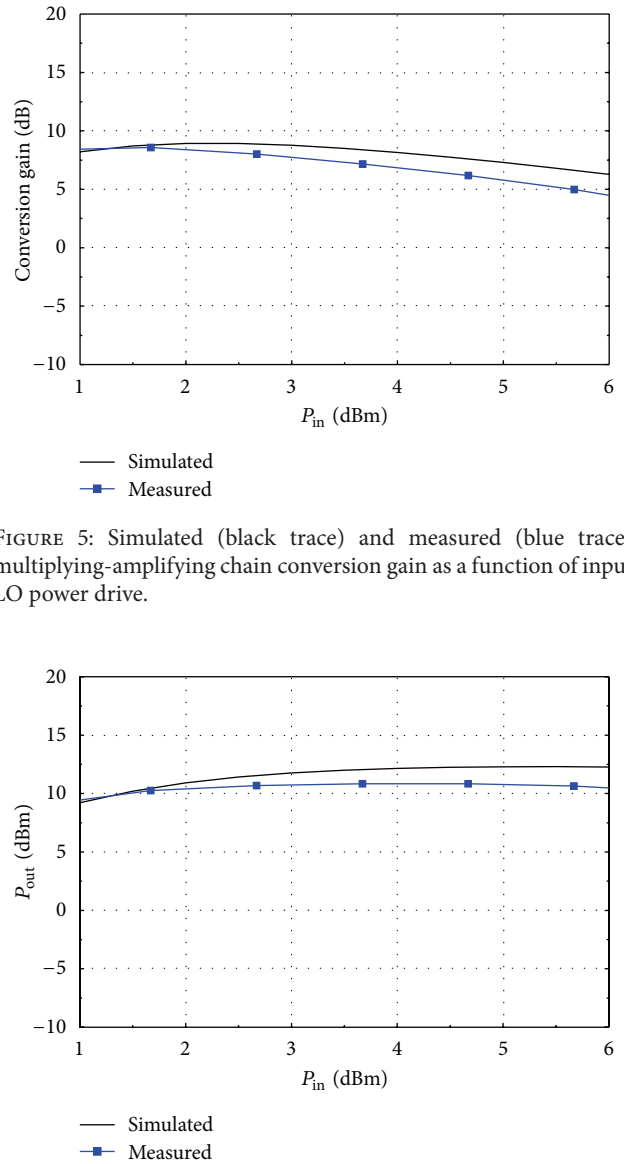

FIGURE 5: Simulated (black trace) and measured (blue trace) multiplying-amplifying chain conversion gain as a function of input LO power drive.

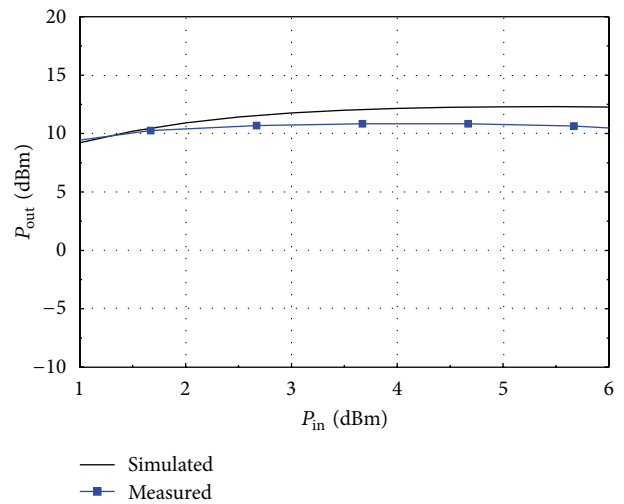

FIGURE 6: Simulated (black trace) and measured (blue trace) multiplying-amplifying chain output power as a function of input LO power drive.

the LO source, equal to 8 dB, and 11 dBm, respectively, in good agreement with simulated results (Figures 5 and 6 resp.). Under the same large-signal operating conditions, the ratio between the desired 8th LO harmonic and the highest spurious product is around 20 dBc, a rejection level that actually allows the direct connection between the amplifying/ multiplying chain and the mixer LO input.

The amplifying-mixing section exhibits a DC power consumption of about 40 mW. Moreover, the structure is featured by a pretty good matching level (see Figure 7), especially remarkable if the relative bandwidths are considered: −15 dB at the RF port (40% bandwidth) and −9 dB at the IF port (180% bandwidth).

Conversion gain and RF/IF isolation at 7.5 dBm LO power are reported in Figure 8: the former is typically around 10 dB on the entire 33–50 GHz frequency range, while the latter varies from 10 dB to 35 dB as frequency increases; LO leakage

toward RF and IF ports is lower than −43 dB and −33 dB, respectively.

4. SHM Architecture Test Vehicle Design

Such a topology can be split into three main functional blocks (Figure 1(b)), namely, sub-harmonic mixer, RF, and IF amplifiers, whose overall design provides sufficient degrees of freedom to meet different downconverter requirements while maintaining compact overall size.

4.1. Subharmonic Mixer. Considerations similar to the previous, about operating bandwidth, area occupation, and power consumption, make HEMTs in diode configuration the best
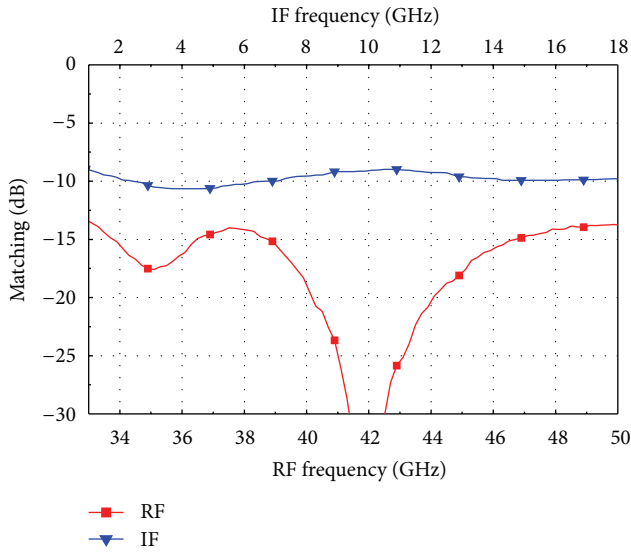
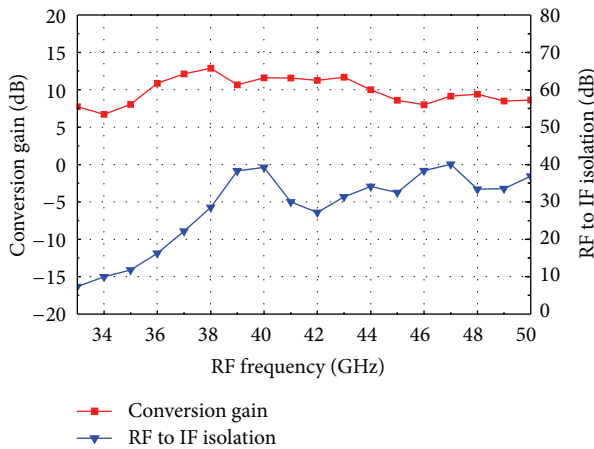FIGURE 7: Measured amplifying-mixing section RF and IF matching.

FIGURE 8: Measured amplifying-mixing section conversion gain and RF/IF isolation.

FIGURE 9: simplified schematic of sub-harmonic mixer.

starting point to develop the mixer structure; a particular care has to be posed to ensure structure symmetry and balancing, given the overlap between IF and LO bands. An anti-parallel diode pair (APDP) constitutes the basic core element with the aim to perform a 2nd order harmonic mixing, when an appropriate balancing level is selected to isolate LO and IF ports. In spite of LO and IF bands overlap, a single-balanced arrangement was found to guarantee an acceptable compromise between conversion gain (better than in doubly balanced ones), isolation (slightly worse), and area occupation (much lower) [21], provided the balancing structure is appropriately selected and sized. To this goal, open literature offers different topologies of balun-based networks that enable an effective trade off between operating bandwidth and area occupation; in this case lumped-element implementation [22], featuring compact size at the expense of narrowband performance, was found to represent the best choice. Finally, the proper application of the RF voltage
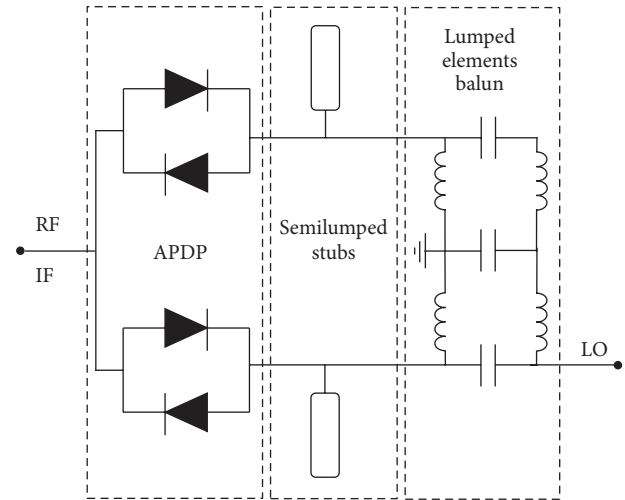
across the balanced APDP was achieved by means of two stubs, implemented with semilumped elements, behaving as an open circuit at LO frequency and as short circuit at RF frequency. The resulting simplified subharmonic mixer schematic is reported in Figure 9.

4.2. RF Amplifier. The main purpose of this block is to provide the system with the adequate amount of conversion gain improving, at the same time, RF port matching and easing overall system noise properties optimization. For this reason, the amplifier was designed by cascading three single stages and accounting for the effective termination on the output port provided by the mixer input impedance. as it will be detailed in the following section, the IF amplifier was designed to exhibit a high impedance level at RF frequency. Three stages, although biased at the same drain voltage, maintain separate DC power supplies; active devices are then self-biased to 0 V regarding the gate supply, in order to reduce the complexity of the biasing circuitry. Furthermore, additional care was paid in controlling output impedance of the RF amplifier at IF frequencies; this impedance was designed to be as high as possible not to affect, with its load, the mixer input and thus allowing the downconverted signal to merely flow towards IF port.

4.3. IF Amplifier. Amplifying section on the IF port is responsible for meeting three fundamental figures of merit: it provides to the system, together with the RF amplifying section, the adequate amount of conversion gain, improves the wideband IF port matching, and guarantees an acceptable level of RF to IF isolation, otherwise unacceptably low. Although the last requirement can be achieved by providing the IF amplifier, in the RF band, with any reactive termination, it is fundamental to choose a high impedance level in order not to affect the RF signal power flow toward the APDP. In light of the aforementioned reasons, distributed amplifier (DA) topology actually represents the only one capable of satisfying the simultaneous requirements of adequate gain and
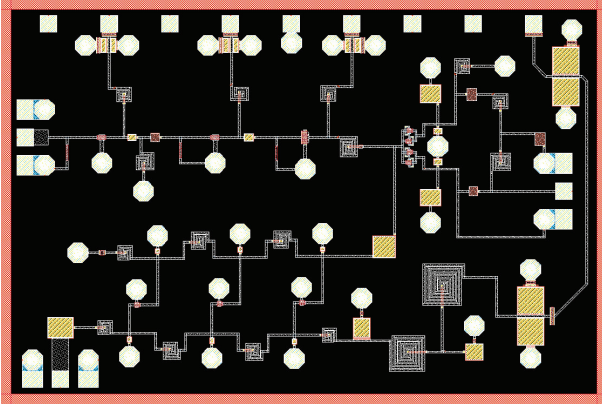
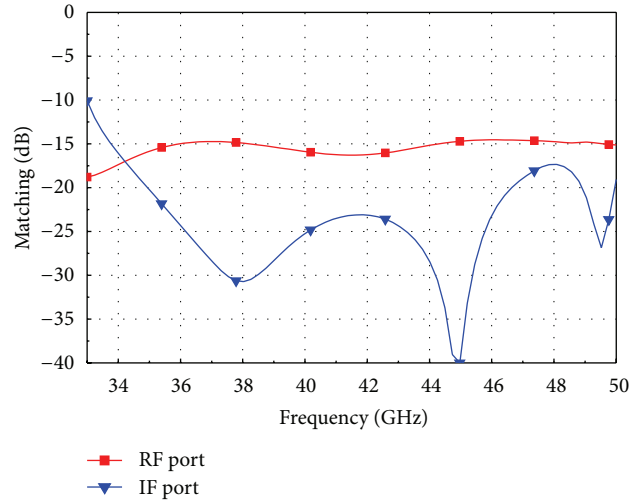Figure 10: Layout of the designed SHM architecture test vehicle MMIC.

Figure 11: Simulated down-converting module RF and IF matching.

Figure 12: Simulated downconverting module conversion gain and RF to IF isolation.

input/output matching in a wideband operation. DA design can be performed both on image impedance base [23], by identically replicating the elementary cells of an artificial transmission line, and on filter synthesis approaches [24], by properly selecting the resulting ladder network values. If requested by design constraints, further degrees of freedom may be achieved by tapering active devices gate periphery [25]. In the present case, the filter synthesis approach had to be preferred to appropriately control the stop-band frequency response and properly filter out the RF signal leakage. Three-cell structure provides a sufficient number of elements to synthesize a 7th order chebycheff low-pass filter, featuring 40 dB out-of-band rejection; again, choosing a series element as the first one in the synthesis results in an input impedance higher than 500 Ohm in most of the RF band.

4.4. SHM Architecture Test Vehicle Performance. Even this second implementation, currently under realization, demonstrates a high level of integration: SHM MMIC shows total area occupation of $3 \times 2\,\text{mm}^2$ and results completely comparable with the MHM one (again, $3 \times 2\,\text{mm}^2$). System layout, depicted in Figure 10, shows RF and IF amplifiers, respectively, in the upper and bottom left part of the chip, with a sub-harmonic mixer occupying the remaining right part. LO, IF, and RF ports are clockwise arranged on the right, lower, and left borders of the chip respectively, whereas amplifiers biasing pads can be recognized along the upper edge. The entire system exhibits a total DC power consumption of 120 mW.

In Figure 11 simulated input (RF) and output (IF) matching are reported: the former is better than −15 dB all over the bandwidth and better than −20 dB in most of the 1–18 GHz range, the latter is typically around −15 dB.

Simulated conversion gain and RF/IF isolation at 10 dBm LO power are reported in Figure 12: conversion gain results to vary between 17 dB and 19 dB in the whole operating bandwidth while RF/IF isolation ranges from 35 dB to 80 dB as frequency increases; LO leakage toward RF and IF ports is lower than −34 dB and −135 dB, respectively.
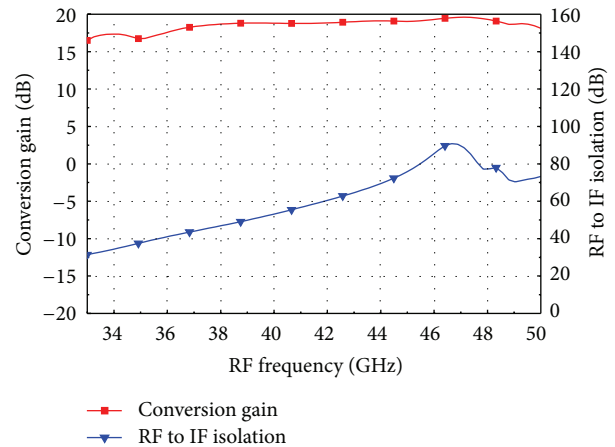
5. Architectures Comparison

Architectures described in previous sections represent different approaches in the realization of downconverting module. Beyond the considerations already performed in Section 2, actual circuit realizations exhibit evident differences concerning the main figures of merit: in Table 1 a summary enabling to draw a direct comparison between two described implementations is reported.

As it can be easily noticed, MHM architecture suffers from a lower conversion gain, worse isolation, and higher DC power consumption but requires 3-4 dBm LO power only at 4 GHz to be effectively implemented. On the other hand, SHM architecture demonstrates better gain and isolation performance, featuring at the same time lower DC power consumption but requires the distribution of a higher LO power at a higher frequency (16 GHz).

Table 1: MHM architecture and SHM architecture main figures of merit.

Parameter	MHM architecture (measured)	SHM architecture (simulated)
Gain (dB)	$\approx$10	$\approx$18
RF/IF isolation (dB)	10 ÷ 40	35 ÷ 80
LO/IF isolation (dB)	33	34
LO/RF isolation (dB)	43	135
RF matching (dB)	<−15	<−15
IF matching (dB)	<−9	<−20
LO frequency (GHz)	4	16
LO power (dBm)	3 ÷ 4	10
DC power consumption (mW)	240	120

6. Conclusion

Two downconverting module architectures for high performance multipixel cameras, both operating in the Q-band frequency range (33–50 GHz) with really ultrabroadband IF section (1–18 GHz), have been illustrated and compared. MHM architecture, fabricated and successfully tested, is based on LO frequency multiplication, whereas SHM architecture, currently under realization, takes advantage of 2nd order harmonic mixing.

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