This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/JEDS.2018.2827164, IEEE Journal of the Electron Devices Society

Material-Device-Circuit Co-design of 2D Materials based Lateral Tunnel FETs

Tarun Agarwal, Gianluca Fiori, Bart Soree, Iuliana Radu, Marc Heyns, and Wim Dehaene

***Abstract*—In this paper, the two-dimensional (2D) materials based lateral TFETs are holistically assessed by co-optimizing the material parameters, device designs, and digital circuit figure-of-merits e.g. energy consumption and delay. Effect of material parameters such as effective mass and bandgap are studied using a two-band quantum simulation approach in the ballistic regime. The selection of 2D material parameters is discussed from the energy-delay perspective. Single-gate and double-gate 2D TFETs are compared with the optimum material parameters. Using a simple analytical model for 2D TFETs, the quantum simulation results for different materials and device designs are analyzed. We show that the gate-to-source fringing fields play a significant role in 2D TFETs performance. To mitigate the effect of fringing fields on tunneling lengths, an interfacial layer (IL) is introduced between High-κ and 2D material, resulting a 3-4x increase in ON current. Using circuit-level metrics, we show that a tri-layer black phosphorus (BP) TFET using IL can outperform monolayer BP MOSFETs for the supply voltages below 0.5 V.**

***Keywords*—Tunnel FETs, Two-dimensional Materials, Black Phosphorus.**

I. Introduction

TUNNEL FETs have been investigated extensively as they promise sub-60 mV/dec sub-threshold swing (SS) at room-temperature, a key to scale supply voltages below 0.5 V [1]. However, ON currents in TFETs are well below that of MOSFET. To achieve reasonable ON currents in TFETs, we need higher transmission probability using lower effective mass and lower bandgap materials with good electrostatics. III-V material based gate-all-around TFETs promise both lower effective mass/bandgap, and excellent electrostatics. Alternatively, 2D materials are considered for TFETs due to their atomic thickness, which offer better scalability in comparison to Si and III-V materials [2]. Moreover, an extensive list of 2D materials with different effective masses and bandgap openings provide multiple alternatives for the material selection [3].

To design a high-performance 2D material based TFET, it is imperative to choose the right 2D material with the optimum bandgap and effective mass [4]. A lower bandgap and higher effective mass 2D material has been reported to offer higher inter-band tunneling currents than lower effective mass and higher bandgap 2D materials [5]. However, to estimate the performance limit of different 2D materials for TFETs, a study accounting for circuit and system level parameters is required. The performance of 2D TFETs can be further boosted by designing the device for good electrostatics and enhanced transmission probabilities. Therefore, a 2D material based double-gate (DG) device is expected to have higher ON currents than single-gate (SG) device, as in the case of bulk materials [6]. However, in case of atomically thin 2D channels, fringing fields are reported to play a significant role in the electrostatic control of 2D material based devices [7]. Therefore, to achieve an optimum device design for 2D TFETs, a study comparing both single-gate and double-gate device options is required.

In this work, we address the selection of right 2D material and device design for n-channel TFETs from the circuit-level perspective. The circuit level figure-of-merits (FOMs) are estimated based on device level characteristics of 2D TFETs obtained from the quantum transport framework, further accounting for system level parameters such as activity factor, and logical depth. The first part of the paper provides a detailed explanation on material & device modeling of 2D TFETs for different effective mass and bandgap materials, and a framework for circuit level FOMs estimation. In second part, we first discuss the selection of right 2D material both from device-level (ON current) and circuit-level (energy-delay product, delay) perspectives. For device design guidelines, both SG and DG device options with 2D materials are compared and thoroughly analyzed. To further boost the performance of 2D TFETs, new device solutions are proposed. Lastly, we assess both black phosphorus and WTe_2 based TFETs by combining different device solutions and then, benchmark the 2D TFETs with monolayer BP FETs using energy-delay figure-of-merits.

II. Modeling and simulation

To estimate the performance of 2D TFETs for energy-efficient digital circuits, the calculation of circuit-level figure-of-merits using device-level characteristics is discussed. Then, we present the material modeling framework to find the optimum material parameters using two-band tight binding (TB) Hamiltonian with a quantum transport simulation framework based on self-consistent solution of Poisson and Schrödinger equation in non-equilibrium Green's function framework [8]. Next, a simple device modeling approach is discussed in order to analyze the quantum simulation results.

A. Circuit-level Estimation

To assess the impact of material and device design parameters of 2D TFETs in digital circuits, we choose delay and energy-delay product (EDP) as circuit level figure-of-merits. We estimate these circuit level metrics for a generic digital

T. Agarwal, B. Soree, I. Radu, and M. Heyns are with Interuniversity Microelectronics Centre (imec), Heverlee, 3001 Belgium. e-mail: Tarun.AgarwalKumar@imec.be.

T. Agarwal, M. Heyns and W. Dehaene are also with the Department of Electrical Engineering, Katholieke Universiteit Leuven, Heverlee, 3001 Belgium.

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/JEDS.2018.2827164, IEEE Journal of the Electron Devices Society

circuit architecture, where a CMOS inverter chain represents the critical path of the combinational block, with balanced p- and n-type 2D TFETs [9]. The number of inverter stages in the critical path is designated as logical depth (L_D). In order to directly assess the impact of material or device design parameters, we normalize the delay and energy-consumption by the total capacitance, which is a reasonable assumption for the scaled technology nodes where the total capacitance is dominated by the device parasitic and back-end-of-line (BEOL) capacitances rather than the intrinsic device capacitance. We can then write the normalized delay of the critical path and total energy per operation of the combinational block in terms of device-level parameters as [9]:

$$\tau_{CP} = \frac{V_{DD}}{I_{ON}}.L_D \tag{1}$$

$$E_{tot} = {V_{DD}}^2(\alpha + L_D\frac{I_{OFF}}{I_{ON}}) \tag{2}$$

$$f_{CP} = \frac{1}{2\tau_{CP}} \tag{3}$$

where τ_{CP} is the delay of the critical path with a logic depth of L_D, while E_{tot} and f_{CP} represent the total energy and the frequency of the operation. Here, τ_{CP} is expressed in $s/(F/m)$ as the device ON currents (I_{ON}) are expressed in μA/μm. The E_{tot} in eq. 2 includes both leakage and dynamic energy consumption, where the domination of either component depends on the activity factor (α) and L_D. Considering the energy-efficient digital CMOS logic design as a possible application domain for 2D TFETs, the circuit FOMs of utmost importance are τ_{CP} and E_{tot}, which decide f_{CP} and EDP expressed as:

$$EDP = E_{tot}.\tau_{CP} = \frac{E_{tot}}{2f_{CP}} \tag{4}$$

Here, EDP signifies that energy and speed are equally weighed for the energy-efficient logic design.

B. Material Modeling

To study the impact of the material parameters on the circuit-level metrics, we use a two-band (conduction and valence) Hamiltonian with the quantum transport simulation framework [8]. The two-band Hamiltonian for an anisotropic effective mass two-dimensional material with hexagonal lattice can be written as a 2x2 Hamiltonian matrix [7], [10]:

$$H_{2D} = \begin{bmatrix} E_{cm} & f(k) \\ f^*(k) & E_{vm} \end{bmatrix} \tag{5}$$

where E_{cm}, and E_{vm} denote the bottom of conduction band, and top of the valence band. Further, bandgap (E_G) of the material can be expressed as: $E_G = E_{cm} - E_{vm}$. Here, the $f(k)$ function, due to nearest neighbors, can be written as:

$$f(k) = t_1 e^{(ik_x a/\sqrt{3})} + 2t_2 e^{(-ik_x a/2\sqrt{3})} cos(\frac{k_y a}{2}). \tag{6}$$

Here, t_1, t_2 represents hopping energies in x and y direction respectively, which are calculated using the effective masses in x and y directions and bandgap of 2D material. Here, k_x, and k_y are wave vectors in x & y directions, while a denotes the lattice constant of the two-dimensional hexagonal lattice. Further, using secular equation, we obtain the dispersion relation for the two-band model given as:

$$E^{\pm}(k) = \frac{(E_{cm} + E_{vm}) \pm \sqrt{(E_{cm} - E_{vm})^2 + 4|f(k)|^2}}{2}. \tag{7}$$

In order to calculate t_1 and t_2 for given effective masses in x and y direction, we use the parabolic effective mass approximation with the two-band model as:

$$\frac{1}{m_x^*} = \frac{1}{\hbar^2}.\frac{\partial^2 E^{\pm}(k)}{\partial k_x^2} \qquad \frac{1}{m_y^*} = \frac{1}{\hbar^2}.\frac{\partial^2 E^{\pm}(k)}{\partial k_y^2} \tag{8}$$

where m_x^* and m_y^* denotes the reduced effective mass in x and y direction. Using eq. 6,7,8, and by taking limit of the second derivative at the minimum energy k-point, we can calculate t_1 and t_2 for given m_x^*, m_y^*, and E_G as:

$$|t_1|^2 = \frac{2\hbar^2 E_G}{3a^2 m_x^*} \qquad |t_2|^2 = \frac{\hbar^2 E_G}{2a^2}[\frac{1}{3m_x^*} + \frac{1}{m_y^*}] \tag{9}$$

C. Device Modeling

Using the above device simulation framework, we can assess the impact of material parameters, compare different device architectures, and optimize a chosen device architecture. To get an insight into the device simulation results, we utilize an analytical modeling framework for 2D lateral TFETs, where the drain current per unit width (I_D) is calculated using the WKB approximation and can be written as follows [5]:

$$\begin{aligned} I_D =& a\, E_{eff}^{1/2}\, \exp(-\frac{b}{E_{eff}}) \Big[\sqrt{\pi}\,(q\,V_R - \frac{c\,E_{eff}}{2})\, erf(\sqrt{\frac{q\,V_R}{c\,E_{eff}}}) \\ &+ \sqrt{q\,V_R\,c\,E_{eff}}\, \exp(\frac{q\,V_R}{c\,E_{eff}})\Big] \end{aligned} \tag{10}$$

where, V_R and E_{eff} represent the reverse bias voltage and electric field at the source-channel tunnel junction, respectively. The coefficients a, b, and c depend on the material parameters and can be given as:

$$\begin{aligned} a =& \frac{q^{3/2}{m_{yR}^*}^{1/2}}{4\pi^2\hbar^{3/2}(2m_x^* E_G)^{1/4}} \\ b =& \frac{4\sqrt{2m_x^*}E_G^{3/2}}{3q\hbar} \\ c =& \frac{q\hbar}{2\sqrt{2m_x^* E_G}} \end{aligned} \tag{11}$$

here, m_{yR}^* denotes the reduced effective mass in the transverse direction, calculated as: $m_{yR}^* = m_{cy}^* m_{vy}^*/(m_{cy}^* + m_{vy}^*)$ [1], where m_{cy}^* and m_{vy}^* represent the electron transverse effective mass in the conduction and valence band, respectively.

To calculate the drain current from eq. 10 for a given 2D material, we need to extract V_R and E_{eff} from the device simulations. Fig. 1(a) shows the schematic of a generic 2D material-based single-gate lateral TFET with E_G of 0.6 eV,

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/JEDS.2018.2827164, IEEE Journal of the Electron Devices Society

and m_x^*, m_y^* of 0.3 m_0. Here, a low doping concentration for drain region is used to reduce ambipolar currents at higher V_{DS}. Furthermore, we assume ohmic metal contacts and abrupt uniform doping profile in the source and drain extensions to project the maximum achievable performance of 2D TFETs. Fig. 1(b) illustrates the energy band-diagram of a 2D TFET in OFF (symbols) and ON states (solid) along the device length by taking a y-cutline at the middle of the 2D material. It depicts the electron energy of conduction & valence bands (left) with absolute value of the electric field (right) along the device length. Here, V_R is calculated by subtracting the conduction band energy in channel from the valence band energy in source and E_{eff} is computed by averaging the absolute electric field values (Fig. 1(b)) in the tunneling window denoted by qV_R. Using the V_R and E_{eff} obtained from the device simulations, we can estimate the ON currents for any 2D material with known m_x^*, m_{yR}^* and E_G. The analytical model provides both an insight into the device simulation results and guidance in designing 2D TFETs.

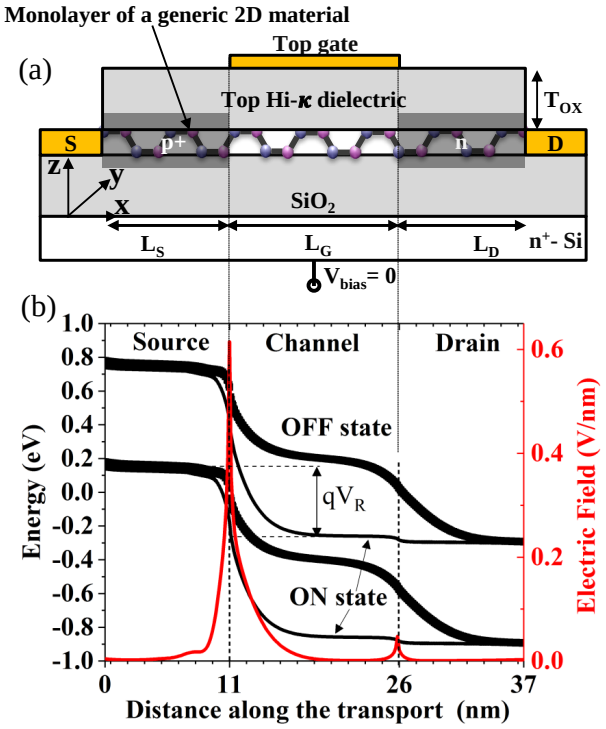

Fig. 1. a) Schematic of a single-gate monolayer 2D material-based TFET with, b) Electron energy in both conduction and valence bands (left) with absolute value of the electric field (right) along the lateral direction for E_G of 0.6 eV, and m_x^* of 0.3 m_0. Here, source and drain extensions are p^+-doped (3.85x10^{13} cm^{-2}), and n-doped (3.85x10^{12} cm^{-2}), respectively. The channel is intrinsic with L_G = 15 nm, L_S = 11 nm, and L_D = 11 nm. t_{HfO_2} is chosen to be 3 nm with ϵ_{HfO_2} = 25, and t_{SiO_2} is chosen to be large enough to not affect the electrostatics.

III. Results and Discussion

To holistically assess the two-dimensional materials based TFETs for energy-efficient digital circuits, we need to co-optimize the material parameters, device designs and energy-delay metrics. Firstly, the selection of optimum material parameters such as carrier effective mass (m_x^*, m_y^*) and E_G are discussed from both device and circuit perspective. Using the optimum material parameters, we then compare different device architectures and propose device designs to further boost the performance of 2D TFETs. Lastly, the selection of OFF current (I_{OFF}) and supply voltage (V_{DD}) to achieve the optimum energy-delay product is discussed.

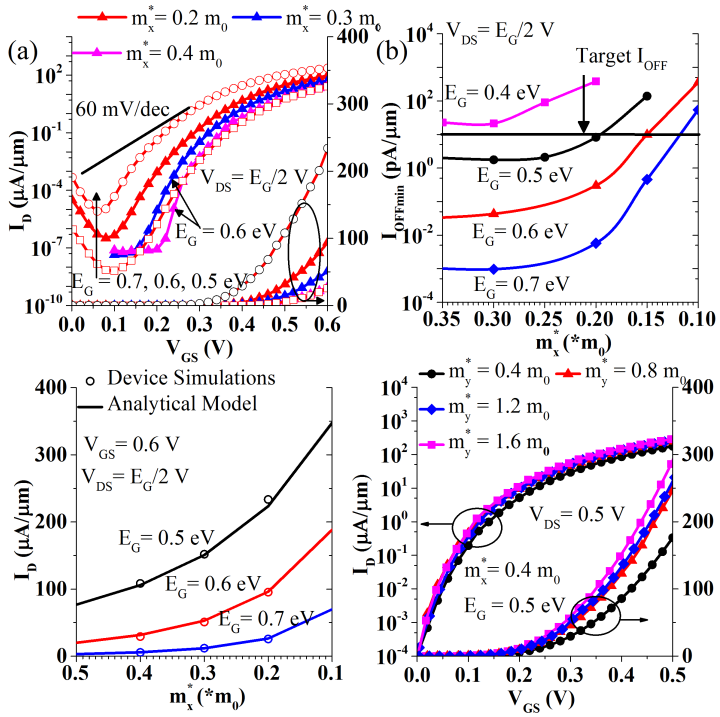

Fig. 2. Impact of the material parameters on, a) Transfer characteristics for different m_x^* at E_G = 0.6 eV and different E_G at m_x^* = 0.2 m_0 for isotropic 2D materials, b) Minimum leakage current with E_G and m_x^* extracted from the transfer characteristics, c) Comparison of modeled and simulated drain currents for different E_G and m_x^*, d) Transfer characteristics with different transverse effective mass for chosen E_G = 0.5 eV and m_x^* = 0.4 m_0, obtained using the two-band quantum simulations.

A. Material Selection

Using the model explained in section II-B along with quantum simulation framework, we calculate the electrical characteristics of a single-gate 2D material-based TFET (Fig. 1(a)) for different materials (i.e. different effective mass and bandgap energies) as shown in Fig. 2(a). It is observed that bandgap (E_G) plays a crucial role in both reducing the OFF current and boosting the ON state current. On the other hand, increasing the effective mass of the material improves the sub-threshold swing (Fig. 2(a)), but by diminishing the ON state current. To understand the m_x^* and E_G trade-off, we plot the minimum leakage current (I_{OFFmin}) with m_x^* for different bandgaps (Fig. 2(b)). It is shown that for a given E_G, the effective mass of the material doesn't significantly affect

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/JEDS.2018.2827164, IEEE Journal of the Electron Devices Society

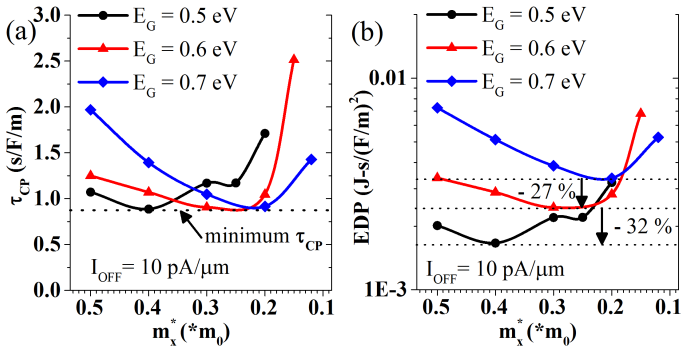

Fig. 3. Using eq. 1 and 2, estimated circuit level metrics (normalized) a) Delay, and b) Energy-Delay Product for different E_G and m_x^* with L_D = 45, α = 3% (from ARM Cortex M0), I_{OFF} = 10 pA/μm, and V_{DD} = E_G/2.

the off-state current after a certain value. On the other hand, a significant reduction in I_{OFFmin} is exhibited with an increase in E_G for a given m_x^*. Thus, Fig. 2(b) provides guidelines in choosing the effective mass and bandgap of 2D materials for a chosen target I_{OFF}. To satisfy the ITRS LSTP requirements (I_{OFF} = 10 pA/μm), 2D TFETs need 2D materials with a bandgap opening of more than 0.5 eV and the carrier effective mass above 0.1 m_0 for the gate lengths of interest (below 20 nm).

Next, to get an insight into the device simulations, we calculate the average electric field in the tunneling window (E_{eff}) and the width of the tunneling window (V_R) from the electrostatic potential obtained using the quantum transport simulations. As shown in Fig. 2(c), the simulated and modeled ON state currents show a good agreement for different m_x^* and E_G. The corresponding values of E_{eff} and V_R for E_G = 0.5, 0.6, 0.7 eV are 0.46, 0.448, 0.43 V/nm, and 0.42, 0.42, 0.34 V, respectively. To further boost the ON state current, a 2D material with anisotropic effective mass properties ($m_y^* > m_x^*$) would be beneficial, as suggested by eq. 10. The device simulations in Fig. 2(d) exhibits that a 2D material with higher transverse effective mass results in higher ON state currents. An anisotropy of 4x in the transverse direction effective mass can result up to 66% increase in the ON state current.

Furthermore, to estimate the impact of material parameters on the circuit level FOMs, we calculate τ_{CP} and EDP from the 2D TFET characteristics (Fig. 2), using the model explained in section II-A. Fig. 3(a) presents that the delay of the critical path has a minimum at an optimum effective mass for a chosen E_G. It shows that we need higher effective masses for smaller bandgap 2D materials to achieve the optimum performance. This is due to the ambipolar (OFF-state) current which dominates for smaller effective mass 2D materials and degrades the sub-threshold swing resulting in lower ON currents at fixed I_{OFF}. However, at an optimum effective mass for a chosen E_G, we observe best of both worlds i.e. better sub-threshold swing and reasonably higher tunneling probabilities, resulting in higher ON currents and lower delay. With further increase in the effective mass, the delay starts to increase again as I_{ON} starts to reduce due to lower tunneling probabilities.

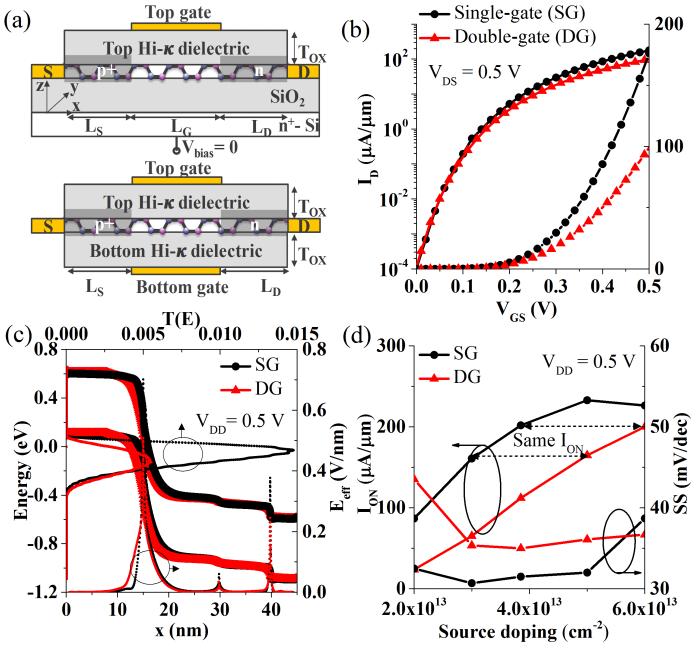

Fig. 4. Comparison of SG and DG 2D TFETs with E_G = 0.5 eV, m_x^* = m_y^* = 0.4 m_0, a) Schematic of SG and DG monolayer 2D TFETs, b) Transfer characteristics at V_{DS} = 0.5 V, c) Band-diagrams with transmission probabilities (T(E)) and electric field profile of SG and DG 2D TFETs in ON state, d) I_{ON} and SS with different source extension doping concentrations. Here, the source and drain extension lengths are 15 nm each side.

Interestingly, Fig. 3(b) shows that the minimum EDP or energy consumption increases with the bandgap of the material due to the need of higher applied supply voltages to achieve a given performance. Thus, we choose the optimum 2D material parameters as: E_G = 0.5 eV and m_x^* = m_y^* = 0.4 m_0, for the chosen gate length of 15 nm. Furthermore, the chosen supply voltage is increased to 0.5 V based on our previous work [9], where both minimum EDP and higher frequency of operation is reported till 0.5 V.

B. Device Design

Using the optimum material parameters, we compare single-gate and double-gate monolayer (ML) 2D material based TFETs (Fig. 4). Contrary to the expectation, it is shown in Fig. 4(b) that a SG monolayer 2D TFET offers higher ON currents in comparison to DG monolayer 2D TFET. Fig. 4(b) exhibits that although the sub-threshold characteristics of SG and DG ML 2D TFET are comparable, the ON-state currents for SG ML 2D TFET are higher, indicating higher tunneling probabilities. Fig. 4(c) shows the tunneling probabilities of SG and DG ML 2D TFETs along with the band diagrams and the absolute electric field profile. It is clearly observed that a sharper source-to-channel junction in SG 2D TFET results in both higher tunneling probabilities and higher peak electric field at source-channel junction with respect to DG 2D TFET. The extracted values of E_{eff} and V_R for SG, DG 2D TFETs comes out to be 0.505, 0.422 V/nm and 0.49, 0.533

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/JEDS.2018.2827164, IEEE Journal of the Electron Devices Society

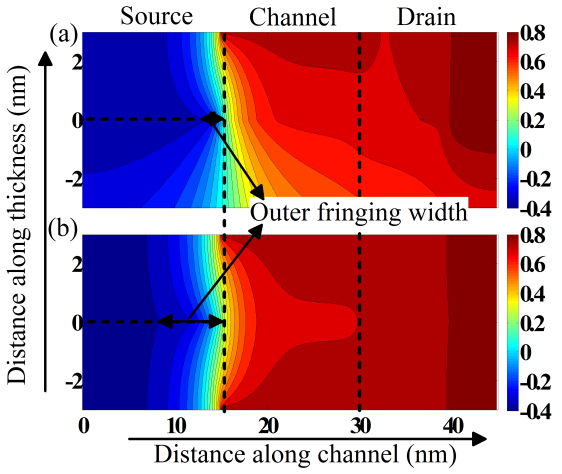

Fig. 5. Effect of fringing fields, a) 2D Potential distribution in SG, showing only the partial back-gate oxide with same thickness as top-gate oxide, b) 2D Potential distribution in DG, showing the gate-induced potential spread at source-channel junction in ON state (V_{DD} = 0.5 V).

V, respectively. The electric field at source-channel junction can be further enhanced using higher source extension doping concentrations. Fig. 4(d) shows behavior of the ON current and SS with source doping concentrations. It is shown that although the ON currents in DG 2D TFET can be matched with SG 2D TFET by increasing the source doping, the ON currents in single-gate 2D TFET are consistently higher than the ON current in DG 2D TFET for a given source doping concentration.

In order to get a qualitative understanding of higher electric field values observed in SG 2D TFETs, 2D potential profiles in SG and DG device structures for the same cross-section are shown in Fig. 5. In ON state (i.e. at high V_{DD} = 0.5 V), Fig. 5 shows the gate-to-source potential distribution or the fringing fields originating from gate edge. It is to be noted that the electrostatic potential in the channel shows higher values than V_{DD} as a result of the work-function engineering which is required to fix the OFF state at V_G = 0 V. In ideal condition, the gate electric field lines would be aligned perpendicular to the channel, resulting in nearly zero outer fringing width, and a steep source-channel junction. While in Fig. 5, it is clearly displayed that the lesser outer fringing width in single-gate device structures result in higher electric fields at source-channel junction, thus higher tunneling probabilities.

In our previous work on 2D FETs in order to reduce the fringing fields, we introduced a low-κ interfacial layer in between High-κ and 2D material, resulting in better electrostatics and enhanced gate-to-channel control [7]. Here, Fig. 6(a) present the gate stacks with 0.5 nm IL and 1.5 nm High-κ i.e. T_{OX} = 2 nm in both SG and DG devices, which need to be carefully designed to mitigate gate tunneling through the gate stack. Fig. 6(b) shows that introducing an IL layer improves both onset voltage (i.e. sub-threshold characteristics) and the ON state (i.e. tunneling probability). For an equivalent effective-oxide-thickness (EOT), introducing IL results in around 3-4x increase in the ON current. Fig. 6(c) and (d)

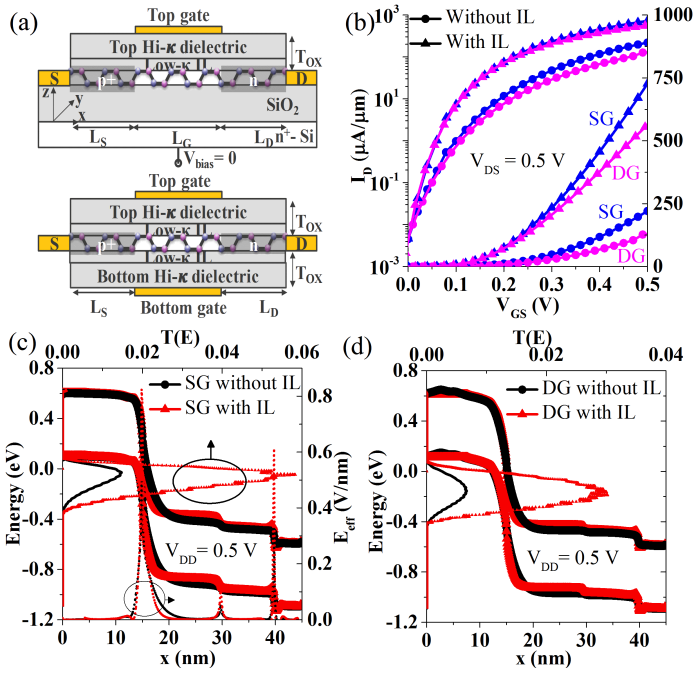

Fig. 6. Proposed device with E_G = 0.5 eV, $m_x^* = m_y^*$ = 0.4 m_0, a) Schematic of SG and DG monolayer 2D TFETs with low-κ interfacial layer between High-κ and 2D material, b) Transfer characteristics comparing both SG and DG devices with/without IL, c), and d) Band-diagrams with transmission probabilities for SG and DG device structures with/without IL.

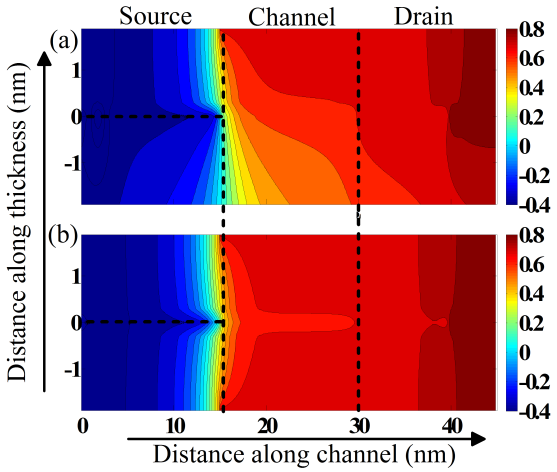

Fig. 7. Effect of fringing fields in devices with IL a) 2D Potential distribution in SG (with partial buried oxide), b) 2D Potential distribution in DG, showing the improved 2D rectilinear potential near source-channel junction (i.e. reduced fringing fields) at ON state.

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/JEDS.2018.2827164, IEEE Journal of the Electron Devices Society

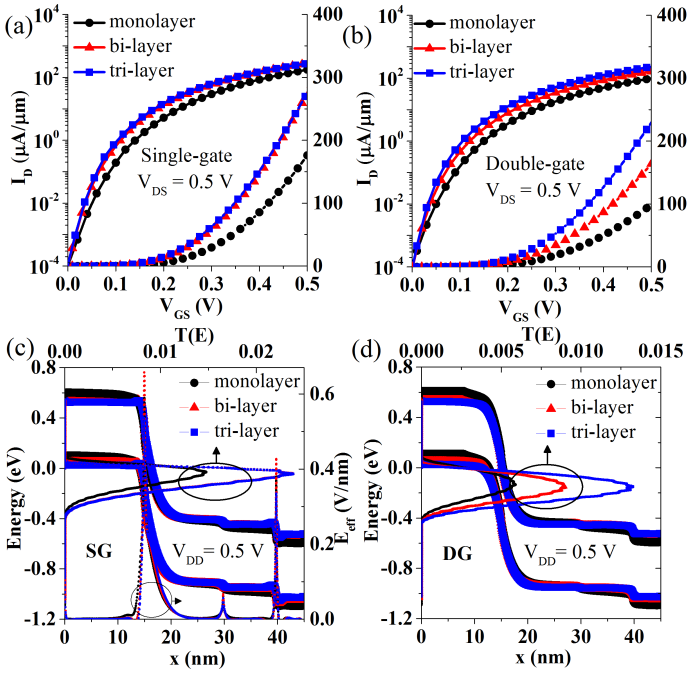

Fig. 8. Effect of channel thickness for equivalent effective mass (0.4 m_0) and bandgap (0.5 eV), a,b) Transfer characteristics of mono-, bi-, and tri-layer 2D material based SG and DG TFETs, c,d) Band-diagrams with transmission probabilities for multi-layer SG and DG 2D TFETs.

indicate an equivalent boost in the transmission probability as the boost in ON currents for both SG and DG devices. A significant reduction in the tunneling distances can be seen in the device structures with IL. As shown in Fig. 7, shorter tunneling lengths at source/channel junction are achieved by shaping the potential to be steeper at the junction. Fig. 7 exhibits a near ideal case, where the potential distribution is highly rectilinear (i.e. lesser fringing fields) in contrast to Fig. 5 where the potential distribution is elliptical. The extracted electric field values for SG and DG 2D TFETs with IL are 0.9 and 0.73 V/nm, which are $\sim$ 70 % higher in comparison to electric field without IL (0.53, 0.45 V/nm).

With an insight on the fringing fields in monolayer 2D materials based SG and DG device structures, we further study the effect of multi-layer 2D materials on the fringing fields, thus the performance. Using the framework of multi-layer 2D materials as given in [8] with t_p=0 eV, performance of mono-, bi-, and tri-layer 2D TFETs are compared in Fig. 8(a) and (b). It is demonstrated that ON current increases with the number of layers for a fixed set of material parameters (m_x^* = m_y^* = 0.4 m_0, and E_G = 0.5 eV). Although in reality, the material parameters also change with the number of 2D layers e.g. monolayer 2D materials have larger E_G than multi-layer 2D materials [3]. But, we restrict ourselves with the same material parameters for mono-, bi-, and tri-layer 2D TFETs, in order to understand the effect of increasing channel thickness. For single-gate case when transitioning from monolayer to bi-layer, we can observe a significant boost in the ON current due to the increased electric field at the source-channel

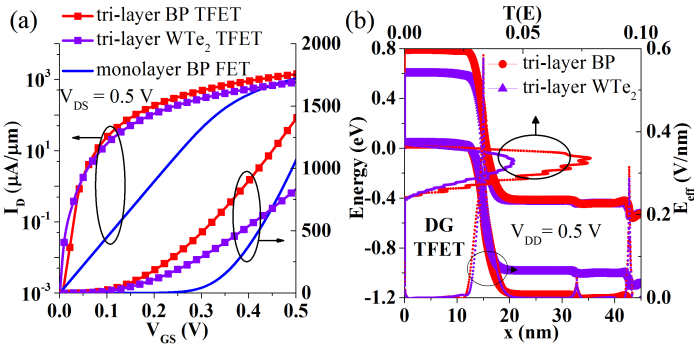

Fig. 9. Double-gate tri-layer BP and WTe_2 TFETs with L_G = 18 nm, a) Transfer characteristics comparison of DG tri-layer 2D material TFETs and DG monolayer BP FET [7], b) Band-diagrams with transmission probabilities for DG tri-layer 2D material TFETs.

junction, effectively increasing the transmission probability, as shown in Fig. 8(c). While the ON current doesn't increase appreciably when transitioning from bi-layer to tri-layer due to the degradation in 2D electrostatics with increasing number of layers, which nullifies the boost in ON current. On the other hand, Fig. 8(b) and (d) show that the double-gate should be the preferred device architecture in case of multi-layer 2D TFETs, as the 2D electrostatics can maintained with DG device, resulting in higher ON currents for tri-layer 2D TFETs than mono- and bi-layer 2D TFETs.

Using the device design guidelines, we then assess the performance of tri-layer 2D materials (Black phosphorus and WTe_2) double-gate TFETs due to their attractive material properties. Although it should be noted that semi-conducting WTe_2 in 2H phase and black phosphorus under ambient conditions are reported to be unstable, efforts to stabilize these 2D materials are ongoing. Thus, we choose tri-layer black phosphorus and WTe_2 to project the performance limits of 2D TFETs. As shown in Fig. 9(a), tri-layer (TL) BP DG TFET exhibits remarkably high ON currents in comparison to tri-layer WTe_2 DG TFETs. Fig. 9(b) indicates that although the peak electric fields at source-channel junction are comparable for both TL BP and WTe_2 TFETs, the transmission probabilities for TL BP are higher than TL WTe_2. This is due to the superior material properties of TL BP (also indicated by eq. 10) i.e. smaller transport effective mass (m_x^* = 0.14 m_0) and larger transverse effective mass (m_{yR}^* = 1.2 m_0) than TL WTe_2 (m_x^* = m_{yR}^* = 0.33 m_0), while the bandgap opening in TL WTe_2 (E_G = 0.56 eV) is smaller than TL BP (E_G = 0.76 eV). Using eq. 10, we get comparable drain currents to the device simulations for $E_{eff} \sim$ 1 V/nm and corresponding material parameters. Additionally, Fig. 9(a) shows the comparison of TL 2D TFETs with a monolayer BP FET [7] for same device parameters. It is clearly shown that TL BP TFETs can outperform 2D FETs for lower supply voltages, while TL WTe_2 DG TFETs offer higher ON currents than ML BP FETs in sub-0.45 V V_{DD} regime at fixed OFF current.

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/JEDS.2018.2827164, IEEE Journal of the Electron Devices Society

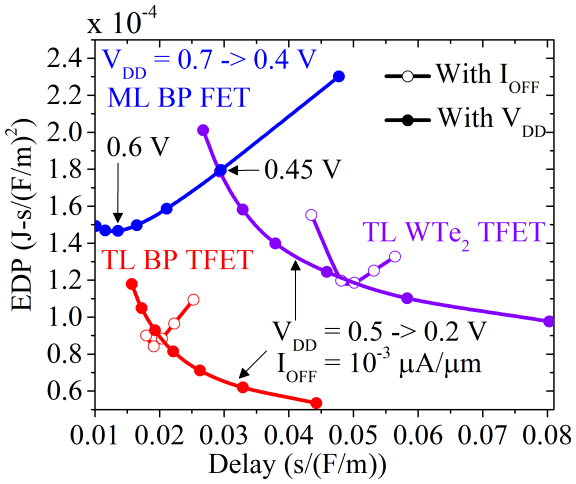

Fig. 10. Benchmarking of tri-layer BP and WTe_2 n-TFETs and monolayer BP n-MOSFET for L_G = 18, showing the estimated EDP and delay for different target I_{OFF}: 10^{-5} to 0.1 μA/μm at V_{DD} = E_G/2 and EDP/delay for different V_{DD} at target I_{OFF} = 1x10^{-3} μA/μm.

C. Energy-delay Optimization

Choosing trilayer BP and WTe_2 DG TFETs, we analyze the effect of OFF current and supply voltages on our circuit level metrics in Fig. 10. We would like to emphasize that the n-TFETs and p-TFETs are assumed to be balanced as mentioned earlier. Therefore, the performance metrics obtained here indicate only the performance of n-TFET across different threshold (or I_{OFF}) and supply voltages. Interestingly, we observe an EDP minimum (symbol) for both material combinations around I_{OFF} = 10^{-3} μA/μm indicating the domination of leakage energy beyond I_{OFF} = 10^{-3} μA/μm. Therefore, we choose 10^{-3} μA/μm as our new target I_{OFF}. Further, Fig. 10 shows that both delay and EDP decrease monotonically with V_{DD}. TL BP TFETs demonstrate both better delay and EDP across different V_{DD} and I_{OFF}. Moreover, TL BP TFETs remain more energy-efficient than ML BP FETs for a given delay in sub-0.5 V supply voltage regime.

IV. Conclusion

In this paper, we have holistically analyzed 2D material based lateral n-TFETs by assessing the impact of the material parameters and different device designs on energy-delay benchmarking with monolayer BP n-FET across different OFF currents and supply voltages. We have shown that 2D TFETs with lower bandgap and higher effective mass display the optimum energy-delay product for a given performance. The anisotropic effective mass 2D materials with relatively smaller bandgap (0.5-0.8 eV) can further boost the performance of 2D TFETs depending on the gate lengths of interest. We have also provided the device design guidelines to further enhance the performance of lateral 2D TFETs. We show that single-gate 2D TFETs can perform better than double-gate 2D TFETs for monolayer 2D channel. However, the double-gate device architecture provides better electrostatic control and thus, performance for multi-layer 2D material TFETs. An analytical model of 2D TFETs is utilized to get insights into the device simulations. Fringing fields are shown to severely limit the performance of 2D TFETs. To mitigate the effect of fringing fields, device architectures with low-κ interfacial layer are introduced, resulting in 3-4x performance boost. Using energy-delay optimization, we show that tri-layer anisotropic effective mass 2D material (e.g. BP) based DG TFETs can outperform monolayer BP FETs in speed for sub-0.6 V supply voltages. However, we would like to emphasize that these high performance 2D lateral TFETs are enabled by high source doping (Fig. 4(d)), which is still a challenge for 2D materials and is being actively investigated.

References

[1] Seabaugh, A. C., and Zhang Q., "Low-Voltage Tunnel Transistors for Beyond CMOS Logic," *Proceedings of the IEEE*, vol.98, no.12, pp.2095-2110, Dec. 2010.

[2] Liu, L., Kumar, S.B., Ouyang, Y. and Guo, J., "Performance limits of monolayer transition metal dichalcogenide transistors," *IEEE Transactions on Electron Devices*, vol.58, no.9, pp.3042-3047, 2011.

[3] Rasmussen, F. A., and Kristian S. T., "Computational 2D materials database: Electronic structure of transition-metal dichalcogenides and oxides," *The Journal of Physical Chemistry C*, vol.119, no.23, pp.13169-13183, Jun. 2015.

[4] Ilatikhameneh, H., Tan, Y., Novakovic, B., Klimeck, G., Rahman, R., and Appenzeller, J., "Tunnel field-effect transistors in 2-D transition metal dichalcogenide materials," *Exploratory Solid-State Computational Devices and Circuits, IEEE Journal on*, vol.1, pp. 12-18, Dec. 2015.

[5] Ma, N., and Jena, D., "Interband tunneling in two-dimensional crystal semiconductors," *Applied Physics Letters*, vol.102, no.13, pp.132102, Apr. 2013.

[6] Verhulst, A.S., Sore, B., Leonelli, D., Vandenberghe, W.G. and Groeseneken, G., "Modeling the single-gate, double-gate, and gate-all-around tunnel field-effect transistor," *Journal of Applied Physics*, 107(2), pp.024518, 2010.

[7] Agarwal, T. K., Soree, B., Radu, I., Raghavan, P., Iannaccone, G., Fiori, G., Dehaene, W. and Heyns, M., "Material-device-circuit co-optimization of 2D material based FETs for ultra-scaled technology nodes," *Scientific reports*, 7(1), p.5016, 2017.

[8] NanoTCAD ViDES, http://vides.nanotcad.com/vides.

[9] Agarwal, T., Radu, I., Raghavan, P., Fiori, G., Thean, A., Heyns, M. and Dehaene, W., "Effect of material parameters on two-dimensional materials based TFETs : An energy-delay perspective," *IEEE European Solid-State Device Research Conference (ESSDERC)*, pp. 47-50, Sept. 2016.

[10] Agarwal, T., Soree, B., Radu, I., Raghavan, P., Fiori, G., Heyns, M., and Dehaene, W., "Material selection and device design guidelines for two-dimensional materials based TFETs," *IEEE European Solid-State Device Research Conference (ESSDERC)*, pp. 54-57, Sept. 2017.