Foreword
Special Issue on Transistors With Steep Subthreshold Swing for Low-Power Electronics

THE increasing power consumption of integrated circuits is today the main impediment to the density scaling of integrated circuit technology. The reduction of supply voltage is the most effective way to reduce power; however, using modern transistors voltage reduction is traded against reduced speed or limited by a rising off-state leakage, neither of which is desirable. A better tradeoff can be achieved if the fundamental current control mechanism provides a steep turn-on characteristic. Steep means better than 60 mV/decade at room temperature, the limit obtained by barrier lowering in a bipolar transistor or metal oxide semiconductor field effect transistor (MOSFET) when the current is dominated by the thermionic emission of carriers above the energy barrier in the base or channel region.

The intensity of experimental and theoretical efforts on steep transistors has been growing worldwide as technical impediments are systematically solved. Subthreshold swings less than 60 mV/decade have been experimentally demonstrated in tunnel field-effect transistors (TFETs) across a wide range of materials systems including carbon nanotubes, Si, and III-Vs. On-currents comparable to MOSFETs have been demonstrated with sub-half-volt supplies. TFETs have received the greatest attention thus far, but are one of a growing number of approaches for achieving steep transistor characteristics.

Our intent with this special issue was to consolidate the latest advances on steep swing transistors with an emphasis on TFETs since this technology is the most highly developed. The call for papers invited submissions that address advances in materials and process technologies, experimental techniques and characterization, modeling and simulation approaches, and design methodologies. We requested papers in: 1) steep transistor concepts; 2) materials and process development; 3) measurements and characterization; 4) modeling and simulations; and 5) device and circuit design.

The special issue begins with five invited papers to provide progress and perspective in the development of TFETs. Uygar Avci, Intel, and Eric Lind, University of Lund, summarize recent progress and current directions in III-V tunnel FETs. The topic of nanowire TFETs is extended in the paper by Qing-Tai Zhao, Forschungszentrum Jülich GmbH, based on the Si and SiGe nanowire systems. Marco Pala, IMEP-LaHC, discusses design options for heterojunction nanowire III-V TFETs based on full quantum 3D simulations. Finally, Peter Asbeck considers the performance of TFETs in low power microwave and mm-wave applications. The 13 contributed papers are divided into three broad themes: 1) device concepts; 2) experimental progress; and 3) modeling and circuit simulation.

The special issue meets our aim of providing a consolidation of the latest advancements in steep subthreshold swing technology. The papers also show that the field is still in an early stage with many competing approaches. Materials, processes, and device understanding is advancing as experiments and models advance. Early assessment of systems impact is giving designers a first look at transistors with the potential to outperform CMOS at low voltages.

DAVID ESSENI, *Guest Editor*
University of Udine
Udine, Italy

ADRIAN M. IONESCU, *Guest Editor*
Ecole Polytechnique Fédérale de Lausanne
Lausanne, Switzerland

ALAN SEABAUGH, *Guest Editor*
University of Notre Dame
Notre Dame, IN, USA

YEE-CHIA YEO, *Guest Editor*
Taiwan Semiconductor Manufacturing Company
Hsinchu, Taiwan

Date of current version 22 April 2015.
Digital Object Identifier 10.1109/JEDS.2015.2418911

David Esseni received the Ph.D. degree in electronic engineering from the University of Bologna. He is currently the Professor of Electronics with the University of Udine, Italy. He was a Visiting Scientist with Bell Laboratories—Lucent Technologies, Murray Hill, NJ, USA, in 2000, and was also a Visiting Professor with the University of Notre Dame, IN, USA, in 2013, supported by a Fulbright Fellowship. He has authored numerous papers and six book chapters in his field of expertise. He has also co-authored the book entitled *Nanoscale MOS Transistors: Semi-Classical Transport and Applications* (Cambridge, U.K.: Cambridge Univ. Press, 2011). He has been an Associate Editor of the IEEE TRANSACTIONS ON ELECTRON DEVICES since 2008. He served or is serving as a member of the technical committees in several conferences, including the International Electron Devices Meeting, the International Reliability Physics Symposium, and the European Solid State Devices Research Conference.

Adrian M. Ionescu received the B.S./M.S. and Ph.D. degrees from the Polytechnic Institute of Bucharest, Romania, and the National Polytechnic Institute of Grenoble, France, in 1989 and 1997, respectively. He is a Professor with the Ecole Polytechnique Fédérale de Lausanne (EPFL), Switzerland. He has held staff or visiting positions with LETI-Commissariat à l'Énergie Atomique, Grenoble, Stanford University, and with the Tokyo Institute of Technology. He is the Founder and the Director of the Nanoelectronic Devices Laboratory, EPFL. He has published over 400 articles in international journals and conference proceedings. He is a recipient of the 2013 IBM Faculty Award, the André Blondel Medal 2009, and Société de l'électricité, de l'électronique et des technologies de l'information et de la communication (SEE), Paris, France, for contributions to the progress in electronic engineering sciences. He served for the International IEEE Electron Devices Meeting, Symposium on Very Large Scale Integration (VLSI) Technology, and Transducers Technical Committees and was also the Technical Program Committee Chair/Co-Chair of the European Solid-State Device Research Conference in 2006 and 2013. He has been an elected member of the Swiss Academy of Technical Sciences since 2015.

Alan Seabaugh received the Ph.D. degree in electrical engineering from the University of Virginia, in 1985. He is a Professor of Electrical Engineering with the University of Notre Dame and the Director of the SRC/DARPA STARnet Center for Low Energy Systems Technology. He was with the National Bureau of Standards (1979–1986), Texas Instruments Central Research Laboratory (1986–1997), and Raytheon (1997–1999) before joining Notre Dame. He has over 300 authored/co-authored papers and holds 23 U.S. patents. He was a recipient of the Symposium on Compound Semiconductors Quantum Devices Award in 2011 for seminal contributions and leadership in semiconductor devices and circuits based on quantum mechanical tunneling.

Yee-Chia Yeo received the B.Eng. and M.Eng. degrees from the National University of Singapore (NUS), and the M.S. and Ph.D. degrees from the University of California, Berkeley, USA. He is the Director of Research and Development, Taiwan Semiconductor Manufacturing Company, Hsinchu, Taiwan. He is on leave from NUS, where he is currently a Professor of Electrical and Computer Engineering. He has co-authored 590 papers and holds 103 U.S. patents. He was a recipient of the 2002 and 2008 IEEE Paul Rappaport Awards.