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RESET Current Reduction for Phase Change Memory Based on Standard 0.13-μm CMOS Technology

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Abstract

In order to reduce the RESET current of phase change memory (PCM), which is fabricated using standard 0.13-μm CMOS technology, we have investigated various process factors that might affect the phase transition process, including doping concentration, diameter of bottom electrode contact (BEC) and different chalcogenide materials. Test results suggest that the PCM memory cell, utilizing $Si_2Sb_2Te_5$ (SST) material as storage element with 80nm BEC, can be operated using a 40ns electrical pulse with current amplitude as small as 0.5mA. This is mainly resulted from the high electrical resistances of the novel chalcogenide both in amorphous and crystalline state, which contribute greatly to the improved efficiency of heating process.

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Keywords: Phase change memory; RESET current; CMOS; SST

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1. Introduction

Nowadays, none of the present single memory technology possesses all the desirable attributes including non-volatility, large volume, high speed for both writing and reading, low power, low cost, long endurance cycle and excellent data retention ability. Therefore, the demand for an ideal memory technology, which has the ability to merge all the attractive features mentioned above, is dramatically growing year after year. PCM, also called Ovonic Unified Memory (OUM), is a very promising candidate to meet this need [1-3].

It is a novel non-volatile semiconductor technology based on reversible phase transitions of a thin film chalcogenide material. Thanks to its excellent electrical performance such as nanosecond-operation, non-volatility, scaling and well compatibility with standard CMOS technology, it is attracting more and more attention among many research groups. However, PCM technology is still facing some critical issues at present, among which the large RESET current and its induced high energy consumption and bulk cell size are the mainly obstacles that hold up the commercially available high density PCM chip[4-7].

In the PCM operation, electrical pulses are applied through the chalcogenide material to generate local joule heating, and then the programmable volume around the bottom electrode contact region can be changed to either crystalline or amorphous state. Normally, a current with higher amplitude and fast quenching are essential to RESET the material to the high resistance amorphous state, while the SET process utilizes only a medium current pulse of longer duration time to change the material to the low resistance crystalline state. Therefore, the level of current pulses for the RESET operation determines the width of the access MOSFET and the volume of PCM. In this work, great attention is paid to reducing the RESET current of PCM through various process tunings with detailed discussion of the electrical characteristics.

2. Cell Structure

The process flow of the fabricated PCM cells are as flows: after the formation of metal-oxide-semiconductor field effect transistor (MOSFET) and common bottom electrode, a window for phase change material patterning will be fabricated. Then chalcogenide alloy is deposited upon the bottom electrode W by RF magnetron method with background pressure of $2*10^{-4}$ Pa, using an alloy target. After that, chemical mechanical polishing (CMP) process is applied to make a damascene structure before the 300 nm top electrode aluminum is deposited and patterned. The PCM cell, as shown in the inset of Fig. 1, is essentially a resistor with variable low-field resistance, which can be measured using a low electrical field (usually 0.1V). Digital information can be stored because the resistance of the cell, which is dependent on the state of chalcogenide material.

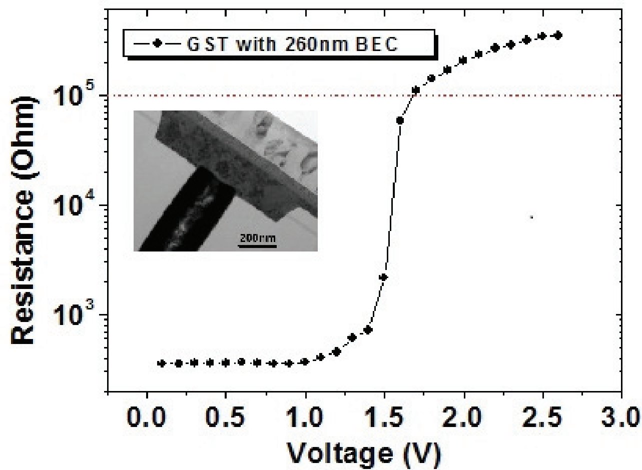

Fig. 1. R-V measurement of the GST cell fabricated using standard 260nm BEC with pulse width of 200 ns. The inset is a TEM image of the fabricated PCM cell element using standard 0.13-μm CMOS technology

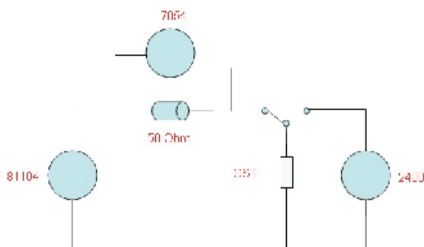

Fig. 2. Schematic drawing of the electrical setup used to program and read the PCM cells

3. Experimental results and discussion

PCM cell element was electrically characterized using pulse generator HP81104 and Keithley model 2400 series sourcemeter. A 50 Ohm load resistor was also added in series and the current amplitude was extracted by measuring the voltage drop on the impedance through a Tektronix DPO 7054 digital phosphor oscilloscope. Fig. 2 illustrates the schematic drawing of the electrical setup used to program and read the PCM cell and Fig. 1 is a typical operational curve of the resistance versus pulse voltage (*R-V*) measurement of the PCM cell, using $Ge_2Sb_2Te_5$ (GST) as storage material, fabricated using standard 260nm BEC when pulse width is settled at 200 ns. The curve was accomplished by applying a sequence of electrical pulses of increasing amplitude by HP 81104 while measuring the PCM resistance in between the pulses through the Keithley 2400. Starting in the low resistance SET state, moving from left to right, the device continues to remain the state with resistance below 1K Ohm as the amplitude is increased, while further increase in the pulse amplitude finally program the PCM cell to a RESET state with resistance larger than 100K Ohm. Normally we define the point where PCM cell was programmed above

100K Ohm as the RESET point and intensive attention was paid to the voltage drop (V_D) through the serial resistance at this point. The RESET current (I_R), defined as the current needed to program the GST cell above 100K Ohm, is a key parameter to characterize the PCM cell fabricated with different processes. Since it is very hard to monitor the resistance during programming process due to the un-linear current-voltage (*I-V*) characteristics [3], I_R can be obtained by dividing V_D by 50 (load resistor). From the Fig. 3 we can see that the lowest RESET current needed to operate the GST cell under standard 0.13-µm CMOS process is above 20 mA.

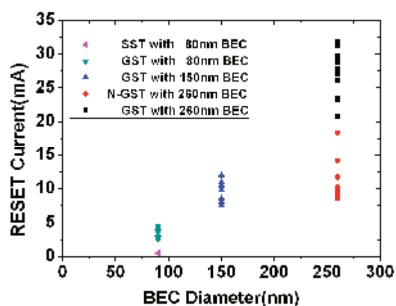

Fig. 3. RESET current of different PCM cells

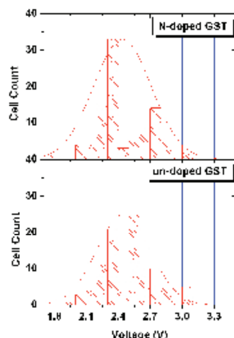

Fig. 4. RESET voltage distribution of the PCM sample cells for N-doped and un-doped process integration

One simple way to reduce the RESET current is impurity doping, which has been proven to be effective by many literature papers [6]. The impurity, if selected correctly, will increase the cell resistance and depress the growth of crystal in GST. In our experiment, Nitrogen (N) was chosen as the dopant. Fig. 4 shows the RESET voltage distribution of the N-doped and un-doped PCM cells. It is obvious that both of the two have almost the same RESET voltage, which is around 2.5V. However, the resistance of the N-doped cell is two times greater than the un-doped one. As illustrated in Fig. 3, only half of the current needed to program the un-doped PCM cell is enough for the N-doped one, which perfectly verified the advantage of impurity doping. However, 8.5mA is still too large for commercial applications.

Another possible way for low current operation is to reduce the BEC size. For comparison, we fabricated two types of PCM cell with BEC size of 130nm and 80nm, respectively. RESET currents of the

two were also measured using the setup introduced above. As BEC size shrinks from 260nm to 80nm, the RESET current decreases from 20mA to almost 2.8mA as illustrated in Fig. 3. The results perfectly verified the relationship between BEC size and the amplitude of RESET current, which further proved that the PCM RESET process is strongly affected by the current density and the MOSFET selector are compliant with the chalcogenide-based PCM scaling capability very well.

Further decrease of BEC is unreliable and will bring on a higher failure rate, and Nitrogen-doping will only contribute to a 50% decrease in the RESET current amlitude. Therefore, the $Si_2Sb_2Te_5$ (SST) is finally proposed as new storage element for PCM, instead of the mostly adopted GST material [8].

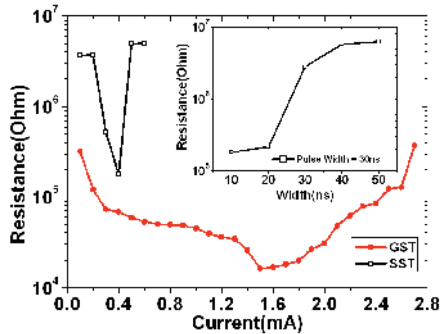

Fig. 5. *R-V* curves for both SST and GST cells. The inset shows the SST cell resistance versus pulse width (current = 500uA)

Fig. 5 shows cell resistance versus application of programming current amplitude when pulse duration is settled at 200 ns for both SST and GST cells with the same 80nm electrode. Starting from the initially as-deposited high resistance state (RESET), the SST cell crystallization process begins when current level reaches 300uA. Further increase in programming current further crystallizes the material at 400uA, which leads to a minimum resistance value of 180K Ohm. When the programming current reaches the level of 500uA, high resistance RESET state exhibits again. It shall be noticed that 500uA is the minimum RESET current ever reported based on 80 nm BEC. Meanwhile, 200ns is unnecessarily longer than the minimum pulse duration with 500uA pulse level. The results shown in the inset of Fig. 5 illustrate the successful RESET operation of SST cell with 40ns pulse width.

As shown in Fig. 5, detailed advantages of SST based PCM cells were summarized as follows: RESET and SET state resistances are about 10 times higher than those of GST; RESET current reduced to a level almost a quarter of GST, which also means that only a quarter of the transistor width are needed to drive the SST cell as compared to GST cell. Based our process integration flow, the gate width finally adopted is 0.7 um for SST based memory cells and the cell size is 0.65 um^2, corresponding to 27 F^2.

To explain the novel electrical switching characteristics of SST material, two major aspects are taken in account. Firstly, as reported in our group's earlier contribute, the phase change process of SST is similar to that of GST while the melting temperature is about 60C lower [8], which means a lower RESET power could be surmised. Secondly, according to the Joule equation, a more resistive PCM cell, which acts as load resistance of the driving circuit, will result in a more effective power delivery.

4. Conclusion

In conclusion, various process factors that might affect the phase transition process of PCM have been studied, including doping concentration, diameter of bottom electrode contact (BEC) and different chalcogenide materials. Test results suggest that a PCM memory cell, utilizing $Si_2Sb_2Te_5$ (SST) material

as storage element with 80nm BEC, can be operated using a 40ns electrical pulse with current amplitude as small as 0.5mA. The large resistance induced ultra low RESET current and short transition time are verified through the successful operation of a 27 F^2 cell element, showing a bright future of further down-scaling of PCM. This is mainly resulted from the high electrical resistances of the novel chalcogenide both in amorphous and crystalline state, which contribute greatly to the improved efficiency of heating process.

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